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FEATURES

- Low phase noise, phase-locked loop (PLL)
 - On-chip VCO tunes from 2.05 GHz to 2.33 GHz
 - External VCO/VCXO to 2.4 GHz optional
 - 1 differential or 2 single-ended reference inputs
 - Reference monitoring capability
 - Automatic revertive and manual reference switchover/holdover modes
 - Accepts LVPECL, LVDS, or CMOS references to 250 MHz
 - Programmable delays in path to PFD
 - Digital or analog lock detect, selectable
- 3 pairs of 1.6 GHz LVPECL outputs
 - Each output pair shares a 1-to-32 divider with coarse phase delay
 - Additive output jitter: 225 fs rms
 - Channel-to-channel skew paired outputs of <10 ps
- Automatic synchronization of all outputs on power-up
- Manual output synchronization available
- Available in a 48-lead LFCSP

APPLICATIONS

- Low jitter, low phase noise clock distribution
- 10/40/100 Gb/sec networking line cards, including SONET, Synchronous Ethernet, OTU2/3/4
- Forward error correction (G.710)
- Clocking high speed ADCs, DACs, DDSs, DDCs, DUCs, MxFEs
- High performance wireless transceivers
- ATE and high performance instrumentation

GENERAL DESCRIPTION

The AD9518-2¹ provides a multi-output clock distribution function with subpicosecond jitter performance, along with an on-chip PLL and VCO. The on-chip VCO tunes from 2.05 GHz to 2.33 GHz. Optionally, an external VCO/VCXO of up to 2.4 GHz can be used.

The AD9518-2 emphasizes low jitter and phase noise to maximize data converter performance, and it can benefit other applications with demanding phase noise and jitter requirements.

The AD9518-2 features six LVPECL outputs (in three pairs). The LVPECL outputs operate to 1.6 GHz.

For applications that require additional outputs, a crystal reference input, zero-delay, or EEPROM for automatic configuration at startup, the AD9520 and AD9522 are available.

FUNCTIONAL BLOCK DIAGRAM

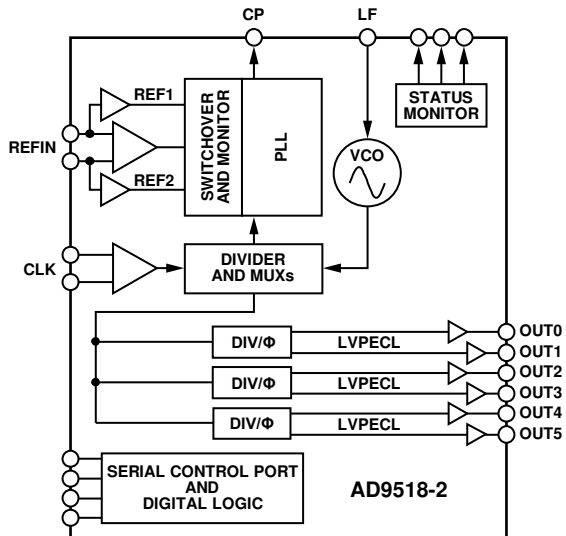


Figure 1.

06431-001

In addition, the AD9516 and AD9517 are similar to the AD9518 but have a different combination of outputs.

Each pair of outputs has dividers that allow both the divide ratio and coarse delay (or phase) to be set. The range of division for the LVPECL outputs is 1 to 32.

The AD9518-2 is available in a 48-lead LFCSP and can be operated from a single 3.3 V supply. An external VCO, which requires an extended voltage range, can be accommodated by connecting the charge pump supply (VCP) to 5 V. A separate LVPECL power supply can be from 2.5 V to 3.3 V (nominal).

The AD9518-2 is specified for operation over the industrial range of -40°C to $+85^{\circ}\text{C}$.

¹ AD9518 is used throughout the data sheet to refer to all the members of the AD9518 family. However, when AD9518-2 is used, it refers to that specific member of the AD9518 family.

Rev. C

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SPECIFICATIONS

Typical values are given for $V_S = V_{S_LVPECL} = 3.3 \text{ V} \pm 5\%$; $V_S \leq V_{CP} \leq 5.25 \text{ V}$; $T_A = 25^\circ\text{C}$; $R_{SET} = 4.12 \text{ k}\Omega$; $CP_{RSET} = 5.1 \text{ k}\Omega$, unless otherwise noted. Minimum and maximum values are given over full V_S and T_A (-40°C to $+85^\circ\text{C}$) variation.

POWER SUPPLY REQUIREMENTS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
V_S	3.135	3.3	3.465	V	$3.3 \text{ V} \pm 5\%$
V_{S_LVPECL}	2.375		V_S	V	Nominally 2.5 V to 3.3 V $\pm 5\%$
V_{CP}	V_S		5.25	V	Nominally 3.3 V to 5.0 V $\pm 5\%$
RSET Pin Resistor		4.12		k Ω	Sets internal biasing currents; connect to ground
CPRSET Pin Resistor	2.7	5.1	10	k Ω	Sets internal CP current range, nominally 4.8 mA ($CP_I_{sb} = 600 \mu\text{A}$); actual current can be calculated by $CP_I_{sb} = 3.06/CPRSET$; connect to ground
BYPASS Pin Capacitor		220		nF	Bypass for internal LDO regulator; necessary for LDO stability; connect to ground

PLL CHARACTERISTICS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VCO (ON-CHIP)					
Frequency Range	2050		2335	MHz	See Figure 11
VCO Gain (K_{VCO})		50		MHz/V	See Figure 6
Tuning Voltage (V_T)	0.5		$V_{CP} - 0.5$	V	$V_{CP} \leq V_S$ when using internal VCO; outside of this range, the CP spurs may increase due to CP up/down mismatch
Frequency Pushing (Open-Loop)		1		MHz/V	
Phase Noise at 100 kHz Offset		-107		dBc/Hz	$f = 2175 \text{ MHz}$
Phase Noise at 1 MHz Offset		-124		dBc/Hz	$f = 2175 \text{ MHz}$
REFERENCE INPUTS					
Differential Mode ($\overline{\text{REFIN}}$, $\overline{\text{REFIN}}$)					Differential mode (can accommodate single-ended input by ac grounding undriven input)
Input Frequency	0		250	MHz	Frequencies below about 1 MHz should be dc-coupled; be careful to match V_{CM} (self-bias voltage)
Input Sensitivity		250		mV p-p	PLL figure of merit (FOM) increases with increasing slew rate (see Figure 10); the input sensitivity is sufficient for ac-coupled LVPECL and LVDS signals
Self-Bias Voltage, $\overline{\text{REFIN}}$	1.35	1.60	1.75	V	Self-bias voltage of $\overline{\text{REFIN}}$ ¹
Self-Bias Voltage, $\overline{\text{REFIN}}$	1.30	1.50	1.60	V	Self-bias voltage of $\overline{\text{REFIN}}$ ¹
Input Resistance, $\overline{\text{REFIN}}$	4.0	4.8	5.9	k Ω	Self-biased ¹
Input Resistance, $\overline{\text{REFIN}}$	4.4	5.3	6.4	k Ω	Self-biased ¹
Dual Single-Ended Mode ($\overline{\text{REF1}}$, $\overline{\text{REF2}}$)					Two single-ended CMOS-compatible inputs
Input Frequency (AC-Coupled)	20		250	MHz	Slew rate $> 50 \text{ V}/\mu\text{s}$
Input Frequency (DC-Coupled)	0		250	MHz	Slew rate $> 50 \text{ V}/\mu\text{s}$; CMOS levels
Input Sensitivity (AC-Coupled)		0.8		V p-p	Should not exceed V_S p-p
Input Logic High	2.0			V	
Input Logic Low			0.8	V	
Input Current	-100		+100	μA	
Pulse Width High/Low	1.8			ns	This value determines the allowable input duty cycle and is the amount of time that a square wave is high/low
Input Capacitance		2		pF	Each pin, $\overline{\text{REFIN}}/\overline{\text{REFIN}}$ ($\overline{\text{REF1}}/\overline{\text{REF2}}$)
PHASE/FREQUENCY DETECTOR (PFD)					
PFD Input Frequency			100	MHz	Antibacklash pulse width = 1.3 ns, 2.9 ns
			45	MHz	Antibacklash pulse width = 6.0 ns
Antibacklash Pulse Width		1.3		ns	Register 0x017[1:0] = 01b
		2.9		ns	Register 0x017[1:0] = 00b; Register 0x017[1:0] = 11b
		6.0		ns	Register 0x017[1:0] = 10b

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CHARGE PUMP (CP)					CP _V is CP pin voltage; V _{CP} is charge pump power supply voltage
I _{CP} Sink/Source					Programmable
High Value		4.8		mA	With CP _{RSET} = 5.1 kΩ
Low Value		0.60		mA	
Absolute Accuracy		2.5		%	CP _V = V _{CP} /2 V
CP _{RSET} Range		2.7/10		kΩ	
I _{CP} High Impedance Mode Leakage		1		nA	
Sink-and-Source Current Matching		2		%	0.5 < CP _V < V _{CP} – 0.5 V
I _{CP} vs. CP _V		1.5		%	0.5 < CP _V < V _{CP} – 0.5 V
I _{CP} vs. Temperature		2		%	CP _V = V _{CP} /2 V
PRESCALER (PART OF N DIVIDER)					See the VCXO/VCO Feedback Divider N—P, A, B, R section
Prescaler Input Frequency					
P = 1 FD			300	MHz	
P = 2 FD			600	MHz	
P = 3 FD			900	MHz	
P = 2 DM (2/3)			200	MHz	
P = 4 DM (4/5)			1000	MHz	
P = 8 DM (8/9)			2400	MHz	
P = 16 DM (16/17)			3000	MHz	
P = 32 DM (32/33)			3000	MHz	
Prescaler Output Frequency			300	MHz	A, B counter input frequency (prescaler input frequency divided by P)
PLL DIVIDER DELAYS					Register 0x019: R, Bits[5:3]; N, Bits[2:0] (see Table 44)
000		Off		ps	
001		330		ps	
010		440		ps	
011		550		ps	
100		660		ps	
101		770		ps	
110		880		ps	
111		990		ps	
NOISE CHARACTERISTICS					
In-Band Phase Noise of the Charge Pump/Phase Frequency Detector (In-Band Is Within the LBW of the PLL)					The PLL in-band phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log(N) (where N is the value of the N divider)
At 500 kHz PFD Frequency		–165		dBc/Hz	
At 1 MHz PFD Frequency		–162		dBc/Hz	
At 10 MHz PFD Frequency		–151		dBc/Hz	
At 50 MHz PFD Frequency		–143		dBc/Hz	
PLL Figure of Merit (FOM)		–220		dBc/Hz	Reference slew rate > 0.25 V/ns; FOM + 10 log(f _{PFD}) is an approximation of the PFD/CP in-band phase noise (in the flat region) inside the PLL loop bandwidth; when running closed-loop, the phase noise, as observed at the VCO output, is increased by 20 log(N)
PLL DIGITAL LOCK DETECT WINDOW ²					Signal available at LD, STATUS, and REFMON pins when selected by appropriate register settings
Required to Lock (Coincidence of Edges)					Selected by Register 0x017[1:0] and Register 0x018[4]
Low Range (ABP 1.3 ns, 2.9 ns)		3.5		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 1b
High Range (ABP 1.3 ns, 2.9 ns)		7.5		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 0b
High Range (ABP 6.0 ns)		3.5		ns	Register 0x017[1:0] = 10b; Register 0x018[4] = 0b
To Unlock After Lock (Hysteresis) ²					
Low Range (ABP 1.3 ns, 2.9 ns)		7		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 1b
High Range (ABP 1.3 ns, 2.9 ns)		15		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 0b
High Range (ABP 6.0 ns)		11		ns	Register 0x017[1:0] = 10b; Register 0x018[4] = 0b

¹ REF_{IN} and $\overline{\text{REFIN}}$ self-bias points are offset slightly to avoid chatter on an open input condition.

² For reliable operation of the digital lock detect, the period of the PFD frequency must be greater than the unlock-after-lock time.

CLOCK INPUTS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK INPUTS (CLK, CLK)					Differential input
Input Frequency	0 ¹		2.4	GHz	High frequency distribution (VCO divider)
	0 ¹		1.6	GHz	Distribution only (VCO divider bypassed)
Input Sensitivity, Differential		150		mV p-p	Measured at 2.4 GHz; jitter performance is improved with slew rates > 1 V/ns
Input Level, Differential			2	V p-p	Larger voltage swings may turn on the protection diodes and may degrade jitter performance
Input Common-Mode Voltage, V_{CM}	1.3	1.57	1.8	V	Self-biased; enables ac coupling
Input Common-Mode Range, V_{CMR}	1.3		1.8	V	With 200 mV p-p signal applied; dc-coupled
Input Sensitivity, Single-Ended		150		mV p-p	CLK ac-coupled; CLK ac-bypassed to RF ground
Input Resistance	3.9	4.7	5.7	k Ω	Self-biased
Input Capacitance		2		pF	

¹ Below about 1 MHz, the input should be dc-coupled. Care should be taken to match V_{CM} .

CLOCK OUTPUTS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL CLOCK OUTPUTS					Termination = 50 Ω to $V_S - 2V$
OUT0, OUT1, OUT2, OUT3, OUT4, OUT5					Differential (OUT, \overline{OUT})
Output Frequency, Maximum	2950			MHz	Using direct to output; see Figure 16 for peak-to-peak differential amplitude
Output High Voltage (V_{OH})	$V_{S_LVPECL} - 1.12$	$V_{S_LVPECL} - 0.98$	$V_{S_LVPECL} - 0.84$	V	
Output Low Voltage (V_{OL})	$V_{S_LVPECL} - 2.03$	$V_{S_LVPECL} - 1.77$	$V_{S_LVPECL} - 1.49$	V	
Output Differential Voltage (V_{OD})	550	790	980	mV	This is $V_{OH} - V_{OL}$ for each leg of a differential pair for default amplitude setting with driver not toggling; the peak-to-peak amplitude measured using a differential probe across the differential pair with the driver toggling is roughly 2x these values (see Figure 16 for variation over frequency)

TIMING CHARACTERISTICS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL					Termination = 50 Ω to $V_S - 2V$; level = 810 mV
Output Rise Time, t_{RP}		70	180	ps	20% to 80%, measured differentially
Output Fall Time, t_{FP}		70	180	ps	80% to 20%, measured differentially
PROPAGATION DELAY, t_{PECL} , CLK-TO-LVPECL OUTPUT					
High Frequency Clock Distribution Configuration	835	995	1180	ps	See Figure 28
Clock Distribution Configuration Variation with Temperature	773	933	1090	ps	See Figure 30
		0.8		ps/ $^{\circ}C$	
OUTPUT SKEW, LVPECL OUTPUTS ¹					
LVPECL Outputs That Share the Same Divider		5	15	ps	
LVPECL Outputs on Different Dividers		13	40	ps	
All LVPECL Outputs Across Multiple Parts			220	ps	

¹ This is the difference between any two similar delay paths while operating at the same voltage and temperature.

CLOCK OUTPUT ADDITIVE PHASE NOISE (DISTRIBUTION ONLY; VCO DIVIDER NOT USED)

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK-TO-LVPECL ADDITIVE PHASE NOISE					Distribution section only; does not include PLL and VCO
CLK = 1 GHz, Output = 1 GHz Divider = 1					Input slew rate > 1 V/ns
At 10 Hz Offset		-109		dBc/Hz	
At 100 Hz Offset		-118		dBc/Hz	
At 1 kHz Offset		-130		dBc/Hz	
At 10 kHz Offset		-139		dBc/Hz	
At 100 kHz Offset		-144		dBc/Hz	
At 1 MHz Offset		-146		dBc/Hz	
At 10 MHz Offset		-147		dBc/Hz	
At 100 MHz Offset		-149		dBc/Hz	
CLK = 1 GHz, Output = 200 MHz Divider = 5					Input slew rate > 1 V/ns
At 10 Hz Offset		-120		dBc/Hz	
At 100 Hz Offset		-126		dBc/Hz	
At 1 kHz Offset		-139		dBc/Hz	
At 10 kHz Offset		-150		dBc/Hz	
At 100 kHz Offset		-155		dBc/Hz	
At 1 MHz Offset		-157		dBc/Hz	
>10 MHz Offset		-157		dBc/Hz	

CLOCK OUTPUT ABSOLUTE PHASE NOISE (INTERNAL VCO USED)

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL ABSOLUTE PHASE NOISE					Internal VCO; direct to LVPECL output
VCO = 2.335 GHz; Output = 2.335 GHz					
At 1 kHz Offset		-46		dBc/Hz	
At 10 kHz Offset		-78		dBc/Hz	
At 100 kHz Offset		-105		dBc/Hz	
At 1 MHz Offset		-124		dBc/Hz	
At 10 MHz Offset		-141		dBc/Hz	
At 40 MHz Offset		-146		dBc/Hz	
VCO = 2.175 GHz; Output = 2.175 GHz					
At 1 kHz Offset		-51		dBc/Hz	
At 10 kHz Offset		-80		dBc/Hz	
At 100 kHz Offset		-107		dBc/Hz	
At 1 MHz Offset		-124		dBc/Hz	
At 10 MHz Offset		-142		dBc/Hz	
At 40 MHz Offset		-146		dBc/Hz	
VCO = 2.05 GHz; Output = 2.05 GHz					
At 1 kHz Offset		-53		dBc/Hz	
At 10 kHz Offset		-82		dBc/Hz	
At 100 kHz Offset		-108		dBc/Hz	
At 1 MHz Offset		-127		dBc/Hz	
At 10 MHz Offset		-142		dBc/Hz	
At 40 MHz Offset		-147		dBc/Hz	

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING INTERNAL VCO)

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup where the reference source is clean, so a wider PLL loop bandwidth is used; reference = 15.36 MHz; R = 1
VCO = 2.21 GHz; LVPECL = 245.76 MHz; PLL LBW = 138 kHz		146		fs rms	Integration BW = 200 kHz to 10 MHz
		329		fs rms	Integration BW = 12 kHz to 20 MHz
VCO = 2.21 GHz; LVPECL = 122.88 MHz; PLL LBW = 138 kHz		151		fs rms	Integration BW = 200 kHz to 10 MHz
		329		fs rms	Integration BW = 12 kHz to 20 MHz
VCO = 2.21 GHz; LVPECL = 61.44 MHz; PLL LBW = 138 kHz		203		fs rms	Integration BW = 200 kHz to 10 MHz
		376		fs rms	Integration BW = 12 kHz to 20 MHz

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK CLEANUP USING INTERNAL VCO)

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup where the reference source is jittery, so a narrower PLL loop bandwidth is used; reference = 10.0 MHz; R = 20
VCO = 2.18 GHz; LVPECL = 155.52 MHz; PLL LBW = 125 Hz		515		fs rms	Integration BW = 12 kHz to 20 MHz
VCO = 2.21 GHz; LVPECL = 122.88 MHz; PLL LBW = 125 Hz		570		fs rms	Integration BW = 12 kHz to 20 MHz

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING EXTERNAL VCXO)

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup using an external 245.76 MHz VCXO (Toyocom TCO-2112); reference = 15.36 MHz; R = 1
LVPECL = 245.76 MHz; PLL LBW = 125 Hz		54		fs rms	Integration BW = 200 kHz to 5 MHz
		77		fs rms	Integration BW = 200 kHz to 10 MHz
		109		fs rms	Integration BW = 12 kHz to 20 MHz
LVPECL = 122.88 MHz; PLL LBW = 125 Hz		79		fs rms	Integration BW = 200 kHz to 5 MHz
		114		fs rms	Integration BW = 200 kHz to 10 MHz
		163		fs rms	Integration BW = 12 kHz to 20 MHz
LVPECL = 61.44 MHz; PLL LBW = 125 Hz		124		fs rms	Integration BW = 200 kHz to 5 MHz
		176		fs rms	Integration BW = 200 kHz to 10 MHz
		259		fs rms	Integration BW = 12 kHz to 20 MHz

CLOCK OUTPUT ADDITIVE TIME JITTER (VCO DIVIDER NOT USED)

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; uses rising edge of clock signal
CLK = 622.08 MHz; LVPECL = 622.08 MHz; Divider = 1		40		fs rms	BW = 12 kHz to 20 MHz
CLK = 622.08 MHz; LVPECL = 155.52 MHz; Divider = 4		80		fs rms	BW = 12 kHz to 20 MHz
CLK = 1.6 GHz; LVPECL = 100 MHz; Divider = 16		215		fs rms	Calculated from SNR of ADC method; DCC not used for even divides
CLK = 500 MHz; LVPECL = 100 MHz; Divider = 5		245		fs rms	Calculated from SNR of ADC method; DCC on

CLOCK OUTPUT ADDITIVE TIME JITTER (VCO DIVIDER USED)

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; uses rising edge of clock signal
CLK = 2.4 GHz; VCO DIV = 2; LVPECL = 100 MHz; Divider = 12; Duty-Cycle Correction = Off		210		fs rms	Calculated from SNR of ADC method

SERIAL CONTROL PORT

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{\text{CS}}$ (INPUT)					$\overline{\text{CS}}$ has an internal 30 k Ω pull-up resistor
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current			3	μA	
Input Logic 0 Current		110		μA	
Input Capacitance		2		pF	
SCLK (INPUT)					SCLK has an internal 30 k Ω pull-down resistor
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		110		μA	
Input Logic 0 Current			1	μA	
Input Capacitance		2		pF	
SDIO (WHEN INPUT)					
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		10		nA	
Input Logic 0 Current		20		nA	
Input Capacitance		2		pF	
SDIO, SDO (OUTPUTS)					
Output Logic 1 Voltage	2.7			V	
Output Logic 0 Voltage			0.4	V	
TIMING					
Clock Rate (SCLK, $1/t_{\text{SCLK}}$)			25	MHz	
Pulse Width High, t_{HIGH}	16			ns	
Pulse Width Low, t_{LOW}	16			ns	
SDIO to SCLK Setup, t_{DS}	2			ns	
SCLK to SDIO Hold, t_{DH}	1.1			ns	
SCLK to Valid SDIO and SDO, t_{DV}			8	ns	
$\overline{\text{CS}}$ to SCLK Setup and Hold, $t_{\text{S, TH}}$	2			ns	
$\overline{\text{CS}}$ Minimum Pulse Width High, t_{PWH}	3			ns	

PD, SYNC, AND RESET PINS

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT CHARACTERISTICS					These pins each have a 30 k Ω internal pull-up resistor
Logic 1 Voltage	2.0			V	
Logic 0 Voltage			0.8	V	
Logic 1 Current			1	μA	
Logic 0 Current		110		μA	
Capacitance		2		pF	
RESET TIMING					
Pulse Width Low	50			ns	
SYNC TIMING					
Pulse Width Low	1.5			High speed clock cycles	High speed clock is CLK input signal

LD, STATUS, AND REFMON PINS

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS					When selected as a digital output (CMOS); there are other modes in which these pins are not CMOS digital outputs; see Table 44, Register 0x017, Register 0x01A, and Register 0x01B
Output Voltage High (V_{OH})	2.7			V	
Output Voltage Low (V_{OL})			0.4	V	
MAXIMUM TOGGLE RATE		100		MHz	Applies when mux is set to any divider or counter output, or PFD up/down pulse; also applies in analog lock detect mode; usually debug mode only; beware that spurs may couple to output when any of these pins are toggling
ANALOG LOCK DETECT Capacitance		3		pF	On-chip capacitance; used to calculate RC time constant for analog lock detect readback; use a pull-up resistor
REF1, REF2, AND VCO FREQUENCY STATUS MONITOR Normal Range	1.02			MHz	Frequency above which the monitor always indicates the presence of the reference
Extended Range (REF1 and REF2 Only)	8			kHz	Frequency above which the monitor always indicates the presence of the reference
LD PIN COMPARATOR Trip Point		1.6		V	
Hysteresis		260		mV	

POWER DISSIPATION

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION, CHIP					
Power-On Default		0.76	1.0	W	No clock; no programming; default register values; does not include power dissipated in external resistors
Full Operation		1.1	1.7	W	PLL on; internal VCO = 2335 MHz; VCO divider = 2; all channel dividers on; six LVPECL outputs at 584 MHz; does not include power dissipated in external resistors
\overline{PD} Power-Down		75	185	mW	\overline{PD} pin pulled low; does not include power dissipated in terminations
\overline{PD} Power-Down, Maximum Sleep		31		mW	\overline{PD} pin pulled low; PLL power-down, Register 0x010[1:0] = 01b; SYNC power-down, Register 0x230[2] = 1b; REF for distribution power-down, Register 0x230[1] = 1b
V_{CP} Supply		4	4.8	mW	PLL operating; typical closed-loop configuration
POWER DELTAS, INDIVIDUAL FUNCTIONS					
VCO Divider		30		mW	VCO divider bypassed
REFIN (Differential)		20		mW	All references off to differential reference enabled
REF1, REF2 (Single-Ended)		4		mW	All references off to REF1 or REF2 enabled; differential reference not enabled
VCO		70		mW	CLK input selected to VCO selected
PLL		75		mW	PLL off to PLL on, normal operation; no reference enabled
Channel Divider		30		mW	Divider bypassed to divide-by-2 to divide-by-32
LVPECL Channel (Divider Plus Output Driver)		160		mW	No LVPECL output on to one LVPECL output on, independent of frequency
LVPECL Driver		90		mW	Second LVPECL output turned on, same channel

TIMING DIAGRAMS

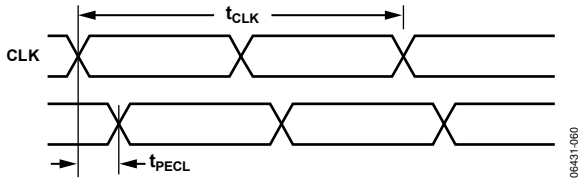


Figure 2. CLK/ $\overline{\text{CLK}}$ to Clock Output Timing, DIV = 1

06431-060

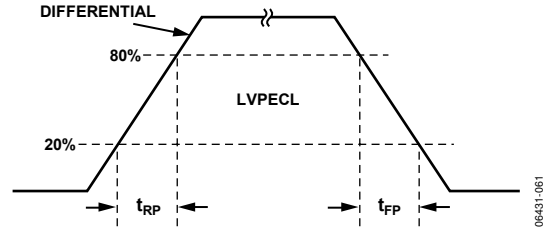


Figure 3. LVPECL Timing, Differential

06431-061

ABSOLUTE MAXIMUM RATINGS

Table 17.

Parameter	Rating
VS, VS_LVPECL to GND	−0.3 V to +3.6 V
VCP to GND	−0.3 V to +5.8 V
REFIN, $\overline{\text{REFIN}}$ to GND	−0.3 V to $V_S + 0.3$ V
REFIN to $\overline{\text{REFIN}}$	−3.3 V to +3.3 V
RSET to GND	−0.3 V to $V_S + 0.3$ V
CPRSET to GND	−0.3 V to $V_S + 0.3$ V
CLK, $\overline{\text{CLK}}$ to GND	−0.3 V to $V_S + 0.3$ V
CLK to $\overline{\text{CLK}}$	−1.2 V to +1.2 V
SCLK, SDIO, SDO, $\overline{\text{CS}}$ to GND	−0.3 V to $V_S + 0.3$ V
OUT0, $\overline{\text{OUT0}}$, OUT1, $\overline{\text{OUT1}}$, OUT2, $\overline{\text{OUT2}}$, OUT3, $\overline{\text{OUT3}}$, OUT4, $\overline{\text{OUT4}}$, OUT5, $\overline{\text{OUT5}}$ to GND	−0.3 V to $V_S + 0.3$ V
$\overline{\text{SYNC}}$ to GND	−0.3 V to $V_S + 0.3$ V
REFMON, STATUS, LD to GND	−0.3 V to $V_S + 0.3$ V
Junction Temperature ¹	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 sec)	300°C

¹ See Table 18 for θ_{JA} .

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 18.

Package Type ¹	θ_{JA}	Unit
48-Lead LFCSP	24.7	°C/W

¹ Thermal impedance measurements were taken on a 4-layer board in still air in accordance with EIA/JESD51-2.

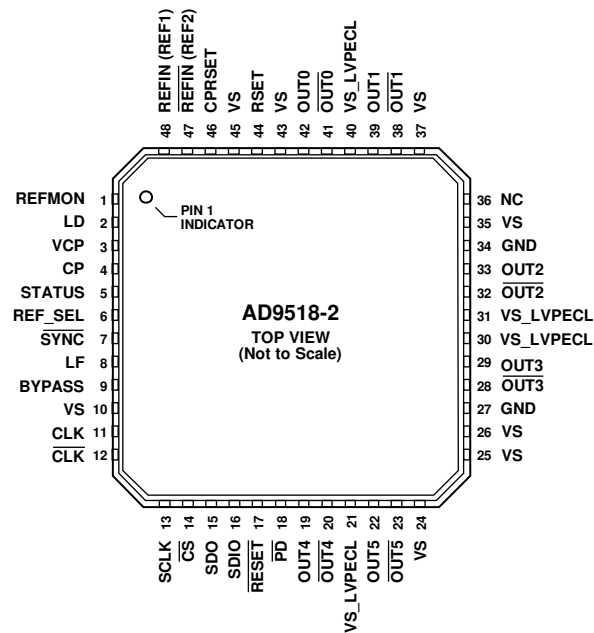
ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES
1. NC = NO CONNECT.
 2. THE EXTERNAL PADDLE ON THE BOTTOM OF THE PACKAGE MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

Figure 4. Pin Configuration

Table 19. Pin Function Descriptions

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
1	O	3.3 V CMOS	REFMON	Reference Monitor (Output). This pin has multiple selectable outputs; see Table 44, Register 0x01B.
2	O	3.3 V CMOS	LD	Lock Detect (Output). This pin has multiple selectable outputs; see Table 44, Register 0x01A.
3	I	Power	VCP	Power Supply for Charge Pump (CP). $V_S \leq V_{CP} \leq 5.0\text{ V}$. This pin is usually 3.3 V for most applications; but if a 5 V external VCXO is used, this pin should be 5 V.
4	O		CP	Charge Pump (Output). Connects to external loop filter.
5	O	3.3 V CMOS	STATUS	Status (Output). This pin has multiple selectable outputs; see Table 44, Register 0x017.
6	I	3.3 V CMOS	REF_SEL	Reference Select. Selects REF1 (low) or REF2 (high). This pin has an internal 30 k Ω pull-down resistor.
7	I	3.3 V CMOS	SYNC	Manual Synchronizations and Manual Holdover. This pin initiates a manual synchronization and is used for manual holdover. Active low. This pin has an internal 30 k Ω pull-up resistor.
8	I	Loop filter	LF	Loop Filter (Input). Connects to VCO control voltage node internally. This pin has 31 pF of internal capacitance to ground, which may influence the loop filter design for large loop bandwidths.
9	O	Loop filter	BYPASS	This pin is for bypassing the LDO to ground with a capacitor.
10, 24, 25, 26, 35, 37, 43, 45	I	Power	VS	3.3 V Power Pins.
11	I	Differential clock input	CLK	Along with $\overline{\text{CLK}}$, this is the self-biased differential input for the clock distribution section. This pin can be left floating if internal VCO is used.
12	I	Differential clock input	$\overline{\text{CLK}}$	Along with CLK, this is the self-biased differential input for the clock distribution section. This pin can be left floating if internal VCO is used.

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
13	I	3.3 V CMOS	SCLK	Serial Control Port Data Clock Signal.
14	I	3.3 V CMOS	\overline{CS}	Serial Control Port Chip Select, Active Low. This pin has an internal 30 k Ω pull-up resistor.
15	O	3.3 V CMOS	SDO	Serial Control Port. Unidirectional serial data output.
16	I/O	3.3 V CMOS	SDIO	Serial Control Port. Bidirectional serial data input/output.
17	I	3.3 V CMOS	\overline{RESET}	Chip Reset, Active Low. This pin has an internal 30 k Ω pull-up resistor.
18	I	3.3 V CMOS	\overline{PD}	Chip Power Down, Active Low. This pin has an internal 30 k Ω pull-up resistor.
19	O	LVPECL	$\overline{OUT4}$	LVPECL Output; One Side of a Differential LVPECL Output.
20	O	LVPECL	$\overline{OUT4}$	LVPECL Output; One Side of a Differential LVPECL Output.
21, 30, 31, 40	I	Power	VS_LVPECL	Extended Voltage 2.5 V to 3.3 V LVPECL Power Pins.
22	O	LVPECL	$\overline{OUT5}$	LVPECL Output; One Side of a Differential LVPECL Output.
23	O	LVPECL	$\overline{OUT5}$	LVPECL Output; One Side of a Differential LVPECL Output.
27, 34		GND	GND	Ground. See the description for EPAD.
28	O	LVPECL	$\overline{OUT3}$	LVPECL Output; One Side of a Differential LVPECL Output.
29	O	LVPECL	$\overline{OUT3}$	LVPECL Output; One Side of a Differential LVPECL Output.
32	O	LVPECL	$\overline{OUT2}$	LVPECL Output; One Side of a Differential LVPECL Output.
33	O	LVPECL	OUT2	LVPECL Output; One Side of a Differential LVPECL Output.
36			NC	No Connection.
38	O	LVPECL	$\overline{OUT1}$	LVPECL Output; One Side of a Differential LVPECL Output.
39	O	LVPECL	OUT1	LVPECL Output; One Side of a Differential LVPECL Output.
41	O	LVPECL	$\overline{OUT0}$	LVPECL Output; One Side of a Differential LVPECL Output.
42	O	LVPECL	OUT0	LVPECL Output; One Side of a Differential LVPECL Output.
44	O	Current set resistor	RSET	Resistor connected here sets internal bias currents. Nominal value = 4.12 k Ω .
46	O	Current set resistor	CPRSET	Resistor connected here sets the CP current range. Nominal value = 5.1 k Ω .
47	I	Reference input	\overline{REFIN} (REF2)	Along with \overline{REFIN} , this is the self-biased differential input for the PLL reference. Alternatively, this pin is a single-ended input for REF2.
48	I	Reference input	REFIN (REF1)	Along with \overline{REFIN} , this is the self-biased differential input for the PLL reference. Alternatively, this pin is a single-ended input for REF1.
EPAD		GND	GND	Ground. The external paddle on the bottom of the package must be connected to ground for proper operation.

TYPICAL PERFORMANCE CHARACTERISTICS

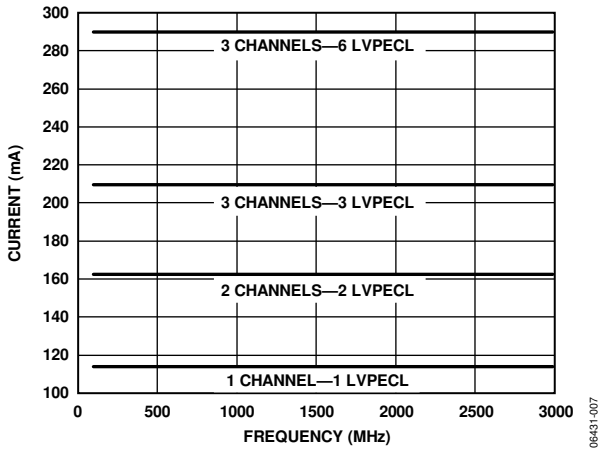


Figure 5. Current vs. Frequency, Direct-to-Output, LVPECL Outputs

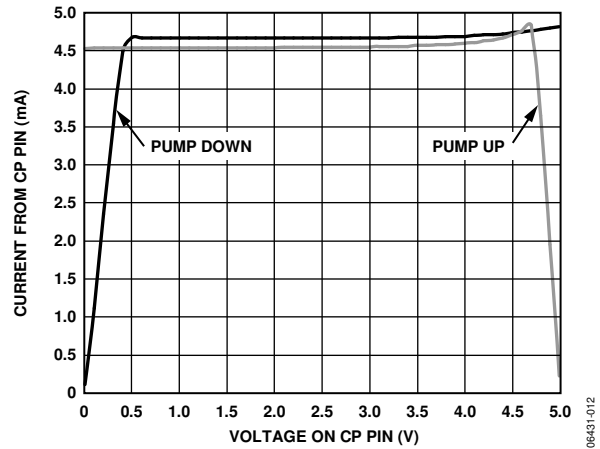


Figure 8. Charge Pump Characteristics at $V_{CP} = 5.0 V$

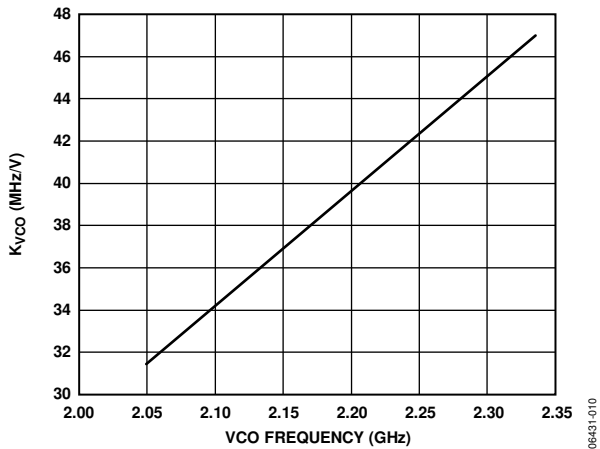


Figure 6. K_{VCO} vs. VCO Frequency

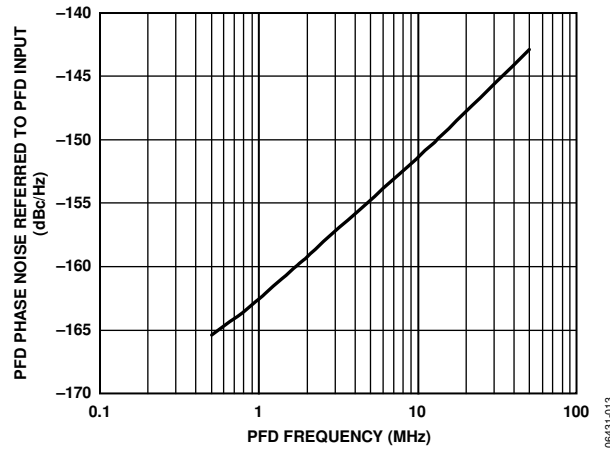


Figure 9. PFD Phase Noise Referred to PFD Input vs. PFD Frequency

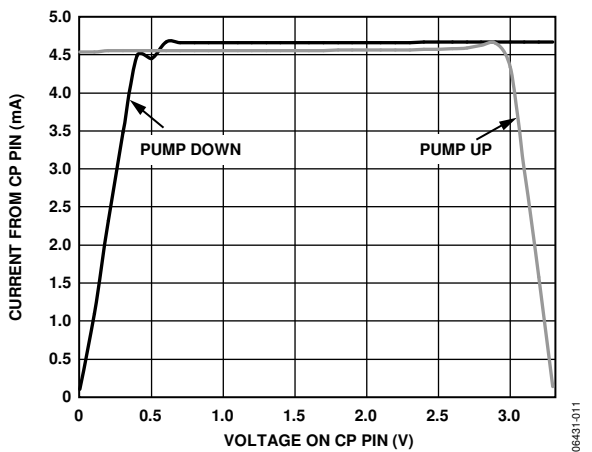


Figure 7. Charge Pump Characteristics at $V_{CP} = 3.3 V$

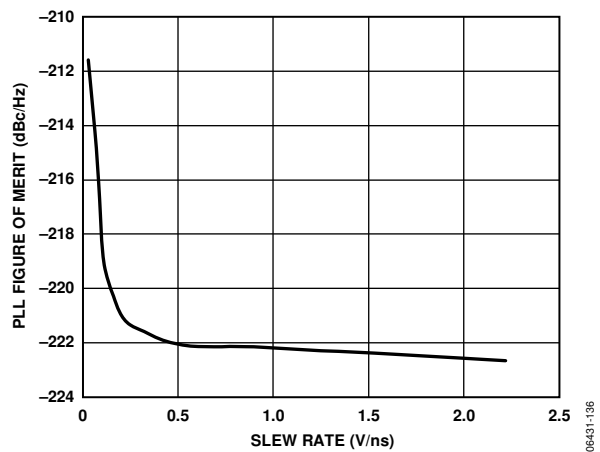


Figure 10. PLL Figure of Merit (FOM) vs. Slew Rate at $\overline{REFIN/REFIN}$

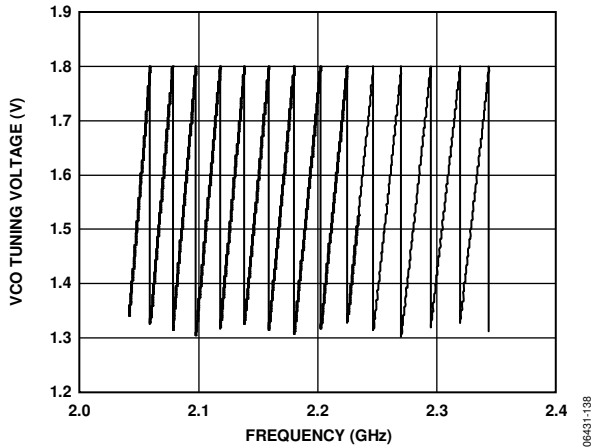


Figure 11. VCO Tuning Voltage vs. Frequency
(Note that VCO calibration centers the dc tuning voltage for the PLL setup that is active during calibration.)

06431-138

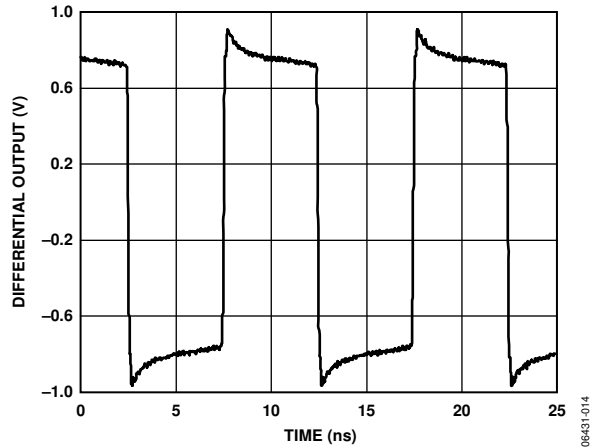


Figure 14. LVPECL Output (Differential) at 100 MHz

06431-014

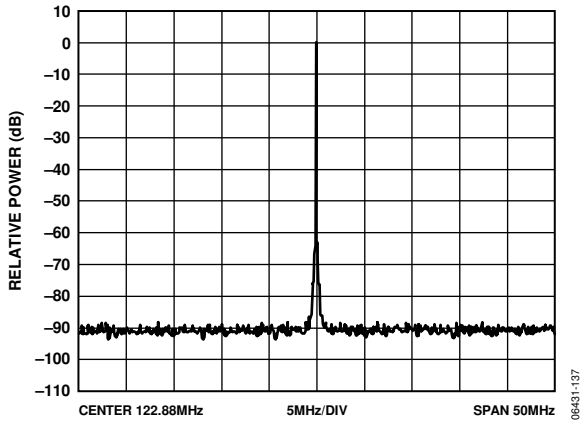


Figure 12. PFD/CP Spurs; 122.88 MHz; PFD = 15.36 MHz;
LBW = 138 kHz; $I_{CP} = 3.0$ mA; $f_{VCO} = 2.21$ GHz

06431-137

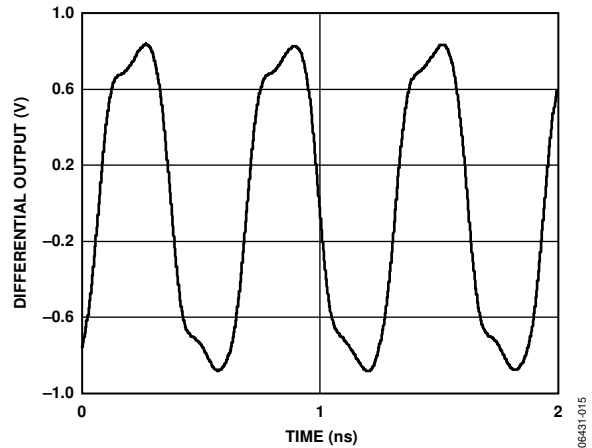


Figure 15. LVPECL Output (Differential) at 1600 MHz

06431-015

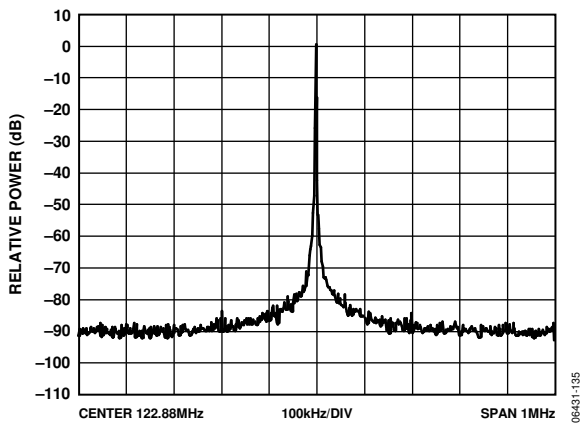


Figure 13. Output Spectrum, LVPECL; 122.88 MHz; PFD = 15.36 MHz;
LBW = 138 kHz; $I_{CP} = 3.0$ mA; $f_{VCO} = 2.21$ GHz

06431-135

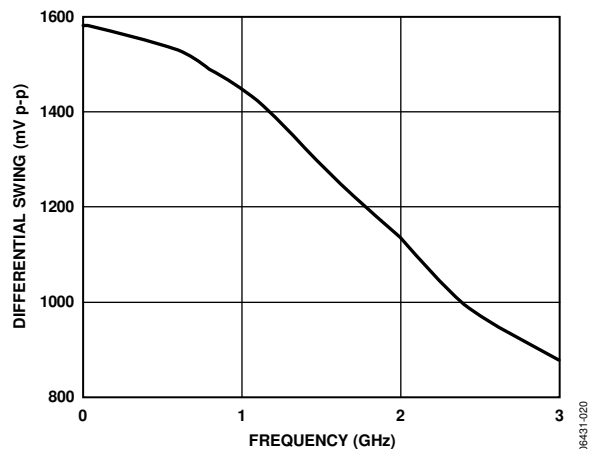


Figure 16. LVPECL Differential Swing vs. Frequency,
Using a Differential Probe Across the Output Pair

06431-020

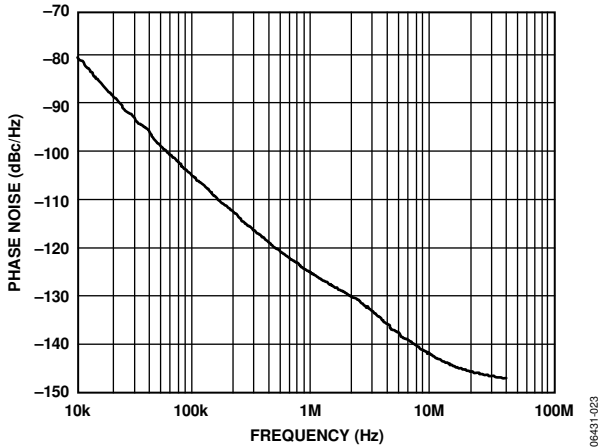


Figure 17. Internal VCO Phase Noise (Absolute) Direct to LVPECL at 2335 MHz

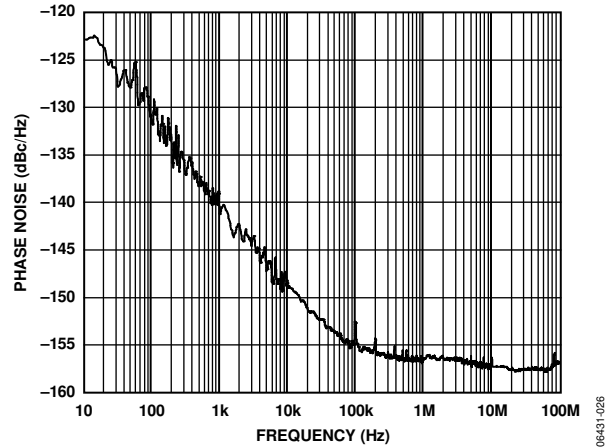


Figure 20. Phase Noise (Additive) LVPECL at 245.76 MHz, Divide-by-1

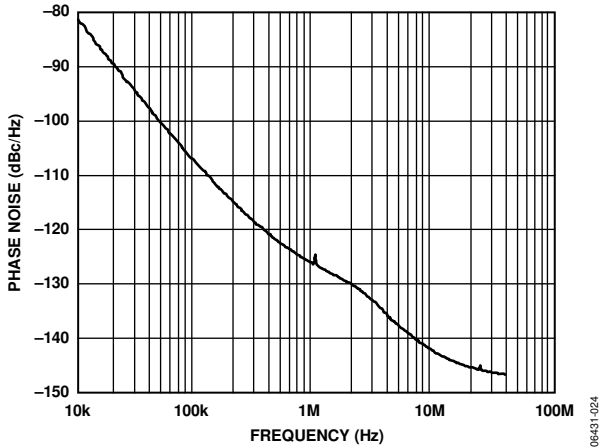


Figure 18. Internal VCO Phase Noise (Absolute) Direct to LVPECL at 2175 MHz

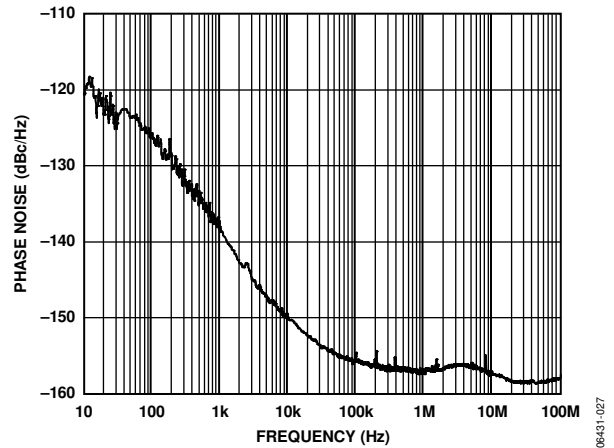


Figure 21. Phase Noise (Additive) LVPECL at 200 MHz, Divide-by-5

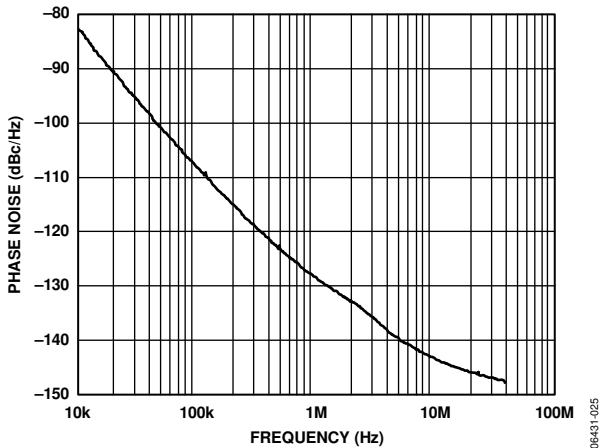


Figure 19. Internal VCO Phase Noise (Absolute) Direct to LVPECL at 2050 MHz

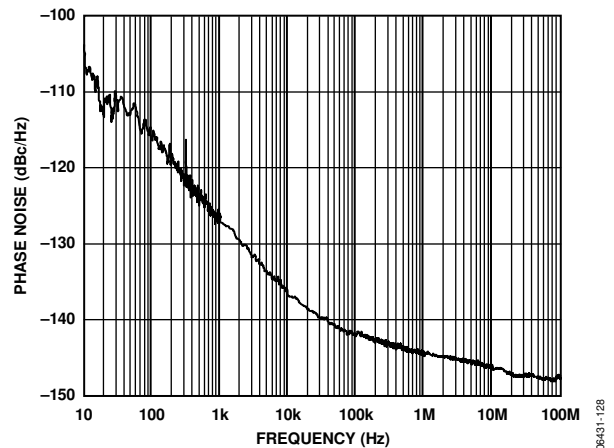


Figure 22. Phase Noise (Additive) LVPECL at 1600 MHz, Divide-by-1

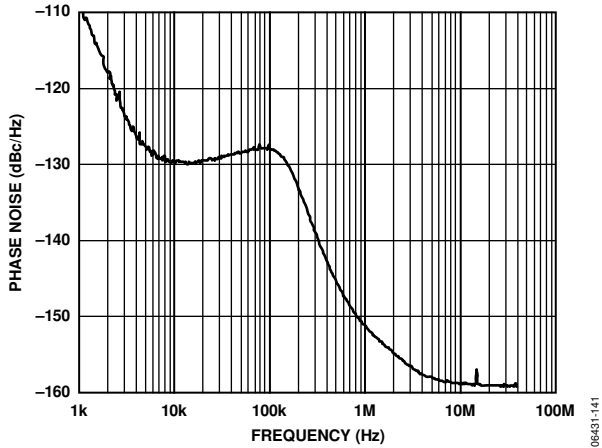


Figure 23. Phase Noise (Absolute) Clock Generation; Internal VCO at 2.21 GHz; PFD = 15.36 MHz; LBW = 138 kHz; LVPECL Output = 122.88 MHz

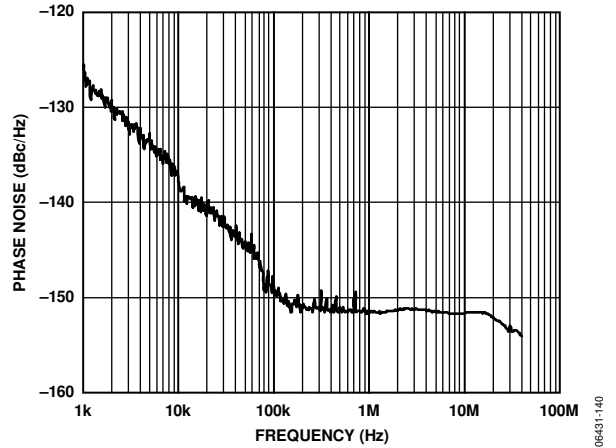


Figure 25. Phase Noise (Absolute); External VCXO (Toyocom TCO-2112) at 245.76 MHz; PFD = 15.36 MHz; LBW = 250 Hz; LVPECL Output = 245.76 MHz

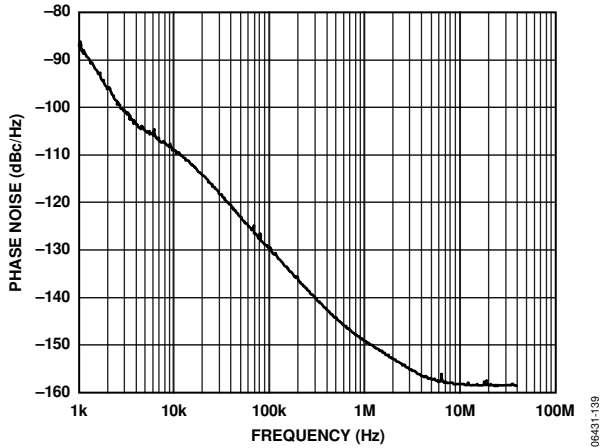


Figure 24. Phase Noise (Absolute) Clock Cleanup; Internal VCO at 2.18 GHz; PFD = 19.44 MHz; LBW = 12.8 kHz; LVPECL Output = 155.52 MHz

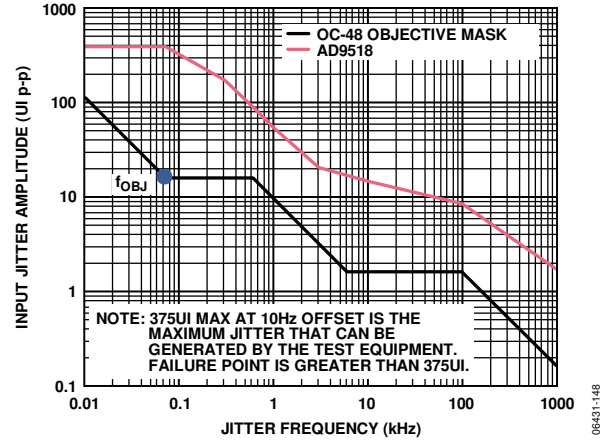


Figure 26. GR-253 Jitter Tolerance Plot

TERMINOLOGY

Phase Jitter and Phase Noise

An ideal sine wave can be thought of as having a continuous and even progression of phase with time from 0° to 360° for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time. This phenomenon is called phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, which is characterized statistically as being Gaussian (normal) in distribution.

This phase jitter leads to a spreading out of the energy of the sine wave in the frequency domain, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in dB) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

It is meaningful to integrate the total power contained within some interval of offset frequencies (for example, 10 kHz to 10 MHz). This is called the integrated phase noise over that frequency offset interval and can be readily related to the time jitter due to the phase noise within that offset frequency interval.

Phase noise has a detrimental effect on the performance of ADCs, DACs, and RF mixers. It lowers the achievable dynamic range of the converters and mixers, although they are affected in somewhat different ways.

Time Jitter

Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings varies. In a square wave, the time jitter is a displacement of the

edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in units of seconds root mean square (rms) or 1 sigma of the Gaussian distribution.

Time jitter that occurs on a sampling clock for a DAC or an ADC decreases the signal-to-noise ratio (SNR) and dynamic range of the converter. A sampling clock with the lowest possible jitter provides the highest performance from a given converter.

Additive Phase Noise

Additive phase noise is the amount of phase noise that can be attributed to the device or subsystem being measured. The phase noise of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device impacts the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contributes its own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise. When there are multiple contributors to phase noise, the total is the square root of the sum of squares of the individual contributors.

Additive Time Jitter

Additive time jitter is the amount of time jitter that can be attributed to the device or subsystem being measured. The time jitter of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device impacts the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contributes its own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.

DETAILED BLOCK DIAGRAM

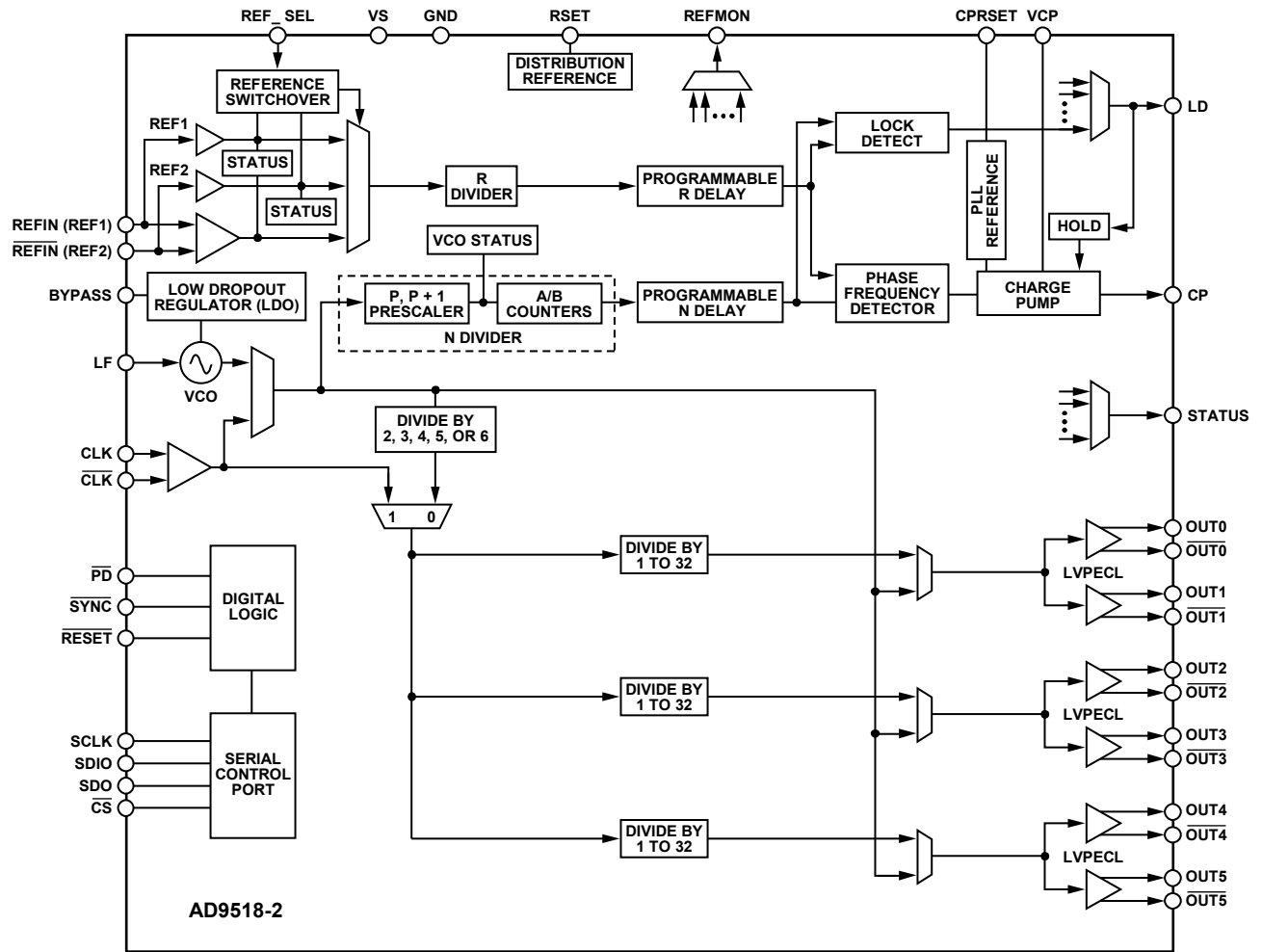


Figure 27. Detailed Block Diagram

06431-022

THEORY OF OPERATION

OPERATIONAL CONFIGURATIONS

The AD9518 can be configured in several ways. These configurations must be set up by loading the control registers (see Table 42 and Table 43 through Table 49). Each section or function must be individually programmed by setting the appropriate bits in the corresponding control register or registers.

High Frequency Clock Distribution—CLK or External VCO > 1600 MHz

The AD9518 power-up default configuration has the PLL powered off and the routing of the input set so that the CLK/CLK input is connected to the distribution section through the VCO divider (divide-by-2/divide-by-3/divide-by-4/divide-by-5/divide-by-6). This is a distribution-only mode that allows for an external input up to 2.4 GHz (see Table 3). The maximum frequency that can be applied to the channel dividers is 1600 MHz; therefore, higher input frequencies must be divided down before reaching the channel dividers. This input routing can also be used for lower input frequencies, but the minimum divide is 2 before the channel dividers.

When the PLL is enabled, this routing also allows the use of the PLL with an external VCO or VCXO with a frequency of less than 2400 MHz. In this configuration, the internal VCO is not used and is powered off. The external VCO/VCXO feeds directly into the prescaler.

The register settings shown in Table 20 are the default values of these registers at power-up or after a reset operation. If the contents of the registers are altered by prior programming after power-up or reset, these registers can also be set intentionally to these values.

After the appropriate register values are programmed, Register 0x232 must be set to 0x01 for the values to take effect.

Table 20. Default Settings of Some PLL Registers

Register	Function
0x010[1:0] = 01b	PLL asynchronous power-down (PLL off).
0x1E0[2:0] = 010b	Set VCO divider = 4.
0x1E1[0] = 0b	Use the VCO divider.
0x1E1[1] = 0b	CLK selected as the source.

When using the internal PLL with an external VCO, the PLL must be turned on.

Table 21. Settings When Using an External VCO

Register	Function
0x010[1:0] = 00b	PLL normal operation (PLL on).
0x010 to 0x01D	PLL settings. Select and enable a reference input; set R, N (P, A, B), PFD polarity, and I_{CP} , according to the intended loop configuration.
0x1E1[1] = 0b	CLK selected as the source.

An external VCO requires an external loop filter that must be connected between CP and the tuning pin of the VCO. This loop filter determines the loop bandwidth and stability of the PLL. Make sure to select the proper PFD polarity for the VCO being used.

Table 22. Setting the PFD Polarity

Register	Function
0x010[7] = 0b	PFD polarity positive (higher control voltage produces higher frequency).
0x010[7] = 1b	PFD polarity negative (higher control voltage produces lower frequency).

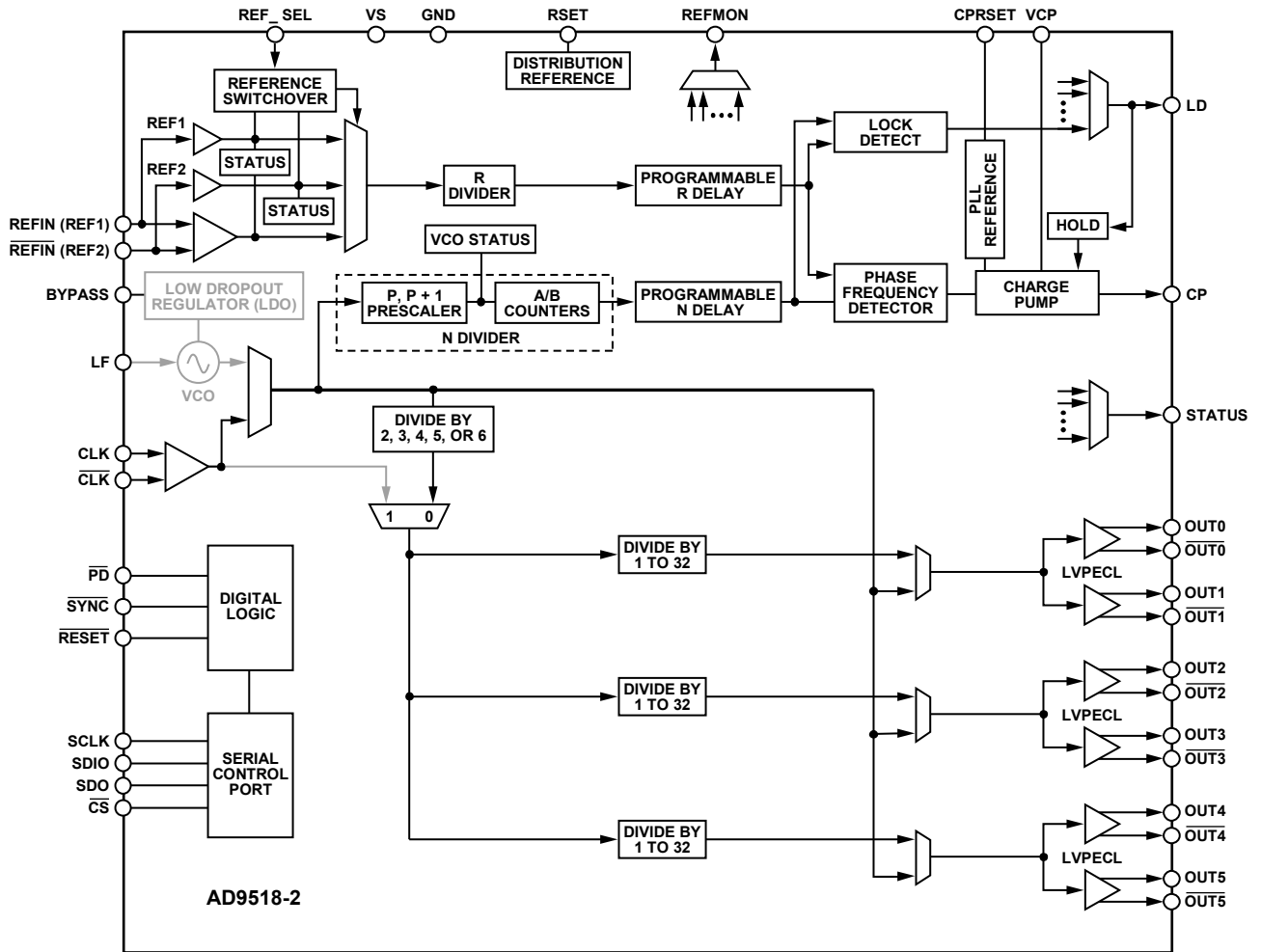


Figure 28. High Frequency Clock Distribution or External VCO > 1600 MHz

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Internal VCO and Clock Distribution

When using the internal VCO and PLL, the VCO divider must be employed to ensure that the frequency presented to the channel dividers does not exceed their specified maximum frequency of 1600 MHz (see Table 3). The internal PLL uses an external loop filter to set the loop bandwidth. The external loop filter is also crucial to the loop stability.

When using the internal VCO, it is necessary to calibrate the VCO (Register 0x018[0]) to ensure optimal performance.

For internal VCO and clock distribution applications, use the register settings that are shown in Table 23.

Table 23. Settings When Using an Internal VCO

Register	Function
0x010[1:0] = 00b	PLL normal operation (PLL on).
0x010 to 0x01D	PLL settings. Select and enable a reference input; set R, N (P, A, B), PFD polarity, and I _{CP} according to the intended loop configuration.
0x018[0] = 0b, 0x232[0] = 1b	Reset VCO calibration. This process is not required the first time after power-up, but it must be performed subsequently.
0x1E0[2:0]	Set VCO divider to divide-by-2, divide-by-3, divide-by-4, divide-by-5, or divide-by-6.
0x1E1[0] = 0b	Use VCO divider as the source for the distribution section.
0x1E1[1] = 1b	Select VCO as the source.
0x018[0] = 1b, 0x232[0] = 1b	Initiate VCO calibration.

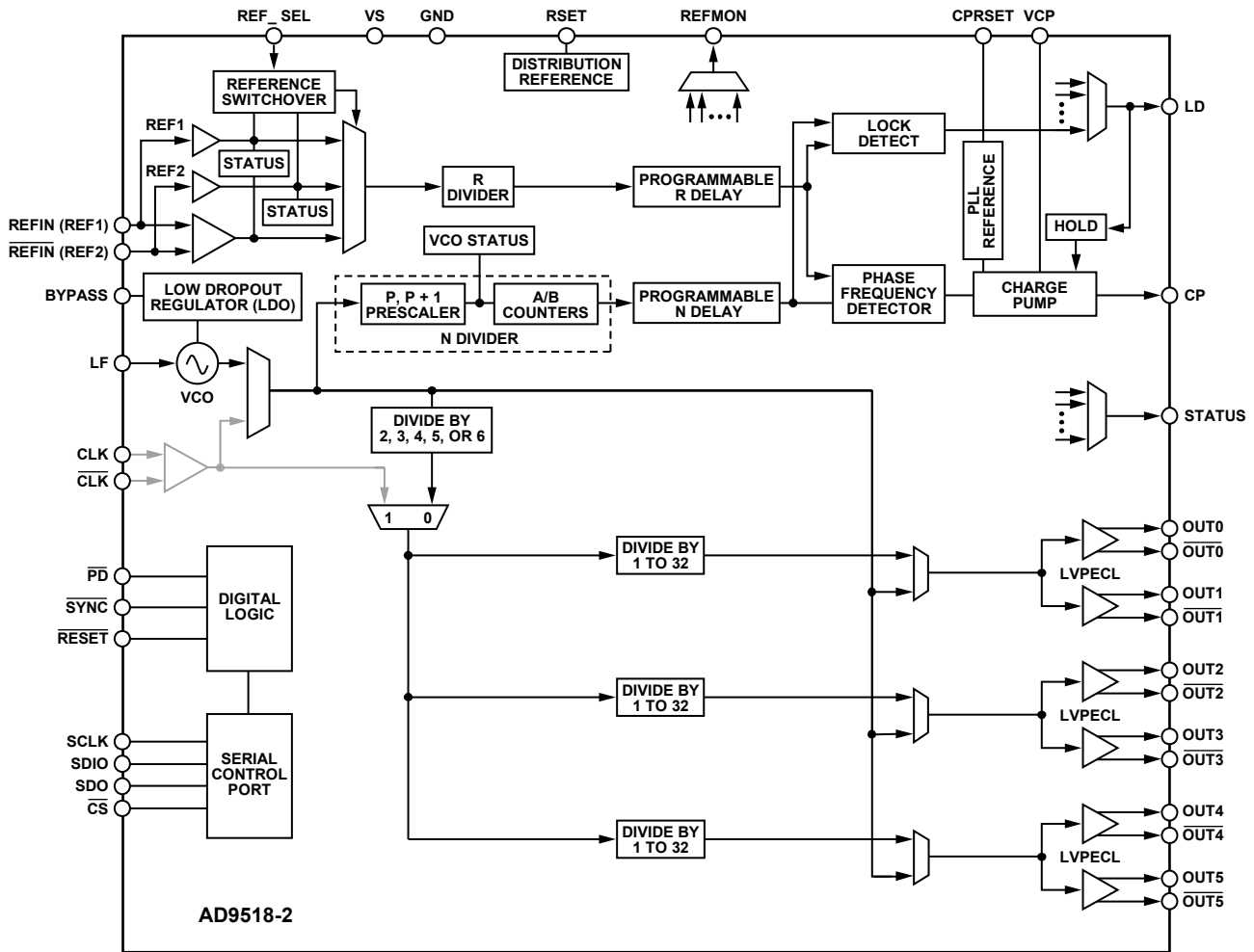


Figure 29. Internal VCO and Clock Distribution

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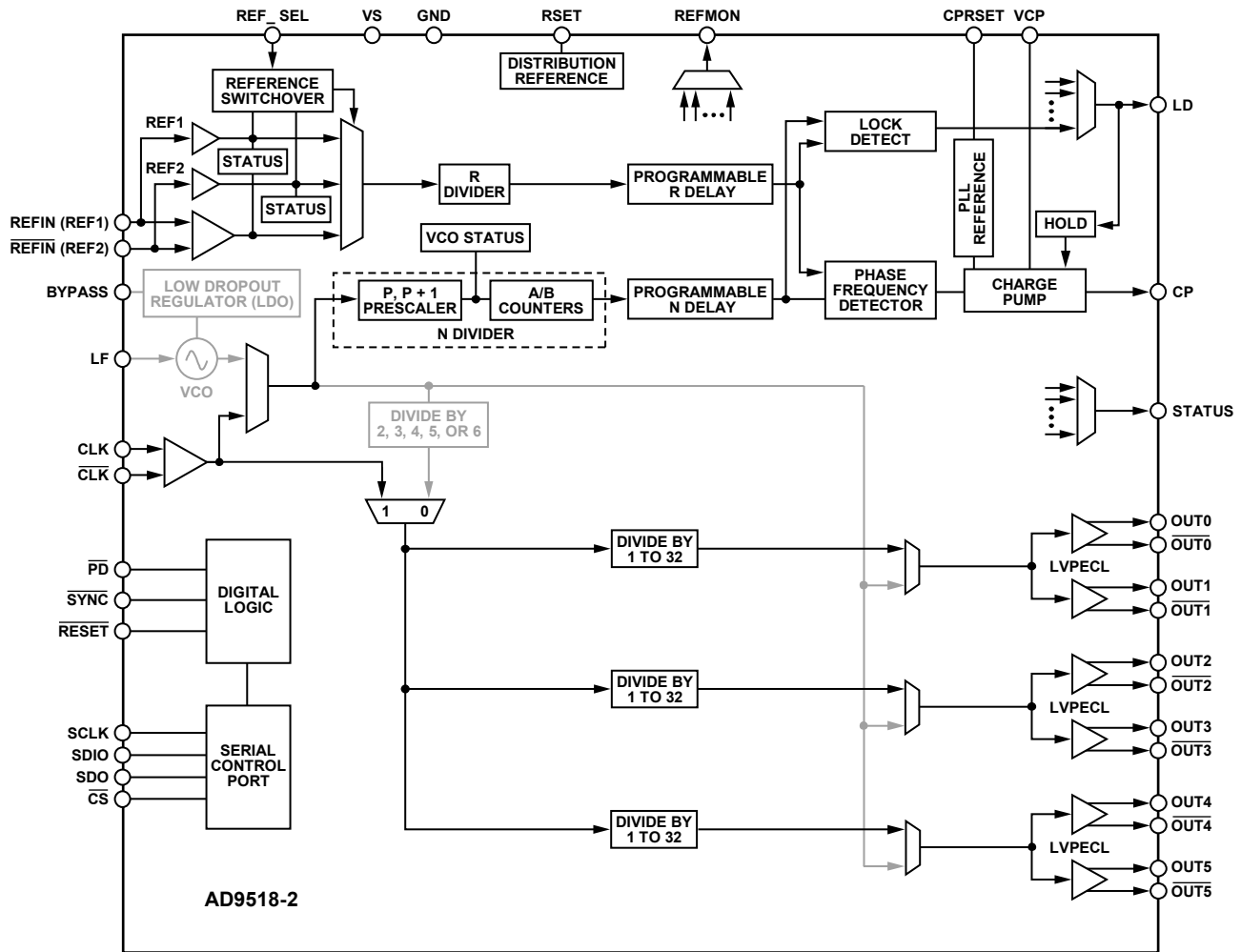


Figure 30. Clock Distribution or External VCO < 1600 MHz

Clock Distribution or External VCO < 1600 MHz

When the external clock source to be distributed or the external VCO/VCXO is less than 1600 MHz, a configuration that bypasses the VCO divider can be used. This configuration differs from the High Frequency Clock Distribution—CLK or External VCO > 1600 MHz section only in that the VCO divider (divide-by-2/divide-by-3/divide-by-4/divide-by-5/divide-by-6) is bypassed. This limits the frequency of the clock source to <1600 MHz (due to the maximum input frequency allowed at the channel dividers).

Configuration and Register Settings

For clock distribution applications where the external clock is less than 1600 MHz, use the register settings shown in Table 24.

Table 24. Settings for Clock Distribution < 1600 MHz

Register	Function
0x010[1:0] = 01b	PLL asynchronous power-down (PLL off)
0x1E1[0] = 1b	Bypass the VCO divider as source for distribution section
0x1E1[1] = 0b	CLK selected as the source

When using the internal PLL with an external VCO of <1600 MHz, the PLL must be turned on.

Table 25. Settings for Using Internal PLL with External VCO < 1600 MHz

Register	Function
0x1E1[0] = 1b	Bypass the VCO divider as source for distribution section
0x010[1:0] = 00b	PLL normal operation (PLL on), along with other appropriate PLL settings in Register 0x010 to Register 0x01D

An external VCO/VCXO requires an external loop filter that must be connected between CP and the tuning pin of the VCO/VCXO. This loop filter determines the loop bandwidth and stability of the PLL. Make sure to select the proper PFD polarity for the VCO/VCXO being used.

Table 26. Setting the PFD Polarity

Register	Function
0x010[7] = 0b	PFD polarity positive (higher control voltage produces higher frequency)
0x010[7] = 1b	PFD polarity negative (higher control voltage produces lower frequency)

After the appropriate register values are programmed, Register 0x232 must be set to 0x01 for the values to take effect.