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12 LVPECL/24 CMOS Output Clock Generator with Integrated 2.2 GHz VCO

Data Sheet

AD9520-2

FEATURES

- Low phase noise, phase-locked loop (PLL)
  - On-chip VCO tunes from 2.02 GHz to 2.335 GHz
  - Optional external 3.3 V/5 V VCO/VCXO to 2.4 GHz
  - 1 differential or 2 single-ended reference inputs
  - Accepts CMOS, LVDS, or LVPECL references to 250 MHz
  - Accepts 16.62 MHz to 33.3 MHz crystal for reference input
  - Optional reference clock doubler
  - Reference monitoring capability
  - Automatic/manual reference holdover and reference switchover modes, with revertive switching
  - Glitch-free switchover between references
  - Automatic recovery from holdover
  - Digital or analog lock detect, selectable
  - Optional zero delay operation
- Twelve 1.6 GHz LVPECL outputs divided into 4 groups
  - Each group of 3 outputs shares a 1-to-32 divider with phase delay
  - Additive output jitter as low as 225 fs rms
  - Channel-to-channel skew grouped outputs < 16 ps
  - Each LVPECL output can be configured as 2 CMOS outputs (for $f_{OUT} \leq 250$ MHz)
- Automatic synchronization of all outputs on power-up
- Manual output synchronization available
- SPI- and I²C-compatible serial control port
- 64-lead LFCSP
- Nonvolatile EEPROM stores configuration settings

APPLICATIONS

- Low jitter, low phase noise clock distribution
- Clock generation and translation for SONET, 10Ge, 10GFC, Synchronous Ethernet, OTU2/3/4
- Forward error correction (G.710)
- Clocking high speed ADCs, DACs, DDSs, DDCs, DUCs, MxFEs
- High performance wireless transceivers
- ATE and high performance instrumentation
- Broadband infrastructures

GENERAL DESCRIPTION

The AD9520-2[1] provides a multioutput clock distribution function with subpicosecond jitter performance, along with an on-chip PLL and VCO. The on-chip VCO tunes from 2.02 GHz to 2.335 GHz. An external 3.3 V/5 V VCO/VCXO of up to 2.4 GHz can also be used.

FUNCTIONAL BLOCK DIAGRAM

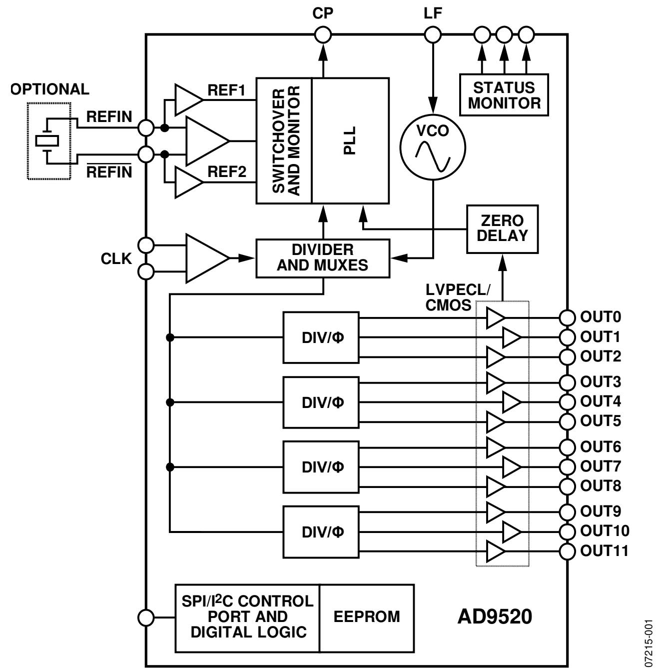

Figure 1.

The AD9520-2 serial interface supports both SPI and I²C ports. An in-package EEPROM, which can be programmed through the serial interface, can store user-defined register settings for power-up and chip reset.

The AD9520-2 features 12 LVPECL outputs in four groups. Any of the 1.6 GHz LVPECL outputs can be reconfigured as two 250 MHz CMOS outputs. If an application requires LVDS drivers instead of LVPECL drivers, refer to the AD9522-2.

Each group of three outputs has a divider that allows both the divide ratio (from 1 to 32) and the phase offset or coarse time delay to be set.

The AD9520-2 is available in a 64-lead LFCSP and can be operated from a single 3.3 V supply. The external VCO can have an operating voltage of up to 5.5 V. A separate output driver power supply can be from 2.375 V to 3.465 V.

The AD9520-2 is specified for operation over the standard industrial range of −40°C to +85°C.

[1]AD9520 is used throughout this data sheet to refer to all the members of the AD9520 family. However, when AD9520-2 is used, it refers to that specific member of the AD9520 family.

Rev. B **Document Feedback**

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- AD9520-2 Evaluation Board

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Application Notes

- AN-0983: Introduction to Zero-Delay Clock Timing Techniques

Data Sheet

- AD9520-2: 12 LVPECL/24 CMOS Output Clock Generator with Integrated 2.2 GHz VCO Data Sheet

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- Evaluation Software Documentation

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- Evaluation Software Tools

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- ADIsimCLK Design and Evaluation Software
- AD9520-x IBIS Models

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- CN0186

REFERENCE MATERIALS

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- RF Source Booklet

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- AD9520-2 Material Declaration
- PCN-PDN Information
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TABLE OF CONTENTS

REVISION HISTORY

10/2016—Rev. A to Rev. B

8/13—Rev. 0 to Rev. A

9/08—Revision 0: Initial Version

SPECIFICATIONS

Typical is given for $V_S = V_{S\_DRV}$ = 3.3 V ± 5%; $V_S \le V_{CP} \le$ 5.25 V; T_A = 25°C; R_{SET} = 4.12 kΩ; CP_{RSET} = 5.1 kΩ, unless otherwise noted. Minimum and maximum values are given over full V_S and T_A (−40°C to +85°C) variation.

POWER SUPPLY REQUIREMENTS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER PINS					
VS	3.135	3.3	3.465	V	3.3 V ± 5%
VS_DRV	2.375		V_S	V	Nominally 2.5 V to 3.3 V ± 5%
VCP	V_S		5.25	V	Nominally 3.3 V to 5.0 V ± 5%
CURRENT SET RESISTORS					
RSET Pin Resistor		4.12		kΩ	Sets internal biasing currents; connect to ground
CPRSET Pin Resistor		5.1		kΩ	Sets internal CP current range, nominally 4.8 mA (CP_lsb = 600 μA); actual current can be calculated by CP_lsb = 3.06/CP_{RSET}; connect to ground
BYPASS PIN CAPACITOR		220		nF	Bypass for internal LDO regulator; necessary for LDO stability; connect to ground

PLL CHARACTERISTICS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VCO (ON CHIP)					
Frequency Range	2020		2335	MHz	
VCO Gain (K_{VCO})		38		MHz/V	See Figure 8
Tuning Voltage (V_T)	0.5		V_{CP} − 0.5	V	$V_T \le V_S$ when using internal VCO
Frequency Pushing (Open-Loop)		1		MHz/V	
Phase Noise at 1 kHz Offset		−52		dBc/Hz	f = 2175 MHz
Phase Noise at 100 kHz Offset		−108		dBc/Hz	f = 2175 MHz
Phase Noise at 1 MHz Offset		−128		dBc/Hz	f = 2175 MHz
REFERENCE INPUTS					
Differential Mode (REFIN, $\overline{\text{REFIN}}$)					Differential mode (can accommodate single-ended input by ac grounding undriven input)
Input Frequency	0		250	MHz	Frequencies below about 1 MHz should be dc-coupled; be careful to match V_{CM} (self-bias voltage)
Input Sensitivity		280		mV p-p	PLL figure of merit (FOM) increases with increasing slew rate (see Figure 12); the input sensitivity is sufficient for ac-coupled LVDS and LVPECL signals
Self-Bias Voltage, REFIN	1.35	1.60	1.75	V	Self-bias voltage of REFIN[1]
Self-Bias Voltage, $\overline{\text{REFIN}}$	1.30	1.50	1.60	V	Self-bias voltage of $\overline{\text{REFIN}}$[1]
Input Resistance, REFIN	4.0	4.8	5.9	kΩ	Self-biased[1]
Input Resistance, $\overline{\text{REFIN}}$	4.4	5.3	6.4	kΩ	Self-biased[1]
Dual Single-Ended Mode (REF1, REF2)					Two single-ended CMOS-compatible inputs
Input Frequency (AC-Coupled with DC Offset Off)	10		250	MHz	Slew rate must be > 50 V/μs
Input Frequency (AC-Coupled with DC Offset On)			250	MHz	Slew rate must be > 50 V/μs, and input amplitude sensitivity specification must be met; see the input sensitivity parameter
Input Frequency (DC-Coupled)	0		250	MHz	Slew rate > 50 V/μs; CMOS levels
Input Sensitivity (AC-Coupled with DC Offset Off)	0.55		3.28	V p-p	V_{IH} should not exceed V_S
Input Sensitivity (AC-Coupled with DC Offset On)	1.5		2.78	V p-p	V_{IH} should not exceed V_S
Input Logic High, DC Offset Off	2.0			V	
Input Logic Low, DC Offset Off			0.8	V	
Input Current	−100		+100	µA	
Input Capacitance		2		pF	Each pin, REFIN (REF1)/$\overline{\text{REFIN}}$ (REF2)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Pulse Width High/Low	1.8			ns	The amount of time that a square wave is high/low; determines the allowable input duty cycle
Crystal Oscillator					
Crystal Resonator Frequency Range	16.62		33.33	MHz	
Maximum Crystal Motional Resistance			30	Ω	
PHASE/FREQUENCY DETECTOR (PFD)					
PFD Input Frequency			100	MHz	Antibacklash pulse width = 1.3 ns
			45	MHz	Antibacklash pulse width = 2.9 ns
Reference Input Clock Doubler Frequency	0.004		50	MHz	
Antibacklash Pulse Width		1.3		ns	Register 0x017[1:0] = 01b
		2.9		ns	Register 0x017[1:0] = 00b; Register 0x017[1:0] = 11b
		6.0		ns	Register 0x017[1:0] = 10b
CHARGE PUMP (CP)					CP_V is the CP pin voltage; V_{CP} is the charge pump power supply voltage (VCP pin)
I_{CP} Sink/Source					Programmable
High Value		4.8		mA	With CP_{RSET} = 5.1 kΩ; higher I_{CP} is possible by changing CP_{RSET}
Low Value		0.60		mA	With CP_{RSET} = 5.1 kΩ; lower I_{CP} is possible by changing CP_{RSET}
Absolute Accuracy		2.5		%	$CP_V = V_{CP}/2$
CPRSET Range	2.7		10	kΩ	
I_{CP} High Impedance Mode Leakage		1		nA	
Sink-and-Source Current Matching		1		%	0.5 V < CP_V < V_{CP} − 0.5 V; CP_V is the CP pin voltage; V_{CP} is the charge pump power supply voltage (VCP pin)
I_{CP} vs. V_{CP}		1.5		%	0.5 V < CP_V < V_{CP} − 0.5 V
I_{CP} vs. Temperature		2		%	$CP_V = V_{CP}/2$
PRESCALER (PART OF N DIVIDER)					
Prescaler Input Frequency					
P = 1 FD			300	MHz	
P = 2 FD			600	MHz	
P = 3 FD			900	MHz	
P = 2 DM (2/3)			200	MHz	
P = 4 DM (4/5)			1000	MHz	
P = 8 DM (8/9)			2400	MHz	
P = 16 DM (16/17)			3000	MHz	
P = 32 DM (32/33)			3000	MHz	
Prescaler Output Frequency			300	MHz	A, B counter input frequency (prescaler input frequency divided by P)
PLL N DIVIDER DELAY					Register 0x019[2:0]; see Table 54
000		Off			
001		385		ps	
010		486		ps	
011		623		ps	
100		730		ps	
101		852		ps	
110		976		ps	
111		1101		ps	
PLL R DIVIDER DELAY					Register 0x019[5:3]; see Table 54
000		Off			
001		365		ps	
010		486		ps	
011		608		ps	
100		730		ps	
101		852		ps	
110		976		ps	
111		1101		ps	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PHASE OFFSET IN ZERO DELAY					REF refers to REFIN (REF1)/$\overline{\text{REFIN}}$ (REF2)
Phase Offset (REF-to-LVPECL Clock Output Pins) in Internal Zero Delay Mode	560	1060	1310	ps	When N delay and R delay are bypassed
Phase Offset (REF-to-LVPECL Clock Output Pins) in Internal Zero Delay Mode	−320	+50	+240	ps	When N delay setting = 110b, and R delay is bypassed
Phase Offset (REF-to-CLK Input Pins) in External Zero Delay Mode	140	630	870	ps	When N delay and R delay are bypassed
Phase Offset (REF-to-CLK Input Pins) in External Zero Delay Mode	−460	−20	+200	ps	When N delay setting = 011b, and R delay is bypassed
NOISE CHARACTERISTICS					
In-Band Phase Noise of the Charge Pump/Phase Frequency Detector[2]					The PLL in-band phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log(N) (where N is the value of the N divider)
500 kHz PFD Frequency		−165		dBc/Hz	
1 MHz PFD Frequency		−162		dBc/Hz	
10 MHz PFD Frequency		−152		dBc/Hz	
50 MHz PFD Frequency		−144		dBc/Hz	
PLL Figure of Merit (FOM)		−222		dBc/Hz	Reference slew rate > 0.5 V/ns; FOM + 10 log(f_{PFD}) is an approximation of the PFD/CP in-band phase noise (in the flat region) inside the PLL loop bandwidth; when running closed-loop, the phase noise, as observed at the VCO output, is increased by 20 log(N); PLL figure of merit decreases with decreasing slew rate; see Figure 12
PLL DIGITAL LOCK DETECT WINDOW[3]					Signal available at the LD, STATUS, and REFMON pins when selected by appropriate register settings; the lock detect threshold varies linearly with the value of the CP_{RSET} resistor
Lock Threshold (Coincidence of Edges)					Selected by Register 0x017[1:0] and Register 0x018[4] (this is the threshold to go from unlock to lock)
Low Range (ABP 1.3 ns, 2.9 ns)		3.5		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 1b
High Range (ABP 1.3 ns, 2.9 ns)		7.5		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 0b
High Range (ABP 6.0 ns)		3.5		ns	Register 0x017[1:0] = 10b; Register 0x018[4] = 0b
Unlock Threshold (Hysteresis)[3]					Selected by Register 0x017[1:0] and Register 0x018[4] (this is the threshold to go from lock to unlock)
Low Range (ABP 1.3 ns, 2.9 ns)		7		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 1b
High Range (ABP 1.3 ns, 2.9 ns)		15		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 0b
High Range (ABP 6.0 ns)		11		ns	Register 0x017[1:0] = 10b; Register 0x018[4] = 0b

[1] The REFIN and $\overline{\text{REFIN}}$ self-bias points are offset slightly to avoid chatter on an open input condition.
[2] In-band means within the LBW of the PLL.
[3] For reliable operation of the digital lock detect, the period of the PFD frequency must be greater than the unlock-after-lock time.

CLOCK INPUTS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK INPUTS (CLK, $\overline{\text{CLK}}$)					Differential input
Input Frequency	0[1]		2.4	GHz	High frequency distribution (VCO divider)
	0[1]		2.0	GHz	Distribution only (VCO divider bypassed); this is the frequency range supported by the channel divider for all divide ratios except divide-by-17 and divide-by-3
	0[1]		1.6	GHz	Distribution only (VCO divider bypassed); this is the frequency range supported by all channel divider ratios
Input Sensitivity, Differential		150		mV p-p	Measured at 2.4 GHz; jitter performance is improved with slew rates > 1 V/ns; the input sensitivity is sufficient for ac-coupled LVDS and LVPECL signals
Input Level, Differential			2	V p-p	Larger voltage swings can turn on the protection diodes and can degrade jitter performance
Input Common-Mode Voltage, V_{CM}	1.3	1.57	1.8	V	Self-biased; enables ac coupling
Input Common-Mode Range, V_{CMR}	1.3		1.8	V	With 200 mV p-p signal applied; dc-coupled
Input Sensitivity, Single-Ended		150		mV p-p	CLK ac-coupled; $\overline{\text{CLK}}$ ac-bypassed to RF ground
Input Resistance	3.9	4.7	5.7	kΩ	Self-biased
Input Capacitance		2		pF	

[1] Below about 1 MHz, the input should be dc-coupled. Care should be taken to match V_{CM}.

CLOCK OUTPUTS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL CLOCK OUTPUTS					Termination = 50 Ω to V_{S_DRV} − 2 V
OUT0, OUT1, OUT2, OUT3, OUT4, OUT5, OUT6, OUT7, OUT8, OUT9, OUT10, OUT11					Differential (OUT, $\overline{\text{OUT}}$)
Output Frequency, Maximum	2400			MHz	Using direct to output (see Figure 20); higher frequencies are possible, but the resulting amplitude does not meet the V_{OD} specification; the maximum output frequency is limited by either the maximum VCO frequency or the frequency at the CLK inputs, depending on the AD9520-2 configuration
Output High Voltage, V_{OH}	V_{S_DRV} − 1.07	V_{S_DRV} − 0.96	V_{S_DRV} − 0.84	V	
Output Low Voltage, V_{OL}	V_{S_DRV} − 1.95	V_{S_DRV} − 1.79	V_{S_DRV} −1.64	V	
Output Differential Voltage, V_{OD}	660	820	950	mV	V_{OH} − V_{OL} for each leg of a differential pair for default amplitude setting with the driver not toggling; the peak-to-peak amplitude measured using a differential probe across the differential pair with the driver toggling is roughly 2× these values (see Figure 20 for variation over frequency)
CMOS CLOCK OUTPUTS					
OUT0A, OUT0B, OUT1A, OUT1B, OUT2A, OUT2B, OUT3A, OUT3B, OUT4A, OUT4B, OUT5A, OUT5B, OUT6A, OUT6B, OUT7A, OUT7B, OUT8A, OUT8B, OUT9A, OUT9B, OUT10A, OUT10B, OUT11A, OUT11B					Single-ended; termination = 10 pF
Output Frequency			250	MHz	See Figure 21
Output Voltage High, V_{OH}	V_S − 0.1			V	1 mA load, V_{S_DRV} = 3.3 V/2.5 V
Output Voltage Low, V_{OL}			0.1	V	1 mA load, V_{S_DRV} = 3.3 V/2.5 V
Output Voltage High, V_{OH}	2.7			V	10 mA load, V_{S_DRV} = 3.3 V
Output Voltage Low, V_{OL}			0.5	V	10 mA load, V_{S_DRV} = 3.3 V
Output Voltage High, V_{OH}	1.8			V	10 mA load, V_{S_DRV} = 2.5 V
Output Voltage Low, V_{OL}			0.6	V	10 mA load, V_{S_DRV} = 2.5 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Source Current					Damage to the part can result if values are exceeded
Static			20	mA	
Dynamic			16	mA	
Sink Current					Damage to the part can result if values are exceeded
Static			8	mA	
Dynamic			16	mA	

TIMING CHARACTERISTICS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT RISE/FALL TIMES					Termination = 50 Ω to VS_DRV − 2 V
Output Rise Time, t_{RP}		130	170	ps	20% to 80%, measured differentially (rise/fall times are independent of V_S and are valid for V_{S_DRV} = 3.3 V and 2.5 V)
Output Fall Time, t_{FP}		130	170	ps	80% to 20%, measured differentially (rise/fall times are independent of V_S and are valid for V_{S_DRV} = 3.3 V and 2.5 V)
PROPAGATION DELAY, t_{PECL}, CLK-TO-LVPECL OUTPUT					
For All Divide Values	850	1050	1280	ps	High frequency clock distribution configuration
	800	970	1180	ps	Clock distribution configuration
Variation with Temperature		1.0		ps/°C	
OUTPUT SKEW, LVPECL OUTPUTS[1]					Termination = 50 Ω to V_{S_DRV} − 2 V
LVPECL Outputs Sharing the Same Divider		5	16	ps	V_{S_DRV} = 3.3 V
		5	20	ps	V_{S_DRV} = 2.5 V
LVPECL Outputs on Different Dividers		5	45	ps	V_{S_DRV} = 3.3 V
		5	60	ps	V_{S_DRV} = 2.5 V
All LVPECL Outputs Across Multiple Parts			190	ps	V_{S_DRV} = 3.3 V and 2.5 V
CMOS OUTPUT RISE/FALL TIMES					Termination = open
Output Rise Time, t_{RC}		750	960	ps	20% to 80%; C_{LOAD} = 10 pF; V_{S_DRV} = 3.3 V
Output Fall Time, t_{FC}		715	890	ps	80% to 20%; C_{LOAD} = 10 pF; V_{S_DRV} = 3.3 V
Output Rise Time, t_{RC}		965	1280	ps	20% to 80%; C_{LOAD} = 10 pF; V_{S_DRV} = 2.5 V
Output Fall Time, t_{FC}		890	1100	ps	80% to 20%; C_{LOAD} = 10 pF; V_{S_DRV} = 2.5 V
PROPAGATION DELAY, t_{CMOS}, CLK-TO-CMOS OUTPUT					Clock distribution configuration
For All Divide Values	2.1	2.75	3.55	ns	V_{S_DRV} = 3.3 V
		3.35		ns	V_{S_DRV} = 2.5 V
Variation with Temperature		2		ps/°C	V_{S_DRV} = 3.3 V and 2.5 V
OUTPUT SKEW, CMOS OUTPUTS[1]					
CMOS Outputs Sharing the Same Divider		7	85	ps	V_{S_DRV} = 3.3 V
		10	105	ps	V_{S_DRV} = 2.5 V
All CMOS Outputs on Different Dividers		10	240	ps	V_{S_DRV} = 3.3 V
		10	285	ps	V_{S_DRV} = 2.5 V
All CMOS Outputs Across Multiple Parts			600	ps	V_{S_DRV} = 3.3 V
			620	ps	V_{S_DRV} = 2.5 V
OUTPUT SKEW, LVPECL-TO-CMOS OUTPUTS[1]					All settings identical; different logic type
Outputs Sharing the Same Divider	1.18	1.76	2.48	ns	LVPECL to CMOS on same part
Outputs on Different Dividers	1.20	1.78	2.50	ns	LVPECL to CMOS on same part

[1] The output skew is the difference between any two similar delay paths while operating at the same voltage and temperature.

Timing Diagrams

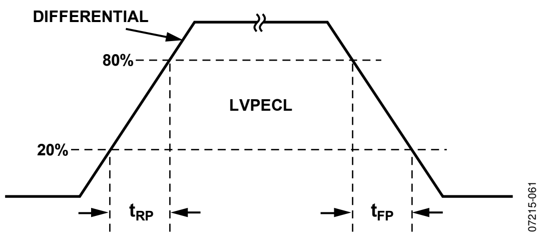


Figure 2. LVPECL Timing, Differential

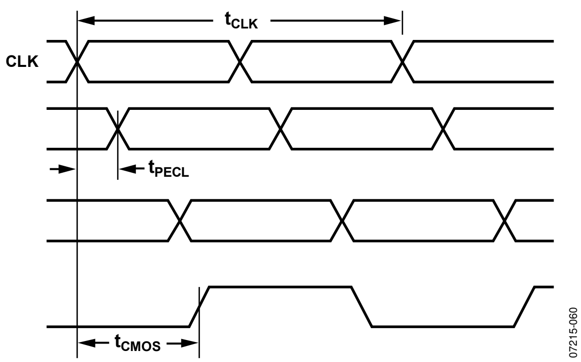


Figure 3. CLK/$\overline{CLK}$ to Clock Output Timing, DIV = 1

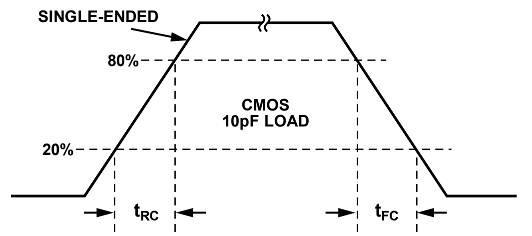


Figure 4. CMOS Timing, Single-Ended, 10 pF Load

CLOCK OUTPUT ADDITIVE PHASE NOISE (DISTRIBUTION ONLY; VCO DIVIDER NOT USED)

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK-TO-LVPECL ADDITIVE PHASE NOISE					Distribution section only; does not include PLL and VCO
CLK = 1 GHz, Output = 1 GHz					Input slew rate > 1 V/ns
Divider = 1					
10 Hz Offset		−107		dBc/Hz	
100 Hz Offset		−117		dBc/Hz	
1 kHz Offset		−127		dBc/Hz	
10 kHz Offset		−135		dBc/Hz	
100 kHz Offset		−142		dBc/Hz	
1 MHz Offset		−145		dBc/Hz	
10 MHz Offset		−147		dBc/Hz	
100 MHz Offset		−150		dBc/Hz	
CLK = 1 GHz, Output = 200 MHz					Input slew rate > 1 V/ns
Divider = 5					
10 Hz Offset		−122		dBc/Hz	
100 Hz Offset		−132		dBc/Hz	
1 kHz Offset		−143		dBc/Hz	
10 kHz Offset		−150		dBc/Hz	
100 kHz Offset		−156		dBc/Hz	
1 MHz Offset		−157		dBc/Hz	
>10 MHz Offset		−157		dBc/Hz	
CLK-TO-CMOS ADDITIVE PHASE NOISE					Distribution section only; does not include PLL and VCO
CLK = 1 GHz, Output = 250 MHz					Input slew rate > 1 V/ns
Divider = 4					
10 Hz Offset		−107		dBc/Hz	
100 Hz Offset		−119		dBc/Hz	
1 kHz Offset		−125		dBc/Hz	
10 kHz Offset		−134		dBc/Hz	
100 kHz Offset		−144		dBc/Hz	
1 MHz Offset		−148		dBc/Hz	
>10 MHz Offset		−154		dBc/Hz	
CLK = 1 GHz, Output = 50 MHz					Input slew rate > 1 V/ns
Divider = 20					
10 Hz Offset		−126		dBc/Hz	
100 Hz Offset		−133		dBc/Hz	
1 kHz Offset		−140		dBc/Hz	
10 kHz Offset		−148		dBc/Hz	
100 kHz Offset		−157		dBc/Hz	
1 MHz Offset		−160		dBc/Hz	
>10 MHz Offset		−163		dBc/Hz	

CLOCK OUTPUT ABSOLUTE PHASE NOISE (INTERNAL VCO USED)

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL ABSOLUTE PHASE NOISE					Internal VCO; direct-to-LVPECL output and for loop bandwidths < 1 kHz
VCO = 2.335 GHz; Output = 2.335 GHz					
1 kHz Offset		−49		dBc/Hz	
10 kHz Offset		−80		dBc/Hz	
100 kHz Offset		−105		dBc/Hz	
1 MHz Offset		−125		dBc/Hz	
10 MHz Offset		−140		dBc/Hz	
40 MHz Offset		−146		dBc/Hz	
VCO = 2.175 GHz; Output = 2.175 GHz					
1 kHz Offset		−52		dBc/Hz	
10 kHz Offset		−83		dBc/Hz	
100 kHz Offset		−108		dBc/Hz	
1 MHz Offset		−128		dBc/Hz	
10 MHz Offset		−142		dBc/Hz	
40 MHz Offset		−147		dBc/Hz	
VCO = 2.05 GHz; Output = 2.05 GHz					
1 kHz Offset		−55		dBc/Hz	
10 kHz Offset		−84		dBc/Hz	
100 kHz Offset		−110		dBc/Hz	
1 MHz Offset		−130		dBc/Hz	
10 MHz Offset		−142		dBc/Hz	
40 MHz Offset		−147		dBc/Hz	

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING INTERNAL VCO)

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup where the reference source is clean, so a wider PLL loop bandwidth is used; reference = 15.36 MHz; R divider = 1
VCO = 2.212 GHz; LVPECL = 245.76 MHz; PLL LBW = 66 kHz		145		fs rms	Integration BW = 200 kHz to 10 MHz
		321		fs rms	Integration BW = 12 kHz to 20 MHz
VCO = 2.212 GHz; LVPECL = 122.88 MHz; PLL LBW = 66 kHz		155		fs rms	Integration BW = 200 kHz to 10 MHz
		324		fs rms	Integration BW = 12 kHz to 20 MHz
VCO = 2.212 GHz; LVPECL = 61.44 MHz; PLL LBW = 66 kHz		169		fs rms	Integration BW = 200 kHz to 10 MHz
		336		fs rms	Integration BW = 12 kHz to 20 MHz

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK CLEANUP USING INTERNAL VCO)

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup where the reference source is jittery, so a narrower PLL loop bandwidth is used; reference = 19.44 MHz; R divider = 162
VCO = 2.177 GHz; LVPECL = 155.52 MHz; PLL LBW = 2.1 kHz		569		fs rms	Integration BW = 12 kHz to 20 MHz
VCO = 2.212 GHz; LVPECL = 122.88 MHz; PLL LBW = 2.2 kHz		599		fs rms	Integration BW = 12 kHz to 20 MHz

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING EXTERNAL VCXO)

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup using an external 245.76 MHz VCXO (Toyocom TCO-2112); reference = 15.36 MHz; R divider = 1
LVPECL = 245.76 MHz; PLL LBW = 125 Hz		54		fs rms	Integration BW = 200 kHz to 5 MHz
		77		fs rms	Integration BW = 200 kHz to 10 MHz
		109		fs rms	Integration BW = 12 kHz to 20 MHz
LVPECL = 122.88 MHz; PLL LBW = 125 Hz		79		fs rms	Integration BW = 200 kHz to 5 MHz
		114		fs rms	Integration BW = 200 kHz to 10 MHz
		163		fs rms	Integration BW = 12 kHz to 20 MHz
LVPECL = 61.44 MHz; PLL LBW = 125 Hz		124		fs rms	Integration BW = 200 kHz to 5 MHz
		176		fs rms	Integration BW = 200 kHz to 10 MHz
		259		fs rms	Integration BW = 12 kHz to 20 MHz

CLOCK OUTPUT ADDITIVE TIME JITTER (VCO DIVIDER NOT USED)

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; measured at rising edge of clock signal
CLK = 622.08 MHz		46		fs rms	Integration bandwidth = 12 kHz to 20 MHz
Any LVPECL Output = 622.08 MHz					
Divide Ratio = 1					
CLK = 622.08 MHz		64		fs rms	Integration bandwidth = 12 kHz to 20 MHz
Any LVPECL Output = 155.52 MHz					
Divide Ratio = 4					
CLK = 1000 MHz		223		fs rms	Calculated from SNR of ADC method
Any LVPECL Output = 100 MHz					Broadband jitter
Divide Ratio = 10					
CLK = 500 MHz		209		fs rms	Calculated from SNR of ADC method
Any LVPECL Output = 100 MHz					Broadband jitter
Divide Ratio = 5					
CMOS OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO
CLK = 200 MHz		325		fs rms	Calculated from SNR of ADC method
Any CMOS Output Pair = 100 MHz					Broadband jitter
Divide Ratio = 2					

CLOCK OUTPUT ADDITIVE TIME JITTER (VCO DIVIDER USED)

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; uses rising edge of clock signal
CLK = 1.0 GHz; VCO DIV = 5; LVPECL = 100 MHz; Channel Divider = 2; Duty-Cycle Correction = Off		230		fs rms	Calculated from SNR of ADC method (broadband jitter)
CLK = 500 MHz; VCO DIV = 5; LVPECL = 100 MHz; Bypass Channel Divider; Duty-Cycle Correction = On		215		fs rms	Calculated from SNR of ADC method (broadband jitter)
CMOS OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; uses rising edge of clock signal
CLK = 200 MHz; VCO DIV = 2; CMOS = 100 MHz; Bypass Channel Divider; Duty-Cycle Correction = Off		326		fs rms	Calculated from SNR of ADC method (broadband jitter)
CLK = 1600 MHz; VCO DIV = 2; CMOS = 100 MHz; Channel Divider = 8; Duty-Cycle Correction = Off		362		fs rms	Calculated from SNR of ADC method (broadband jitter)

SERIAL CONTROL PORT—SPI MODE

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{CS}$ (INPUT)					$\overline{CS}$ has an internal 30 kΩ pull-up resistor
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current			3	µA	
Input Logic 0 Current		−110		µA	The minus sign indicates that current is flowing out of the AD9520-2, which is due to the internal pull-up resistor
Input Capacitance		2		pF	
SCLK (INPUT IN SPI MODE)					SCLK has an internal 30 kΩ pull-down resistor in SPI mode, but not in I²C mode
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		110		µA	
Input Logic 0 Current			1	µA	
Input Capacitance		2		pF	
SDIO (INPUT IN BIDIRECTIONAL MODE)					
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		1		µA	
Input Logic 0 Current		1		µA	
Input Capacitance		2		pF	
SDIO, SDO (OUTPUTS)					
Output Logic 1 Voltage	2.7			V	
Output Logic 0 Voltage			0.4	V	
TIMING					
Clock Rate (SCLK, $1/t_{SCLK}$)			25	MHz	
Pulse Width High, t_{HIGH}	16			ns	
Pulse Width Low, t_{LOW}	16			ns	
SDIO to SCLK Setup, t_{DS}	4			ns	
SCLK to SDIO Hold, t_{DH}	0			ns	
SCLK to Valid SDIO and SDO, t_{DV}			11	ns	
$\overline{CS}$ to SCLK Setup and Hold, t_S, t_C	2			ns	
$\overline{CS}$ Minimum Pulse Width High, t_{PWH}	3			ns	

SERIAL CONTROL PORT—I²C MODE

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDA, SCL (WHEN INPUTTING DATA)					
Input Logic 1 Voltage	$0.7 \times V_S$			V	
Input Logic 0 Voltage			$0.3 \times V_S$	V	
Input Current with an Input Voltage Between $0.1 \times V_S$ and $0.9 \times V_S$	−10		+10	µA	
Hysteresis of Schmitt Trigger Inputs	$0.015 \times V_S$			V	
Pulse Width of Spikes That Must Be Suppressed by the Input Filter, t_{SPIKE}			50	ns	
SDA (WHEN OUTPUTTING DATA)					
Output Logic 0 Voltage at 3 mA Sink Current			0.4	V	
Output Fall Time from VIH_{MIN} to VIL_{MAX} with a Bus Capacitance from 10 pF to 400 pF	$20 + 0.1\ C_b$		250	ns	C_b = capacitance of one bus line in pF
TIMING					Note that all I²C timing values are referred to VIH_{MIN} ($0.3 \times VS$) and VIL_{MAX} levels ($0.7 \times V_S$)
Clock Rate (SCL, f_{I2C})			400	kHz	
Bus Free Time Between a Stop and Start Condition, t_{IDLE}	1.3			µs	
Setup Time for a Repeated Start Condition, $t_{SET; STR}$	0.6			µs	
Hold Time (Repeated) Start Condition, $t_{HLD; STR}$	0.6			µs	After this period, the first clock pulse is generated
Setup Time for Stop Condition, $t_{SET; STP}$	0.6			µs	
Low Period of the SCL Clock, t_{LOW}	1.3			µs	
High Period of the SCL Clock, t_{HIGH}	0.6			µs	
SCL, SDA Rise Time, t_{RISE}	$20 + 0.1\ C_b$		300	ns	
SCL, SDA Fall Time, t_{FALL}	$20 + 0.1\ C_b$		300	ns	
Data Setup Time, $t_{SET; DAT}$	120			ns	This is a minor deviation from the original I²C specification of 100 ns minimum
Data Hold Time, $t_{HLD; DAT}$	140		880	ns	This is a minor deviation from the original I²C specification of 0 ns minimum[1]
Capacitive Load for Each Bus Line, C_b			400	pF	

[1] According to the original I²C specification, an I²C master must also provide a minimum hold time of 300 ns for the SDA signal to bridge the undefined region of the SCL falling edge.

$\overline{\text{PD}}$, EEPROM, $\overline{\text{RESET}}$, AND $\overline{\text{SYNC}}$ PINS

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT CHARACTERISTICS					Each pin has a 30 kΩ internal pull-up resistor
Logic 1 Voltage	2.0			V	
Logic 0 Voltage			0.8	V	
Logic 1 Current			1	μA	
Logic 0 Current		−110		μA	The minus sign indicates that current is flowing out of the AD9520-2, which is due to the internal pull-up resistor
Capacitance		2		pF	
RESET TIMING					
Pulse Width Low	500			ns	
$\overline{\text{RESET}}$ Inactive to Start of Register Programming	100			ns	
$\overline{\text{SYNC}}$ TIMING					
Pulse Width Low	1.3			ns	High speed clock is CLK input signal

SERIAL PORT SETUP PINS—SP1, SP0

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SP1, SP0					These pins do not have internal pull-up/pull-down resistors
Logic Level 0			$0.25 \times V_S$	V	V_S is the voltage on the VS pin
Logic Level ½	$0.4 \times V_S$		$0.65 \times V_S$	V	These pins can be floated to obtain Logic Level ½; if floating the pin, connect a capacitor to ground
Logic Level 1	$0.8 \times V_S$			V	

LD, STATUS, AND REFMON PINS

Table 17.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS					When selected as a digital output (CMOS); there are other modes in which these pins are not CMOS digital outputs; see Table 54,Register 0x017, Register 0x01A, and Register 0x01B
Output Voltage High, V_{OH}	2.7			V	
Output Voltage Low, V_{OL}			0.4	V	
MAXIMUM TOGGLE RATE		100		MHz	Applies when mux is set to any divider or counter output, or PFD up/down pulse; also applies in analog lock detect mode; usually debug mode only; beware that spurs can couple to output when any pin is toggling
ANALOG LOCK DETECT					
Capacitance		3		pF	On-chip capacitance; used to calculate RC time constant for analog lock detect readback; use a pull-up resistor
REF1, REF2, AND VCO FREQUENCY STATUS MONITOR					
Normal Range	1.02			MHz	Frequency above which the monitor indicates the presence of the reference
Extended Range	8			kHz	Frequency above which the monitor indicates the presence of the reference
LD PIN COMPARATOR					
Trip Point		1.6		V	
Hysteresis		260		mV	

POWER DISSIPATION

Table 18.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION, CHIP					Does not include power dissipated in external resistors; all LVPECL outputs terminated with 50 Ω to V_{CC} − 2 V; all CMOS outputs have 10 pF capacitive loading; V_{S_DRV} = 3.3 V
Power-On Default		1.32	1.5	W	No clock; no programming; default register values
PLL Locked; One LVPECL Output Enabled		0.55	0.64	W	f_{REF} = 25 MHz; f_{OUT} = 225 MHz; VCO = 2250 MHz; VCO divider = 2; one LVPECL output and output divider enabled; zero delay off; I_{CP} = 4.8 mA
PLL Locked; One CMOS Output Enabled		0.52	0.62	W	f_{REF} = 25 MHz; f_{OUT} = 62.5 MHz; VCO = 2250 MHz; VCO divider = 2; one CMOS output and output divider enabled; zero delay off; I_{CP} = 4.8 mA
Distribution Only Mode; VCO Divider On; One LVPECL Output Enabled		0.39	0.46	W	f_{CLK} = 2.4 GHz; f_{OUT} = 200 MHz; VCO divider = 2; one LVPECL output and output divider enabled; zero delay off
Distribution Only Mode; VCO Divider Off; One LVPECL Output Enabled		0.36	0.42	W	f_{CLK} = 2.4 GHz; f_{OUT} = 200 MHz; VCO divider bypassed; one LVPECL output and output divider enabled; zero delay off
Maximum Power, Full Operation		1.5	1.7	W	PLL on; internal VCO = 2250 MHz; VCO divider = 2; all channel dividers on; 12 LVPECL outputs at 125 MHz; zero delay on
$\overline{PD}$ Power-Down		60	80	mW	$\overline{PD}$ pin pulled low; does not include power dissipated in termination resistors
$\overline{PD}$ Power-Down, Maximum Sleep		24	43	mW	$\overline{PD}$ pin pulled low; PLL power-down, Register 0x010[1:0] = 01b; power-down SYNC, Register 0x230[2] = 1b; power-down distribution reference, Register 0x230[1] = 1b
VCP Supply		4	4.8	mW	PLL operating; typical closed-loop configuration
POWER DELTAS, INDIVIDUAL FUNCTIONS					Power delta when a function is enabled/disabled
VCO Divider On/Off		32	40	mW	VCO divider not used
REFIN (Differential) Off		25	30	mW	Delta between reference input off and differential reference input mode
REF1, REF2 (Single-Ended) On/Off		15	20	mW	Delta between reference inputs off and one singled-ended reference enabled; double this number if both REF1 and REF2 are powered up
VCO On/Off		67	104	mW	Internal VCO disabled; CLK input selected
PLL Dividers and Phase Detector On/Off		51	63	mW	PLL off to PLL on, normal operation; no reference enabled
LVPECL Channel		121	144	mW	No LVPECL output on to one LVPECL output on; channel divider is set to 1
LVPECL Driver		51	73	mW	Second LVPECL output turned on, same channel
CMOS Channel		145	180	mW	No CMOS output on to one CMOS output on; channel divider is set to 1; f_{OUT} = 62.5 MHz and 10 pF of capacitive loading
CMOS Driver On/Off		11	24	mW	Additional CMOS outputs within the same channel turned on
Channel Divider Enabled		40	57	mW	Delta between divider bypassed (divide-by-1) and divide-by-2 to divide-by-32
Zero Delay Block On/Off		30	34	mW	

ABSOLUTE MAXIMUM RATINGS

Table 19.

Parameter	Rating
VS to GND	−0.3 V to +3.6 V
VCP, CP to GND	−0.3 V to +5.8 V
VS_DRV to GND	−0.3 V to +3.6 V
REFIN, $\overline{\text{REFIN}}$ to GND	−0.3 V to V_S + 0.3 V
RSET, LF, BYPASS to GND	−0.3 V to V_S + 0.3 V
CPRSET to GND	−0.3 V to V_S + 0.3 V
CLK, $\overline{\text{CLK}}$ to GND	−0.3 V to V_S + 0.3 V
CLK to $\overline{\text{CLK}}$	−1.2 V to +1.2 V
SCLK/SCL, SDIO/SDA, SDO, $\overline{\text{CS}}$ to GND	−0.3 V to V_S + 0.3 V
OUT0, $\overline{\text{OUT0}}$, OUT1, $\overline{\text{OUT1}}$, OUT2, $\overline{\text{OUT2}}$, OUT3, $\overline{\text{OUT3}}$, OUT4, $\overline{\text{OUT4}}$, OUT5, $\overline{\text{OUT5}}$, OUT6, $\overline{\text{OUT6}}$, OUT7, $\overline{\text{OUT7}}$, OUT8, $\overline{\text{OUT8}}$, OUT9, $\overline{\text{OUT9}}$, OUT10, $\overline{\text{OUT10}}$, OUT11, $\overline{\text{OUT11}}$ to GND	−0.3 V to V_S + 0.3 V
$\overline{\text{SYNC}}$, $\overline{\text{RESET}}$, $\overline{\text{PD}}$ to GND	−0.3 V to V_S + 0.3 V
REFMON, STATUS, LD to GND	−0.3 V to V_S + 0.3 V
SP0, SP1, EEPROM to GND	−0.3 V to V_S + 0.3 V
Junction Temperature[1]	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 sec)	300°C

[1] See Table 20 for θ_{JA}.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

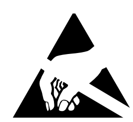
THERMAL RESISTANCE

Thermal impedance measurements were taken on a JEDEC JESD51-5 2S2P test board in still air, in accordance with JEDEC JESD51-2. See the Thermal Performance section for more details.

Table 20.

Package Type	θ_{JA}	Unit
64-Lead LFCSP (CP-64-4)	22	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

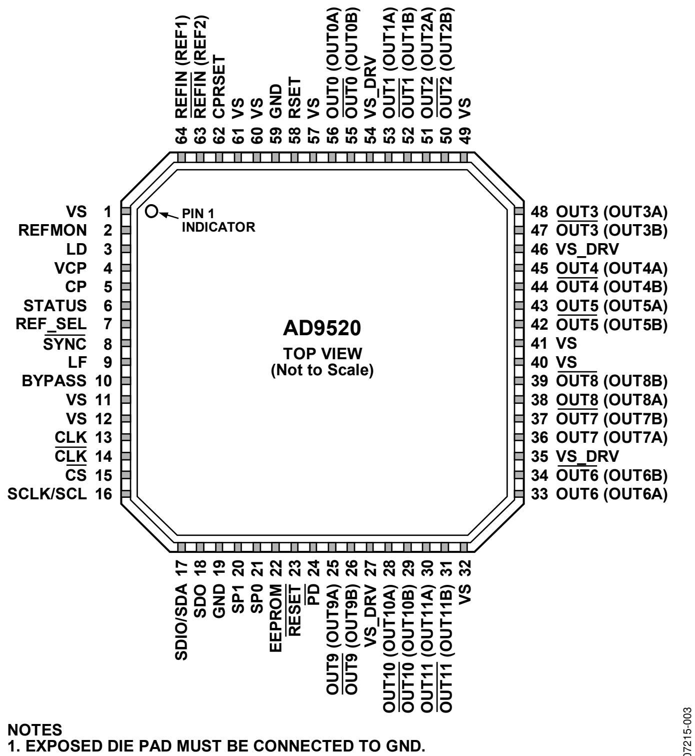


Figure 5. Pin Configuration

Table 21. Pin Function Descriptions

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
1, 11, 12, 32, 40, 41, 49, 57, 60, 61	I	Power	VS	3.3 V Power Pins.
2	O	3.3 V CMOS	REFMON	Reference Monitor (Output). This pin has multiple selectable outputs.
3	O	3.3 V CMOS	LD	Lock Detect (Output). This pin has multiple selectable outputs.
4	I	Power	VCP	Power Supply for Charge Pump (CP); $V_S \leq V_{CP} \leq 5.25$ V. VCP must still be connected to 3.3 V if the PLL is not used.
5	O	Loop filter	CP	Charge Pump (Output). This pin connects to an external loop filter; it can be left unconnected if the PLL is not used.
6	O	3.3 V CMOS	STATUS	Programmable Status Output.
7	I	3.3 V CMOS	REF_SEL	Reference Select. This pin selects REF1 (low) or REF2 (high) and has an internal 30 kΩ pull-down resistor.
8	I	3.3 V CMOS	$\overline{\text{SYNC}}$	Manual Synchronization and Manual Holdover. This pin initiates a manual synchronization and is used for manual holdover. Active low. This pin has an internal 30 kΩ pull-up resistor.
9	I	Loop filter	LF	Loop Filter (Input). This pin connects internally to the VCO control voltage node.
10	O	Loop filter	BYPASS	This pin is for bypassing the LDO to ground with a 220 nF capacitor. It can be left unconnected if the PLL is not used.
13	I	Differential clock input	CLK	Along with $\overline{\text{CLK}}$, this pin is the differential input for the clock distribution section.
14	I	Differential clock input	$\overline{\text{CLK}}$	Along with CLK, this pin is the differential input for the clock distribution section. If a single-ended input is connected to the CLK pin, connect a 0.1 μF bypass capacitor from this pin to ground.

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
15	I	3.3 V CMOS	$\overline{\text{CS}}$	Serial Control Port Chip Select; Active Low. This pin has an internal 30 kΩ pull-up resistor.
16	I	3.3 V CMOS	SCLK/SCL	Serial Control Port Clock Signal. This pin has an internal 30 kΩ pull-down resistor in SPI mode but is high impedance in I^{2}C mode.
17	I/O	3.3 V CMOS	SDIO/SDA	Serial Control Port Bidirectional Serial Data In/Out.
18	O	3.3 V CMOS	SDO	Serial Control Port Unidirectional Serial Data Out.
19, 59	I	GND	GND	Ground Pins.
20	I	Three-level logic	SP1	Select SPI or I^{2}C as the serial interface port and select the I^{2}C slave address in I^{2}C mode. Three-level logic. This pin is internally biased for the open logic level.
21	I	Three-level logic	SP0	Select SPI or I^{2}C as the serial interface port and select the I^{2}C slave address in I^{2}C mode. Three-level logic. This pin is internally biased for the open logic level.
22	I	3.3 V CMOS	EEPROM	Setting this pin high selects the register values stored in the internal EEPROM to be loaded at reset and/or power-up. Setting this pin low causes the AD9520-2 to load the hard-coded default register values at power-up/reset (unless Register 0xB02[1] is used. See the Soft Reset via the Serial Port section). This pin has an internal 30 kΩ pull-down resistor. Note that, to guarantee proper loading of the EEPROM during startup, a high-low-high pulse on the $\overline{\text{RESET}}$ pin should occur after the power supply has stabilized.
23	I	3.3 V CMOS	$\overline{\text{RESET}}$	Chip Reset, Active Low. This pin has an internal 30 kΩ pull-up resistor.
24	I	3.3 V CMOS	$\overline{\text{PD}}$	Chip Power-Down, Active Low. This pin has an internal 30 kΩ pull-up resistor.
25	O	LVPECL or CMOS	OUT9 (OUT9A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
26	O	LVPECL or CMOS	$\overline{\text{OUT9}}$ (OUT9B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
27, 35, 46, 54	I	Power	VS_DRV	Output Driver Power Supply Pins. As a group, these pins can be set to either 2.5 V or 3.3 V. All four pins must be set to the same voltage.
28	O	LVPECL or CMOS	OUT10 (OUT10A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
29	O	LVPECL or CMOS	$\overline{\text{OUT10}}$ (OUT10B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
30	O	LVPECL or CMOS	OUT11 (OUT11A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
31	O	LVPECL or CMOS	$\overline{\text{OUT11}}$ (OUT11B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
33	O	LVPECL or CMOS	OUT6 (OUT6A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
34	O	LVPECL or CMOS	$\overline{\text{OUT6}}$ (OUT6B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
36	O	LVPECL or CMOS	OUT7 (OUT7A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
37	O	LVPECL or CMOS	$\overline{\text{OUT7}}$ (OUT7B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
38	O	LVPECL or CMOS	OUT8 (OUT8A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
39	O	LVPECL or CMOS	$\overline{\text{OUT8}}$ (OUT8B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
42	O	LVPECL or CMOS	$\overline{\text{OUT5}}$ (OUT5B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
43	O	LVPECL or CMOS	OUT5 (OUT5A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
44	O	LVPECL or CMOS	$\overline{\text{OUT4}}$ (OUT4B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
45	O	LVPECL or CMOS	OUT4 (OUT4A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
47	O	LVPECL or CMOS	$\overline{\text{OUT3}}$ (OUT3B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
48	O	LVPECL or CMOS	OUT3 (OUT3A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
50	O	LVPECL or CMOS	$\overline{\text{OUT2}}$ (OUT2B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
51	O	LVPECL or CMOS	OUT2 (OUT2A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
52	O	LVPECL or CMOS	$\overline{\text{OUT1}}$ (OUT1B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
53	O	LVPECL or CMOS	OUT1 (OUT1A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
55	O	LVPECL or CMOS	$\overline{\text{OUT0}}$ (OUT0B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
56	O	LVPECL or CMOS	OUT0 (OUT0A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
58	O	Current set resistor	RSET	Clock Distribution Current Set Resistor. Connect a 4.12 kΩ resistor from this pin to GND.
62	O	Current set resistor	CPRSET	Charge Pump Current Set Resistor. Connect a 5.1 kΩ resistor from this pin to GND. This resistor can be omitted if the PLL is not used.
63	I	Reference input	$\overline{\text{REFIN}}$ (REF2)	Along with REFIN, this is the differential input for the PLL reference. Alternatively, this pin is a single-ended input for REF2.
64	I	Reference input	REFIN (REF1)	Along with $\overline{\text{REFIN}}$, this is the differential input for the PLL reference. Alternatively, this pin is a single-ended input for REF1.
EPAD		GND	GND	The exposed die pad must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

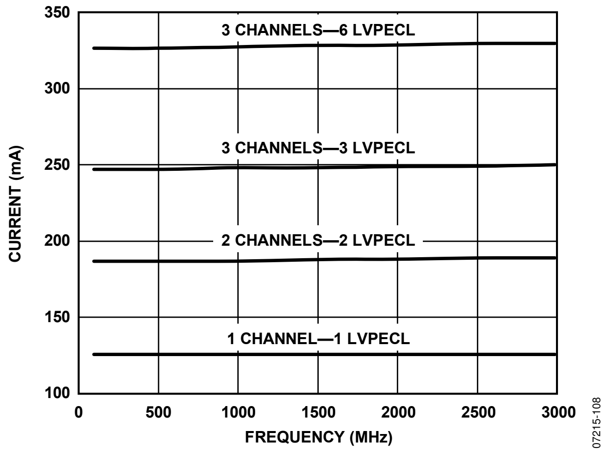


Figure 6. Total Current vs. Frequency, CLK-to-Output (PLL Off), LVPECL Outputs Terminated 50 Ω to V_{S_DRV} − 2 V

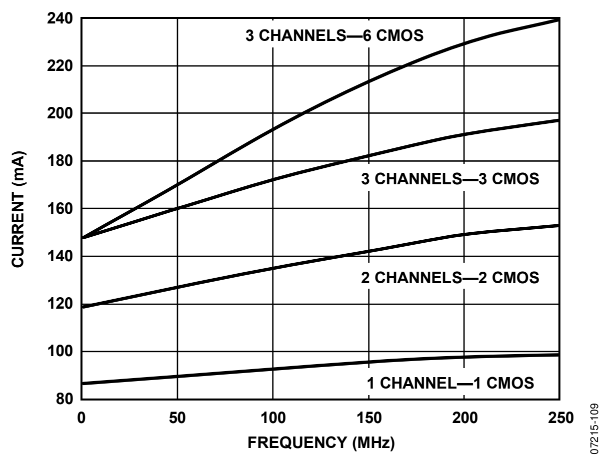


Figure 7. Total Current vs. Frequency, CLK-to-Output (PLL Off), CMOS Outputs with 10 pF Load

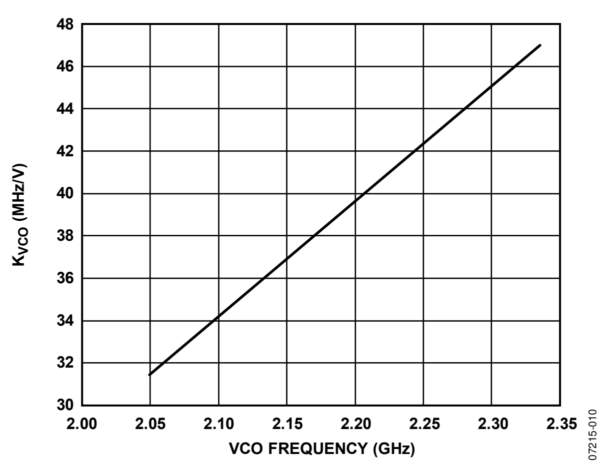


Figure 8. K_{VCO} vs. VCO Frequency

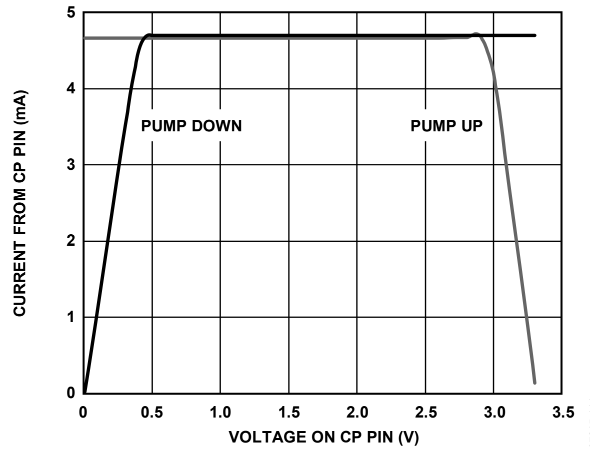


Figure 9. Charge Pump Characteristics at CP_V = 3.3 V

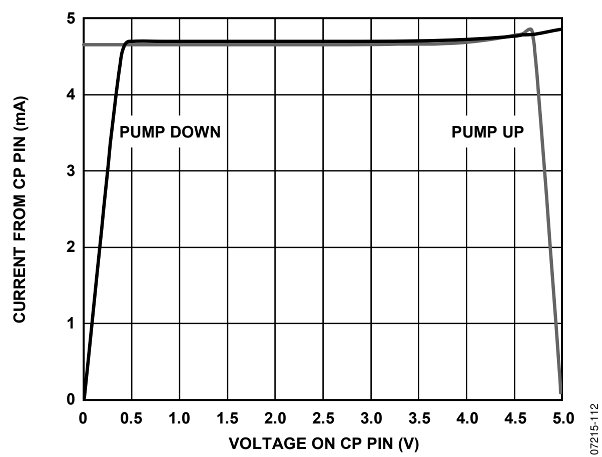


Figure 10. Charge Pump Characteristics at CP_V = 5.0 V

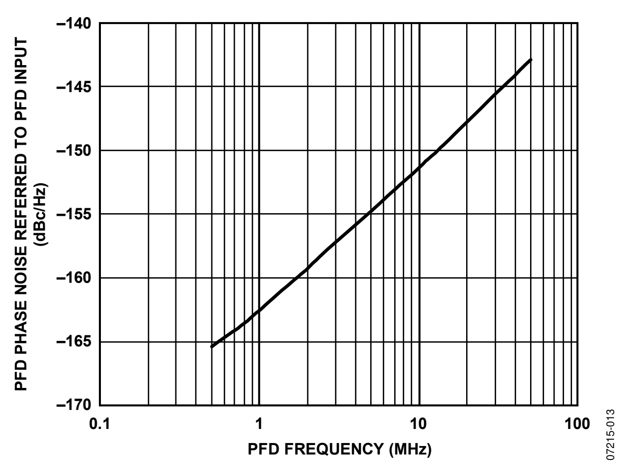


Figure 11. PFD Phase Noise Referred to PFD Input vs. PFD Frequency

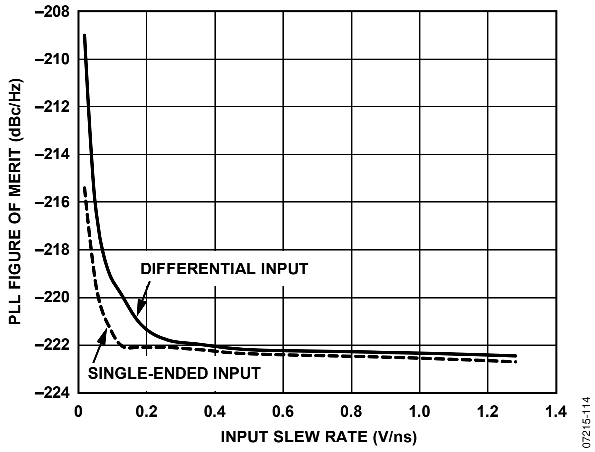


Figure 12. PLL Figure of Merit (FOM) vs. Slew Rate at REFIN/$\overline{\text{REFIN}}$

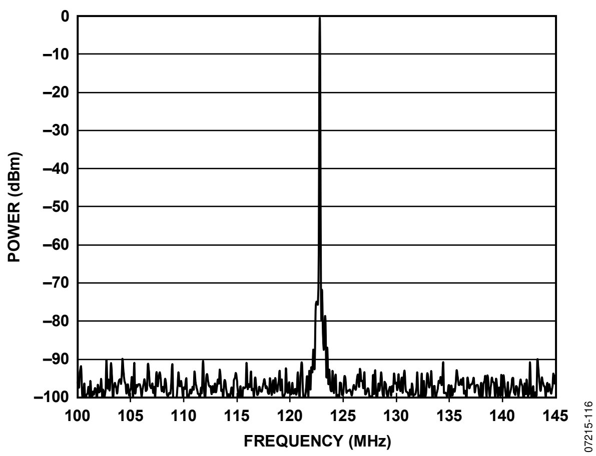


Figure 13. PFD/CP Spurs; 122.88 MHz; PFD = 15.36 MHz; LBW = 127 kHz; I_{CP} = 3.0 mA; f_{VCO} = 2211.84 MHz

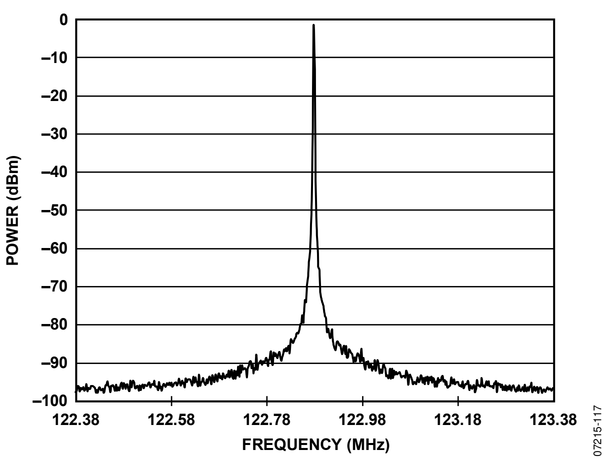


Figure 14. Output Spectrum, LVPECL; 122.88 MHz; PFD = 15.36 MHz; LBW = 127 kHz; I_{CP} = 3.0 mA; f_{VCO} = 2211.84 MHz

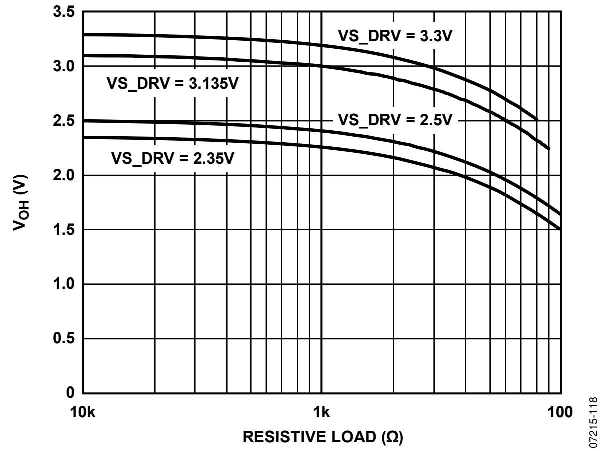


Figure 15. CMOS Output V_{OH} (Static) vs. R_{LOAD} (to Ground)

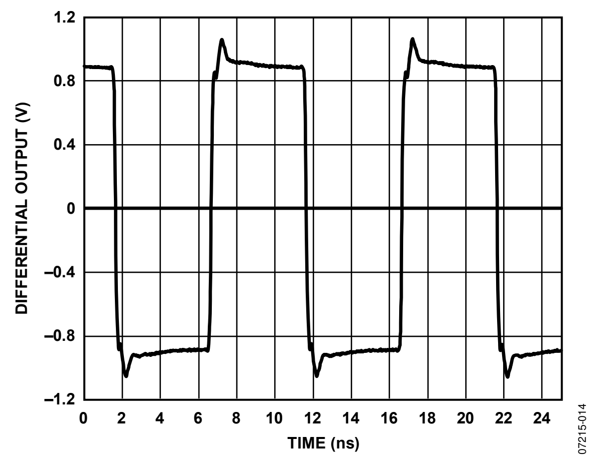


Figure 16. LVPECL Output (Differential) at 100 MHz

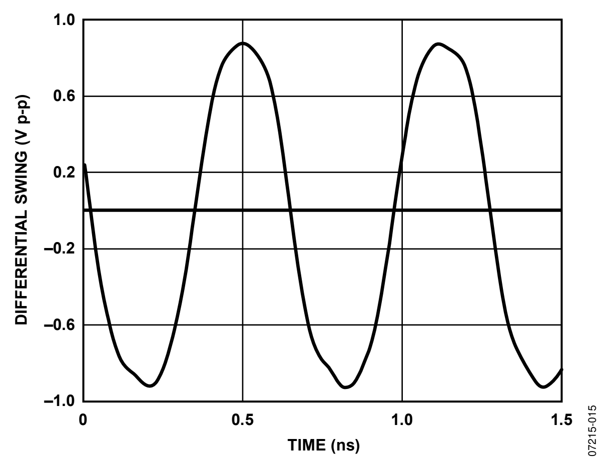


Figure 17. LVPECL Differential Voltage Swing at 1600 MHz

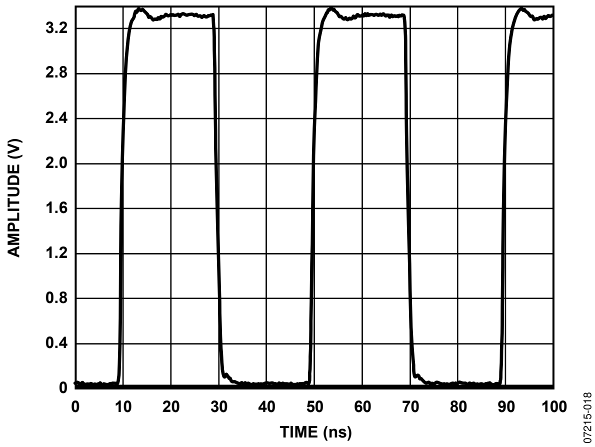


Figure 18. CMOS Output with 10 pF Load at 25 MHz

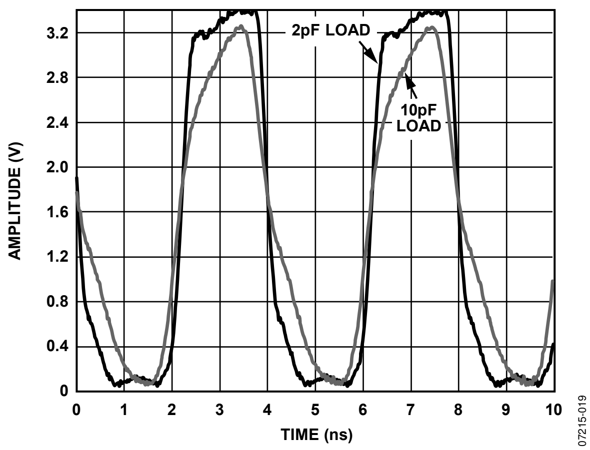


Figure 19. CMOS Output with 2 pF and 10 pF Load at 250 MHz

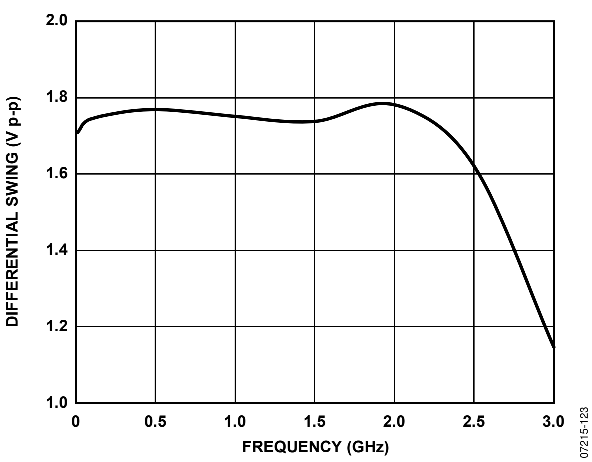


Figure 20. LVPECL Differential Voltage Swing vs. Frequency

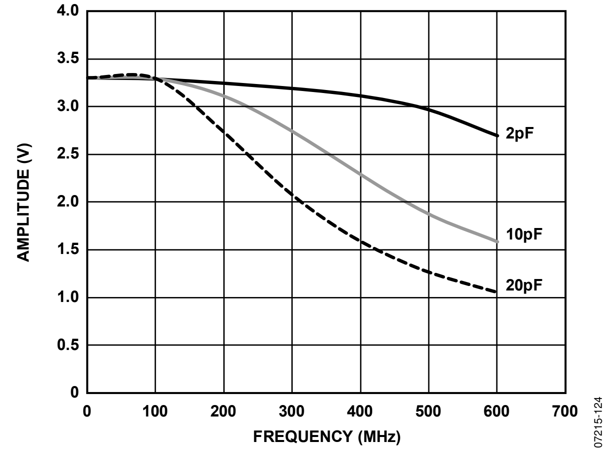


Figure 21. CMOS Output Swing vs. Frequency and Capacitive Load

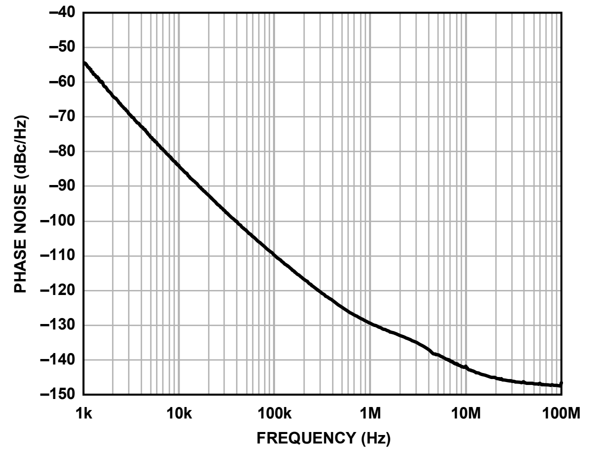


Figure 22. Internal VCO Phase Noise (Absolute), Direct-to-LVPECL at 2050 MHz

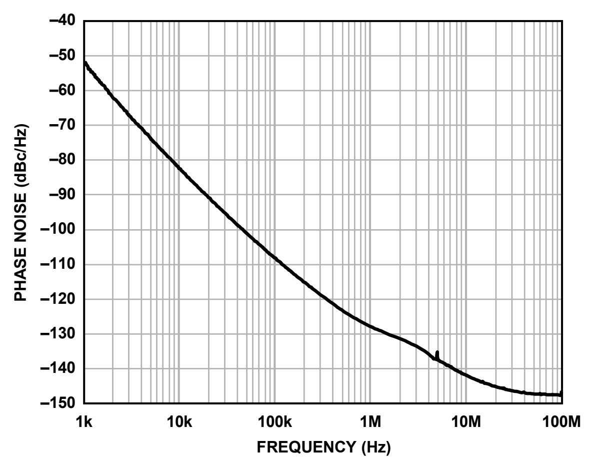


Figure 23. Internal VCO Phase Noise (Absolute), Direct-to-LVPECL at 2175 MHz

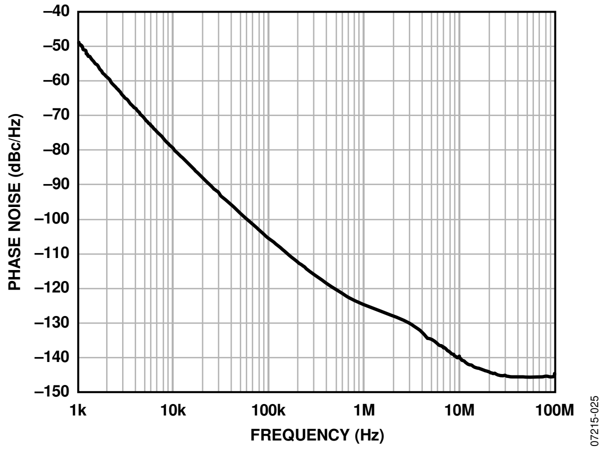


Figure 24. Internal VCO Phase Noise (Absolute), Direct-to-LVPECL at 2335 MHz

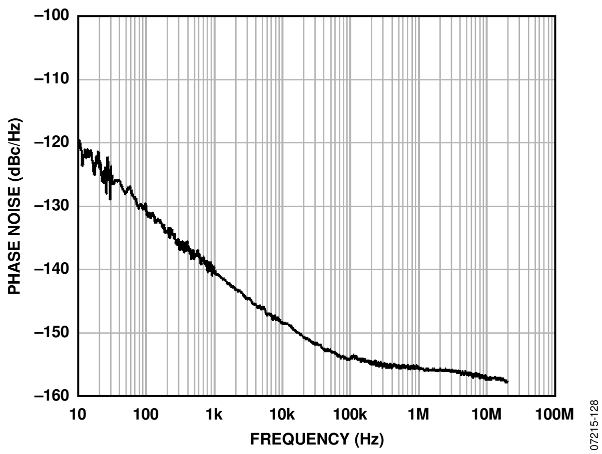


Figure 25. Additive (Residual) Phase Noise, CLK-to-LVPECL at 245.76 MHz, Divide-by-1

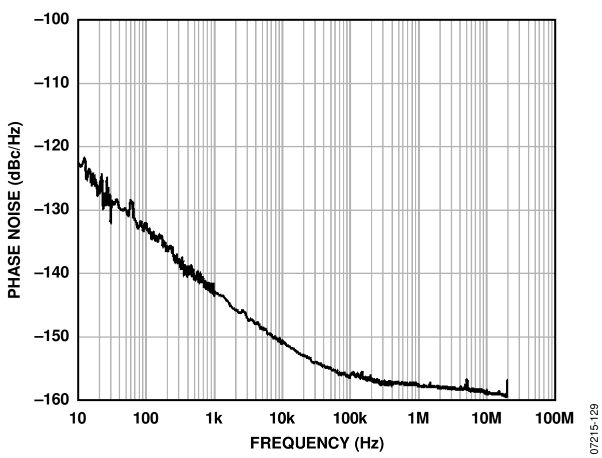


Figure 26. Additive (Residual) Phase Noise, CLK-to-LVPECL at 200 MHz, Divide-by-5

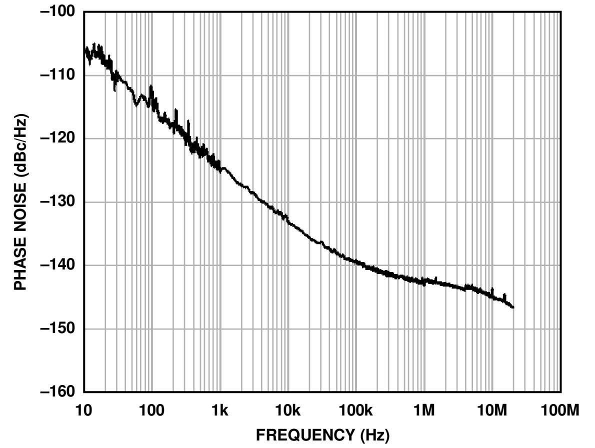


Figure 27. Additive (Residual) Phase Noise, CLK-to-LVPECL at 1600 MHz, Divide-by-1

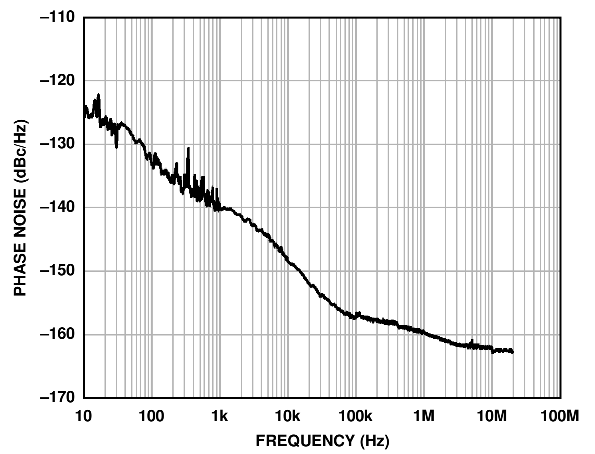


Figure 28. Additive (Residual) Phase Noise, CLK-to-CMOS at 50 MHz, Divide-by-20

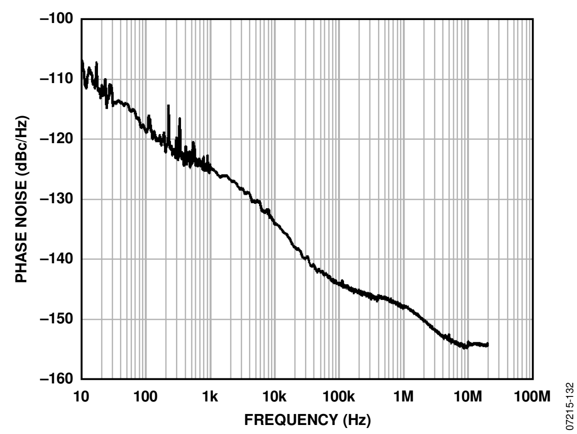


Figure 29. Additive (Residual) Phase Noise, CLK-to-CMOS at 250 MHz, Divide-by-4