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12 LVDS/24 CMOS Output Clock Generator with Integrated 2.2 GHz VCO

Data Sheet

AD9522-2

FEATURES

- Low phase noise, phase-locked loop (PLL)
  - On-chip voltage controlled oscillator (VCO) tunes from 2.02 GHz to 2.335 GHz
  - Supports external 3.3 V/5 V VCO/VCXO to 2.4 GHz
  - 1 differential or 2 single-ended reference inputs
  - Accepts CMOS, LVPECL, or LVDS references to 250 MHz
  - Accepts 16.62 MHz to 33.3 MHz crystal for reference input
  - Optional reference clock doubler
  - Reference monitoring capability
  - Revertive automatic and manual reference switchover/holdover modes
  - Glitch-free switchover between references
  - Automatic recovery from holdover
  - Digital or analog lock detect, selectable
  - Optional zero delay operation
- Twelve 800 MHz LVDS outputs divided into 4 groups
  - Each group of 3 has a 1-to-32 divider with phase delay
  - Additive output jitter as low as 242 fs rms
  - Channel-to-channel skew grouped outputs < 60 ps
  - Each LVDS output can be configured as 2 CMOS outputs (for $f_{OUT} \leq 250$ MHz)
- Automatic synchronization of all outputs on power-up
- Manual synchronization of outputs as needed
- SPI- and I^2C-compatible serial control port
- 64-lead LFCSP
- Nonvolatile EEPROM stores configuration settings

APPLICATIONS

- Low jitter, low phase noise clock distribution
- Clock generation and translation for SONET, 10Ge, 10G FC, and other 10 Gbps protocols
- Forward error correction (G.710)
- Clocking high speed ADCs, DACs, DDSs, DDCs, DUCs, MxFEs
- High performance wireless transceivers
- ATE and high performance instrumentation
- Broadband infrastructures

GENERAL DESCRIPTION

The AD9522-2[1] provides a multioutput clock distribution function with subpicosecond jitter performance, along with an on-chip PLL and VCO. The on-chip VCO tunes from 2.02 GHz to 2.335 GHz. An external 3.3 V/5 V VCO/VCXO of up to 2.4 GHz can also be used.

FUNCTIONAL BLOCK DIAGRAM

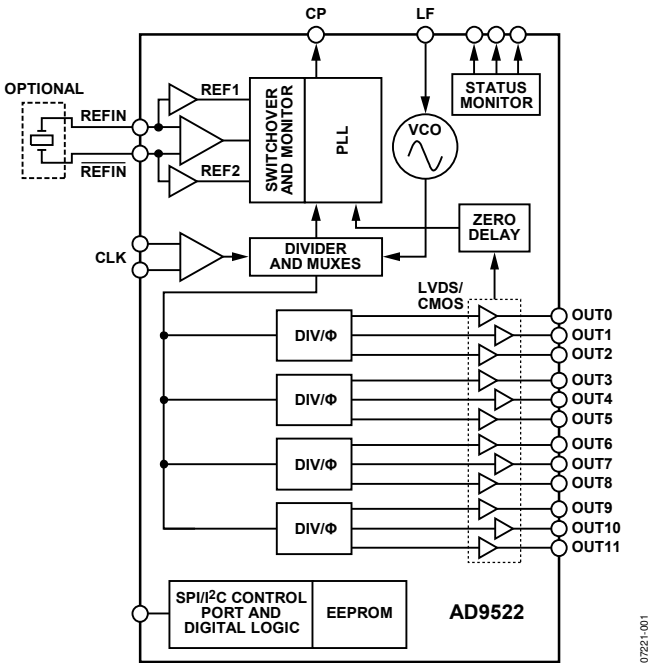

Figure 1.

The AD9522 serial interface supports both SPI and I^2C® ports. An in-package EEPROM can be programmed through the serial interface and store user-defined register settings for power-up and chip reset.

The AD9522 features 12 LVDS outputs in four groups. Any of the 800 MHz LVDS outputs can be reconfigured as two 250 MHz CMOS outputs.

Each group of outputs has a divider that allows both the divide ratio (from 1 to 32) and the phase (coarse delay) to be set.

The AD9522 is available in a 64-lead LFCSP and can be operated from a single 3.3 V supply. The external VCO can have an operating voltage up to 5.5 V.

The AD9522 is specified for operation over the standard industrial range of −40°C to +85°C.

The AD9520-2 is an equivalent part to the AD9522-2 featuring LVPECL/CMOS drivers instead of LVDS/CMOS drivers.

[1] The AD9522 is used throughout this data sheet to refer to all the members of the AD9522 family. However, when AD9522-2 is used, it is referring to that specific member of the AD9522 family.

Rev. A
Document Feedback

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- AN-0983: Introduction to Zero-Delay Clock Timing Techniques

Data Sheet

- AD9522-2: 12 LVDS/24 CMOS Output Clock Generator with Integrated 2.2 GHz VCO Data Sheet

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- Evaluation Software Documentation

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- AD9522-x IBIS Models

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REVISION HISTORY

3/15—Rev. 0 to Rev. A

11/08—Revision 0: Initial Version

SPECIFICATIONS

Typical (typ) is given for VS = 3.3 V ± 5%; VS ≤ VCP ≤ 5.25 V; T_A = 25°C; RSET = 4.12 kΩ; CPRSET = 5.1 kΩ, unless otherwise noted. Minimum (min) and maximum (max) values are given over full VS and T_A (−40°C to +85°C) variation.

POWER SUPPLY REQUIREMENTS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VS	3.135	3.3	3.465	V	3.3 V ± 5%
VCP	VS		5.25	V	This supply is usually at the same voltage as VS; set VCP = 5.0 V ± 5% only if connecting a 5 V external VCO/VCXO
RSET Pin Resistor		4.12		kΩ	Sets internal biasing currents; connect to ground
CPRSET Pin Resistor		5.1		kΩ	Sets internal CP current range, nominally 4.8 mA (CP_Isb = 600 µA); actual current can be calculated by CP_Isb = 3.06/CPRSET; connect to ground
BYPASS Pin Capacitor		220		nF	Bypass for internal LDO regulator; necessary for LDO stability; connect to ground

PLL CHARACTERISTICS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VCO (ON-CHIP)					
Frequency Range	2020		2335	MHz	
VCO Gain (K_{VCO})		38		MHz/V	See Figure 8
Tuning Voltage (V_T)	0.5		VCP − 0.5	V	VCP ≤ VS when using internal VCO
Frequency Pushing (Open-Loop)		1		MHz/V	
Phase Noise at 1 kHz Offset		−61		dBc/Hz	LVDS output; f_{VCO} = 2175 MHz; f_{OUT} = 725 MHz
Phase Noise at 100 kHz Offset		−117		dBc/Hz	LVDS output; f_{VCO} = 2175 MHz; f_{OUT} = 725 MHz
Phase Noise at 1 MHz Offset		−135		dBc/Hz	LVDS output; f_{VCO} = 2175 MHz; f_{OUT} = 725 MHz
REFERENCE INPUTS					
Differential Mode (REFIN, $\overline{\text{REFIN}}$)					Differential mode (can accommodate single-ended input by ac grounding the unused complementary input)
Input Frequency	0		250	MHz	Frequencies below about 1 MHz must be dc-coupled; be careful to match V_{CM} (self-bias voltage)
Input Sensitivity		280		mV p-p	PLL figure of merit (FOM) increases with increasing slew rate (see Figure 12); the input sensitivity is sufficient for ac-coupled LVDS and LVPECL signals
Self-Bias Voltage, REFIN	1.35	1.60	1.75	V	Self-bias voltage of REFIN[1]
Self-Bias Voltage, $\overline{\text{REFIN}}$	1.30	1.50	1.60	V	Self-bias voltage of $\overline{\text{REFIN}}$[1]
Input Resistance, REFIN	4.0	4.8	5.9	kΩ	Self-biased[1]
Input Resistance, $\overline{\text{REFIN}}$	4.4	5.3	6.4	kΩ	Self-biased[1]
Dual Single-Ended Mode (REF1, REF2)					Two single-ended CMOS-compatible inputs
Input Frequency (AC-Coupled with DC Offset Off)	10		250	MHz	Slew rate must be > 50 V/µs
Input Frequency (AC-Coupled with DC Offset On)			250	MHz	Slew rate must be > 50 V/µs, and input amplitude sensitivity specification must be met; see input sensitivity
Input Frequency (DC-Coupled)	0		250	MHz	Slew rate > 50 V/µs; CMOS levels
Input Sensitivity (AC-Coupled with DC Offset Off)	0.55		3.28	V p-p	VIH must not exceed VS
Input Sensitivity (AC-Coupled with DC Offset On)	1.5		2.78	V p-p	VIH must not exceed VS
Input Logic High, DC Offset Off	2.0			V	
Input Logic Low, DC Offset Off			0.8	V	
Input Current	−100		+100	µA	
Input Capacitance		2		pF	Each pin, REFIN (REF1)/$\overline{\text{REFIN}}$ (REF2)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Pulse Width High/Low	1.8			ns	Amount of time a square wave is high/low determines the allowable input duty cycle
Crystal Oscillator					
Crystal Resonator Frequency Range	16.62		33.33	MHz	
Maximum Crystal Motional Resistance			30	Ω	
PHASE/FREQUENCY DETECTOR (PFD)					
PFD Input Frequency			100	MHz	Antibacklash pulse width = 1.3 ns, 2.9 ns
			45	MHz	Antibacklash pulse width = 6.0 ns
Reference Input Clock Doubler Frequency	0.004		50	MHz	Antibacklash pulse width = 1.3 ns, 2.9 ns
Antibacklash Pulse Width		1.3		ns	Register 0x017[1:0] = 01b
		2.9		ns	Register 0x017[1:0] = 00b; Register 0x017[1:0] = 11b
		6.0		ns	Register 0x017[1:0] = 10b
CHARGE PUMP (CP)					
I_{CP} Sink/Source					Programmable
High Value		4.8		mA	With CPRSET = 5.1 kΩ; higher I_{CP} is possible by changing CPRSET
Low Value		0.60		mA	With CPRSET = 5.1 kΩ; lower I_{CP} is possible by changing CPRSET
Absolute Accuracy		2.5		%	Charge pump voltage set to $V_{CP}/2$
CPRSET Range	2.7		10	kΩ	
I_{CP} High Impedance Mode Leakage		1		nA	
Sink-and-Source Current Matching		1		%	0.5 V < V_{CP} < VCP − 0.5 V; V_{CP} is the voltage on the CP (charge pump) pin; VCP is the voltage on the VCP power supply pin
I_{CP} vs. V_{CP}		1.5		%	0.5 V < V_{CP} < VCP − 0.5 V
I_{CP} vs. Temperature		2		%	V_{CP} = VCP/2 V
PRESCALER (PART OF N DIVIDER)					
Prescaler Input Frequency					
P = 1 FD			300	MHz	
P = 2 FD			600	MHz	
P = 3 FD			900	MHz	
P = 2 DM (2/3)			200	MHz	
P = 4 DM (4/5)			1000	MHz	
P = 8 DM (8/9)			2400	MHz	
P = 16 DM (16/17)			3000	MHz	
P = 32 DM (32/33)			3000	MHz	
Prescaler Output Frequency			300	MHz	A, B counter input frequency (prescaler input frequency divided by P)
PLL N DIVIDER DELAY					Register 0x019[2:0]; see Table 53
000		Off			
001		385		ps	
010		504		ps	
011		623		ps	
100		743		ps	
101		866		ps	
110		989		ps	
111		1112		ps	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PLL R DIVIDER DELAY					Register 0x019[5:3]; see Table 53
000		Off			
001		365		ps	
010		486		ps	
011		608		ps	
100		730		ps	
101		852		ps	
110		976		ps	
111		1101		ps	
PHASE OFFSET IN ZERO DELAY					REF refers to REFIN (REF1)/$\overline{\text{REFIN}}$ (REF2)
Phase Offset (REF-to-LVDS Clock Output Pins) in Internal Zero Delay Mode	1890	2348	3026	ps	When N delay and R delay are bypassed
Phase Offset (REF-to-LVDS Clock Output Pins) in Internal Zero Delay Mode	900	1217	1695	ps	When N delay = Setting 111 and R delay is bypassed
Phase Offset (REF-to-CLK Input Pins) in External Zero Delay Mode	318	677	1085	ps	When N delay and R delay are bypassed
Phase Offset (REF-to-CLK Input Pins) in External Zero Delay Mode	−329	+33	+360	ps	When N delay = Setting 011 and R delay is bypassed
NOISE CHARACTERISTICS					
In-Band Phase Noise of the Charge Pump/ Phase Frequency Detector (In-Band Means Within the LBW of the PLL)					The PLL in-band phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log(N) (where N is the value of the N divider)
at 500 kHz PFD Frequency		−165		dBc/Hz	
at 1 MHz PFD Frequency		−162		dBc/Hz	
at 10 MHz PFD Frequency		−152		dBc/Hz	
at 50 MHz PFD Frequency		−144		dBc/Hz	
PLL Figure of Merit (FOM)		−222		dBc/Hz	Reference slew rate > 0.5 V/ns; FOM + 10 log(f_{PFD}) is an approximation of the PFD/CP in-band phase noise (in the flat region) inside the PLL loop bandwidth; when running closed-loop, the phase noise, as observed at the VCO output, is increased by 20 log(N); PLL figure of merit decreases with decreasing slew rate; see Figure 12
PLL DIGITAL LOCK DETECT WINDOW[2]					Signal available at the LD, STATUS, and REFMON pins when selected by appropriate register settings; lock detect window settings can be varied by changing the CPRSET resistor
Lock Threshold (Coincidence of Edges)					Selected by Register 0x017[1:0] and Register 0x018[4] (this is the threshold to go from unlock to lock)
Low Range (ABP 1.3 ns, 2.9 ns)		3.5		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 1b
High Range (ABP 1.3 ns, 2.9 ns)		7.5		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 0b
High Range (ABP 6.0 ns)		3.5		ns	Register 0x017[1:0] = 10b; Register 0x018[4] = 0b
Unlock Threshold (Hysteresis)[2]					Selected by Register 0x017[1:0] and Register 0x018[4] (this is the threshold to go from lock to unlock)
Low Range (ABP 1.3 ns, 2.9 ns)		7		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 1b
High Range (ABP 1.3 ns, 2.9 ns)		15		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 0b
High Range (ABP 6.0 ns)		11		ns	Register 0x017[1:0] = 10b; Register 0x018[4] = 0b

[1] The REFIN and $\overline{\text{REFIN}}$ self-bias points are offset slightly to avoid chatter on an open input condition.
[2] For reliable operation of the digital lock detect, the period of the PFD frequency must be greater than the unlock-after-lock time.

CLOCK INPUTS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK INPUTS (CLK, $\overline{CLK}$)					Differential input
Input Frequency	0[1]		2.4	GHz	High frequency distribution (VCO divider)
	0[1]		2	GHz	Distribution only (VCO divider bypassed); this is the frequency range supported by the channel divider; see the Channel Divider Maximum Frequency section
Input Sensitivity, Differential		150		mV p-p	Measured at 2.4 GHz; jitter performance is improved with slew rates > 1 V/ns
Input Level, Differential			2	V p-p	Larger voltage swings can turn on the protection diodes and can degrade jitter performance
Input Common-Mode Voltage, V_{CM}	1.3	1.57	1.8	V	Self-biased; enables ac coupling
Input Common-Mode Range, V_{CMR}	1.3		1.8	V	With 200 mV p-p signal applied; dc-coupled
Input Sensitivity, Single-Ended		150		mV p-p	CLK ac-coupled; $\overline{CLK}$ ac-bypassed to RF ground
Input Resistance	3.9	4.7	5.7	kΩ	Self-biased
Input Capacitance		2		pF	

[1] Below about 1 MHz, the input must be dc-coupled. Take care to match V_{CM}.

CLOCK OUTPUTS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS CLOCK OUTPUTS					Termination = 100 Ω across differential pair
OUT0, OUT1, OUT2, OUT3, OUT4, OUT5, OUT6, OUT7, OUT8, OUT9, OUT10, OUT11					Differential (OUT, $\overline{OUT}$)
Output Frequency			800	MHz	The AD9522 outputs toggle at higher frequencies, but the output amplitude may not meet the V_{OD} specification
Output Differential Voltage, V_{OD}	247	360	454	mV	$V_{OH} - V_{OL}$ for each leg of a differential pair for default amplitude setting with the driver not toggling; the peak-to-peak amplitude measured using a differential probe across the differential pair with the driver toggling is roughly 2× these values (see Figure 20)
Delta V_{OD}			25	mV	Absolute difference between voltage swing of normal pin and inverted pin, output driver static
Output Offset Voltage, V_{OS}	1.125	1.25	1.375	V	$(V_{OH} + V_{OL})/2$ across a differential pair
Delta V_{OS}			25	mV	This is the absolute value of the difference between V_{OS} when the normal output is high vs. when the complementary output is high
Short-Circuit Current, I_{SA}, I_{SB}		14	24	mA	Output shorted to GND
Tristate Leakage Current per Output		<1		nA	Output in tristate with 100 Ω across differential pair
CMOS CLOCK OUTPUTS					
OUT0A, OUT0B, OUT1A, OUT1B, OUT2A, OUT2B, OUT3A, OUT3B, OUT4A, OUT4B, OUT5A, OUT5B, OUT6A, OUT6B, OUT7A, OUT7B, OUT8A, OUT8B, OUT9A, OUT9B, OUT10A, OUT10B, OUT11A, OUT11B					Single-ended; termination = 10 pF
Output Frequency			250	MHz	See Figure 21
Output Voltage High, V_{OH}	VS – 0.1			V	At 1 mA load
Output Voltage Low, V_{OL}			0.1	V	At 1 mA load
Output Voltage High, V_{OH}	2.7			V	At 10 mA load
Output Voltage Low, V_{OL}			0.5	V	At 10 mA load

TIMING CHARACTERISTICS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS OUTPUT RISE/FALL TIMES					Termination = 100 Ω across differential pair
Output Rise Time, t_{RP}		150	350	ps	20% to 80%, measured differentially
Output Fall Time, t_{FP}		150	350	ps	80% to 20%, measured differentially
PROPAGATION DELAY, t_{LVDS}, CLK-TO-LVDS OUTPUT					
For All Divide Values	1866	2313	2812	ps	High frequency clock distribution configuration
	1808	2245	2740	ps	Clock distribution configuration
Variation with Temperature		1		ps/°C	
OUTPUT SKEW, LVDS OUTPUTS[1]					Termination = 100 Ω across differential pair
LVDS Outputs That Share the Same Divider		7	60	ps	
LVDS Outputs on Different Dividers		19	162	ps	
All LVDS Outputs Across Multiple Parts			432	ps	
CMOS OUTPUT RISE/FALL TIMES					Termination = open
Output Rise Time, t_{RC}		625	835	ps	20% to 80%; C_{LOAD} = 10 pF
Output Fall Time, t_{FC}		625	800	ps	80% to 20%; C_{LOAD} = 10 pF
PROPAGATION DELAY, t_{CMOS}, CLK-TO-CMOS OUTPUT					Clock distribution configuration
For All Divide Values	1913	2400	2950	ps	
Variation with Temperature		2		ps/°C	
OUTPUT SKEW, CMOS OUTPUTS[1]					
CMOS Outputs That Share the Same Divider		10	55	ps	
All CMOS Outputs on Different Dividers		27	230	ps	
All CMOS Outputs Across Multiple Parts			500	ps	
OUTPUT SKEW, LVDS-TO-CMOS OUTPUT[1]					All settings identical; different logic type
Outputs That Share the Same Divider	−31	+152	+495	ps	LVDS to CMOS on the same part
Outputs That Are on Different Dividers	−193	+160	+495	ps	LVDS to CMOS on the same part

[1] The output skew is the difference between any two similar delay paths while operating at the same voltage and temperature.

Timing Diagrams

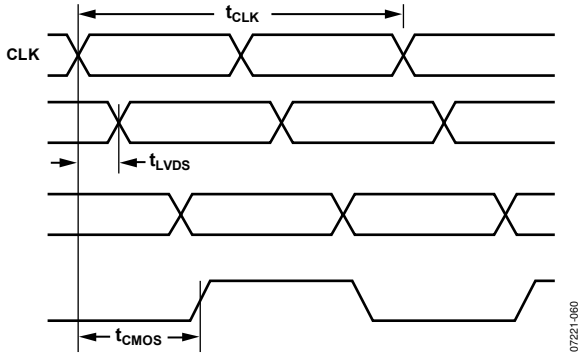

Figure 2. CLK/$\overline{CLK}$ to Clock Output Timing, DIV = 1

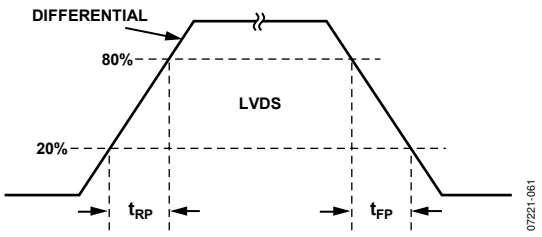

Figure 3. LVDS Timing, Differential

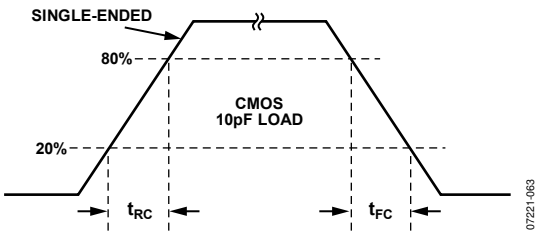

Figure 4. CMOS Timing, Single-Ended, 10 pF Load

CLOCK OUTPUT ADDITIVE PHASE NOISE (DISTRIBUTION ONLY; VCO DIVIDER NOT USED)

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK-TO-LVDS ADDITIVE PHASE NOISE					Distribution section only; does not include PLL and VCO
CLK = 1.6 GHz, Output = 800 MHz					Input slew rate > 1 V/ns
Divider = 2					
At 10 Hz Offset		−100		dBc/Hz	
At 100 Hz Offset		−110		dBc/Hz	
At 1 kHz Offset		−117		dBc/Hz	
At 10 kHz Offset		−126		dBc/Hz	
At 100 kHz Offset		−134		dBc/Hz	
At 1 MHz Offset		−137		dBc/Hz	
At 10 MHz Offset		−147		dBc/Hz	
At 100 MHz Offset		−148		dBc/Hz	
CLK = 1 GHz, Output = 200 MHz					Input slew rate > 1 V/ns
Divider = 5					
At 10 Hz Offset		−111		dBc/Hz	
At 100 Hz Offset		−123		dBc/Hz	
At 1 kHz Offset		−132		dBc/Hz	
At 10 kHz Offset		−141		dBc/Hz	
At 100 kHz Offset		−146		dBc/Hz	
At 1 MHz Offset		−150		dBc/Hz	
>10 MHz Offset		−156		dBc/Hz	
CLK-TO-CMOS ADDITIVE PHASE NOISE					Distribution section only; does not include PLL and VCO
CLK = 1 GHz, Output = 500 MHz					Input slew rate > 1 V/ns
Divider = 2					
At 10 Hz Offset		−102		dBc/Hz	
At 100 Hz Offset		−114		dBc/Hz	
At 1 kHz Offset		−122		dBc/Hz	
At 10 kHz Offset		−129		dBc/Hz	
At 100 kHz Offset		−135		dBc/Hz	
At 1 MHz Offset		−140		dBc/Hz	
>10 MHz Offset		−150		dBc/Hz	
CLK = 1 GHz, Output = 50 MHz					Input slew rate > 1 V/ns
Divider = 20					
At 10 Hz Offset		−125		dBc/Hz	
At 100 Hz Offset		−136		dBc/Hz	
At 1 kHz Offset		−144		dBc/Hz	
At 10 kHz Offset		−152		dBc/Hz	
At 100 kHz Offset		−157		dBc/Hz	
At 1 MHz Offset		−160		dBc/Hz	
>10 MHz Offset		−164		dBc/Hz	

CLOCK OUTPUT ABSOLUTE PHASE NOISE (INTERNAL VCO USED)

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS ABSOLUTE PHASE NOISE					Internal VCO; VCO divider = 3; LVDS output and for loop bandwidths < 1 kHz
VCO = 2335 MHz; Output = 778.3 MHz					
At 1 kHz Offset		−59		dBc/Hz	
At 10 kHz Offset		−90		dBc/Hz	
At 100 kHz Offset		−115		dBc/Hz	
At 1 MHz Offset		−133		dBc/Hz	
At 10 MHz Offset		−147		dBc/Hz	
At 40 MHz Offset		−150		dBc/Hz	
VCO = 2175 MHz; Output = 725 MHz					
At 1 kHz Offset		−61		dBc/Hz	
At 10 kHz Offset		−92		dBc/Hz	
At 100 kHz Offset		−117		dBc/Hz	
At 1 MHz Offset		−135		dBc/Hz	
At 10 MHz Offset		−148		dBc/Hz	
At 40 MHz Offset		−150		dBc/Hz	
VCO = 2020 MHz; Output = 673.3 MHz					
At 1 kHz Offset		−63		dBc/Hz	
At 10 kHz Offset		−94		dBc/Hz	
At 100 kHz Offset		−119		dBc/Hz	
At 1 MHz Offset		−136		dBc/Hz	
At 10 MHz Offset		−149		dBc/Hz	
At 40 MHz Offset		−150		dBc/Hz	

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING INTERNAL VCO)

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup where the reference source is clean, so a wider PLL loop bandwidth is used; reference = 15.36 MHz; R DIV = 1
VCO = 2212 MHz; LVDS = 245.76 MHz; PLL LBW = 55 kHz		171		fs rms	Integration bandwidth = 200 kHz to 10 MHz
		342		fs rms	Integration bandwidth = 12 kHz to 20 MHz
VCO = 2212 MHz; LVDS = 122.88 MHz; PLL LBW = 55 kHz		183		fs rms	Integration bandwidth = 200 kHz to 10 MHz
		350		fs rms	Integration bandwidth = 12 kHz to 20 MHz
VCO = 2212 MHz; LVDS = 61.44 MHz; PLL LBW = 55 kHz		210		fs rms	Integration bandwidth = 200 kHz to 10 MHz
		407		fs rms	Integration bandwidth = 12 kHz to 20 MHz

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK CLEANUP USING INTERNAL VCO)

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup where the reference source is jittery, so a narrower PLL loop bandwidth is used; reference = 19.44 MHz; R DIV = 162
VCO = 2177 MHz; LVDS = 155.52 MHz; PLL LBW = 1.8 kHz		625		fs rms	Integration bandwidth = 12 kHz to 20 MHz
VCO = 2212 MHz; LVDS = 122.88 MHz; PLL LBW = 1.8 kHz		648		fs rms	Integration bandwidth = 12 kHz to 20 MHz

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING EXTERNAL VCXO)

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup using an external 245.76 MHz VCXO (Toyocom TCO-2112); reference = 15.36 MHz; R DIV = 1
LVDS = 245.76 MHz; PLL LBW = 125 Hz		87		fs rms	Integration bandwidth = 200 kHz to 5 MHz
		108		fs rms	Integration bandwidth = 200 kHz to 10 MHz
		146		fs rms	Integration bandwidth = 12 kHz to 20 MHz
LVDS = 122.88 MHz; PLL LBW = 125 Hz		120		fs rms	Integration bandwidth = 200 kHz to 5 MHz
		151		fs rms	Integration bandwidth = 200 kHz to 10 MHz
		207		fs rms	Integration bandwidth = 12 kHz to 20 MHz
LVDS = 61.44 MHz; PLL LBW = 125 Hz		157		fs rms	Integration bandwidth = 200 kHz to 5 MHz
		210		fs rms	Integration bandwidth = 200 kHz to 10 MHz
		295		fs rms	Integration bandwidth = 12 kHz to 20 MHz

CLOCK OUTPUT ADDITIVE TIME JITTER (VCO DIVIDER NOT USED)

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; measured at rising edge of clock signal
CLK = 622.08 MHz Any LVDS Output = 622.08 MHz Divide Ratio = 1		69		fs rms	Integration bandwidth = 12 kHz to 20 MHz
CLK = 622.08 MHz Any LVDS Output = 155.52 MHz Divide Ratio = 4		116		fs rms	Integration bandwidth = 12 kHz to 20 MHz
CLK = 100 MHz Any LVDS Output = 100 MHz Divide Ratio = 1		263		fs rms	Calculated from SNR of ADC method Broadband jitter
CLK = 500 MHz Any LVDS Output = 100 MHz Divide Ratio = 5		242		fs rms	Calculated from SNR of ADC method Broadband jitter
CMOS OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO
CLK = 200 MHz Any CMOS Output Pair = 100 MHz Divide Ratio = 2		289		fs rms	Calculated from SNR of ADC method Broadband jitter

CLOCK OUTPUT ADDITIVE TIME JITTER (VCO DIVIDER USED)

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; uses rising edge of clock signal
CLK = 500 MHz; VCO DIV = 5; LVDS = 100 MHz; Bypass Channel Divider; Duty-Cycle Correction = On		248		fs rms	Calculated from SNR of ADC method (broadband jitter)
CMOS OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; uses rising edge of clock signal
CLK = 200 MHz; VCO DIV = 2; CMOS = 100 MHz; Bypass Channel Divider; Duty-Cycle Correction = Off		290		fs rms	Calculated from SNR of ADC method (broadband jitter)
CLK = 200 MHz; VCO DIV = 1; CMOS = 100 MHz; Bypass Channel Divider; Duty-Cycle Correction = Off		288		fs rms	Calculated from SNR of ADC method (broadband jitter)

SERIAL CONTROL PORT—SPI MODE

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{CS}$ (INPUT)					$\overline{CS}$ has an internal 30 kΩ pull-up resistor
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current			3	μA	
Input Logic 0 Current		−110		μA	The minus sign indicates that current is flowing out of the AD9522, which is due to the internal pull-up resistor
Input Capacitance		2		pF	
SCLK (INPUT) IN SPI MODE					SCLK has an internal 30 kΩ pull-down resistor in SPI mode, but not in I^2C mode
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		110		μA	
Input Logic 0 Current			1	μA	
Input Capacitance		2		pF	
SDIO (WHEN AN INPUT IN BIDIRECTIONAL MODE)					
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		1		μA	
Input Logic 0 Current		1		μA	
Input Capacitance		2		pF	
SDIO, SDO (OUTPUTS)					
Output Logic 1 Voltage	2.7			V	At 1 mA current; maximum recommended current: 5 mA
Output Logic 0 Voltage			0.4	V	At 1 mA current
TIMING					
Clock Rate (SCLK, $1/t_{SCLK}$)			25	MHz	
Pulse Width High, t_{HIGH}	16			ns	
Pulse Width Low, t_{LOW}	16			ns	
SDIO to SCLK Setup, t_{DS}	4			ns	
SCLK to SDIO Hold, t_{DH}	0			ns	
SCLK to Valid SDIO and SDO, t_{DV}			11	ns	
$\overline{CS}$ to SCLK Setup and Hold, t_S, t_C	2			ns	
$\overline{CS}$ Minimum Pulse Width High, t_{PWH}	3			ns	

SERIAL CONTROL PORT—I²C MODE

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDA, SCL (WHEN INPUTTING DATA)					
Input Logic 1 Voltage	0.7 × VS			V	
Input Logic 0 Voltage			0.3 × VS	V	
Input Current with an Input Voltage Between 0.1 × VS and 0.9 × VS	−10		+10	µA	
Hysteresis of Schmitt Trigger Inputs	0.015 × VS			V	
Pulse Width of Spikes That Must Be Suppressed by the Input Filter, t_{SPIKE}			50	ns	
SDA (WHEN OUTPUTTING DATA)					
Output Logic 0 Voltage at 3 mA Sink Current			0.4	V	
Output Fall Time from VIH_{MIN} to VIL_{MAX} with a Bus Capacitance from 10 pF to 400 pF	20 + 0.1 C_b		250	ns	C_b = capacitance of one bus line in pF
TIMING					Note that all I²C timing values refer to VIH_{MIN} (0.3 × VS) and VIL_{MAX} levels (0.7 × VS)
Clock Rate (SCL, f_{I2C})			400	kHz	
Bus Free Time Between a Stop and Start Condition, t_{IDLE}	1.3			µs	
Setup Time for a Repeated Start Condition, $t_{SET;\ STR}$	0.6			µs	
Hold Time (Repeated) Start Condition (After This Period, the First Clock Pulse Is Generated), $t_{HLD;\ STR}$	0.6			µs	
Setup Time for Stop Condition, $t_{SET;\ STP}$	0.6			µs	
Low Period of the SCL Clock, t_{LOW}	1.3			µs	
High Period of the SCL Clock, t_{HIGH}	0.6			µs	
SCL, SDA Rise Time, t_{RISE}	20 + 0.1 C_b		300	ns	C_b = capacitance of one bus line in pF
SCL, SDA Fall Time, t_{FALL}	20 + 0.1 C_b		300	ns	C_b = capacitance of one bus line in pF
Data Setup Time, $t_{SET;\ DAT}$	120			ns	This is a minor deviation from the original I²C specification of 100 ns minimum
Data Hold Time, $t_{HLD;\ DAT}$	140		880	ns	This is a minor deviation from the original I²C specification of 0 ns minimum[1]
Capacitive Load for Each Bus Line, C_b			400	pF	

[1] According to the original I²C specification, an I²C master must also provide a minimum hold time of 300 ns for the SDA signal to bridge the undefined region of the SCL falling edge.

$\overline{PD}$, $\overline{SYNC}$, AND $\overline{RESET}$ PINS

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT CHARACTERISTICS					Each of these pins has an 30 kΩ internal pull-up resistor
Logic 1 Voltage	2.0			V	
Logic 0 Voltage			0.8	V	
Logic 1 Current			1	µA	
Logic 0 Current		−110		µA	The minus sign indicates that current is flowing out of the AD9522, which is due to the internal pull-up resistor
Capacitance		2		pF	
RESET TIMING					
Pulse Width Low	50			ns	
$\overline{RESET}$ Inactive to Start of Register Programming	100			ns	
$\overline{SYNC}$ TIMING					
Pulse Width Low	1.3			ns	High speed clock is CLK input signal

SERIAL PORT SETUP PINS: SP1, SP0

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SP1, SP0					These pins do not have internal pull-up/pull-down resistors
Logic Level 0			0.25 × VS	V	VS is the voltage on the VS pin
Logic Level ½	0.4 × VS		0.65 × VS	V	User can float these pins to obtain Logic Level ½; if floating this pin, connect a capacitor to ground
Logic Level 1	0.8 × VS			V	

LD, STATUS, AND REFMON PINS

Table 17.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS					When selected as a digital output (CMOS); there are other modes in which these pins are not CMOS digital outputs; see Table 53, Register 0x017, Register 0x01A, and Register 0x01B
Output Voltage High, V_{OH}	2.7			V	At 1 mA current; maximum recommended current: 5 mA
Output Voltage Low, V_{OL}			0.4	V	At 1 mA current.
MAXIMUM TOGGLE RATE		100		MHz	Applies when mux is set to any divider or counter output, or PFD up/down pulse; also applies in analog lock detect mode; usually debug mode only; note that spurs can couple to output when any of these pins are toggling
ANALOG LOCK DETECT					
Capacitance		3		pF	On-chip capacitance; used to calculate RC time constant for analog lock detect read back; use a pull-up resistor
REF1, REF2, AND VCO FREQUENCY STATUS MONITOR					
Normal Range	1.02			MHz	Frequency above which the monitor indicates the presence of the reference
Extended Range	8			kHz	Frequency above which the monitor indicates the presence of the reference
LD PIN COMPARATOR					
Trip Point		1.6		V	
Hysteresis		260		mV	

POWER DISSIPATION

Table 18.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION, CHIP					Does not include power dissipated in external resistors; all LVDS outputs terminated with 100 Ω across differential pair; all CMOS outputs have 10 pF capacitive loading
Power-On Default		0.88	1.0	W	No clock; no programming; default register values
PLL Locked; One LVDS Output Enabled		0.54	0.63	W	f_{REF} = 25 MHz; f_{OUT} = 250 MHz; VCO = 2250 MHz; VCO divider = 3; one LVDS output and output divider enabled; zero delay off; I_{CP} = 4.8 mA
PLL Locked; One CMOS Output Enabled		0.55	0.66	W	f_{REF} = 25 MHz; f_{OUT} = 62.5 MHz; VCO = 2250 MHz; VCO divider = 3; one CMOS output and output divider enabled; zero delay off; I_{CP} = 4.8 mA
Distribution Only Mode; VCO Divider On; One LVDS Output Enabled		0.36	0.43	W	f_{CLK} = 2.4 GHz; f_{OUT} = 200 MHz; VCO divider = 2; one LVDS output and output divider enabled; zero delay off
Distribution Only Mode; VCO Divider Off; One LVDS Output Enabled		0.33	0.4	W	f_{CLK} = 2.4 GHz; f_{OUT} = 200 MHz; VCO divider bypassed; one LVDS output and output divider enabled; zero delay off
Maximum Power, Full Operation		1.1	1.3	W	PLL on; internal VCO = 2250 MHz; VCO divider = 3; all channel dividers on; 12 LVDS outputs at 125 MHz; zero delay on
$\overline{PD}$ Power-Down		35	50	mW	$\overline{PD}$ pin pulled low; does not include power dissipated in termination resistors
$\overline{PD}$ Power-Down, Maximum Sleep		27	43	mW	$\overline{PD}$ pin pulled low; PLL power-down, Register 0x010[1:0] = 01b; power-down SYNC, Register 0x230[2] = 1b; power-down distribution reference, Register 0x230[1] = 1b
VCP Supply		2.38	8	mW	PLL operating; typical closed-loop configuration
POWER DELTAS, INDIVIDUAL FUNCTIONS					Power delta when a function is enabled/disabled
VCO Divider On/Off		33	43	mW	VCO divider not used
REFIN (Differential) Off		25	31	mW	Delta between reference input off and differential reference input mode
REF1, REF2 (Single-Ended) On/Off		16	22	mW	Delta between reference inputs off and one single-ended reference enabled; double this number if both REF1 and REF2 are powered up
VCO On/Off		60	95	mW	Internal VCO disabled; CLK input selected
PLL Dividers and Phase Detector On/Off		54	67	mW	PLL off to PLL on, normal operation; no reference enabled
LVDS Channel		118	146	mW	No LVDS output on to one LVDS output on; channel divider set to 1
LVDS Driver		11	15	mW	Second LVDS output turned on, same channel
CMOS Channel		120	154	mW	No CMOS output on to one CMOS output on; channel divider set to 1; f_{OUT} = 62.5 MHz and 10 pF of capacitive loading
CMOS Driver On/Off		16	30	mW	Additional CMOS outputs within the same channel turned on
Channel Divider Enabled		33	40	mW	Delta between divider bypassed (divide-by-1) and divide-by-2 to divide-by-32
Zero Delay Block On/Off		30	35	mW	

ABSOLUTE MAXIMUM RATINGS

Table 19.

Parameter or Pin	With Respect to	Rating
VS	GND	−0.3 V to +3.6 V
VCP, CP	GND	−0.3 V to +5.8 V
REFIN, $\overline{\text{REFIN}}$	GND	−0.3 V to VS + 0.3 V
RSET, LF, BYPASS	GND	−0.3 V to VS + 0.3 V
CPRSET	GND	−0.3 V to VS + 0.3 V
CLK, $\overline{\text{CLK}}$	GND	−0.3 V to VS + 0.3 V
CLK	$\overline{\text{CLK}}$	−1.2 V to +1.2 V
SCLK/SCL, SDIO/SDA, SDO, $\overline{\text{CS}}$	GND	−0.3 V to VS + 0.3 V
OUT0, $\overline{\text{OUT0}}$, OUT1, $\overline{\text{OUT1}}$, OUT2, $\overline{\text{OUT2}}$, OUT3, $\overline{\text{OUT3}}$, OUT4, $\overline{\text{OUT4}}$, OUT5, $\overline{\text{OUT5}}$, OUT6, $\overline{\text{OUT6}}$, OUT7, $\overline{\text{OUT7}}$, OUT8, $\overline{\text{OUT8}}$, OUT9, $\overline{\text{OUT9}}$, OUT10, $\overline{\text{OUT10}}$, OUT11, $\overline{\text{OUT11}}$	GND	−0.3 V to VS + 0.3 V
$\overline{\text{SYNC}}$, $\overline{\text{RESET}}$, $\overline{\text{PD}}$	GND	−0.3 V to VS + 0.3 V
REFMON, STATUS, LD	GND	−0.3 V to VS + 0.3 V
SP0, SP1, EEPROM	GND	−0.3 V to VS + 0.3 V
Junction Temperature[1]		125°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (10 sec)		300°C

[1] See the Specifications section for operating temperature range (T_A).

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal impedance measurements were taken on a JEDEC JESD51-5 2S2P test board in still air in accordance with JEDEC JESD51-2. See the Thermal Performance section for more details.

Table 20.

Package Type	θ_{JA}	Unit
64-Lead LFCSP (CP-64-4)	22	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

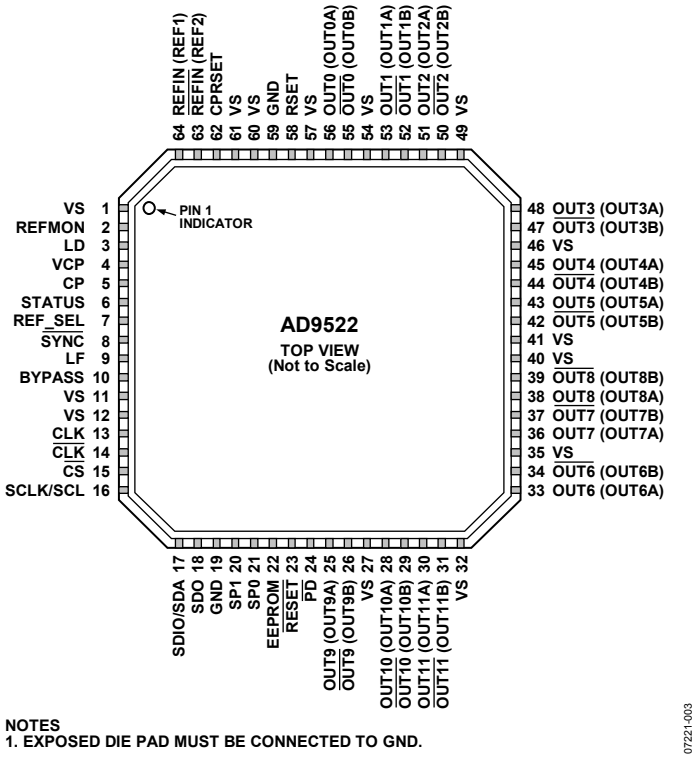

Figure 5. Pin Configuration

Table 21. Pin Function Descriptions

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
1, 11, 12, 27, 32, 35, 40, 41, 46, 49, 54, 57, 60, 61	I	Power	VS	3.3 V Power Pins.
2	O	3.3 V CMOS	REFMON	Reference Monitor (Output). This pin has multiple selectable outputs.
3	O	3.3 V CMOS	LD	Lock Detect (Output). This pin has multiple selectable outputs.
4	I	Power	VCP	Power Supply for Charge Pump (CP); VS ≤ VCP ≤ 5.25 V. VCP must still be connected to 3.3 V if the PLL is not used.
5	O	Loop filter	CP	Charge Pump (Output). This pin connects to an external loop filter. This pin can be left unconnected if the PLL is not used.
6	O	3.3 V CMOS	STATUS	Programmable Status Output.
7	I	3.3 V CMOS	REF_SEL	Reference Select. It selects REF1 (low) or REF2 (high). This pin has an internal 30 kΩ pull-down resistor.
8	I	3.3 V CMOS	$\overline{\text{SYNC}}$	Manual Synchronizations and Manual Holdover. This pin initiates a manual synchronization and is used for manual holdover. Active low. This pin has an internal 30 kΩ pull-up resistor.
9	I	Loop filter	LF	Loop Filter (Input). It connects internally to the VCO control voltage node.
10	O	Loop filter	BYPASS	This pin is for bypassing the LDO to ground with a 220 nF capacitor. This pin can be left unconnected if the PLL is not used.
13	I	Differential clock input	CLK	Along with $\overline{\text{CLK}}$, this pin is the differential input for the clock distribution section.
14	I	Differential clock input	$\overline{\text{CLK}}$	Along with CLK, this pin is the differential input for the clock distribution section. If a single-ended input is connected to the CLK pin, connect a 0.1 µF bypass capacitor from this pin to ground.

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
15	I	3.3 V CMOS	$\overline{CS}$	Serial Control Port Chip Select; Active Low. This pin has an internal 30 kΩ pull-up resistor.
16	I	3.3 V CMOS	SCLK/SCL	Serial Control Port Clock Signal. This pin has an internal 30 kΩ pull-down resistor in SPI mode but is high impedance in I^2C mode.
17	I/O	3.3 V CMOS	SDIO/SDA	Serial Control Port Bidirectional Serial Data In/Out.
18	O	3.3 V CMOS	SDO	Serial Control Port Unidirectional Serial Data Out.
19, 59	I	GND	GND	Ground Pins.
20	I	Three-level logic	SP1	Select SPI or I^2C as the serial interface port and select the I^2C slave address in I^2C mode. Three-level logic. This pin is internally biased for the open logic level.
21	I	Three-level logic	SP0	Select SPI or I^2C as the serial interface port and select the I^2C slave address in I^2C mode. Three-level logic. This pin is internally biased for the open logic level.
22	I	3.3 V CMOS	EEPROM	Setting this pin high selects the register values stored in the internal EEPROM to be loaded at reset and/or power-up. Setting this pin low causes the AD9522 to load the hard-coded default register values at power-up/reset. This pin has an internal 30 kΩ pull-down resistor. Note that to guarantee the proper loading of EEPROM during startup, a high-low-high pulse on the $\overline{RESET}$ pin occurs after the power supply stabilizes.
23	I	3.3 V CMOS	$\overline{RESET}$	Chip Reset, Active Low. This pin has an internal 30 kΩ pull-up resistor.
24	I	3.3 V CMOS	$\overline{PD}$	Chip Power-Down, Active Low. This pin has an internal 30 kΩ pull-up resistor.
25	O	LVDS or CMOS	OUT9 (OUT9A)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
26	O	LVDS or CMOS	$\overline{OUT9}$ (OUT9B)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
28	O	LVDS or CMOS	OUT10 (OUT10A)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
29	O	LVDS or CMOS	$\overline{OUT10}$ (OUT10B)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
30	O	LVDS or CMOS	OUT11 (OUT11A)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
31	O	LVDS or CMOS	$\overline{OUT11}$ (OUT11B)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
33	O	LVDS or CMOS	OUT6 (OUT6A)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
34	O	LVDS or CMOS	$\overline{OUT6}$ (OUT6B)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
36	O	LVDS or CMOS	OUT7 (OUT7A)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
37	O	LVDS or CMOS	$\overline{OUT7}$ (OUT7B)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
38	O	LVDS or CMOS	OUT8 (OUT8A)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
39	O	LVDS or CMOS	$\overline{OUT8}$ (OUT8B)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
42	O	LVDS or CMOS	$\overline{OUT5}$ (OUT5B)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
43	O	LVDS or CMOS	OUT5 (OUT5A)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
44	O	LVDS or CMOS	$\overline{OUT4}$ (OUT4B)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
45	O	LVDS or CMOS	OUT4 (OUT4A)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
47	O	LVDS or CMOS	$\overline{\text{OUT3}}$ (OUT3B)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
48	O	LVDS or CMOS	OUT3 (OUT3A)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
50	O	LVDS or CMOS	$\overline{\text{OUT2}}$ (OUT2B)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
51	O	LVDS or CMOS	OUT2 (OUT2A)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
52	O	LVDS or CMOS	$\overline{\text{OUT1}}$ (OUT1B)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
53	O	LVDS or CMOS	OUT1 (OUT1A)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
55	O	LVDS or CMOS	$\overline{\text{OUT0}}$ (OUT0B)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
56	O	LVDS or CMOS	OUT0 (OUT0A)	Clock Output. This pin can be configured as one side of a differential LVDS output or as a single-ended CMOS output.
58	O	Current set resistor	RSET	Clock Distribution Current Set Resistor. Connect a 4.12 kΩ resistor from this pin to GND.
62	O	Current set resistor	CPRSET	Charge Pump Current Set Resistor. Connect a 5.1 kΩ resistor from this pin to GND. This resistor can be omitted if the PLL is not used.
63	I	Reference input	$\overline{\text{REFIN}}$ (REF2)	Along with REFIN, this is the differential input for the PLL reference. Alternatively, this pin is a single-ended input for REF2.
64	I	Reference input	REFIN (REF1)	Along with $\overline{\text{REFIN}}$, this is the differential input for the PLL reference. Alternatively, this pin is a single-ended input for REF1.
EPAD		GND	GND	The exposed die pad must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

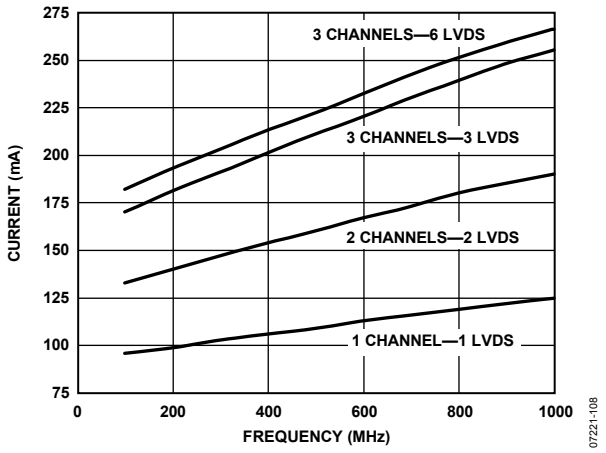

Figure 6. Total Current vs. Frequency, CLK-to-Output (PLL Off), Channel and VCO Divider Bypassed, LVDS Outputs Terminated 100 Ω Across Differential Pair

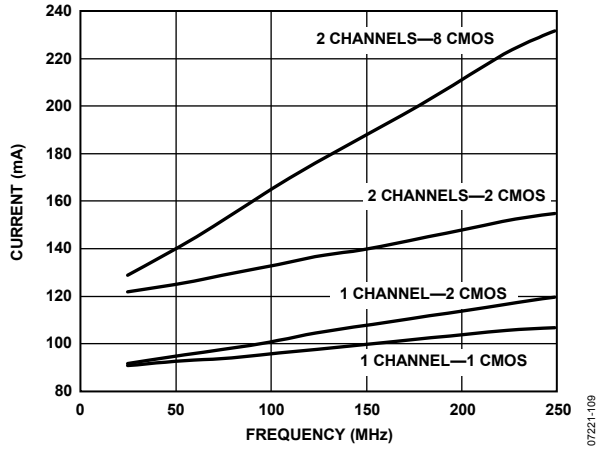

Figure 7. Total Current vs. Frequency, CLK-to-Output (PLL Off), Channel and VCO Divider Bypassed, CMOS Outputs with 10 pF Load

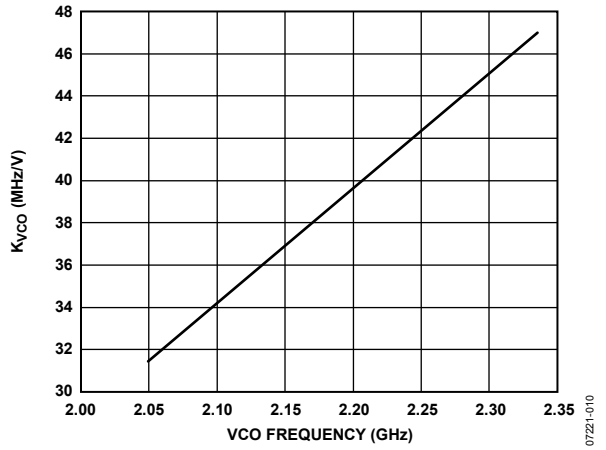

Figure 8. K_{VCO} vs. VCO Frequency

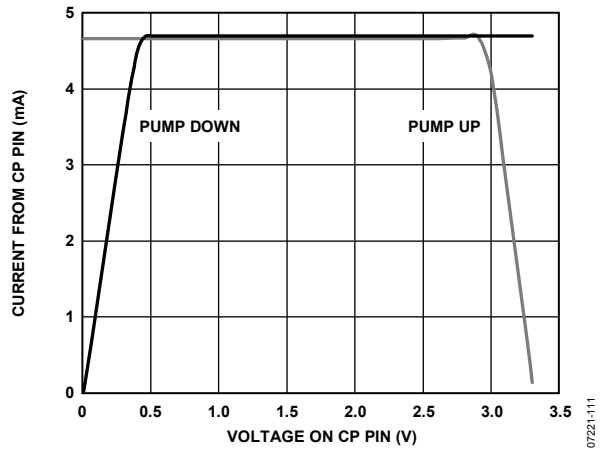

Figure 9. Charge Pump Characteristics at VCP = 3.3 V

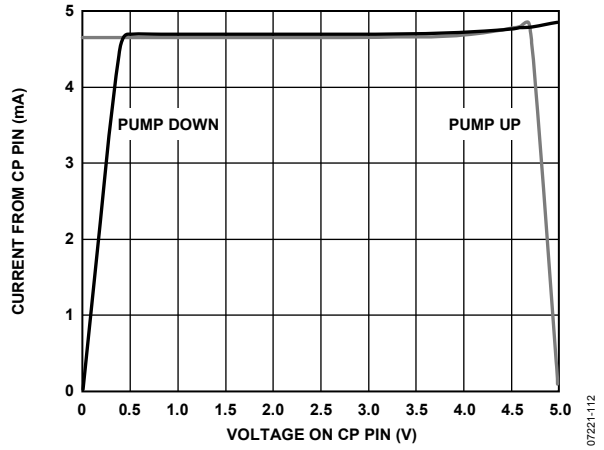

Figure 10. Charge Pump Characteristics at VCP = 5.0 V

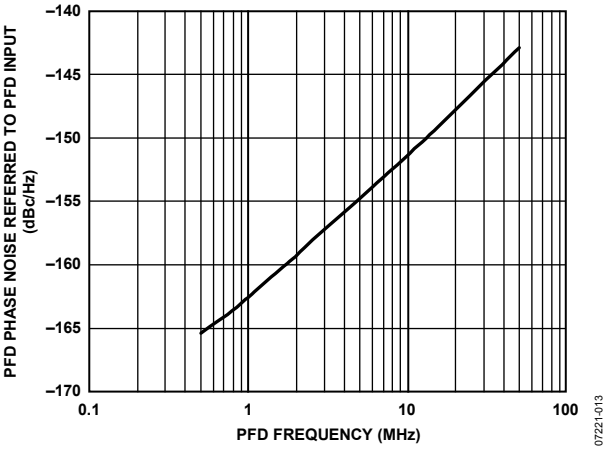

Figure 11. PFD Phase Noise Referred to PFD Input vs. PFD Frequency

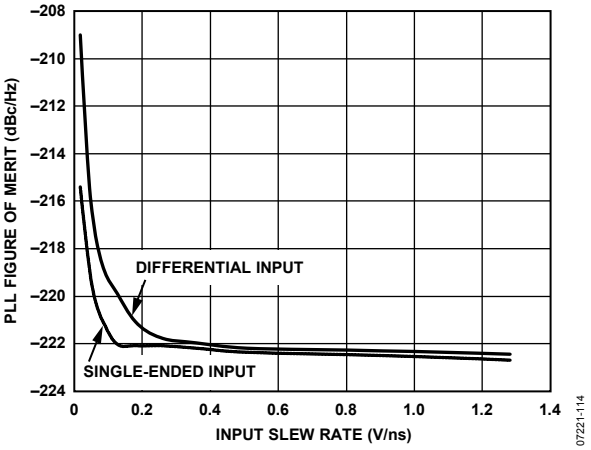

Figure 12. PLL Figure of Merit (FOM) vs. Slew Rate at REFIN/$\overline{\text{REFIN}}$

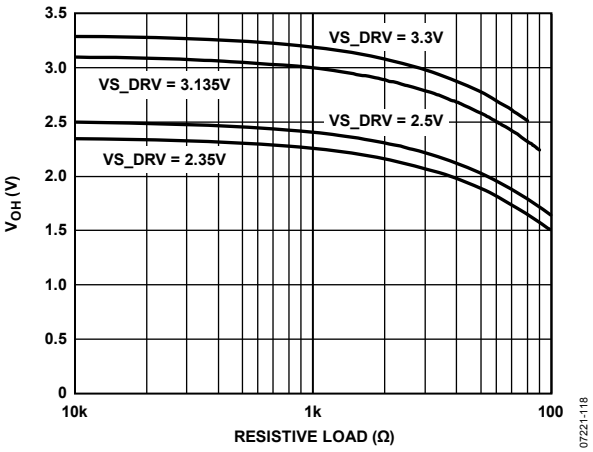

Figure 15. CMOS Output V_{OH} (Static) vs. R_{LOAD} (to Ground)

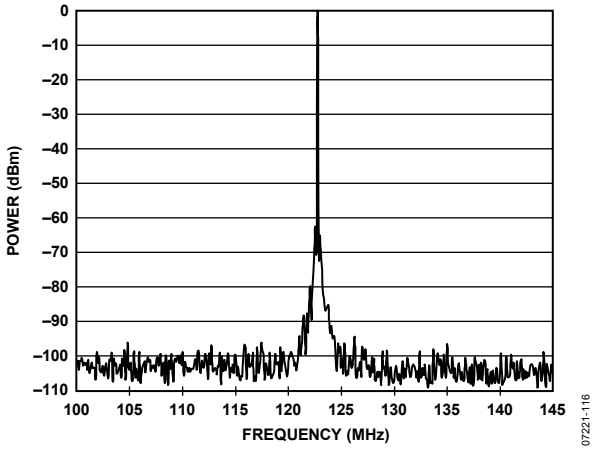

Figure 13. PFD/CP Spurs; 122.88 MHz; PFD = 15.36 MHz; LBW = 127 kHz; I_{CP} = 3.0 mA; f_{VCO} = 2212 MHz

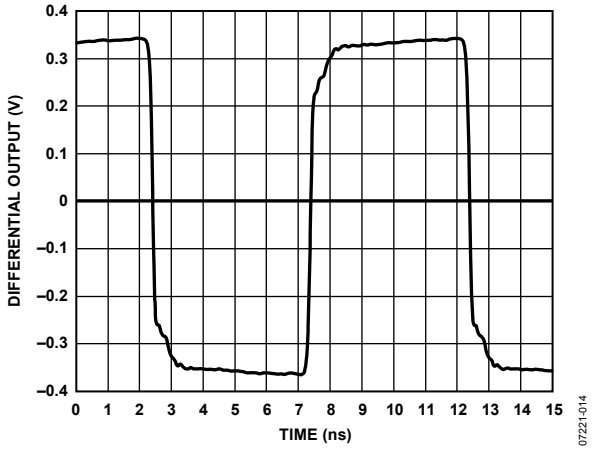

Figure 16. LVDS Output (Differential) at 100 MHz, Output Terminated 100 Ω Across Differential Pair

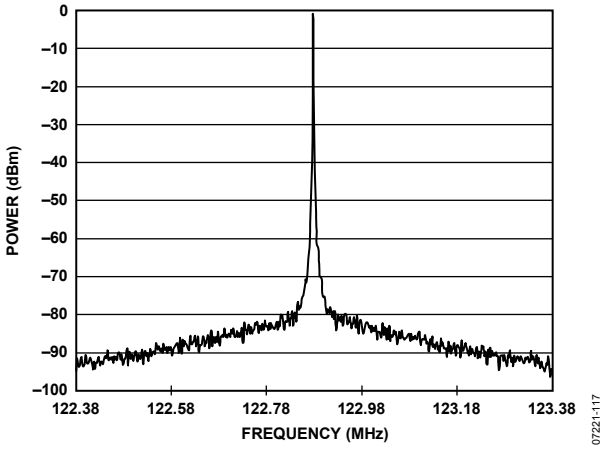

Figure 14. Output Spectrum, LVDS; 122.88 MHz; PFD = 15.36 MHz; LBW = 127 kHz; I_{CP} = 3.0 mA; f_{VCO} = 2212 MHz

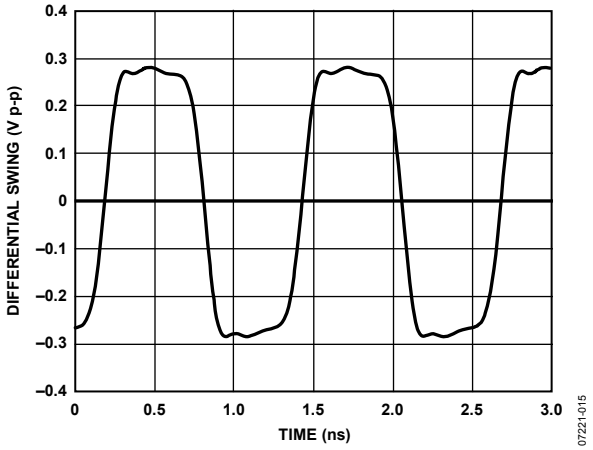

Figure 17. LVDS Differential Voltage Swing at 800 MHz, Output Terminated 100 Ω Across Differential Pair

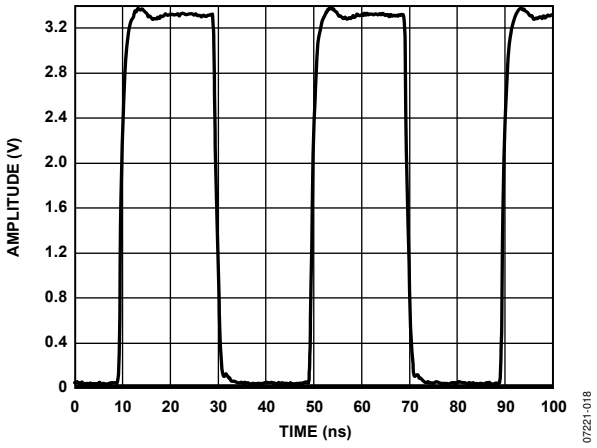

Figure 18. CMOS Output with 10 pF Load at 25 MHz

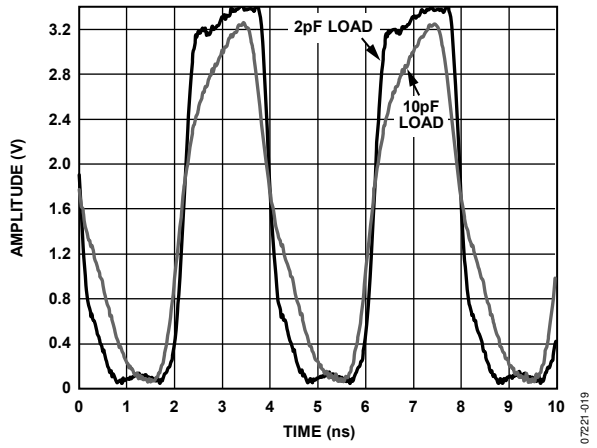

Figure 19. CMOS Output with 2 pF and 10 pF Load at 250 MHz

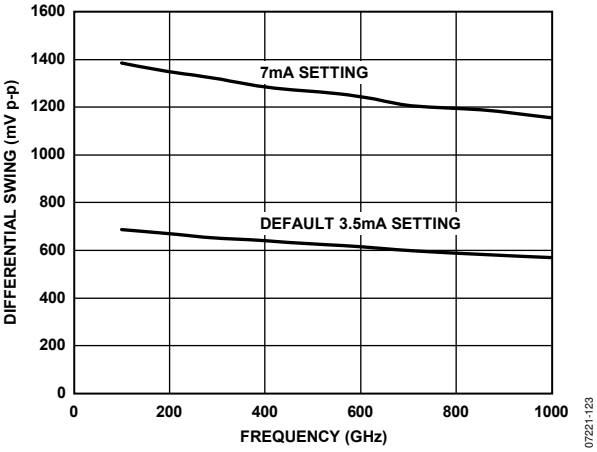

Figure 20. LVDS Differential Voltage Swing vs. Frequency, Output Terminated 100 Ω Across Differential Pair

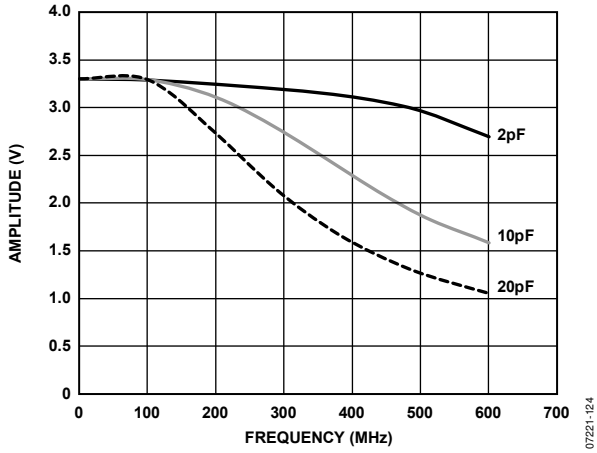

Figure 21. CMOS Output Swing vs. Frequency and Capacitive Load

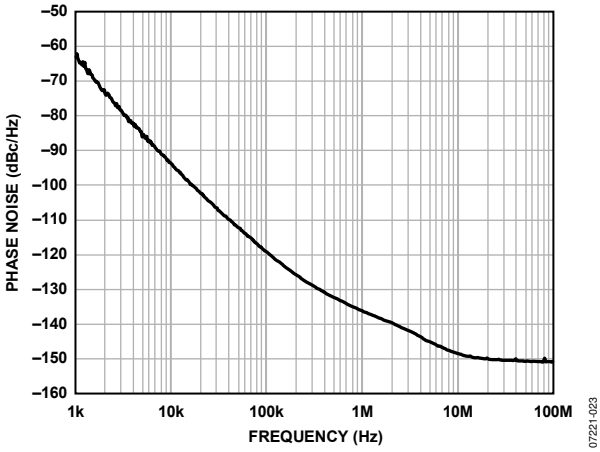

Figure 22. Internal VCO Phase Noise (Absolute), LVDS Output at 673.3 MHz

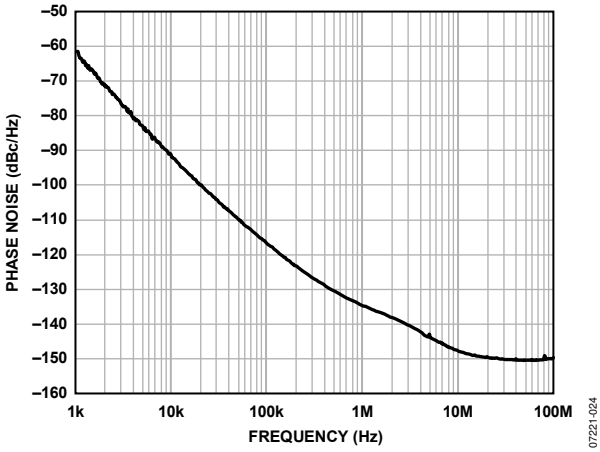

Figure 23. Internal VCO Phase Noise (Absolute), LVDS Output at 725 MHz

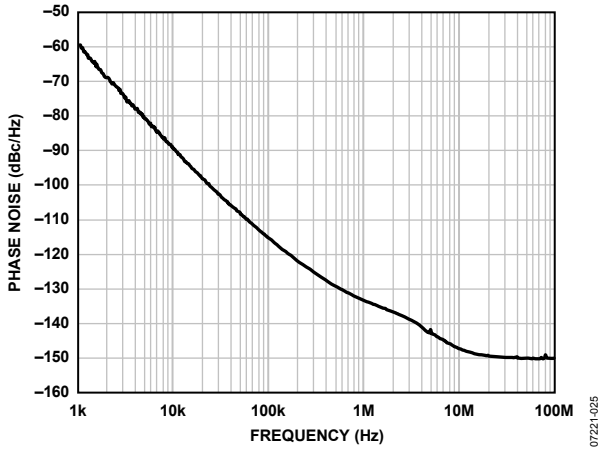

Figure 24. Internal VCO Phase Noise (Absolute), LVDS Output at 778.3 MHz

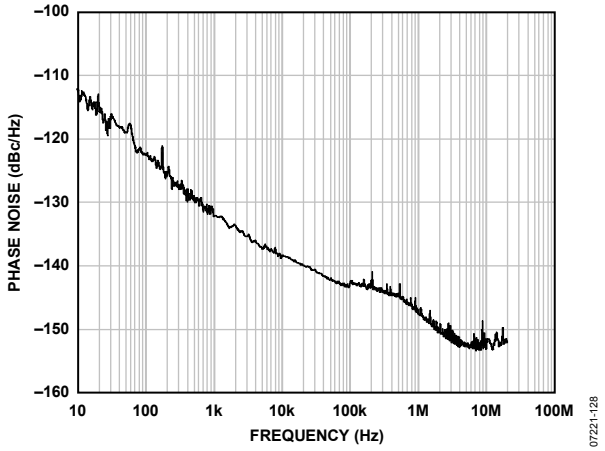

Figure 25. Additive (Residual) Phase Noise, CLK-to-LVDS at 245.76 MHz, Divide-by-1

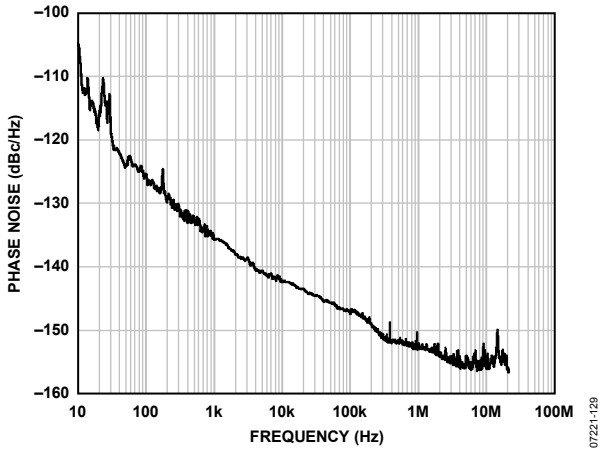

Figure 26. Additive (Residual) Phase Noise, CLK-to-LVDS at 200 MHz, Divide-by-5

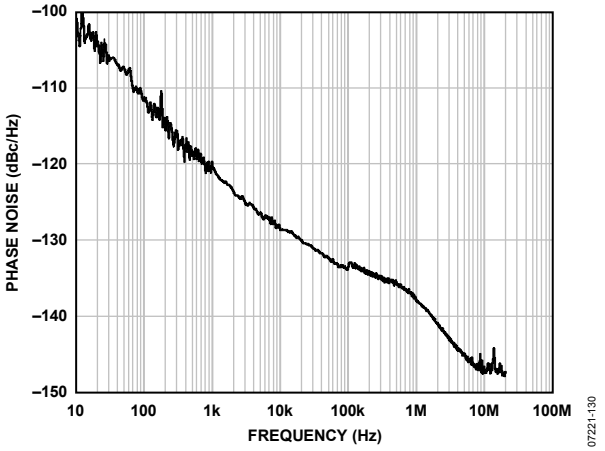

Figure 27. Additive (Residual) Phase Noise, CLK-to-LVDS at 800 MHz, Divide-by-1

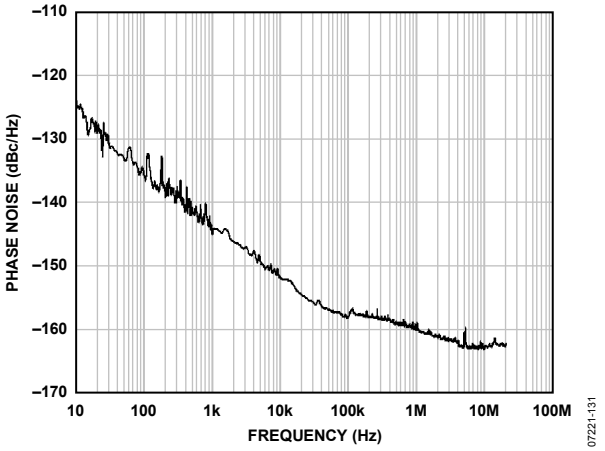

Figure 28. Additive (Residual) Phase Noise, CLK-to-CMOS at 50 MHz, Divide-by-20

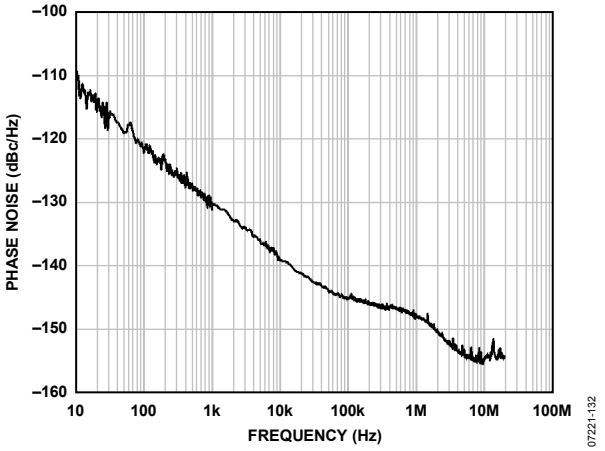

Figure 29. Additive (Residual) Phase Noise, CLK-to-CMOS at 250 MHz, Divide-by-4