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ANALOG DEVICES

Low Jitter Clock Generator with 14 LVPECL/LVDS/HSTL/29 LVCMOS Outputs

Data Sheet

AD9523-1

FEATURES

Output frequency: <1 MHz to 1 GHz
Start-up frequency accuracy: <±100 ppm (determined by
    VCXO reference accuracy)
Zero delay operation
    Input-to-output edge timing: <150 ps
Dual VCO dividers
14 outputs: configurable LVPECL, LVDS, HSTL, and LVCMOS
14 dedicated output dividers with jitter-free adjustable delay
Adjustable delay: 63 resolution steps of ½ period of VCO
    output divider
Output-to-output skew: <50 ps
Duty cycle correction for odd divider settings
Automatic synchronization of all outputs on power-up
Absolute output jitter: <150 fs at 122.88 MHz
    Integration range: 12 kHz to 20 MHz
Broadband timing jitter: 124 fs
Digital lock detect
Nonvolatile EEPROM stores configuration settings
SPI- and I²C-compatible serial control port
Dual PLL architecture
    PLL1
        Low bandwidth for reference input clock cleanup with
            external VCXO
        Phase detector rate up to 130 MHz
        Redundant reference inputs
        Automatic and manual reference switchover modes
            Revertive and nonrevertive switching
        Loss of reference detection with holdover mode
        Low noise LVCMOS output from VCXO used for RF/IF
            synthesizers
    PLL2
        Phase detector rate up to 259 MHz
        Integrated low noise VCO

APPLICATIONS

LTE and multicarrier GSM base stations
Wireless and broadband infrastructure
Medical instrumentation
Clocking high speed ADCs, DACs, DDSs, DDCs, DUCs, MxFEs
Low jitter, low phase noise clock distribution
Clock generation and translation for SONET, 10Ge, 10G FC,
    and other 10 Gbps protocols
Forward error correction (G.710)
High performance wireless transceivers
ATE and high performance instrumentation
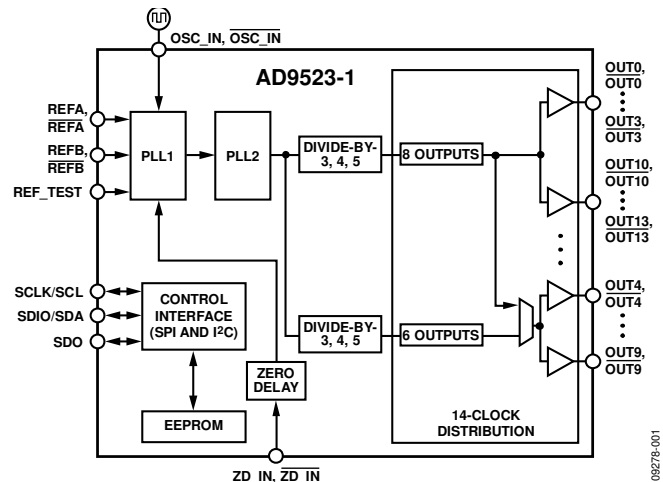
FUNCTIONAL BLOCK DIAGRAM

Figure 1.

GENERAL DESCRIPTION

The AD9523-1 provides a low power, multi-output, clock distribution function with low jitter performance, along with an on-chip PLL and VCO with two VCO dividers. The on-chip VCO tunes from 2.94 GHz to 3.1 GHz.

The AD9523-1 is designed to support the clock requirements for long term evolution (LTE) and multicarrier GSM base station designs. It relies on an external VCXO to provide the reference jitter cleanup to achieve the restrictive low phase noise requirements necessary for acceptable data converter SNR performance.

The input receivers, oscillator, and zero delay receiver provide both single-ended and differential operation. When connected to a recovered system reference clock and a VCXO, the device generates 14 low noise outputs with a range of 1 MHz to 1 GHz, and one dedicated buffered output from the input PLL (PLL1). The frequency and phase of one clock output relative to another clock output can be varied by means of a divider phase select function that serves as a jitter-free, coarse timing adjustment in increments that are equal to half the period of the signal coming out of the VCO.

An in-package EEPROM can be programmed through the serial interface to store user-defined register settings for power-up and chip reset.

AD9523-1* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD-FMCDAQ2-EBZ Evaluation Board
- AD9523/AD9523-1 Evaluation Board
- FPGA Mezzanine Card for Wireless Communications

DOCUMENTATION

Application Notes

- AN-1066: Power Supply Considerations for AD9523, AD9524, and AD9523-1 Low Noise Clocks

Data Sheet

- AD9523-1: Low Jitter Clock Generator with14 LVPECL/ LVDS/HSTL/29 LVCMOS Outputs

User Guides

- UG-182: Evaluation Board User Guide for AD9523-1 Clock Generator

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD9523 Low Jitter Clock Generator Linux Driver

TOOLS AND SIMULATIONS

- ADIsimCLK Design and Evaluation Software
- AD9523/AD9523-1 IBIS Model

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

Technical Articles

- Dual-Loop Clock Generator Cleans Jitter, Provides Multiple High-Frequency Outputs

DESIGN RESOURCES

- AD9523-1 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9523-1 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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REVISION HISTORY

SPECIFICATIONS

f_{VCXO} = 122.88 MHz single-ended, REFA and REFB on differential at 30.72 MHz, f_{VCO} = 2949.12 MHz, doubler is on, unless otherwise noted. Typical is given for VDD = 3.3 V ± 5%, and T_A = 25°C, unless otherwise noted. Minimum and maximum values are given over the full VDD and T_A (−40°C to +85°C) variation, as listed in Table 1.

CONDITIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
VDD3_PLL, Supply Voltage for PLL1 and PLL2	3.135	3.3	3.465	V	3.3 V ± 5%
VDD3_VCO, Supply Voltage for VCO	3.135	3.3	3.465	V	3.3 V ± 5%
VDD3_REF, Supply Voltage Clock Output Drivers Reference	3.135	3.3	3.465	V	3.3 V ± 5%
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers	3.135	3.3	3.465	V	3.3 V ± 5%
VDD1.8_OUT[x:y],[1] Supply Voltage Clock Dividers	1.768	1.8	1.832	V	1.8 V ± 5%
AMBIENT TEMPERATURE RANGE, T_A	−40	+25	+85	°C	
JUNCTION TEMPERATURE, T_J			+115	°C	

[1] x and y are the pair of differential outputs that share the same power supply. For example, VDD3_OUT[0:1] is Supply Voltage Clock Output OUT0, $\overline{OUT0}$ (Pin 68 and Pin 67, respectively) and Supply Voltage Clock Output OUT1, $\overline{OUT1}$ (Pin 65 and Pin 64, respectively).

SUPPLY CURRENT

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLIES OTHER THAN CLOCK OUTPUT DRIVERS					
VDD3_PLL, Supply Voltage for PLL1 and PLL2		37	41.9	mA	Decreases by 9 mA typical if REFB is turned off
VDD3_VCO, Supply Voltage for VCO and VCO Divider M1		70	75.8	mA	All outputs use VCO Divider M1
VDD3_REF, Supply Voltage Clock Output Drivers Reference					
VCO Divider M1 Enabled					
LVPECL Mode, LVDS Mode		4	5.1	mA	Use VCO Divider M1; only one output driver is turned on; for each additional output that is turned on, the current increments by 1.2 mA maximum
HSTL Mode, CMOS Mode		3	3.6	mA	Use VCO Divider M1; values are independent of the number of outputs turned on
VCO Divider M2 Enabled					
LVPECL Mode, LVDS Mode		26	30.1	mA	Use VCO Divider M2; only one output driver is turned on; for each additional output that is turned on, the current increments by 1.2 mA maximum
HSTL Mode, CMOS Mode		24.5	28.6	mA	Use VCO Divider M2; values are independent of the number of outputs turned on
VDD1.8_OUT[x:y],[1] Supply Voltage Clock Dividers		3.2	5.8	mA	Current for each divider: f = 122.88 MHz
VDD1.8_OUT[x:y],[1] Supply Voltage Clock Dividers		6.4	12	mA	Current for each divider: f = 983.04 MHz
CLOCK OUTPUT DRIVERS—LOWER POWER MODE OFF					Channel x control register, Bit 4 = 0
LVDS Mode, 7 mA					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		11.5	13.2	mA	f = 122.88 MHz
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		40	45	mA	f = 983.04 MHz
LVDS Mode, 3.5 mA					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		6.5	7.5	mA	f = 122.88 MHz
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		23	26.3	mA	f = 983.04 MHz
LVPECL Mode					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		13	14.4	mA	f = 122.88 MHz
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		41	46.5	mA	f = 983.04 MHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL Mode, 16 mA					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		20	24.2	mA	f = 122.88 MHz
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		50	59.1	mA	f = 983.04 MHz
HSTL Mode, 8 mA					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		14	16.7	mA	f = 122.88 MHz
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		42.5	49	mA	f = 983.04 MHz
CMOS Mode (Single-Ended)					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		2	2.4	mA	f = 15.36 MHz, 10 pF Load
CLOCK OUTPUT DRIVERS—LOWER POWER MODE ON					Channel x control register, Bit 4 = 1
LVDS Mode, 7 mA					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		10	10.8	mA	f = 122.88 MHz
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		27	29.8	mA	f = 983.04 MHz
LVDS Mode, 3.5 mA					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		6.5	7.5	mA	f = 122.88 MHz
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		23	26.3	mA	f = 983.04 MHz
LVPECL Mode					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		11	12.4	mA	f = 122.88 MHz
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		28	31.2	mA	f = 983.04 MHz
HSTL Mode, 16 mA					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		20	24.3	mA	f = 122.88 MHz
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		50	59.1	mA	f = 983.04 MHz
HSTL Mode, 8 mA					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		11	12.7	mA	f = 122.88 MHz
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		27	31.8	mA	f = 983.04 MHz

[1] x and y are the pair of differential outputs that share the same power supply. For example, VDD3_OUT[0:1] is Supply Voltage Clock Output OUT0, OUT0 (Pin 68 and Pin 67, respectively) and Supply Voltage Clock Output OUT1, OUT1 (Pin 65 and Pin 64, respectively).

POWER DISSIPATION

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION					Does not include power dissipated in termination resistors
Typical Configuration		898	984.7	mW	Clock distribution outputs running as follows: 7 LVPECL at 122.88 MHz, 3 LVDS (3.5 mA) at 61.44 MHz, 3 LVDS (3.5 mA) at 245.76 MHz, 1 single-ended CMOS 10 pF load at 122.88 MHz, 1 differential input reference at 30.72 MHz; f_{VCXO} = 122.88 MHz, f_{VCO} = 2949.12 MHz, VCO Divider M1 at 3, and VCO Divider M2 is off; PLL2 BW = 530 kHz
$\overline{PD}$, Power-Down		74	98.2	mW	$\overline{PD}$ pin pulled low, with typical configuration conditions
INCREMENTAL POWER DISSIPATION					
Base Typical Configuration		393	434.7	mW	Absolute total power with clock distribution; 1 LVPECL output (OUT0) running at 122.88 MHz; 1 differential input reference at 30.72 MHz; f_{VCXO} = 122.88 MHz, f_{VCO} = 2949.12 MHz, VCO Divider M1 at 3; VCO Divider M2 is off
Switched to One Input, Reference Single-Ended Mode		−28.5	−8	mW	Running at 30.72 MHz
Switched to Two Inputs, Reference Differential Mode		26	44.6	mW	Running at 30.72 MHz
Switched to Two Inputs, Reference Single-Ended Mode		−27.5	−5.1	mW	Running at 30.72 MHz
VCO Divider M2		76	88.3	mW	Incremental power increase VCO Divider M2 (OUT4) from base typical
Output Distribution, Driver On					Incremental power increase (OUT1) from base typical
LVDS Mode					
3.5 mA		29	34.8	mW	Single 3.5 mA LVDS output at 122.88 MHz
		88	105.6	mW	Single 3.5 mA LVDS output at 983.04 MHz
7 mA		43	50	mW	Single 7 mA LVDS output at 122.88 MHz
		141	164	mW	Single 7 mA LVDS output at 983.04 MHz
LVPECL Mode		46	51	mW	Single LVPECL output at 122.88 MHz
		144	159	mW	Single LVPECL output at 983.04 MHz
HSTL Mode					
8 mA		44	51	mW	Single 8 mA HSTL output at 122.88 MHz
		143	165	mW	Single 8 mA HSTL output at 983.04 MHz
16 mA		48	55	mW	Single 16 mA HSTL output at 122.88 MHz
		153	176	mW	Single 16 mA HSTL output at 983.04 MHz
CMOS Mode		6.6	7.9	mW	Single 3.3 V CMOS output at 15.36 MHz
		9.9	11.9	mW	Dual complementary 3.3 V CMOS output at 15.36 MHz
		9.9	11.9	mW	Dual in-phase 3.3 V CMOS output at 15.36 MHz
Output Distribution, Driver On					Lower power mode on, (Channel x control register, Bit 4 = 1)
LVDS Mode					
3.5 mA		28.5	33.6	mW	Single 3.5 mA LVDS output at 122.88 MHz
		88	105.6	mW	Single 3.5 mA LVDS output at 983.04 MHz
7 mA		37	42.9	mW	Single 7 mA LVDS output at 122.88 MHz
		98	113.7	mW	Single 7 mA LVDS output at 983.04 MHz
LVPECL Mode		40.5	46	mW	Single LVPECL output at 122.88 MHz
		100	110	mW	Single LVPECL output at 983.04 MHz
HSTL Mode					
8 mA		34	39.1	mW	Single 8 mA HSTL output at 122.88 MHz
		94	108.1	mW	Single 8 mA HSTL output at 983.04 MHz
16 mA		48	55.2	mW	Single 16 mA HSTL output at 122.88 MHz
		153	176	mW	Single 16 mA HSTL output at 983.04 MHz

REFA, $\overline{REFA}$, REFB, $\overline{REFB}$, OSC_IN, $\overline{OSC\_IN}$, AND ZD_IN, $\overline{ZD\_IN}$ INPUT CHARACTERISTICS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL MODE					
Input Frequency Range			400	MHz	
Input Slew Rate (OSC_IN)	400			V/μs	Minimum limit imposed for jitter performance
Common-Mode Internally Generated Input Voltage	0.6	0.7	0.8	V	
Input Common-Mode Range	1.025		1.475	V	For dc-coupled LVDS (maximum swing)
Differential Input Voltage, Sensitivity Frequency < 250 MHz	100			mV p-p	Capacitive coupling required; can accommodate single-ended input by ac grounding of unused input; instantaneous voltage on either pin must not exceed the 1.8 V dc supply rails
Differential Input Voltage, Sensitivity Frequency > 250 MHz	200			mV p-p	Capacitive coupling required; can accommodate single-ended input by ac grounding of unused input; instantaneous voltage on either pin must not exceed the 1.8 V dc supply rails
Differential Input Resistance		4.8		kΩ	
Differential Input Capacitance		1		pF	
Duty Cycle					Duty cycle limits are set by pulse width high and pulse width low
Pulse Width Low	1			ns	
Pulse Width High	1			ns	
CMOS MODE, SINGLE-ENDED INPUT					
Input Frequency Range			250	MHz	
Input High Voltage	2.0			V	
Input Low Voltage			0.8	V	
Input Capacitance		1		pF	
Duty Cycle					Duty cycle limits are set by pulse width high and pulse width low
Pulse Width Low	1.6			ns	
Pulse Width High	1.6			ns	

OSC_CTRL OUTPUT CHARACTERISTICS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT VOLTAGE					
High	VDD3_PLL – 0.15			V	$R_{LOAD} > 20$ kΩ
Low			150	mV	

REF_TEST INPUT CHARACTERISTICS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REF_TEST INPUT					
Input Frequency Range			250	MHz	
Input High Voltage	2.0			V	
Input Low Voltage			0.8	V	

PLL1 OUTPUT CHARACTERISTICS

Table 7.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
MAXIMUM OUTPUT FREQUENCY		250		MHz	
Rise Time/Fall Time (20% to 80%)		387	665	ps	15 pF load
Duty Cycle	45	50	55	%	f = 250 MHz
OUTPUT VOLTAGE HIGH					Output driver static
	VDD3_PLL − 0.25			V	Load current = 10 mA
	VDD3_PLL − 0.1			V	Load current = 1 mA
OUTPUT VOLTAGE LOW					Output driver static
			0.2	V	Load current = 10 mA
			0.1	V	Load current = 1 mA
MAXIMUM PFD FREQUENCY					High is the initial PLL1 antibacklash pulse width setting. The user must program Register 0x019[4] = 1b to enable SPI control of the antibacklash pulse width to the setting defined in Register 0x019[3:2] and Table 39.
Antibacklash Pulse Width					
Minimum			130	MHz	
Low			90	MHz	
High			65	MHz	
Maximum			45	MHz	

[1] CMOS driver strength: strong (see Table 52).

OUT0, $\overline{OUT0}$ TO OUT13, $\overline{OUT13}$ DISTRIBUTION OUTPUT CHARACTERISTICS

Duty cycle performance is specified with the invert divider bit set to 1, and the divider phase bits set to 0.5. (For example, for Channel 0, 0x190[7] = 1 and 0x192[7:2] = 1.)

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL MODE					
Maximum Output Frequency		1		GHz	Minimum VCO/maximum dividers
Rise Time/Fall Time (20% to 80%)		117	147	ps	100 Ω termination across output pair
Duty Cycle	47	50	52	%	f < 500 MHz
	43	48	52	%	f = 500 MHz to 800 MHz
	40	49	54	%	f = 800 MHz to 1 GHz
Differential Output Voltage Swing	643	775	924	mV	Magnitude of voltage across pins; output driver static
Common-Mode Output Voltage	VDD − 1.5	VDD − 1.4	VDD − 1.25	V	Output driver static
SCALED HSTL MODE, 16 mA					
Maximum Output Frequency		1		GHz	Minimum VCO/maximum dividers
Rise Time/Fall Time (20% to 80%)		112	141	ps	100 Ω termination across output pair
Duty Cycle	47	50	52	%	f < 500 MHz
	44	48	51	%	f = 500 MHz to 800 MHz
	40	49	54	%	f = 800 MHz to 1 GHz
Differential Output Voltage Swing	1.3	1.6	1.7	mV	Nominal supply
Supply Sensitivity		0.6		mV/mV	Change in output swing vs. VDD3_OUT[x:y] ($\Delta V_{OD}/\Delta VDD3$)
Common-Mode Output Voltage	VDD − 1.76	VDD − 1.6	VDD − 1.42	V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS MODE, 3.5 mA					
Maximum Output Frequency		1		GHz	
Rise Time/Fall Time (20% to 80%)		138	161	ps	100 Ω termination across output pair
Duty Cycle	48	51	53	%	f < 500 MHz
	43	49	53	%	f = 500 MHz to 800 MHz
	41	49	55	%	f = 800 MHz to 1 GHz
Differential Output Voltage Swing					
Balanced	247		454	mV	Voltage swing between output pins; output driver static
Unbalanced			50	mV	Absolute difference between voltage swing of normal pin and inverted pin
Common-Mode Output Voltage	1.125		1.375	V	Output driver static
Common-Mode Difference			50	mV	Voltage difference between output pins; output driver static
Short-Circuit Output Current		3.5	24	mA	Output driver static
CMOS MODE					
Maximum Output Frequency		250		MHz	
Rise Time/Fall Time (20% to 80%)		387	665	ps	15 pF load
Duty Cycle	45	50	55	%	f = 250 MHz
Output Voltage High					Output driver static
	VDD − 0.25			V	Load current = 10 mA
	VDD − 0.1			V	Load current = 1 mA
Output Voltage Low					Output driver static
			0.2	V	Load current = 10 mA
			0.1	V	Load current = 1 mA

TIMING ALIGNMENT CHARACTERISTICS

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT TIMING SKEW					Delay off on all outputs; maximum deviation between rising edges of outputs; all outputs are on, unless otherwise noted
Between Outputs in Same Group[1]					
LVPECL, HSTL, and LVDS					
Between LVPECL, HSTL, and LVDS Outputs		30	183	ps	
CMOS					
Between CMOS Outputs		100	300	ps	Single-ended, true phase, high-Z mode
Mean Delta Between Groups[1]		50			
Adjustable Delay	0		63	Steps	Resolution step; for example, 8 × 0.5/1 GHz
Resolution Step		500		ps	½ period of 1 GHz
Zero Delay					
Between Input Clock Edge on REFA or REFB to ZD_IN Input Clock Edge, External Zero Delay Mode		150	500	ps	PLL1 settings: PFD = 7.68 MHz, I_{CP} = 63.5 µA, R_{ZERO} = 10 kΩ, antibacklash pulse width is at maximum, BW = 40 Hz, REFA and ZD_IN are set to differential mode

[1] There are three groups of outputs. They are as follows: the top outputs group, consisting of OUT0, OUT1, OUT2, and OUT3; the right outputs group, consisting of OUT4, OUT5, OUT6, OUT7, OUT8, and OUT9; and the bottom outputs group, consisting of OUT10, OUT11, OUT12, and OUT13.

JITTER AND NOISE CHARACTERISTICS

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT ABSOLUTE RMS TIME JITTER					Application example based on a typical setup (see Table 3); f = 122.88 MHz
LVPECL Mode, HSTL Mode, LVDS Mode					
		109		fs	Integrated BW = 200 kHz to 5 MHz
		115		fs	Integrated BW = 200 kHz to 10 MHz
		150		fs	Integrated BW = 12 kHz to 20 MHz
		177		fs	Integrated BW = 10 kHz to 61 MHz
		187		fs	Integrated BW = 1 kHz to 61 MHz
		124		fs	Integrated BW = 1 MHz to 61 MHz

PLL2 CHARACTERISTICS

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VCO (ON CHIP)					
Frequency Range	2940		3100	MHz	
Gain		45		MHz/V	
PLL2 FIGURE OF MERIT (FOM)		−226		dBc/Hz	
MAXIMUM PFD FREQUENCY					
Antibacklash Pulse Width					High is the initial PLL2 antibacklash pulse width setting. The user must program Register 0x019[4] = 1b to enable SPI control of the antibacklash pulse width to the setting defined in Register 0x00F2[3:2] and Table 46.
Minimum			259	MHz	
Low			200	MHz	
High			135	MHz	
Maximum			80	MHz	

LOGIC INPUT PINS—$\overline{PD}$, $\overline{SYNC}$, $\overline{RESET}$, EEPROM_SEL, REF_SEL

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE					
Input High	2.0			V	
Input Low			0.8	V	
INPUT LOW CURRENT		±80	±250	µA	The minus sign indicates that, due to the internal pull-up resistor, current is flowing out of the AD9523-1
CAPACITANCE		3		pF	
RESET TIMING					
Pulse Width Low	50			ns	
Inactive to Start of Register Programming	100			ns	
SYNC TIMING					
Pulse Width Low	1.5			ns	High speed clock is the CLK input signal

STATUS OUTPUT PINS—STATUS1, STATUS0

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE					
Output High	2.94			V	
Output Low			0.4	V	

SERIAL CONTROL PORT—SPI MODE

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{CS}$ (INPUT)					$\overline{CS}$ has an internal 40 kΩ pull-up resistor
Voltage					
Input Logic 1		2.0		V	
Input Logic 0		0.8		V	
Current					
Input Logic 1		30		µA	
Input Logic 0		−110		µA	The minus sign indicates that, due to the internal pull-up resistor, current is flowing out of the AD9523-1
Input Capacitance		2		pF	
SCLK (INPUT) IN SPI MODE					SCLK has an internal 40 kΩ pull-down resistor in SPI mode but not in I²C mode
Voltage					
Input Logic 1		2.0		V	
Input Logic 0		0.8		V	
Current					
Input Logic 1		240		µA	
Input Logic 0		1		µA	
Input Capacitance		2		pF	
SDIO (WHEN INPUT IS IN BIDIRECTIONAL MODE)					
Voltage					
Input Logic 1		2.0		V	
Input Logic 0		0.8		V	
Current					
Input Logic 1		1		µA	
Input Logic 0		1		µA	
Input Capacitance		2		pF	
SDIO, SDO (OUTPUTS)					
Output Logic 1 Voltage	2.7			V	
Output Logic 0 Voltage			0.4	V	
TIMING					
Clock Rate (SCLK, $1/t_{SCLK}$)			25	MHz	
Pulse Width High, t_{HIGH}	8			ns	
Pulse Width Low, t_{LOW}	12			ns	
SDIO to SCLK Setup, t_{DS}	3.3			ns	
SCLK to SDIO Hold, t_{DH}	0			ns	
SCLK to Valid SDIO and SDO, t_{DV}			14	ns	
$\overline{CS}$ to SCLK Setup, t_S	10			ns	
$\overline{CS}$ to SCLK Setup and Hold, t_S, t_C	0			ns	
$\overline{CS}$ Minimum Pulse Width High, t_{PWH}	6			ns	

SERIAL CONTROL PORT—I²C MODE

VDD = VDD3_REF, unless otherwise noted.

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDA, SCL (WHEN INPUTTING DATA)					
Input Logic 1 Voltage	$0.7 \times VDD$			V	
Input Logic 0 Voltage			$0.3 \times VDD$	V	
Input Current with an Input Voltage Between $0.1 \times VDD$ and $0.9 \times VDD$	−10		+10	µA	
Hysteresis of Schmitt Trigger Inputs	$0.015 \times VDD$			V	
Pulse Width of Spikes That Must Be Suppressed by the Input Filter, t_{SPIKE}			50	ns	
SDA (WHEN OUTPUTTING DATA)					
Output Logic 0 Voltage at 3 mA Sink Current			0.4	V	
Output Fall Time from VIH_{MIN} to VIL_{MAX} with a Bus Capacitance from 10 pF to 400 pF	$20 + 0.1\ C_B$[1]		250	ns	
TIMING					Note that all I²C timing values are referred to VIH_{MIN} ($0.3 \times VDD$) and VIL_{MAX} levels ($0.7 \times VDD$)
Clock Rate (SCL, f_{I2C})			400	kHz	
Bus Free Time Between a Stop and Start Condition, t_{IDLE}	1.3			µs	
Setup Time for a Repeated Start Condition, $t_{SET;\ STR}$	0.6			µs	
Hold Time (Repeated) Start Condition, $t_{HLD;\ STR}$	0.6			µs	After this period, the first clock pulse is generated
Setup Time for a Stop Condition, $t_{SET;\ STP}$	0.6			µs	
Low Period of the SCL Clock, t_{LOW}	1.3			µs	
High Period of the SCL Clock, t_{HIGH}	0.6			µs	
SCL, SDA Rise Time, t_{RISE}	$20 + 0.1\ C_B$[1]		300	ns	
SCL, SDA Fall Time, t_{FALL}	$20 + 0.1\ C_B$[1]		300	ns	
Data Setup Time, $t_{SET;\ DAT}$	100			ns	
Data Hold Time, $t_{HLD;\ DAT}$	100		880	ns	This is a minor deviation from the original I²C specification of 0 ns minimum[2]
Capacitive Load for Each Bus Line, C_B[1]			400	pF	

[1] C_B is the capacitance of one bus line in picofarads (pF).
[2] According to the original I²C specification, an I²C master must also provide a minimum hold time of 300 ns for the SDA signal to bridge the undefined region of the SCL falling edge.

ABSOLUTE MAXIMUM RATINGS

Table 16.

Parameter	Rating
VDD3_PLL, VDD3_REF, VDD3_OUT[x:y], LDO_VCO to GND	−0.3 V to +3.6 V
REFA, $\overline{\text{REFA}}$, REFB, $\overline{\text{REFB}}$ to GND	−0.3 V to +3.6 V
SCLK/SCL, SDIO/SDA, SDO, $\overline{\text{CS}}$ to GND	−0.3 V to +3.6 V
OUT0, $\overline{\text{OUT0}}$, OUT1, $\overline{\text{OUT1}}$, OUT2, $\overline{\text{OUT2}}$, OUT3, $\overline{\text{OUT3}}$, OUT4, $\overline{\text{OUT4}}$, OUT5, $\overline{\text{OUT5}}$, OUT6, $\overline{\text{OUT6}}$, OUT7, $\overline{\text{OUT7}}$, OUT8, $\overline{\text{OUT8}}$, OUT9, $\overline{\text{OUT9}}$, OUT10, $\overline{\text{OUT10}}$, OUT11, $\overline{\text{OUT11}}$, OUT12, $\overline{\text{OUT12}}$, OUT13, $\overline{\text{OUT13}}$ to GND	−0.3 V to +3.6 V
$\overline{\text{SYNC}}$, $\overline{\text{RESET}}$, $\overline{\text{PD}}$, REF_SEL to GND	−0.3 V to +3.6 V
STATUS0, STATUS1 to GND	−0.3 V to +3.6 V
SP0, SP1, EEPROM_SEL to GND	−0.3 V to +3.6 V
VDD1.8_OUT[x:y], LDO_PLL1, LDO_DIV_M1 to GND	2 V
Junction Temperature[1]	115°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 sec)	300°C

[1] See Table 17 for θ_{JA}.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 17. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JC}[1, 3]	θ_{JB}[1, 4]	Ψ_{JT}[1, 2]	Unit
72-Lead LFCSP, 10 mm × 10 mm	0	21.3	1.7	12.6	0.1	°C/W
	1.0	20.1			0.2	°C/W
	2.5	18.1			0.3	°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Additional power dissipation information can be found in the Power Dissipation and Thermal Considerations section.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS
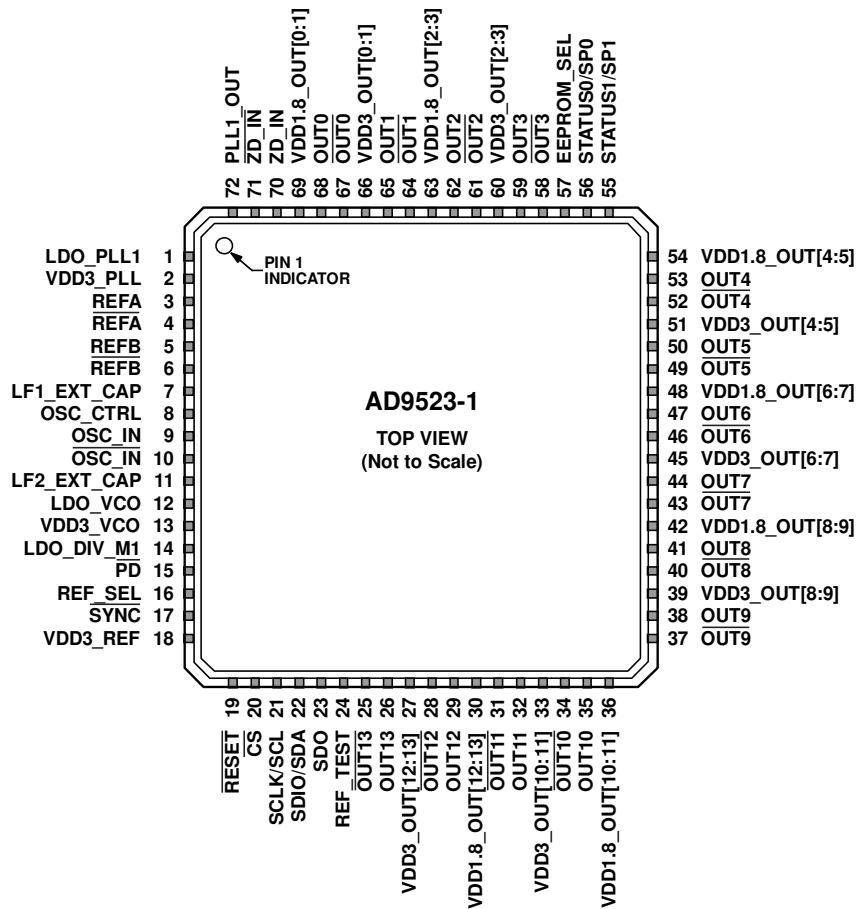
NOTES
1. THE EXPOSED PADDLE IS THE GROUND CONNECTION ON THE CHIP. IT MUST BE SOLDERED
   TO THE ANALOG GROUND OF THE PCB TO ENSURE PROPER FUNCTIONALITY
   AND HEAT DISSIPATION, NOISE, AND MECHANICAL STRENGTH BENEFITS.

Figure 2. Pin Configuration

Table 18. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	LDO_PLL1	P/O	1.8 V Internal LDO Regulator Decoupling Pin for PLL1. Connect a 0.47 μF decoupling capacitor from this pin to ground. Note that for best performance, the LDO bypass capacitor must be placed in close proximity to the device.
2	VDD3_PLL	P	3.3 V Supply PLL1 and PLL2. Use the same supply as VCXO.
3	REFA	I	Reference Clock Input A. Along with $\overline{REFA}$, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
4	$\overline{REFA}$	I	Complementary Reference Clock Input A. Along with REFA, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3V CMOS input.
5	REFB	I	Reference Clock Input B. Along with $\overline{REFB}$, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
6	$\overline{REFB}$	I	Complementary Reference Clock Input B. Along with REFB, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
7	LF1_EXT_CAP	O	PLL1 External Loop Filter Capacitor. Connect this pin to ground.
8	OSC_CTRL	O	Oscillator Control Voltage. Connect this pin to the voltage control pin of the external oscillator.
9	OSC_IN	I	PLL1 Oscillator Input. Along with $\overline{OSC\_IN}$, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
10	$\overline{OSC\_IN}$	I	Complementary PLL1 Oscillator Input. Along with OSC_IN, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.

Pin No.	Mnemonic	Type¹	Description
11	LF2_EXT_CAP	O	PLL2 External Loop Filter Capacitor Connection. Connect capacitor to this pin and the LDO_VCO pin.
12	LDO_VCO	P/O	2.5 V LDO Internal Regulator Decoupling Pin for VCO. Connect a 0.47 μF decoupling capacitor from this pin to ground. Note that, for best performance, the LDO bypass capacitor must be placed in close proximity to the device.
13	VDD3_VCO	P	3.3 V Supply for VCO and VCO M1 Divider.
14	LDO_DIV_M1	P/O	1.8 V LDO Regulator Decoupling Pin for VCO Divider M1. Connect a 0.47 μF decoupling capacitor from this pin to ground. Note that, for best performance, the LDO bypass capacitor must be placed in close proximity to the device.
15	$\overline{PD}$	I	Chip Power-Down, Active Low. This pin has an internal 40 kΩ pull-up resistor.
16	REF_SEL	I	Reference Input Select. This pin has an internal 40 kΩ pull-down resistor.
17	$\overline{SYNC}$	I	Manual Synchronization. This pin initiates a manual synchronization and has an internal 40 kΩ pull-up resistor.
18	VDD3_REF	P	3.3 V Supply for Output Clock Drivers Reference and VCO Divider M2.
19	$\overline{RESET}$	I	Digital Input, Active Low. Resets internal logic to default states. This pin has an internal 40 kΩ pull-up resistor.
20	$\overline{CS}$	I	Serial Control Port Chip Select, Active Low. This pin has an internal 40 kΩ pull-up resistor.
21	SCLK/SCL	I	Serial Control Port Clock Signal for SPI Mode (SCLK) or I²C Mode (SCL). Data clock for serial programming. This pin has an internal 40 kΩ pull-down resistor in SPI mode but is high impedance in I²C mode.
22	SDIO/SDA	I/O	Serial Control Port Bidirectional Serial Data In/Data Out for SPI Mode (SDIO) or I²C Mode (SDA).
23	SDO	O	Serial Data Output. Use this pin to read data in 4-wire mode (high impedance in 3-wire mode). There is no internal pull-up/pull-down resistor on this pin.
24	REF_TEST	I	Test Input to PLL1 Phase Detector.
25	$\overline{OUT13}$	O	Complementary Square Wave Clocking Output 13. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
26	OUT13	O	Square Wave Clocking Output 13. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
27	VDD3_OUT[12:13]	P	3.3 V Supply for Output 12 and Output 13 Clock Drivers.
28	$\overline{OUT12}$	O	Complementary Square Wave Clocking Output 12. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
29	OUT12	O	Square Wave Clocking Output 12. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
30	VDD1.8_OUT[12:13]	P	1.8 V Supply for Output 12 and Output 13 Clock Dividers.
31	$\overline{OUT11}$	O	Complementary Square Wave Clocking Output 11. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
32	OUT11	O	Square Wave Clocking Output 11. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
33	VDD3_OUT[10:11]	P	3.3 V Supply for Output 10 and Output 11 Clock Drivers.
34	$\overline{OUT10}$	O	Complementary Square Wave Clocking Output 10. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
35	OUT10	O	Square Wave Clocking Output 10. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
36	VDD1.8_OUT[10:11]	P	1.8 V Supply for Output 10 and Output 11 Clock Dividers.
37	$\overline{OUT9}$	O	Complementary Square Wave Clocking Output 9. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
38	OUT9	O	Square Wave Clocking Output 9. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
39	VDD3_OUT[8:9]	P	3.3 V Supply for Output 8 and Output 9 Clock Drivers.
40	$\overline{OUT8}$	O	Complementary Square Wave Clocking Output 8. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
41	OUT8	O	Square Wave Clocking Output 8. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
42	VDD1.8_OUT[8:9]	P	1.8 V Supply for Output 8 and Output 9 Clock Dividers.
43	$\overline{OUT7}$	O	Complementary Square Wave Clocking Output 7. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
44	OUT7	O	Square Wave Clocking Output 7. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.

Pin No.	Mnemonic	Type[1]	Description
45	VDD3_OUT[6:7]	P	3.3 V Supply for Output 6 and Supply Output 7 Clock Drivers.
46	$\overline{\text{OUT6}}$	O	Complementary Square Wave Clocking Output 6. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
47	OUT6	O	Square Wave Clocking Output 6. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
48	VDD1.8_OUT[6:7]	P	1.8 V Supply for Output 6 and Output 7 Clock Dividers.
49	$\overline{\text{OUT5}}$	O	Complementary Square Wave Clocking Output 5. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
50	OUT5	O	Square Wave Clocking Output 5. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
51	VDD3_OUT[4:5]	P	3.3 V Supply for Output 4 and Output 5 Clock Drivers.
52	$\overline{\text{OUT4}}$	O	Complementary Square Wave Clocking Output 4. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
53	OUT4	O	Square Wave Clocking Output 4. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
54	VDD1.8_OUT[4:5]	P	1.8 V Supply for Output 4 and Output 5 Clock Dividers.
55	STATUS1/SP1	I/O	Lock Detect and Other Status Signals (STATUS1)/I²C Address (SP1). This pin has an internal 40 kΩ pull-down resistor.
56	STATUS0/SP0	I/O	Lock Detect and Other Status Signals (STATUS0)/I²C Address (SP0). This pin has an internal 40 kΩ pull-down resistor.
57	EEPROM_SEL	I	EEPROM Select. Setting this pin high selects the register values stored in the internal EEPROM to be loaded at reset and/or power-up. Setting this pin low causes the AD9523-1 to load the hard-coded default register values at power-up/reset. This pin has an internal 40 kΩ pull-down resistor.
58	$\overline{\text{OUT3}}$	O	Complementary Square Wave Clocking Output 3. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
59	OUT3	O	Square Wave Clocking Output 3. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
60	VDD3_OUT[2:3]	P	3.3 V Supply for Output 2 and Output 3 Clock Drivers.
61	$\overline{\text{OUT2}}$	O	Complementary Square Wave Clocking Output 2. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
62	OUT2	O	Square Wave Clocking Output 2. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
63	VDD1.8_OUT[2:3]	P	1.8 V Supply for Output 2 and Output 3 Clock Dividers.
64	$\overline{\text{OUT1}}$	O	Complementary Square Wave Clocking Output 1. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
65	OUT1	O	Square Wave Clocking Output 1. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
66	VDD3_OUT[0:1]	P	3.3 V Supply for Output 0 and Output 1 Clock Drivers.
67	$\overline{\text{OUT0}}$	O	Complementary Square Wave Clocking Output 0. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
68	OUT0	O	Square Wave Clocking Output 0. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
69	VDD1.8_OUT[0:1]	P	1.8 V Supply for Output 0 and Output 1 Clock Dividers.
70	ZD_IN	I	External Zero Delay Clock Input. Along with $\overline{\text{ZD\_IN}}$, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
71	$\overline{\text{ZD\_IN}}$	I	Complementary External Zero Delay Clock Input. Along with ZD_IN, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
72	PLL1_OUT	O	Single-Ended CMOS Output from PLL1. This pin has settings for weak and strong in Register 0x1BA, Bit 4 (see Table 52).
EP	EP, GND	GND	Exposed Paddle. The exposed paddle is the ground connection on the chip. It must be soldered to the analog ground of the PCB to ensure proper functionality and heat dissipation, noise, and mechanical strength benefits.

[1] P = power, I = input, O = output, I/O = input/output, P/O = power/output, GND = ground.

TYPICAL PERFORMANCE CHARACTERISTICS

f_{VCXO} = 122.88 MHz, REFA differential at 30.72 MHz, f_{VCO} = 2949.12 MHz, and doubler is off, unless otherwise noted.
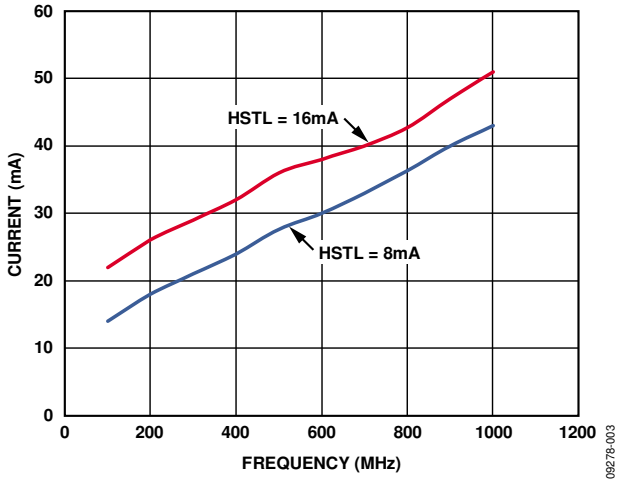

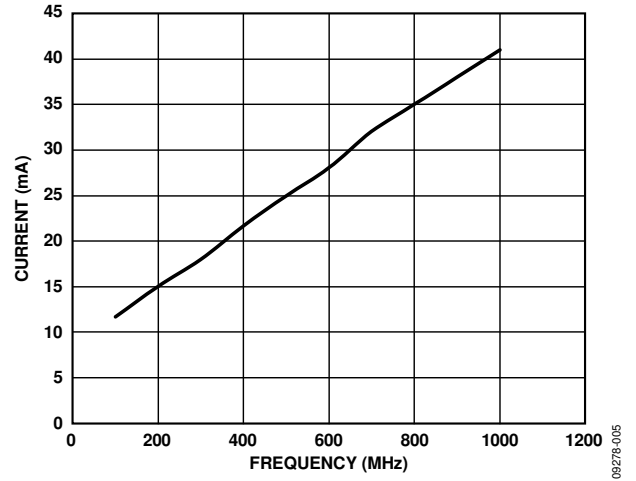Figure 3. VDD3_OUT[x:y] Current (Typical) vs. Frequency;
HSTL Mode at 16 mA and 8 mA

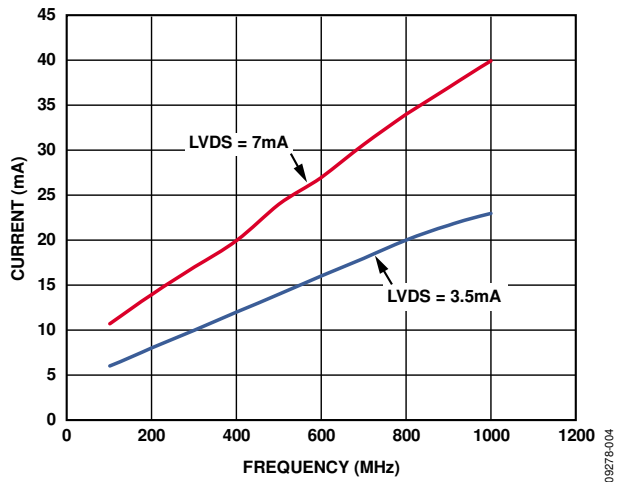Figure 5. VDD3_OUT[x:y] Current (Typical) vs. Frequency, LVPECL Mode

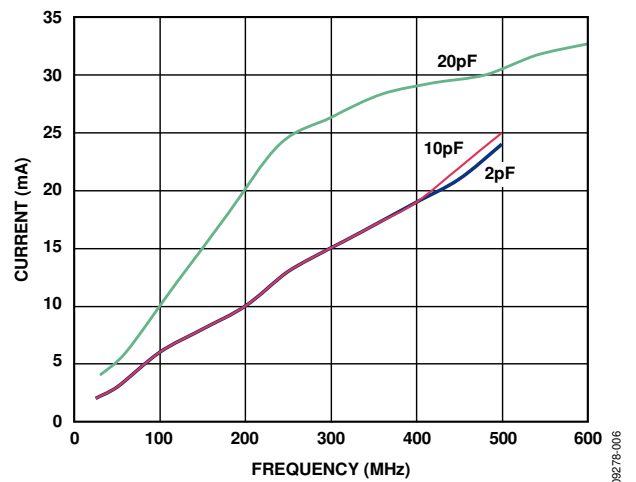Figure 4. VDD3_OUT[x:y] Current (Typical) vs. Frequency;
LVDS Mode at 7 mA and 3.5 mA

Figure 6. VDD3_OUT[x:y] Current (Typical) vs. Frequency;
CMOS Mode at 20 pF, 10 pF, and 2 pF Load
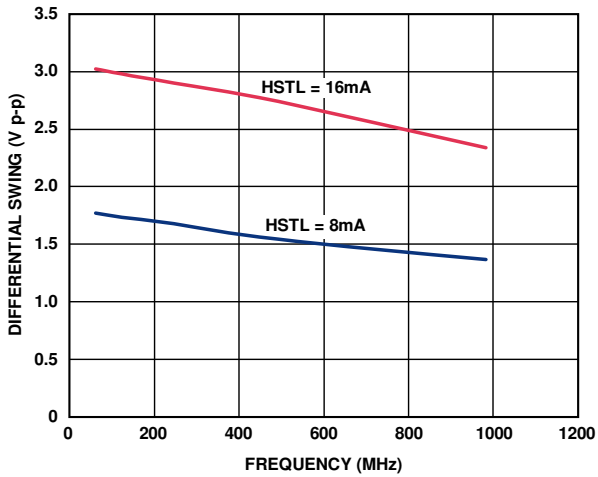
Figure 7. Differential Voltage Swing vs. Frequency;
HSTL Mode at 16 mA and 8 mA

Figure 8. Differential Voltage Swing vs. Frequency, LVPECL Mode

Figure 9. Differential Voltage Swing vs. Frequency;
LVDS Mode at 7 mA and 3.5 mA
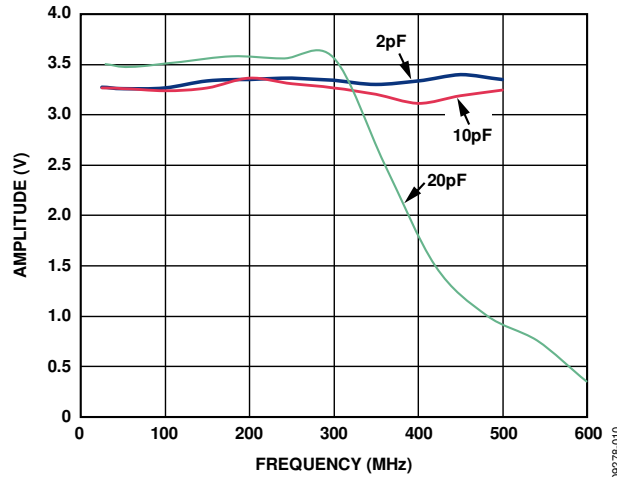
Figure 10. Amplitude vs. Frequency and Capacitive Load;
CMOS Mode at 2 pF, 10 pF, and 20 pF Load
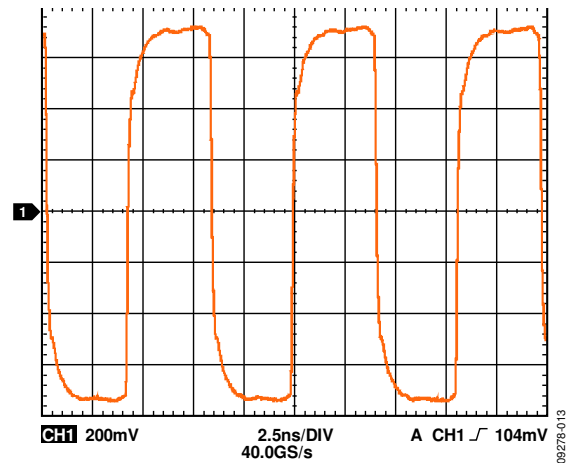
Figure 11. Output Waveform (Differential), LVPECL at 122.88 MHz
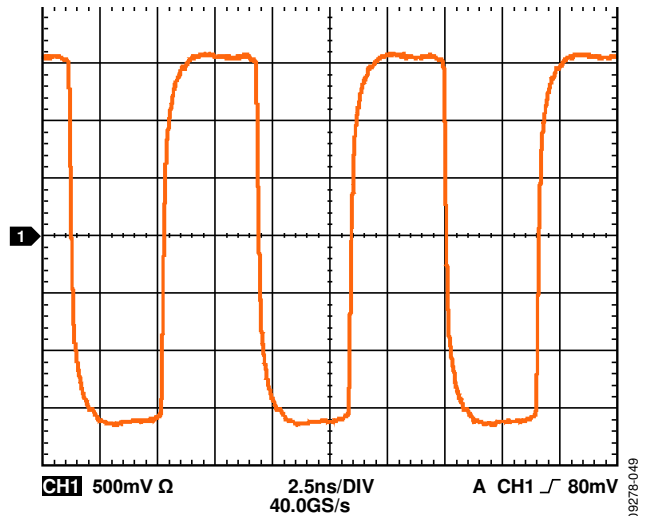
Figure 12. Output Waveform (Differential), HSTL at 16 mA, 122.88 MHz
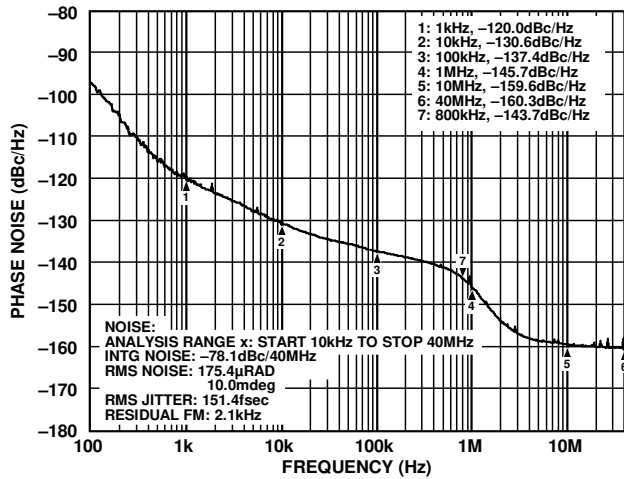
Figure 13. Phase Noise, Output = 184.32 MHz
(VCXO = 122.88 MHz, Crystek VCXO CVHD-950); Doubler On
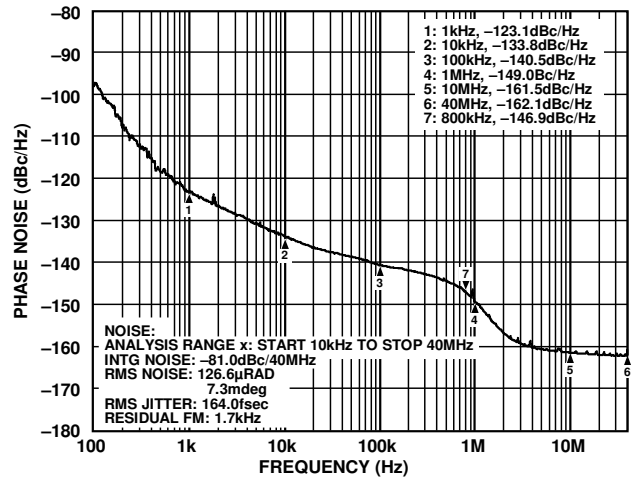
Figure 15. Phase Noise, Output = 122.88 MHz
(VCXO = 122.88 MHz, Crystek VCXO CVHD-950); Doubler On
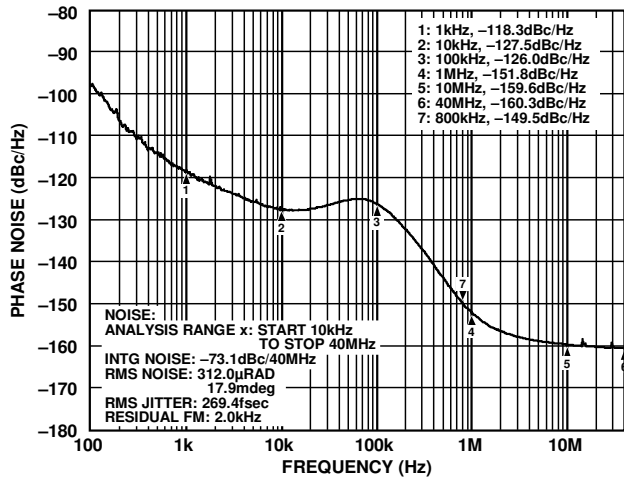
Figure 14. Phase Noise, Output = 184.32 MHz
(VCXO = 122.88 MHz, Crystek VCXO CVHD-950); Doubler On;
Optimized for Low 800 kHz Offset Noise
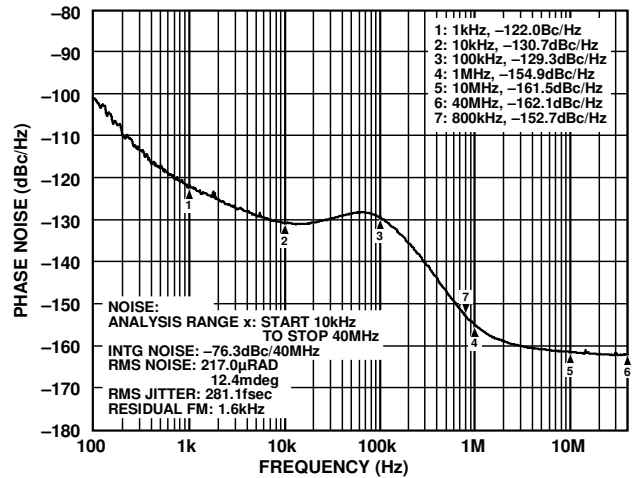
Figure 16. Phase Noise, Output = 122.88 MHz
(VCXO = 122.88 MHz, Crystek VCXO CVHD-950); Doubler On;
Optimized for Low 800 kHz Offset Noise

INPUT/OUTPUT TERMINATION RECOMMENDATIONS
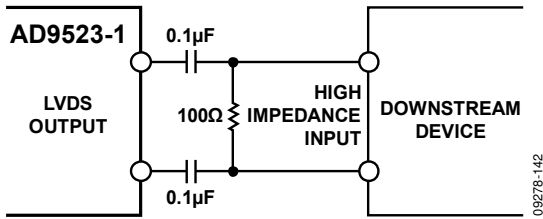
Figure 17. AC-Coupled LVDS Output Driver

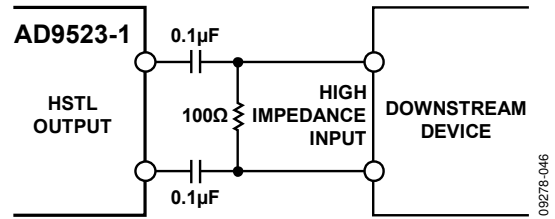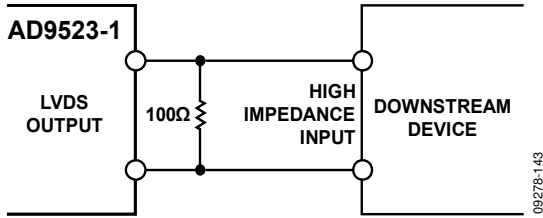*Figure 21. AC-Coupled HSTL Output Driver*
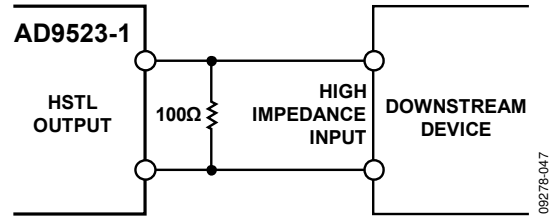

Figure 18. DC-Coupled LVDS Output Driver

Figure 22. DC-Coupled HSTL Output Driver

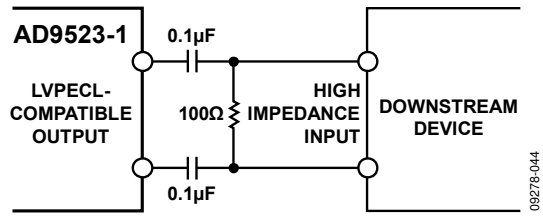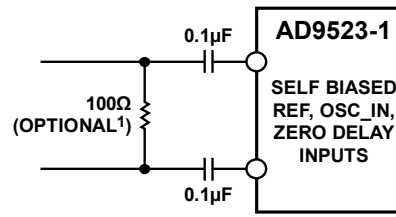*Figure 19. AC-Coupled LVPECL Output Driver*

¹RESISTOR VALUE DEPENDS UPON REQUIRED TERMINATION OF SOURCE.

Figure 23. REF, OSC_IN, and Zero Delay Input Differential Mode

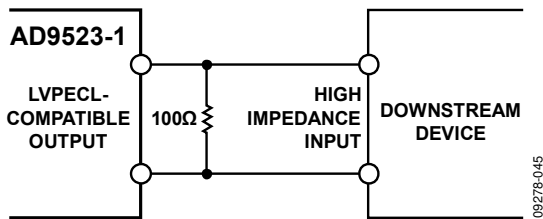*Figure 20. DC-Coupled LVPECL Output Driver*

TERMINOLOGY

Phase Jitter and Phase Noise

An ideal sine wave can be thought of as having a continuous and even progression of phase with time from 0° to 360° for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time. This phenomenon is called phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, which is characterized statistically as being Gaussian (normal) in distribution.

This phase jitter leads to a spreading out of the energy of the sine wave in the frequency domain, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in decibels) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

It is meaningful to integrate the total power contained within some interval of offset frequencies (for example, 10 kHz to 10 MHz). This is called the integrated phase noise over that frequency offset interval and can be readily related to the time jitter due to the phase noise within that offset frequency interval.

Phase noise has a detrimental effect on the performance of ADCs, DACs, and RF mixers. It lowers the achievable dynamic range of the converters and mixers, although they are affected in somewhat different ways.

Time Jitter

Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings varies. In a square wave, the time jitter is a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in seconds root mean square (rms) or 1 sigma of the Gaussian distribution.

Time jitter that occurs on a sampling clock for a DAC or an ADC decreases the signal-to-noise ratio (SNR) and dynamic range of the converter. A sampling clock with the lowest possible jitter provides the highest performance from a given converter.

Additive Phase Noise

Additive phase noise is the amount of phase noise that is attributable to the device or subsystem being measured. The phase noise of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device impacts the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contributes its own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise. When there are multiple contributors to phase noise, the total is the square root of the sum of squares of the individual contributors.

Additive Time Jitter

Additive time jitter is the amount of time jitter that is attributable to the device or subsystem being measured. The time jitter of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device impacts the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contributes its own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.
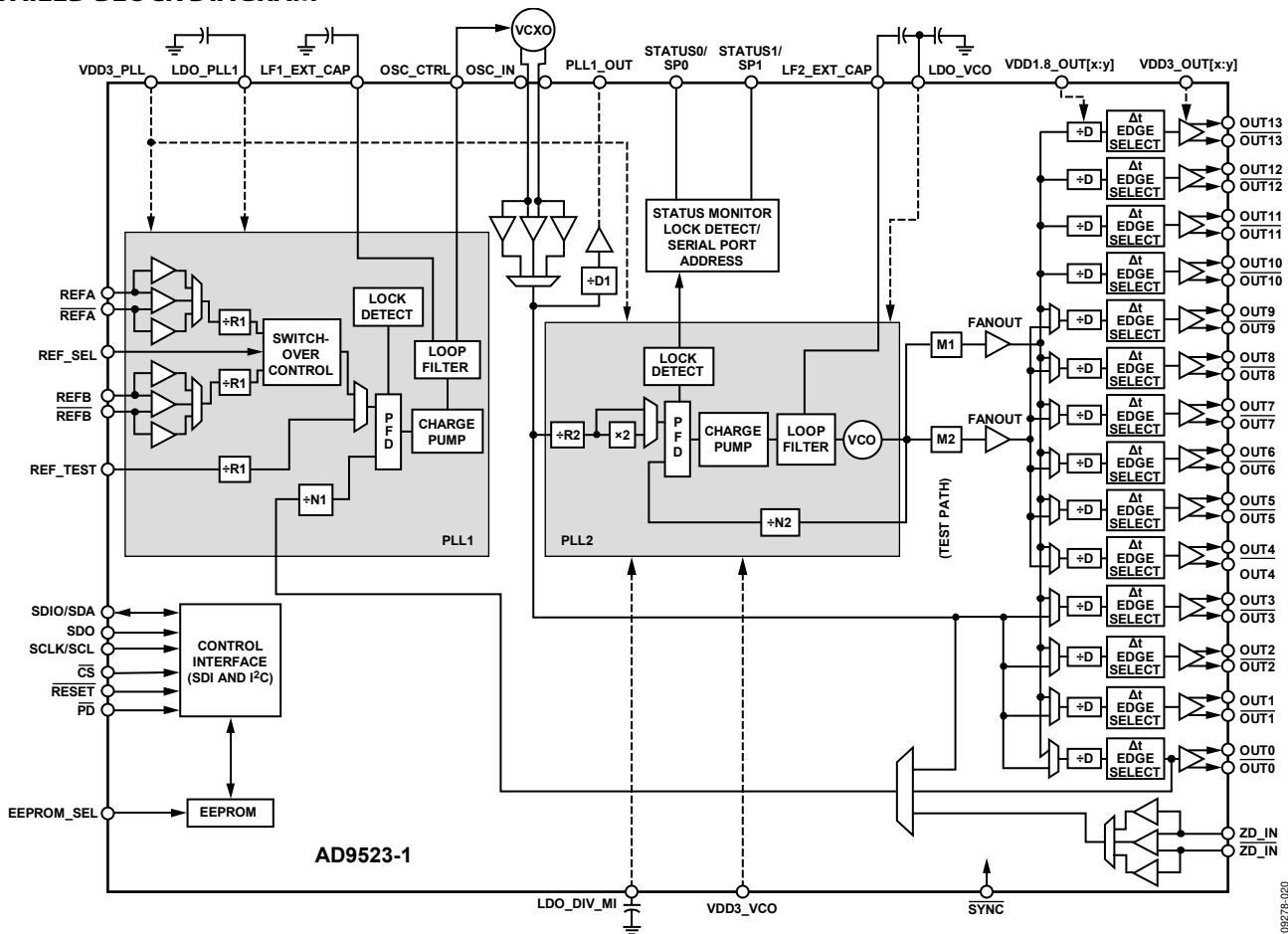
THEORY OF OPERATION

DETAILED BLOCK DIAGRAM

Figure 24. Top Level Diagram

OVERVIEW

The AD9523-1 is a clock generator that employs integer-N-based phase-locked loops (PLL). The device architecture consists of two cascaded PLL stages. The first stage, PLL1, consists of an integer division PLL that uses an external voltage-controlled crystal oscillator (VCXO) from 15 MHz to 250 MHz. PLL1 has a narrow-loop bandwidth that provides initial jitter cleanup of the input reference signal. The second stage, PLL2, is a frequency multiplying PLL that translates the first stage output frequency to a range of 2.94 GHz to 2.96 GHz. PLL2 incorporates an integer-based feedback divider that enables integer frequency multiplication. Programmable integer dividers (1 to 1024) follow PLL2, establishing a final output frequency of 1 GHz or less.

The AD9523-1 includes reference signal processing blocks that enable a smooth switching transition between two reference inputs. This circuitry automatically detects the presence of the reference input signals. If only one input is present, the device uses it as the active reference. If both are present, one becomes the active reference and the other becomes the backup reference. If the active reference fails, the circuitry automatically switches to the backup reference (if available), making it the new active reference.

A register setting determines what action to take if the failed reference is once again available: either stay on Reference B or revert to Reference A. If neither reference is usable, the AD9523-1 supports a holdover mode. A reference select pin (REF_SEL, Pin 16) is available to manually select which input reference is active (see Table 42). The accuracy of the holdover is dependent on the external VCXO frequency stability at half supply voltage.

Any of the divider settings are programmable via the serial programming port, enabling a wide range of input/output frequency ratios under program control. The dividers also include a programmable delay to adjust timing of the output signals, if required.

The 14 outputs are compatible with LVPECL, LVDS, HSTL, and 3.3 V CMOS logic levels (see the Input/Output Termination Recommendations section. All differential output logic settings require a single 100 Ω differential termination.

The loop filters of each PLL are integrated and programmable. Only a single external capacitor for each of the two PLL loop filters is required.

The AD9523-1 operates over the extended industrial temperature range of −40°C to +85°C.

COMPONENT BLOCKS—INPUT PLL (PLL1)

PLL1 General Description

Fundamentally, the input PLL (referred to as PLL1) consists of a phase-frequency detector (PFD), charge pump, passive loop filter, and an external VCXO operating in a closed loop (see Figure 26).

PLL1 has the flexibility to operate with a loop bandwidth of approximately 10 Hz to 100 Hz. This relatively narrow loop bandwidth gives the AD9523-1 the ability to suppress jitter that appears on the input references (REFA and REFB). The output of PLL1 then becomes a low jitter phase-locked version of the reference input system clock.

PLL1 Reference Clock Inputs

The AD9523-1 features two separate differential reference clock inputs, REFA and REFB. These inputs can be configured to operate in full differential mode or single-ended CMOS mode.

In differential mode, these pins are internally self biased. If REFA or REFB is driven single-ended, the unused side ($\overline{REFA}$, $\overline{REFB}$) should be decoupled via a suitable capacitor to a quiet ground. Figure 23 shows the equivalent circuit of REFA or REFB. It is possible to dc couple to these inputs, but the dc operation point should be set as specified in the Specifications tables.

To operate either the REFA input or the REFB input in 3.3 V CMOS mode, the user must set Bit 5 or Bit 6, respectively, in Register 0x01A (see Table 40). The single-ended inputs can be driven by either a dc-coupled CMOS level signal or an ac-coupled sine wave or square wave.

The differential reference input receiver is powered down when the differential reference input is not selected, or when the PLL is powered down. The single-ended buffers power down when the PLL is powered down, when their respective individual power-down registers are set, or when the differential receiver is selected.

The REFB R divider uses the same value as the REFA R divider unless Bit 7, the enable REFB R divider independent division control bit in Register 0x01C, is programmed as shown in Table 42.

OSC_IN Input

The OSC_IN receiver connects to the PLL1 feedback divider and to the PLL2 PFD through an optional doubler. This input receiver is identical to the PLL1 REFA and REFB receivers. Control bits for this receiver are located in Register 0x01A[1:0]. Figure 23 shows the recommended differential input termination to the OSC_IN receiver.

The OSC_IN receiver is powered down when the PLL1 power-down bit is set (Register 0x233[2] = 1b). When using the AD9523-1 in a mode of operation that bypasses PLL1, the PLL1 power-down bit must be disabled (Register 0x233[2] = 0b).

PLL1 Loop Filter

The PLL1 loop filter requires the connection of an external capacitor from LF1_EXT_CAP (Pin 7) to ground. The value of

the external capacitor depends on the use of an external VCXO and the configuration parameters, such as input clock rate and desired bandwidth. Normally, a 0.3 µF capacitor allows the loop bandwidth to range from 10 Hz to 100 Hz and ensures loop stability over the intended operating parameters of the device (see Table 43 for R_{ZERO} values). The operating loop bandwidth (LBW) of PLL1 can be used as a metric to estimate the time required for the PLL to phase lock. In general, PLL1 is phase locked within 10 loop bandwidth time constants, τ_{LBW}, where $\tau_{LBW} = 1/LBW$. Therefore, PLL_TO (see Figure 46) equals $10 \times \tau_{LBW}$.

Figure 25. PLL1 Loop Filter

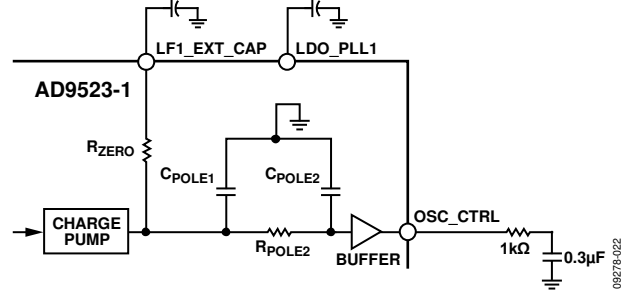**Table 19. PLL1 Loop Filter Programmable Values**

R_{ZERO} (kΩ)	C_{POLE1} (nF)	R_{POLE2} (kΩ)	C_{POLE2} (nF)	LF1_EXT_CAP[1] (µF)
883	1.5 fixed	165 fixed	0.337 fixed	0.3
677				
341				
135				
10				
External				

[1] External loop filter capacitor.

An external R-C low-pass filter should be used at the OSC_CTRL output. The values shown in Figure 25 add an additional low-pass pole at ~530 Hz. This R-C network filters the noise associated with the OSC_CTRL buffer to achieve the best noise performance at the 1 kHz offset region.
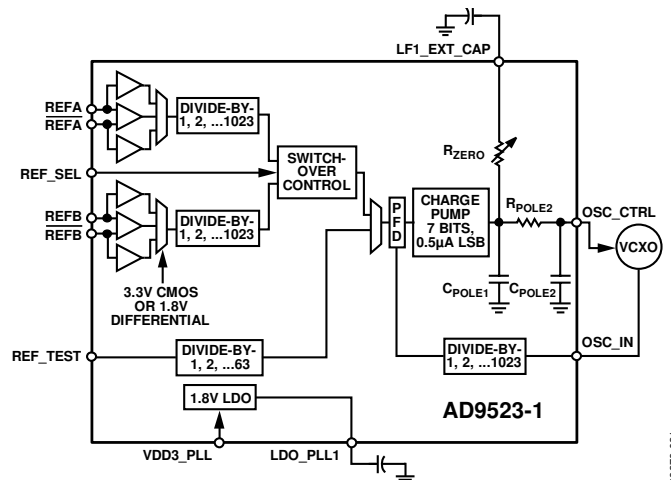

Figure 26. Input PLL (PLL1) Block Diagram

PLL1 Input Dividers

Each reference input feeds a dedicated reference divider block. The input dividers provide division of the reference frequency in integer steps from 1 to 1023. They provide the bulk of the frequency prescaling that is necessary to reduce the reference frequency to accommodate the bandwidth that is typically desired for PLL1.

PLL1 Reference Switchover

The reference monitor verifies the presence/absence of the prescaled REFA and REFB signals (that is, after division by the input dividers). The status of the reference monitor guides the activity of the switchover control logic. The AD9523-1 supports automatic and manual PLL reference clock switching between REFA (the REFA and REFA pins) and REFB (the REFB and REFB pins). This feature supports networking and infrastructure applications that require redundant references.

There are several configurable modes of reference switchover. The manual switchover is achieved either via a programming register setting or by using the REF_SEL pin. The automatic switchover occurs when REFA disappears and there is a reference on REFB.

The reference automatic switchover can be set to work as follows:

- Nonrevertive: stay on REFB. Switch from REFA to REFB when REFA disappears, but do not switch back to REFA if it reappears. If REFB disappears, then go back to REFA.
- Revert to REFA. Switch from REFA to REFB when REFA disappears. Return to REFA from REFB when REFA returns.

See Table 42 for the PLL1 miscellaneous control register bit settings.

PLL1 Holdover

In the absence of both input references, the device enters holdover mode. Holdover is a secondary function that is provided by PLL1. Because PLL1 has an external VCXO available as a frequency source, it continues to operate in the absence of the input reference signals. When the device switches to holdover, the charge pump tristates. The device continues operating in this mode until a reference signal becomes available. Then the device exits holdover mode, and PLL1 resynchronizes with the active reference. In addition to tristate, the charge pump can be forced to VCC/2 during holdover (Register 0x01C, Bit 6; see Table 42).

COMPONENT BLOCKS—OUTPUT PLL (PLL2)

PLL2 General Description

The output PLL (referred to as PLL2) consists of an optional input reference doubler, reference divider, phase-frequency detector (PFD), a partially integrated analog loop filter (see Figure 27), an integrated voltage-controlled oscillator (VCO), and a feedback divider. The VCO produces a nominal 3.0 GHz signal with an output divider that is capable of division ratios of 3, 4, and 5.

The PFD of the output PLL drives a charge pump that increases, decreases, or holds constant the charge stored on the loop filter capacitors (both internal and external). The stored charge results in a voltage that sets the output frequency of the VCO. The feedback loop of the PLL causes the VCO control voltage to vary in a way that phase locks the PFD input signals.

The gain of PLL2 is proportional to the current delivered by the charge pump. The loop filter bandwidth is chosen to reduce noise contributions from PLL sources that could degrade phase noise requirements.

The output PLL has a VCO with multiple bands spanning a range of 2.94 GHz to 3.1 GHz. However, the actual operating frequency within a particular band depends on the control voltage that appears on the loop filter capacitor. The control voltage causes the VCO output frequency to vary linearly within the selected band. This frequency variability allows the control loop of the output PLL to synchronize the VCO output signal with the reference signal applied to the PFD. Typically, the device automatically selects the appropriate band as part of its calibration process (invoked via the VCO control register at Address 0x0F3, shown in Table 47).
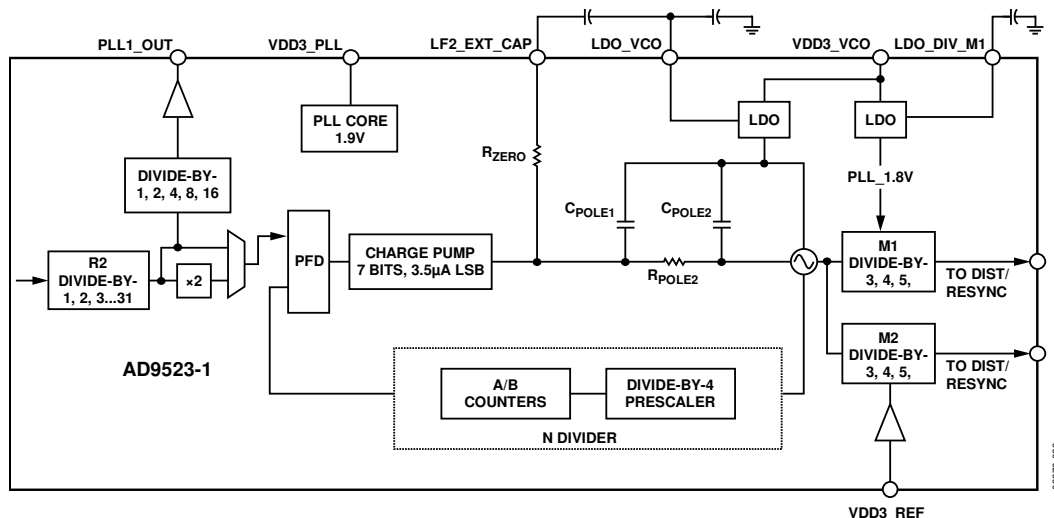

Figure 27. Output PLL (PLL2) Block Diagram