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Jitter Cleaner and Clock Generator with 14 Differential or 29 LVCMOS Outputs

Data Sheet **AD9523**

FEATURES

Output frequency: <1 MHz to 1 GHz
Start-up frequency accuracy: <±100 ppm (determined by VCXO reference accuracy)
Zero delay operation
- **Input-to-output edge timing: <150 ps**

14 outputs: configurable LVPECL, LVDS, HSTL, and LVCMOS
14 dedicated output dividers with jitter-free adjustable delay
Adjustable delay: 63 resolution steps of ½ period of VCO output divider
Output-to-output skew: <50 ps
Duty cycle correction for odd divider settings
Automatic synchronization of all outputs on power-up
Absolute output jitter: <200 fs at 122.88 MHz
- **Integration range: 12 kHz to 20 MHz**

Distribution phase noise floor: −160 dBc/Hz
Digital lock detect
Nonvolatile EEPROM stores configuration settings
SPI- and I²C-compatible serial control port
Dual PLL architecture
- **PLL1**
  - **Low bandwidth for reference input clock cleanup with external VCXO**
  - **Phase detector rate up to130 MHz**
  - **Redundant reference inputs**
  - **Automatic and manual reference switchover modes**
    - **Revertive and nonrevertive switching**
  - **Loss of reference detection with holdover mode**
  - **Low noise LVCMOS output from VCXO used for RF/IF synthesizers**
- **PLL2**
  - **Phase detector rate up to 259 MHz**
  - **Integrated low noise VCO**

APPLICATIONS

LTE and multicarrier GSM base stations
Wireless and broadband infrastructure
Medical instrumentation
Clocking high speed ADCs, DACs, DDSs, DDCs, DUCs, MxFEs
Low jitter, low phase noise clock distribution
Clock generation and translation for SONET, 10Ge, 10G FC, and other 10 Gbps protocols
Forward error correction (G.710)
High performance wireless transceivers
ATE and high performance instrumentation

FUNCTIONAL BLOCK DIAGRAM

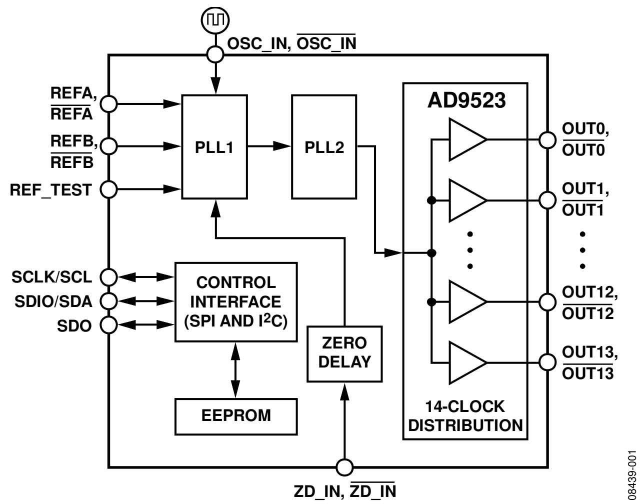

Figure 1.

GENERAL DESCRIPTION

The AD9523 provides a low power, multi-output, clock distribution function with low jitter performance, along with an on-chip PLL and VCO. The on-chip VCO tunes from 3.6 GHz to 4.0 GHz.

The AD9523 is designed to support the clock requirements for long term evolution (LTE) and multicarrier GSM base station designs. It relies on an external VCXO to provide the reference jitter cleanup to achieve the restrictive low phase noise requirements necessary for acceptable data converter SNR performance.

The input receivers, oscillator, and zero delay receiver provide both single-ended and differential operation. When connected to a recovered system reference clock and a VCXO, the device generates 14 low noise outputs with a range of 1 MHz to 1 GHz, and one dedicated buffered output from the input PLL (PLL1). The frequency and phase of one clock output relative to another clock output can be varied by means of a divider phase select function that serves as a jitter-free coarse timing adjustment in increments that are equal to half the period of the signal coming out of the VCO.

An in-package EEPROM can be programmed through the serial interface to store user-defined register settings for power-up and chip reset.

Rev. D **Document Feedback**

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- AD9523/AD9523-1 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1066: Power Supply Considerations for AD9523, AD9524, and AD9523-1 Low Noise Clocks

Data Sheet

- AD9523: Jitter Cleaner and Clock Generator with 14 Differential or 29 LVCMOS Outputs Data Sheet

User Guides

- UG-169: Evaluating the AD9523/AD9524 Clock Generator

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD9523 Low Jitter Clock Generator Linux Driver

TOOLS AND SIMULATIONS

- ADIsimCLK Design and Evaluation Software
- AD9523/AD9523-1 IBIS Model

REFERENCE MATERIALS

Customer Case Studies

- Datang Mobile Case Study

Product Selection Guide

- RF Source Booklet

Technical Articles

- Dual-Loop Clock Generator Cleans Jitter, Provides Multiple High-Frequency Outputs

DESIGN RESOURCES

- AD9523 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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9/15—Rev. C to Rev. D

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3/11—Rev. A to Rev. B

11/10—Rev. 0 to Rev. A

7/10—Revision 0: Initial Version

SPECIFICATIONS

f_{VCXO} = 122.88 MHz single ended, REFA and REFB on differential at 30.72 MHz, f_{VCO} = 3932.16 MHz, doubler is off, channel control low power mode off, divider phase = 1, unless otherwise noted. Typical is given for VDD = 3.3 V ± 5% and T_A = 25°C, unless otherwise noted. Minimum and maximum values are given over the full VDD and T_A (−40°C to +85°C) variation, as listed in Table 1.

CONDITIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
VDD3_PLL1, Supply Voltage for PLL1		3.3		V	3.3 V ± 5%
VDD3_PLL2, Supply Voltage for PLL2		3.3		V	3.3 V ± 5%
VDD3_REF, Supply Voltage Clock Output Drivers Reference		3.3		V	3.3 V ± 5%
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		3.3		V	3.3 V ± 5%
VDD1.8_OUT[x:y],[1] Supply Voltage Clock Dividers		1.8		V	1.8 V ± 5%
TEMPERATURE					
Ambient Temperature Range, T_A	−40	+25	+85	°C	
Junction Temperature, T_J			115	°C	

[1] x and y are the pair of differential outputs that share the same power supply. For example, VDD3_OUT[0:1] is Supply Voltage Clock Output OUT0, $\overline{\text{OUT0}}$ (Pin 68 and Pin 67, respectively) and Supply Voltage Clock Output OUT1, $\overline{\text{OUT1}}$ (Pin 65 and Pin 64, respectively).

SUPPLY CURRENT

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLIES OTHER THAN CLOCK OUTPUT DRIVERS					
VDD3_PLL1, Supply Voltage for PLL1		37	43	mA	Decreases by 9 mA typical if REFB is turned off
VDD3_PLL2, Supply Voltage for PLL2		67	77.7	mA	
VDD3_REF, Supply Voltage Clock Output Drivers Reference					
LVPECL Mode		5	6	mA	Only one output driver turned on; for each additional output that is turned on, the current increments by 1.2 mA maximum
LVDS Mode		4	4.8	mA	Only one output driver turned on; for each additional output that is turned on, the current increments by 1.2 mA maximum
HSTL Mode		3	3.6	mA	Values are independent of the number of outputs turned on
CMOS Mode		3	3.6	mA	Values are independent of the number of outputs turned on
VDD1.8_OUT[x:y],[1] Supply Voltage Clock Dividers[2]		3.5	4.2	mA	Current for each divider: f = 245.76 MHz
CLOCK OUTPUT DRIVERS					
LVDS Mode, 7 mA					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		16	17.4	mA	f = 61.44 MHz
LVDS Mode, 3.5 mA					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		5	6.2	mA	f = 245.76 MHz
LVPECL Mode					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		17	18.9	mA	f = 122.88 MHz
HSTL Mode, 16 mA					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		21	24.0	mA	f = 122.88 MHz
HSTL Mode, 8 mA					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		14	16.3	mA	f = 122.88 MHz
CMOS Mode (Single-Ended)					
VDD3_OUT[x:y],[1] Supply Voltage Clock Output Drivers		2	2.4	mA	f = 15.36 MHz, 10 pF load

[1] x and y are the pair of differential outputs that share the same power supply. For example, VDD3_OUT[0:1] is Supply Voltage Clock Output OUT0, $\overline{\text{OUT0}}$ (Pin 68 and Pin 67, respectively) and Supply Voltage Clock Output OUT1, $\overline{\text{OUT1}}$ (Pin 65 and Pin 64, respectively).
[2] The current for Pin 63 (VDD1_OUT[0:3]) is 2× that of the other VDD11.8_OUT[x:y] pairs.

POWER DISSIPATION

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION					Does not include power dissipated in termination resistors
Typical Configuration		876	970	mW	Clock distribution outputs running as follows: seven LVPECL outputs at 122.88 MHz, three LVDS outputs (3.5 mA) at 61.44 MHz, three LVDS outputs (3.5 mA) at 245.76 MHz, one CMOS 10 pF load at 122.88 MHz, and one differential input reference at 30.72 MHz; f_{VCXO} = 122.88 MHz, f_{VCO} = 3932.16 MHz; PLL2 BW = 530 kHz, doubler is off
$\overline{PD}$, Power-Down		101	132.2	mW	$\overline{PD}$ pin pulled low, with typical configuration conditions
INCREMENTAL POWER DISSIPATION					
Low Power Typical Configuration		389	450	mW	Absolute total power with clock distribution; one LVPECL output running at 122.88 MHz; one differential input reference at 30.72 MHz; f_{VCXO} = 122.88 MHz, f_{VCO} = 3932.16 MHz; doubler is off
Output Distribution, Driver On					Incremental power increase (OUT1) from low power typical
LVDS		15.3	18.4	mW	Single 3.5 mA LVDS output at 245.76 MHz
		47.8	55.4	mW	Single 7 mA LVDS output at 61.44 MHz
LVPECL		50.1	54.9	mW	Single LVPECL output at 122.88 MHz
HSTL		40.2	46.3	mW	Single 8 mA HSTL output at 122.88 MHz
		43.7	50.3	mW	Single 16 mA HSTL output at 122.88 MHz
CMOS		6.6	7.9	mW	Single 3.3 V CMOS output at 15.36 MHz
		9.9	11.9	mW	Dual complementary 3.3 V CMOS output at 122.88 MHz
		9.9	11.9	mW	Dual in-phase 3.3 V CMOS output at 122.88 MHz

REFA, $\overline{REFA}$, REFB, $\overline{REFB}$, OSC_IN, $\overline{OSC\_IN}$, AND ZD_IN, $\overline{ZD\_IN}$ INPUT CHARACTERISTICS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL MODE					
Input Frequency Range			400	MHz	
Input Slew Rate (OSC_IN)	400			V/µs	Minimum limit imposed for jitter performance
Common-Mode Internally Generated Input Voltage	0.6	0.7	0.8	V	
Input Common-Mode Range	1.025		1.475	V	For dc-coupled LVDS (maximum swing)
Differential Input Voltage, Sensitivity Frequency < 250 MHz	100			mV p-p	Capacitive coupling required; can accommodate single-ended input by ac grounding of unused input; the instantaneous voltage on either pin must not exceed the 1.8 V dc supply rails
Differential Input Voltage, Sensitivity Frequency > 250 MHz	200			mV p-p	Capacitive coupling required; can accommodate single-ended input by ac grounding of unused input; the instantaneous voltage on either pin must not exceed the 1.8 V dc supply rails
Differential Input Resistance		4.8		kΩ	
Differential Input Capacitance		1		pF	
Duty Cycle					Duty cycle bounds are set by pulse width high and pulse width low
Pulse Width Low	1			ns	
Pulse Width High	1			ns	
CMOS MODE SINGLE-ENDED INPUT					
Input Frequency Range			250	MHz	
Input High Voltage	1.62			V	
Input Low Voltage			0.52	V	
Input Threshold Voltage		1.0		V	When ac coupling to the input receiver, the user must dc bias the input to 1 V; the single-ended CMOS input is 3.3 V compatible
Input Capacitance		1		pF	
Duty Cycle					Duty cycle bounds are set by pulse width high and pulse width low
Pulse Width Low	1.6			ns	
Pulse Width High	1.6			ns	

OSC_CTRL OUTPUT CHARACTERISTICS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT VOLTAGE					
High	VDD3_PLL1 − 0.15			V	R_{LOAD} > 20 kΩ
Low			150	mV	

REF_TEST INPUT CHARACTERISTICS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REF_TEST INPUT					
Input Frequency Range			250	MHz	
Input High Voltage	2.0			V	
Input Low Voltage			0.8	V	

PLL1 CHARACTERISTICS

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PLL1 FIGURE OF MERIT (FOM)		−226		dBc/Hz	
MAXIMUM PFD FREQUENCY					
Antibacklash Pulse Width					High is the initial PLL1 antibacklash pulse width setting. The user must program Register 0x019[4] = 1b to enable SPI control of the antibacklash pulse width to the setting defined in Register 0x019[3:2] and Table 40.
Minimum			130	MHz	
Low			90	MHz	
High			65	MHz	
Maximum			45	MHz	

PLL1 OUTPUT CHARACTERISTICS

Table 8.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
MAXIMUM OUTPUT FREQUENCY		250		MHz	
Rise/Fall Time (20% to 80%)		387	665	ps	15 pF load
Duty Cycle	45	50	55	%	f = 250 MHz
OUTPUT VOLTAGE HIGH					Output driver static
	VDD3_PLL1 − 0.25			V	Load current = 10 mA
	VDD3_PLL1 − 0.1			V	Load current = 1 mA
OUTPUT VOLTAGE LOW					Output driver static
			0.2	V	Load current = 10 mA
			0.1	V	Load current = 1 mA

[1] CMOS driver strength = strong (see Table 52).

DISTRIBUTION OUTPUT CHARACTERISTICS (OUT0, $\overline{\text{OUT0}}$ TO OUT13, $\overline{\text{OUT13}}$)

Duty cycle performance is specified with the invert divider bit set to 1, and the divider phase bits set to 0.5. (For example, for Channel 0, 0x190[7] = 1 and 0x192[7:2] = 1.) Output Voltage Reference VDD in Table 9 refers to the 3.3 VDD3_OUT[x:y] supply.

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL MODE					
Maximum Output Frequency		1		GHz	Minimum VCO/maximum dividers
Rise Time/Fall Time (20% to 80%)		117	147	ps	100 Ω termination across output pair
Duty Cycle	47	50	52	%	f < 500 MHz
	43	48	52	%	f = 500 MHz to 800 MHz
	40	49	54	%	f = 800 MHz to 1 GHz
Differential Output Voltage Magnitude	643	775	924	mV	Voltage across pins, output driver static
Common-Mode Output Voltage	VDD – 1.5	VDD – 1.4	VDD – 1.25	V	Output driver static
SCALED HSTL MODE, 16 mA					
Maximum Output Frequency		1		GHz	Minimum VCO/maximum dividers
Rise Time/Fall Time (20% to 80%)		112	141	ps	100 Ω termination across output pair
Duty Cycle	47	50	52	%	f < 500 MHz
	44	48	51	%	f = 500 MHz to 800 MHz
	40	49	54	%	f = 800 MHz to 1 GHz
Differential Output Voltage Magnitude	1.3	1.6	1.7	V	Voltage across pins, output driver static; nominal supply
Supply Sensitivity		0.6		mV/mV	Change in output swing vs. VDD3_OUT[x:y] ($\Delta V_{OD}/\Delta VDD3$)
Common-Mode Output Voltage	VDD – 1.76	VDD – 1.6	VDD – 1.42	V	
LVDS MODE, 3.5 mA					
Maximum Output Frequency		1		GHz	
Rise Time/Fall Time (20% to 80%)		138	161	ps	100 Ω termination across output pair
Duty Cycle	48	51	53	%	f < 500 MHz
	43	49	53	%	f = 500 MHz to 800 MHz
	41	49	55	%	f = 800 MHz to 1 GHz
Differential Output Voltage Magnitude					
Balanced	247		454	mV	Voltage across pins; output driver static
Unbalanced			50	mV	Absolute difference between voltage magnitude of normal pin and inverted pin
Common-Mode Output Voltage	1.125		1.375	V	Output driver static
Common-Mode Difference			50	mV	Voltage difference between output pins; output driver static
Short-Circuit Output Current		3.5	24	mA	Output driver static
CMOS MODE					
Maximum Output Frequency		250		MHz	
Rise Time/Fall Time (20% to 80%)		387	665	ps	15 pF load
Duty Cycle	45	50	55	%	f = 250 MHz
Output Voltage High					Output driver static
	VDD – 0.25			V	Load current = 10 mA
	VDD – 0.1			V	Load current = 1 mA
Output Voltage Low					Output driver static
			0.2	V	Load current = 10 mA
			0.1	V	Load current = 1 mA

TIMING ALIGNMENT CHARACTERISTICS

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT TIMING SKEW					Delay off on all outputs; maximum deviation between rising edges of outputs; all outputs are on, unless otherwise noted
Between Outputs in Same Group[1]					
LVPECL, HSTL, and LVDS					
Between LVPECL, HSTL, and LVDS Outputs		30	183	ps	
CMOS					
Between CMOS Outputs		100	300	ps	Single-ended true phase high-Z mode
Mean Delta Between Groups[1]		50			
Adjustable Delay	0		63	Steps	Resolution step; for example, 8 × 0.5/1 GHz
Resolution Step		500		ps	½ period of 1 GHz
Zero Delay					
Between Input Clock Edge on REFA or REFB to ZD_IN Input Clock Edge, External Zero Delay Mode		150	500	ps	PLL1 settings: PFD = 7.68 MHz, I_{CP} = 63.5 µA, R_{ZERO} = 10 kΩ, antibacklash pulse width is at maximum, BW = 40 Hz, REFA and ZD_IN are set to differential mode

[1] There are three groups of outputs. They are as follows: the top outputs group: OUT0, OUT1, OUT2, OUT3; the right outputs group: OUT4, OUT5, OUT6, OUT7, OUT8, OUT9; and the bottom outputs group: OUT10, OUT11, OUT12, OUT13.

JITTER AND NOISE CHARACTERISTICS

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT ABSOLUTE RMS TIME JITTER					Application example based on a typical setup (see Table 3); f = 122.88 MHz
LVPECL Mode, HSTL Mode, LVDS Mode					
		125		fs	Integrated BW = 200 kHz to 5 MHz
		136		fs	Integrated BW = 200 kHz to 10 MHz
		169		fs	Integrated BW = 12 kHz to 20 MHz
		212		fs	Integrated BW = 10 kHz to 61 MHz
		223		fs	Integrated BW = 1 kHz to 61 MHz

PLL2 CHARACTERISTICS

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VCO (ON CHIP)					
Frequency Range	3600		4000	MHz	
Gain		45		MHz/V	
PLL2 FIGURE OF MERIT (FOM)		−226		dBc/Hz	
MAXIMUM PFD FREQUENCY					
Antibacklash Pulse Width					High is the initial PLL2 antibacklash pulse width setting. The user must program Register 0x0F2[4] = 1b to enable SPI control of the antibacklash pulse width to the setting defined in Register 0x0F2[3:2] and Table 47.
Minimum			259	MHz	
Low			200	MHz	
High			135	MHz	
Maximum			80	MHz	

LOGIC INPUT PINS—$\overline{PD}$, EEPROM_SEL, REF_SEL, $\overline{RESET}$, $\overline{SYNC}$

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE					
Input High	2.0			V	
Input Low			0.8	V	
INPUT LOW CURRENT		±80	±250	µA	The minus sign indicates that, due to the internal pull-up resistor, current is flowing out of the AD9523
CAPACITANCE		3		pF	
$\overline{RESET}$ TIMING					
Pulse Width Low	50			ns	
Inactive to Start of Register Programming	100			ns	
$\overline{SYNC}$ TIMING					
Pulse Width Low	1.5			ns	High speed clock is CLK input signal

STATUS OUTPUT PINS—STATUS1, STATUS0

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE					
Output High	2.94			V	
Output Low			0.4	V	

SERIAL CONTROL PORT—SPI MODE

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{CS}$ (INPUT)					$\overline{CS}$ has an internal 40 kΩ pull-up resistor
Voltage					
Input Logic 1		2.0		V	
Input Logic 0		0.8		V	
Current					
Input Logic 1		30		µA	
Input Logic 0		−110		µA	The minus sign indicates that, due to the internal pull-up resistor, current is flowing out of the AD9523
Input Capacitance		2		pF	
SCLK (INPUT) IN SPI MODE					SCLK has an internal 40 kΩ pull-down resistor in SPI mode but not in I^2C mode
Voltage					
Input Logic 1		2.0		V	
Input Logic 0		0.8		V	
Current					
Input Logic 1		240		µA	
Input Logic 0		1		µA	
Input Capacitance		2		pF	
SDIO (WHEN INPUT IS IN BIDIRECTIONAL MODE)					
Voltage					
Input Logic 1		2.0		V	
Input Logic 0		0.8		V	
Current					
Input Logic 1		1		µA	
Input Logic 0		1		µA	
Input Capacitance		2		pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDIO, SDO (OUTPUTS)					
Output Logic 1 Voltage	2.7			V	
Output Logic 0 Voltage			0.4	V	
TIMING					
Clock Rate (SCLK, $1/t_{SCLK}$)			25	MHz	
Pulse Width High, t_{HIGH}	8			ns	
Pulse Width Low, t_{LOW}	12			ns	
SDIO to SCLK Setup, t_{DS}	3.3			ns	
SCLK to SDIO Hold, t_{DH}	0			ns	
SCLK to Valid SDIO and SDO, t_{DV}			14	ns	
$\overline{CS}$ to SCLK Setup, t_S	10			ns	
$\overline{CS}$ to SCLK Setup and Hold, t_S, t_C	0			ns	
$\overline{CS}$ Minimum Pulse Width High, t_{PWH}	6			ns	

SERIAL CONTROL PORT—I²C MODE

VDD = VDD3_REF, unless otherwise noted.

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDA, SCL (WHEN INPUTTING DATA)					
Input Logic 1 Voltage	0.7 × VDD			V	
Input Logic 0 Voltage			0.3 × VDD	V	
Input Current with an Input Voltage Between 0.1 × VDD and 0.9 × VDD	−10		+10	µA	
Hysteresis of Schmitt Trigger Inputs	0.015 × VDD			V	
Pulse Width of Spikes That Must Be Suppressed by the Input Filter, t_{SPIKE}			50	ns	
SDA (WHEN OUTPUTTING DATA)					
Output Logic 0 Voltage at 3 mA Sink Current			0.4	V	
Output Fall Time from VIH_{MIN} to VIL_{MAX} with a Bus Capacitance from 10 pF to 400 pF	20 + 0.1 C_B[1]		250	ns	
TIMING					Note that all I²C timing values are referred to VIH_{MIN} (0.3 × VDD) and VIL_{MAX} levels (0.7 × VDD)
Clock Rate (SCL, f_{I2C})			400	kHz	
Bus Free Time Between a Stop and Start Condition, t_{IDLE}	1.3			µs	
Setup Time for a Repeated Start Condition, $t_{SET; STR}$	0.6			µs	
Hold Time (Repeated) Start Condition, $t_{HLD; STR}$	0.6			µs	After this period, the first clock pulse is generated
Setup Time for Stop Condition, $t_{SET; STP}$	0.6			µs	
Low Period of the SCL Clock, t_{LOW}	1.3			µs	
High Period of the SCL Clock, t_{HIGH}	0.6			µs	
SCL, SDA Rise Time, t_{RISE}	20 + 0.1 C_B[1]		300	ns	
SCL, SDA Fall Time, t_{FALL}	20 + 0.1 C_B[1]		300	ns	
Data Setup Time, $t_{SET; DAT}$	100			ns	
Data Hold Time, $t_{HLD; DAT}$	100		880	ns	This is a minor deviation from the original I²C specification of 0 ns minimum[2]
Capacitive Load for Each Bus Line, C_B[1]			400	pF	

[1] C_B is the capacitance of one bus line in picofarads (pF).
[2] According to the original I²C specification, an I²C master must also provide a minimum hold time of 300 ns for the SDA signal to bridge the undefined region of the SCL falling edge.

ABSOLUTE MAXIMUM RATINGS

Table 17.

Parameter	Rating
VDD3_PLL1, VDD3_PLL2, VDD3_REF, VDD3_OUT, LDO_VCO to GND	−0.3 V to +3.6 V
REFA, $\overline{\text{REFA}}$, $\overline{\text{REFIN}}$, REFB, $\overline{\text{REFB}}$ to GND	−0.3 V to +3.6 V
SCLK/SCL, SDIO/SDA, SDO, $\overline{\text{CS}}$ to GND	−0.3 V to +3.6 V
OUT0, $\overline{\text{OUT0}}$, OUT1, $\overline{\text{OUT1}}$, OUT2, $\overline{\text{OUT2}}$, OUT3, $\overline{\text{OUT3}}$, OUT4, $\overline{\text{OUT4}}$, OUT5, $\overline{\text{OUT5}}$, OUT6, $\overline{\text{OUT6}}$, OUT7, $\overline{\text{OUT7}}$, OUT8, $\overline{\text{OUT8}}$, OUT9, $\overline{\text{OUT9}}$, OUT10, $\overline{\text{OUT10}}$, OUT11, $\overline{\text{OUT11}}$, OUT12, $\overline{\text{OUT12}}$, OUT13, $\overline{\text{OUT13}}$ to GND	−0.3 V to +3.6 V
$\overline{\text{SYNC}}$, $\overline{\text{RESET}}$, $\overline{\text{PD}}$ to GND	−0.3 V to +3.6 V
STATUS0, STATUS1 to GND	−0.3 V to +3.6 V
SP0, SP1, EEPROM_SEL to GND	−0.3 V to +3.6 V
VDD1.8_OUT, LDO_PLL1, LDO_PLL2 to GND	2 V
Operating Temperature Range	−40°C to +85°C
Junction Temperature	115°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

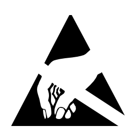
Table 18. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JC}[1, 3]	θ_{JB}[1, 4]	Ψ_{JT}[1, 2]	Unit
72-Lead LFCSP, 10 mm × 10 mm	0	21.3	1.7	12.6	0.1	°C/W
	1.0	20.1			0.2	°C/W
	2.5	18.1			0.3	°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

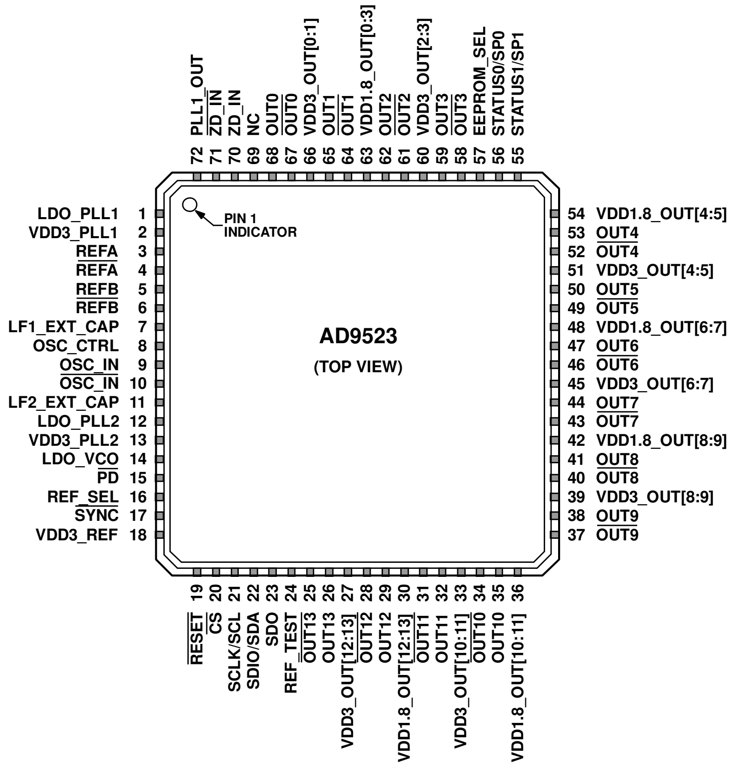
For information about power dissipation, refer to the Power Dissipation and Thermal Considerations section.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. PINS LABELED NC CAN BE ALLOWED TO FLOAT, BUT IT IS BETTER TO CONNECT THESE PINS TO GROUND. AVOID ROUTING HIGH SPEED SIGNALS THROUGH THESE PINS BECAUSE NOISE COUPLING MAY RESULT. ON EXISTING PCB DESIGNS, IT IS ACCEPTABLE TO LEAVE PIN 69 CONNECTED TO 1.8V SUPPLY.
2. THE EXPOSED PADDLE IS THE GROUND CONNECTION ON THE CHIP. IT MUST BE SOLDERED TO THE ANALOG GROUND OF THE PCB TO ENSURE PROPER FUNCTIONALITY AND HEAT DISSIPATION, NOISE, AND MECHANICAL STRENGTH BENEFITS.

08439-002

Figure 2. Pin Configuration

Table 19. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	LDO_PLL1	P/O	1.8 V Internal LDO Regulator Decoupling Pin for PLL1. Connect a 0.47 µF decoupling capacitor from this pin to ground. Note that, for best performance, the LDO bypass capacitor must be placed in close proximity to the device.
2	VDD3_PLL1	P	3.3 V Supply PLL1. Use the same supply as VCXO.
3	REFA	I	Reference Clock Input A. Along with $\overline{\text{REFA}}$, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
4	$\overline{\text{REFA}}$	I	Complementary Reference Clock Input A. Along with REFA, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3V CMOS input.
5	REFB	I	Reference Clock Input B. Along with $\overline{\text{REFB}}$, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
6	$\overline{\text{REFB}}$	I	Complementary Reference Clock Input B. Along with REFB, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
7	LF1_EXT_CAP	O	PLL1 External Loop Filter Capacitor. Connect a loop filter capacitor to this pin and to ground.
8	OSC_CTRL	O	Oscillator Control Voltage. Connect this pin to the voltage control pin of the external oscillator.
9	OSC_IN	I	PLL1 Oscillator Input. Along with $\overline{\text{OSC\_IN}}$, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
10	$\overline{\text{OSC\_IN}}$	I	Complementary PLL1 Oscillator Input. Along with OSC_IN, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
11	LF2_EXT_CAP	O	PLL2 External Loop Filter Capacitor Connection. Connect a capacitor to this pin and LDO_VCO.

Pin No.	Mnemonic	Type[1]	Description
12	LDO_PLL2	P/O	LDO Decoupling Pin for PLL2 1.8 V Internal Regulator. Connect a 0.47 μF decoupling capacitor from this pin to ground. Note that for best performance, the LDO bypass capacitor must be placed in close proximity to the device.
13	VDD3_PLL2	P	3.3 V Supply for PLL2.
14	LDO_VCO	P/O	2.5 V LDO Internal Regulator Decoupling Pin for VCO. Connect a 0.47 μF decoupling capacitor from this pin to ground. Note that, for best performance, the LDO bypass capacitor must be placed in close proximity to the device.
15	$\overline{\text{PD}}$	I	Chip Power-Down, Active Low. This pin has an internal 40 kΩ pull-up resistor.
16	REF_SEL	I	Reference Input Select. This pin has an internal 40 kΩ pull-down resistor.
17	$\overline{\text{SYNC}}$	I	Manual Synchronization. This pin initiates a manual synchronization and has an internal 40 kΩ pull-up resistor.
18	VDD3_REF	P	3.3 V Supply for Output Clock Drivers Reference.
19	$\overline{\text{RESET}}$	I	Digital Input, Active Low. Resets internal logic to default states. This pin has an internal 40 kΩ pull-up resistor.
20	$\overline{\text{CS}}$	I	Serial Control Port Chip Select, Active Low. This pin has an internal 40 kΩ pull-up resistor.
21	SCLK/SCL	I	Serial Control Port Clock Signal for SPI Mode (SCLK) or I^2C Mode (SCL). Data clock for serial programming. This pin has an internal 40 kΩ pull-down resistor in SPI mode but is high impedance in I^2C mode.
22	SDIO/SDA	I/O	Serial Control Port Bidirectional Serial Data In/Data Out for SPI Mode (SDIO) or I^2C Mode (SDA).
23	SDO	O	Serial Data Output. Use this pin to read data in 4-wire mode (high impedance in 3-wire mode). There is no internal pull-up/pull-down resistor on this pin.
24	REF_TEST	I	Test Input to PLL1 Phase Detector.
25	$\overline{\text{OUT13}}$	O	Complementary Square Wave Clocking Output 13. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
26	OUT13	O	Square Wave Clocking Output 13. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
27	VDD3_OUT[12:13]	P	3.3 V Supply for Output 12 and Output 13 Clock Drivers.
28	$\overline{\text{OUT12}}$	O	Complementary Square Wave Clocking Output 12. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
29	OUT12	O	Square Wave Clocking Output 12. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
30	VDD1.8_OUT[12:13]	P	1.8 V Supply for Output 12 and Output 13 Clock Dividers.
31	$\overline{\text{OUT11}}$	O	Complementary Square Wave Clocking Output 11. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
32	OUT11	O	Square Wave Clocking Output 11. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
33	VDD3_OUT[10:11]	P	3.3 V Supply for Output 10 and Output 11 Clock Drivers.
34	$\overline{\text{OUT10}}$	O	Complementary Square Wave Clocking Output 10. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
35	OUT10	O	Square Wave Clocking Output 10. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
36	VDD1.8_OUT[10:11]	P	1.8 V Supply for Output 10 and Output 11 Clock Dividers.
37	$\overline{\text{OUT9}}$	O	Complementary Square Wave Clocking Output 9. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
38	OUT9	O	Square Wave Clocking Output 9. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
39	VDD3_OUT[8:9]	P	3.3 V Supply for Output 8 and Output 9 Clock Drivers.
40	$\overline{\text{OUT8}}$	O	Complementary Square Wave Clocking Output 8. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
41	OUT8	O	Square Wave Clocking Output 8. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
42	VDD1.8_OUT[8:9]	P	1.8 V Supply for Output 8 and Output 9 Clock Dividers.
43	$\overline{\text{OUT7}}$	O	Complementary Square Wave Clocking Output 7. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
44	OUT7	O	Square Wave Clocking Output 7. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
45	VDD3_OUT[6:7]	P	3.3 V Supply for Output 6 and Supply Output 7 Clock Drivers.

Pin No.	Mnemonic	Type[1]	Description
46	$\overline{\text{OUT6}}$	O	Complementary Square Wave Clocking Output 6. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
47	OUT6	O	Square Wave Clocking Output 6. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
48	VDD1.8_OUT[6:7]	P	1.8 V Supply for Output 6 and Output 7 Clock Dividers.
49	$\overline{\text{OUT5}}$	O	Complementary Square Wave Clocking Output 5. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
50	OUT5	O	Square Wave Clocking Output 5. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
51	VDD3_OUT[4:5]	P	3.3 V Supply for Output 4 and Output 5 Clock Drivers.
52	$\overline{\text{OUT4}}$	O	Complementary Square Wave Clocking Output 4. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
53	OUT4	O	Square Wave Clocking Output 4. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
54	VDD1.8_OUT[4:5]	P	1.8 V Supply for Output 4 and Output 5 Clock Dividers.
55	STATUS1/SP1	I/O	Lock Detect and Other Status Signals (STATUS1)/I^2C Address (SP1). This pin has an internal 40 kΩ pull-down resistor.
56	STATUS0/SP0	I/O	Lock Detect and Other Status Signals (STATUS0)/I^2C Address (SP0). This pin has an internal 40 kΩ pull-down resistor.
57	EEPROM_SEL	I	EEPROM Select. Setting this pin high selects the register values stored in the internal EEPROM to be loaded at reset and/or power-up. Setting this pin low causes the AD9523 to load the hard-coded default register values at power-up/reset. This pin has an internal 40 kΩ pull-down resistor.
58	$\overline{\text{OUT3}}$	O	Complementary Square Wave Clocking Output 3. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
59	OUT3	O	Square Wave Clocking Output 3. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
60	VDD3_OUT[2:3]	P	3.3 V Supply for Output 2 and Output 3 Clock Drivers.
61	$\overline{\text{OUT2}}$	O	Complementary Square Wave Clocking Output 2. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
62	OUT2	O	Square Wave Clocking Output 2. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
63	VDD1.8_OUT[0:3]	P	1.8 V Supply for Output 0, Output 1, Output 2, and Output 3 Clock Dividers.
64	$\overline{\text{OUT1}}$	O	Complementary Square Wave Clocking Output 1. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
65	OUT1	O	Square Wave Clocking Output 1. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
66	VDD3_OUT[0:1]	P	3.3 V Supply for Output 0 and Output 1 Clock Drivers.
67	$\overline{\text{OUT0}}$	O	Complementary Square Wave Clocking Output 0. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
68	OUT0	O	Square Wave Clocking Output 0. This pin can be configured as one side of a differential LVPECL/LVDS/HSTL output or as a single-ended CMOS output.
69	NC	P	This pin is not connected internally (see Figure 2).
70	ZD_IN	I	External Zero Delay Clock Input. Along with $\overline{\text{ZD\_IN}}$, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
71	$\overline{\text{ZD\_IN}}$	I	Complementary External Zero Delay Clock Input. Along with ZD_IN, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
72	PLL1_OUT	O	Single-Ended CMOS Output from PLL1. This pin has settings for weak and strong in Register 0x1BA[4] (see Table 52).
EP	EP, GND	GND	Exposed Paddle. The exposed paddle is the ground connection on the chip. It must be soldered to the analog ground of the PCB to ensure proper functionality and heat dissipation, noise, and mechanical strength benefits.

[1] P is power, I is input, O is output, I/O is input/output, P/O is power/output, and GND is ground.

TYPICAL PERFORMANCE CHARACTERISTICS

f_{VCXO} = 122.88 MHz, REFA differential at 30.72 MHz, f_{VCO} = 3686.4 MHz, and doubler is off, unless otherwise noted.

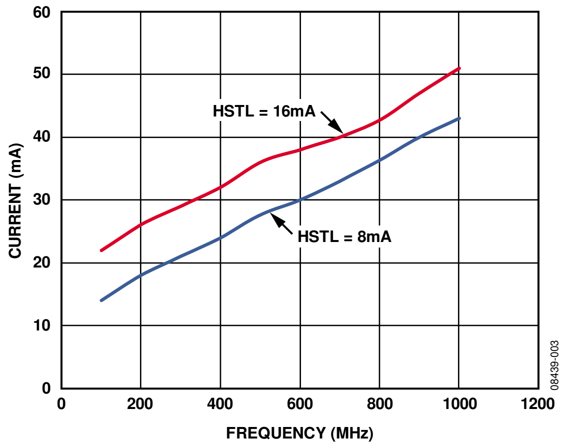


Figure 3. VDD3_OUT[x:y] Current (Typical) vs. Frequency; HSTL Mode, 16 mA and 8 mA

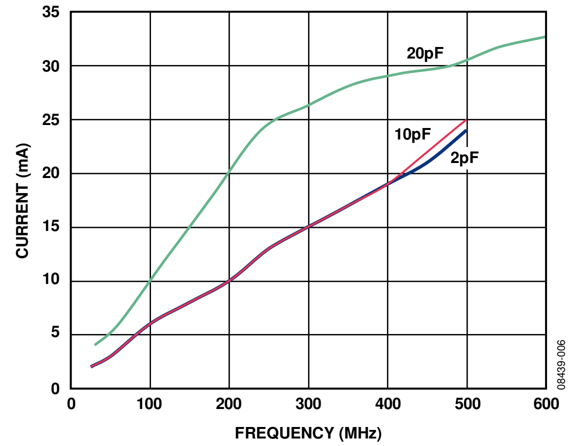


Figure 6. VDD3_OUT[x:y] Current (Typical) vs. Frequency; CMOS Mode, 20 pF, 10 pF, and 2 pF Load

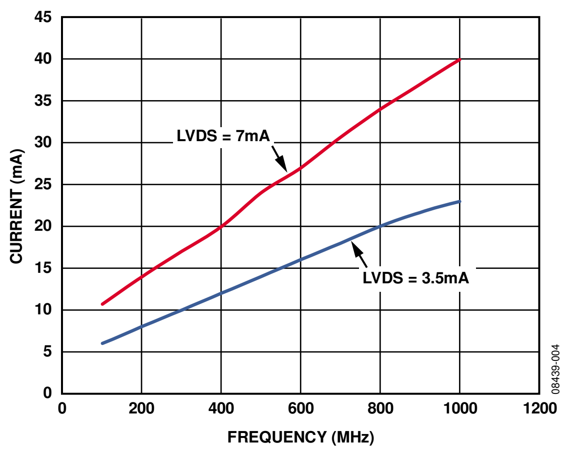


Figure 4. VDD3_OUT[x:y] Current (Typical) vs. Frequency; LVDS Mode, 7 mA and 3.5 mA

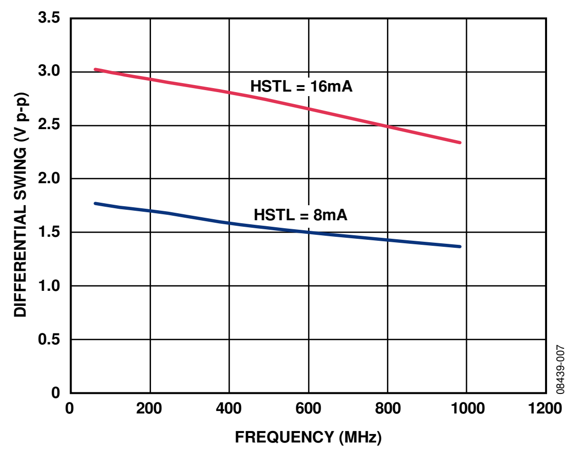


Figure 7. Differential Voltage Swing vs. Frequency; HSTL Mode, 16 mA and 8 mA

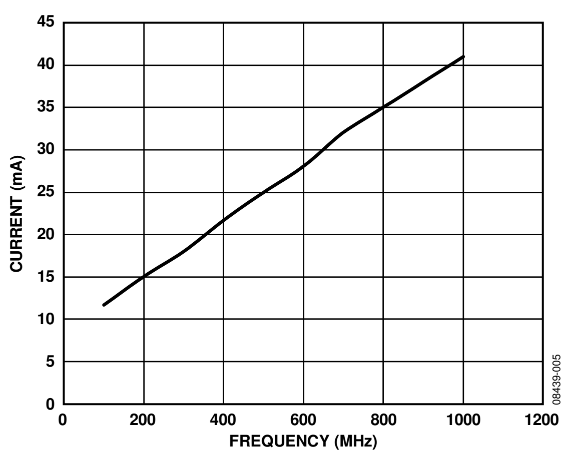


Figure 5. VDD3_OUT[x:y] Current (Typical) vs. Frequency, LVPECL Mode

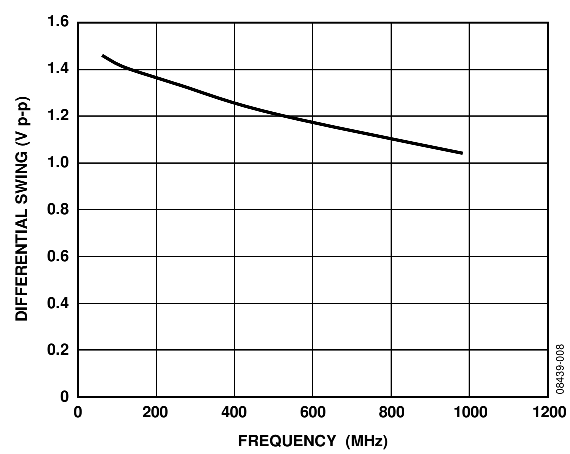


Figure 8. Differential Voltage Swing vs. Frequency, LVPECL Mode

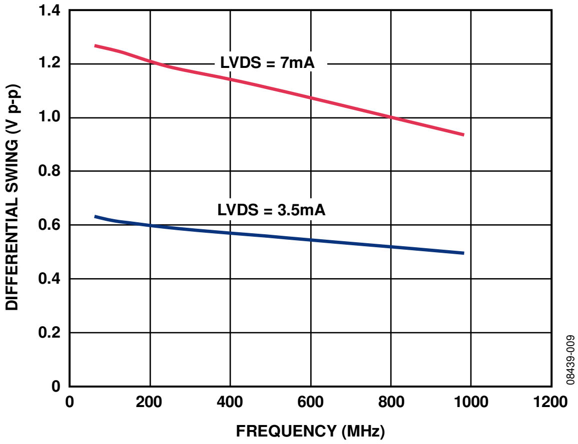


Figure 9. Differential Voltage Swing vs. Frequency; LVDS Mode, 7 mA and 3.5 mA

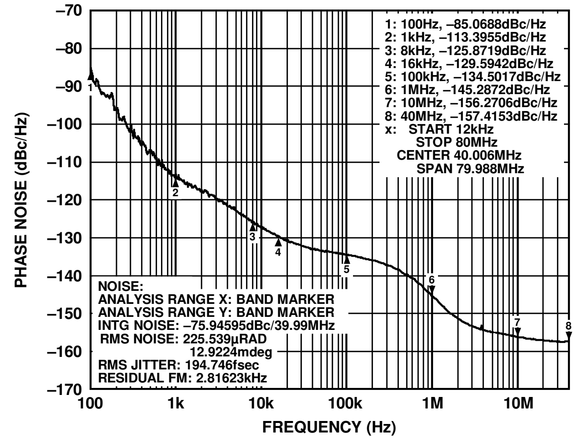


Figure 12. Phase Noise, Output = 184.32 MHz (VCXO = 122.88 MHz, Crystek VCXO CVHD-950)

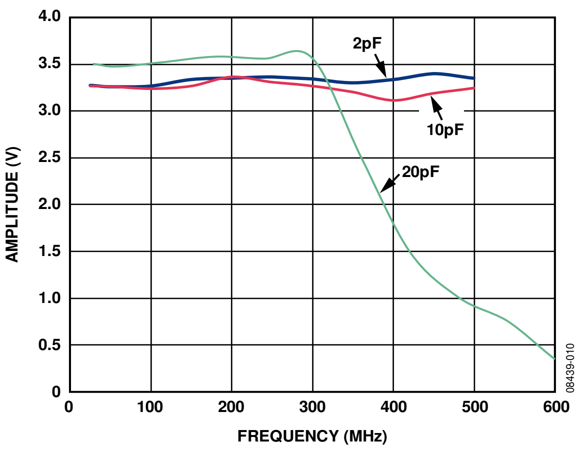


Figure 10. Amplitude vs. Frequency and Capacitive Load; CMOS Mode, 2 pF, 10 pF, and 20 pF

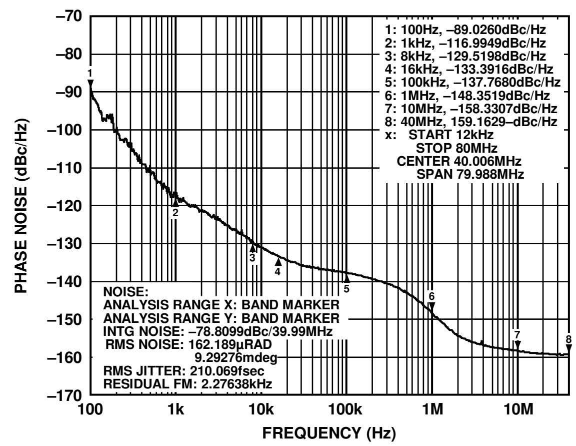


Figure 13. Phase Noise, Output = 122.88 MHz (VCXO = 122.88 MHz, Crystek VCXO CVHD-950; Doubler Is Off)

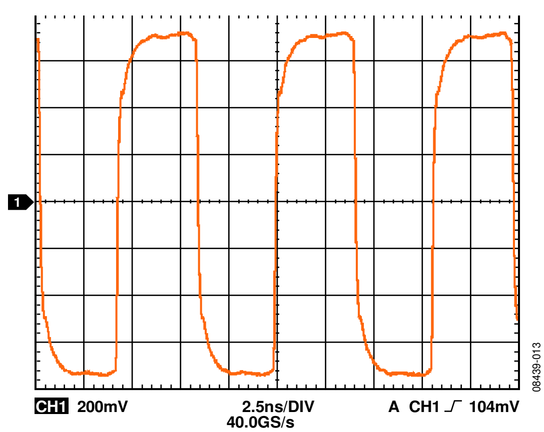


Figure 11. Output Waveform (Differential), LVPECL at 122.88 MHz

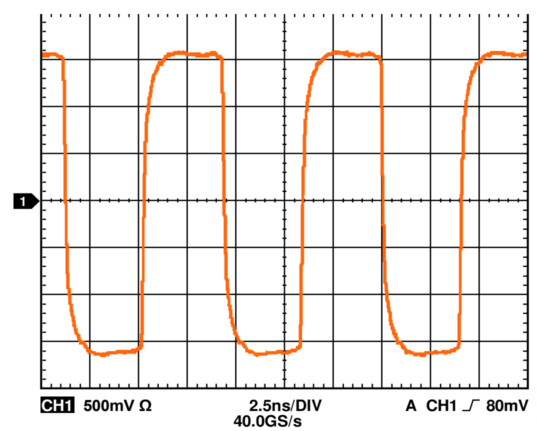


Figure 14. Output Waveform (Differential), HSTL at 16 mA, 122.88 MHz

INPUT/OUTPUT TERMINATION RECOMMENDATIONS

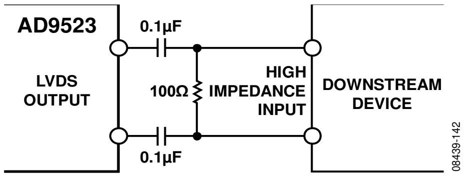


Figure 15. AC-Coupled LVDS Output Driver

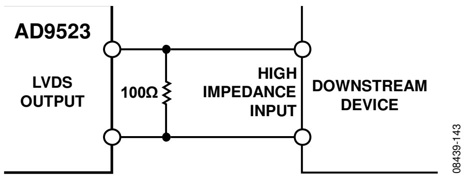


Figure 16. DC-Coupled LVDS Output Driver

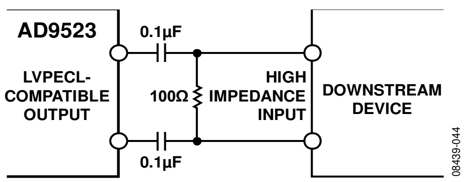


Figure 17. AC-Coupled LVPECL Output Driver

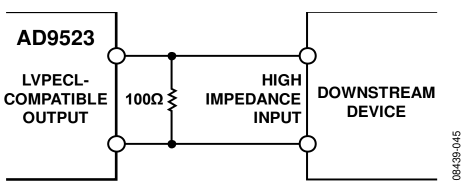


Figure 18. DC-Coupled LVPECL Output Driver

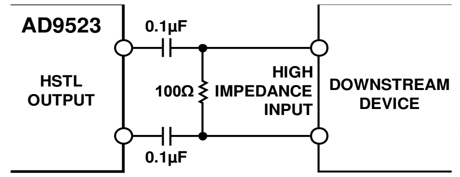


Figure 19. AC-Coupled HSTL Output Driver

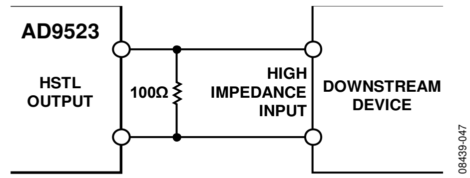


Figure 20. DC-Coupled HSTL Output Driver

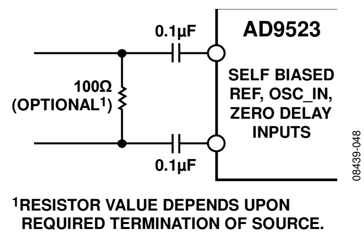


Figure 21. REF, OSC_IN, and Zero Delay Input Differential Mode

TERMINOLOGY

Phase Jitter and Phase Noise

An ideal sine wave can be thought of as having a continuous and even progression of phase with time from 0° to 360° for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time. This phenomenon is called phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, which is characterized statistically as being Gaussian (normal) in distribution.

This phase jitter leads to a spreading out of the energy of the sine wave in the frequency domain, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in decibels) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

It is meaningful to integrate the total power contained within some interval of offset frequencies (for example, 10 kHz to 10 MHz). This is called the integrated phase noise over that frequency offset interval and can be readily related to the time jitter due to the phase noise within that offset frequency interval.

Phase noise has a detrimental effect on the performance of ADCs, DACs, and RF mixers. It lowers the achievable dynamic range of the converters and mixers, although they are affected in somewhat different ways.

Time Jitter

Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings varies. In a square wave, the time jitter is a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in seconds root mean square (rms) or 1 sigma (Σ) of the Gaussian distribution.

Time jitter that occurs on a sampling clock for a DAC or an ADC decreases the signal-to-noise ratio (SNR) and dynamic range of the converter. A sampling clock with the lowest possible jitter provides the highest performance from a given converter.

Additive Phase Noise

Additive phase noise is the amount of phase noise that can be attributed to the device or subsystem being measured. The phase noise of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device impacts the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contributes its own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise. When there are multiple contributors to phase noise, the total is the square root of the sum of squares of the individual contributors.

Additive Time Jitter

Additive time jitter is the amount of time jitter that can be attributed to the device or subsystem being measured. The time jitter of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device impacts the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contributes its own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.

THEORY OF OPERATION

DETAILED BLOCK DIAGRAM

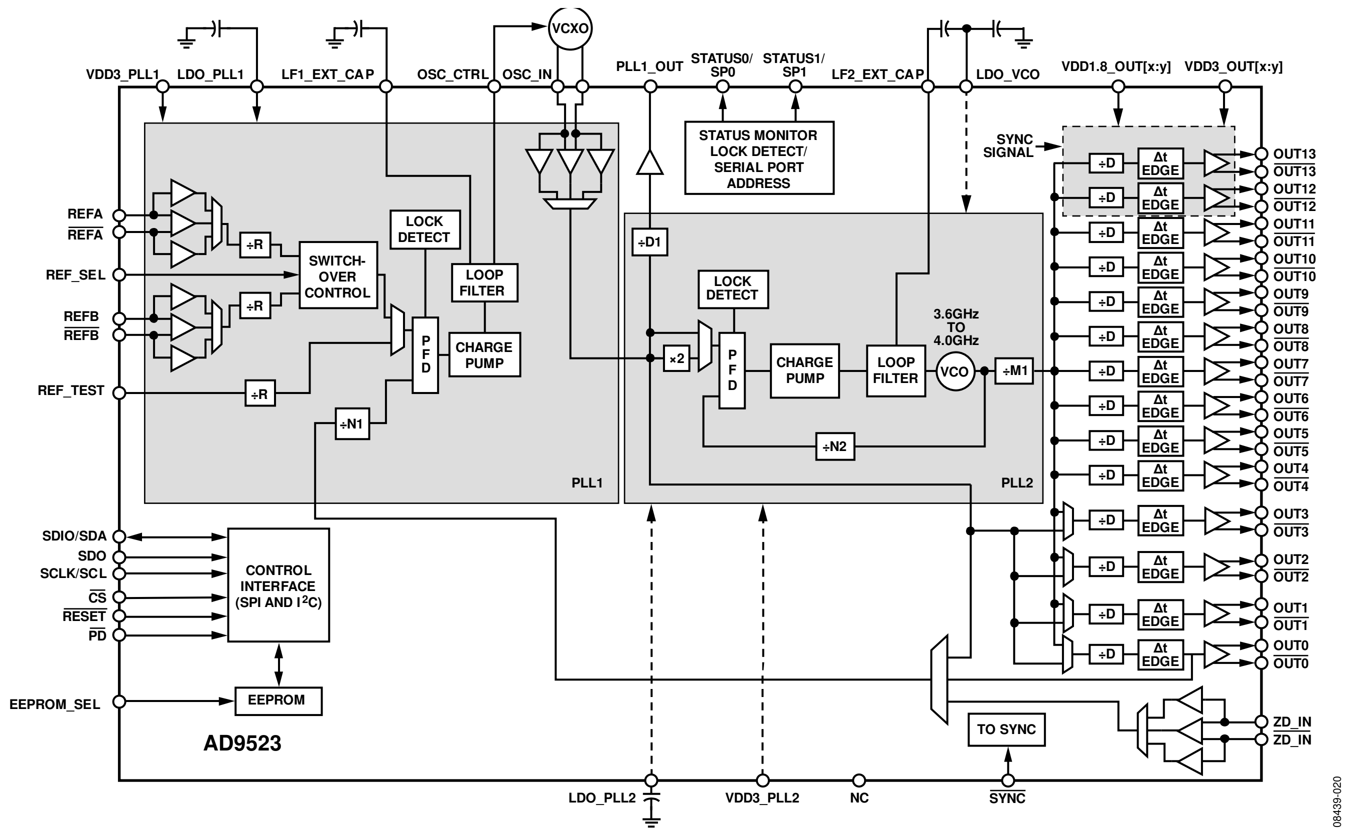


Figure 22. Top Level Diagram

OVERVIEW

The AD9523 is a clock generator that employs integer-N-based phase-locked loops (PLL). The device architecture consists of two cascaded PLL stages. The first stage, PLL1, consists of an integer division PLL that uses an external voltage-controlled crystal oscillator (VCXO) of up to 250 MHz. PLL1 has a narrow-loop bandwidth that provides initial jitter cleanup of the input reference signal. The second stage, PLL2, is a frequency multiplying PLL that translates the first stage output frequency to a range of 3.6 GHz to 4.0 GHz. PLL2 incorporates an integer-based feedback divider that enables integer frequency multiplication. Programmable integer dividers (1 to 1024) follow PLL2, establishing a final output frequency of 1 GHz or less.

The AD9523 includes reference signal processing blocks that enable a smooth switching transition between two reference inputs. This circuitry automatically detects the presence of the reference input signals. If only one input is present, the device uses it as the active reference. If both are present, one becomes the active reference and the other becomes the backup reference. If the active reference fails, the circuitry automatically switches to the backup reference (if available), making it the new active reference. A register setting determines what action to take if the failed reference is once again available: either stay on Reference B or revert to Reference A. If neither reference can be used, the AD9523 supports a holdover mode. A reference select pin (REF_SEL, Pin 16) is available to manually select which input reference is active (see Table 43). The accuracy of the holdover is dependent on the external VCXO frequency stability at half supply voltage.

Any of the divider settings are programmable via the serial programming port, enabling a wide range of input/output frequency ratios under program control. The dividers also include a programmable delay to adjust the timing of the output signals, if required.

The 14 outputs are compatible with LVPECL, LVDS, HSTL, and 1.8 V CMOS logic levels (see the Input/Output Termination Recommendations section). All differential output logic settings require a single 100 Ω differential termination.

The loop filters of each PLL are integrated and programmable. Only a single external capacitor for each of the two PLL loop filters is required.

The AD9523 operates over the extended industrial temperature range of −40°C to +85°C.

COMPONENT BLOCKS—INPUT PLL (PLL1)

PLL1 General Description

Fundamentally, the input PLL (referred to as PLL1) consists of a phase/frequency detector (PFD), charge pump, passive loop filter, and an external VCXO operating in a closed loop.

PLL1 has the flexibility to operate with a loop bandwidth of approximately 10 Hz to 100 Hz. This relatively narrow loop bandwidth gives the AD9523 the ability to suppress jitter that appears on the input references (REFA and REFB). The output of PLL1 then becomes a low jitter phase-locked version of the reference input system clock.

PLL1 Reference Clock Inputs

The AD9523 features two separate PLL1 differential reference clock inputs, REFA and REFB. These inputs can be configured to operate in full differential mode or single-ended CMOS mode.

In differential mode, these pins are internally self biased. If REFA or REFB is driven single-ended in differential mode, the unused side ($\overline{REFA}$, $\overline{REFB}$) should be decoupled via a suitable capacitor to a quiet ground. Figure 21 shows the recommended differential input termination to REFA or REFB. It is possible to dc couple to these inputs, but the dc operation point should be set as specified in the Specifications tables.

To operate either the REFA or the REFB inputs in 3.3 V CMOS mode, set Register 0x01A[6:5] and Register 0x01B[1:0] (see Table 41 and Table 40). The single-ended inputs can be driven by either a dc-coupled CMOS level signal or an ac-coupled sine wave or square wave.

The differential reference input receiver is powered down when the differential reference input is not selected, or when the PLL is powered down. The single-ended buffers power-down when the PLL is powered down, when their respective individual power-down registers are set, or when the differential receiver is selected.

The REFB R divider uses the same value as the REFA R divider unless Register 0x01C[7], the enable REFB R divider independent division control bit, is programmed as shown in Table 43.

OSC_IN Input

The OSC_IN receiver connects to the PLL1 feedback divider and to the PLL2 PFD through an optional doubler. This input receiver is identical to the PLL1 REFA and REFB receivers. Control bits for this receiver are located in Register 0x01A[1:0]. Figure 21 shows the recommended differential input termination to the OSC_IN receiver.

The OSC_IN receiver is powered down when the PLL1 power-down bit is set (Register 0x233[2] = 1b). When using the AD9523 in a mode of operation that bypasses PLL1, the PLL1 power-down bit must be disabled (Register 0x233[2] = 0b).

PLL1 Loop Filter

The PLL1 loop filter requires the connection of an external capacitor from LF1_EXT_CAP (Pin 7) to ground. The value of the external capacitor depends on the use of an external VCXO, as well as such configuration parameters as input clock rate and desired bandwidth. Normally, a 0.3 μF capacitor allows the loop bandwidth to range from 10 Hz to 100 Hz and ensures loop stability over the intended operating parameters of the device (see Table 44 for R_{ZERO} values). The operating loop bandwidth (LBW) of PLL1 can be used as a metric to estimate the time required for the PLL to phase lock. In general, PLL1 is phase locked within 10 loop bandwidth time constants, τ_{LBW}, where $\tau_{LBW} = 1/LBW$. Therefore, PLL_TO (see Figure 44) equals $10 \times \tau_{LBW}$.

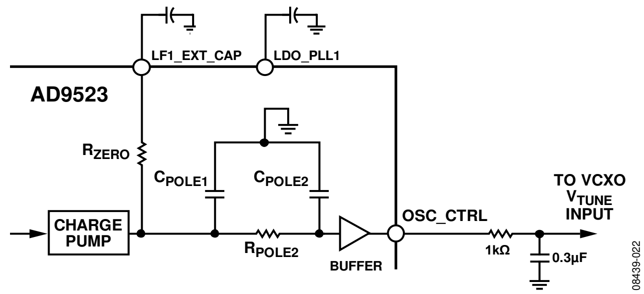


Figure 23. PLL1 Loop Filter

Table 20. PLL1 Loop Filter Programmable Values

R_{ZERO} (kΩ)	C_{POLE1} (nF)	R_{POLE2} (kΩ)	C_{POLE2} (nF)	LF1_EXT_CAP[1] (μF)
883	1.5 fixed	165 fixed	0.337 fixed	0.3
677				
341				
135				
10				
External				

[1] External loop filter capacitor.

An external RC low-pass filter should be used at the OSC_CTRL output. The values shown in Figure 23 add an additional low-pass pole at ~530 Hz. This RC network filters the noise associated with the OSC_CTRL buffer to achieve the best noise performance at the 1 kHz offset region.

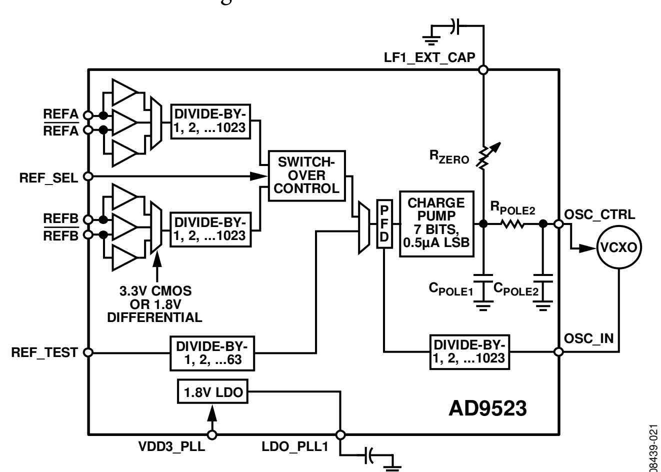


Figure 24. Input PLL (PLL1) Block Diagram

PLL1 Input Dividers

Each reference input feeds a dedicated reference divider block. The input dividers provide division of the reference frequency in integer steps from 1 to 1023. They provide the bulk of the frequency prescaling that is necessary to reduce the reference frequency to accommodate the bandwidth that is typically desired for PLL1.

PLL1 Reference Switchover

The reference monitor verifies the presence/absence of the prescaled REFA and REFB signals (that is, after division by the input dividers). The status of the reference monitor guides the activity of the switchover control logic. The AD9523 supports automatic and manual PLL reference clock switching between REFA (the REFA and $\overline{\text{REFA}}$ pins) and REFB (the REFB and $\overline{\text{REFB}}$ pins). This feature supports networking and infrastructure applications that require redundant references.

There are several configurable modes of reference switchover. Manual reference switchover is achieved either via a programming register setting or by using the REF_SEL pin. Automatic reference switchover occurs when REFA disappears and there is a reference on REFB.

Automatic reference switchover can be set to work as follows:

- Nonrevertive: stay on REFB. Switch from REFA to REFB when REFA disappears, but do not switch back to REFA if it reappears. If REFB disappears, then go back to REFA.
- Revert to REFA: switch from REFA to REFB when REFA disappears. Return to REFA from REFB when REFA returns.

See Table 43 for the PLL1 miscellaneous control register bit settings.

PLL1 Holdover

In the absence of both input references, the device enters holdover mode. Holdover is a secondary function that is provided by PLL1. Because PLL1 has an external VCXO available as a frequency source, it continues to operate in the absence of the input reference signals. When the device switches to holdover, the charge pump tristates. The device continues operating in this mode until a reference signal becomes available. Then the device exits holdover mode, and PLL1 resynchronizes with the active reference. In addition to tristate, the charge pump can be forced to $V_{CC}/2$ during holdover (see Table 43, Register 0x01C[6]).

COMPONENT BLOCKS—OUTPUT PLL (PLL2)

PLL2 General Description

The output PLL (referred to as PLL2) consists of an optional input reference doubler, phase/frequency detector (PFD), a partially integrated analog loop filter (see Figure 25), an integrated voltage controlled oscillator (VCO), and a feedback divider. The VCO produces a nominal 3.8 GHz signal with an output divider that is capable of division ratios of 4 to 11.

The PFD of the output PLL drives a charge pump that increases, decreases, or holds constant the charge stored on the loop filter capacitors (both internal and external). The stored charge results in a voltage that sets the output frequency of the VCO. The feedback loop of the PLL causes the VCO control voltage to vary in a way that phase locks the PFD input signals. The gain of PLL2 is proportional to the current delivered by the charge pump. The loop filter bandwidth is chosen to reduce noise contributions from PLL sources that could degrade phase noise requirements.

The output PLL has a VCO with multiple bands spanning a range of 3.6 GHz to 4.0 GHz. However, the actual operating frequency within a particular band depends on the control voltage that appears on the loop filter capacitor. The control voltage causes the VCO output frequency to vary linearly within the selected band. This frequency variability allows the control loop of the output PLL to synchronize the VCO output signal with the reference signal applied to the PFD. Typically, the device automatically selects the appropriate band as part of its calibration process (invoked via the VCO control register at Address 0x0F3). The VCO is designed to operate over temperature extremes including when the VCO is calibrated at one temperature extreme and operated within another.

Input 2× Frequency Multiplier

The 2× frequency multiplier provides the option to double the frequency at the PLL2 input. This allows the user to take advantage of a higher frequency at the input to the PLL (PFD) and, thus, allows for reduced in-band phase noise and greater separation between the frequency generated by the PLL and the modulation spur associated with PFD. However, increased reference spur separation results in harmonic spurs introduced by the frequency multiplier that increase as the duty cycle deviates from 50% at the OSC_IN inputs. Therefore, beneficial use of the frequency multiplier is application-specific. Typically, a VCXO with proper interfacing has a duty cycle that is approximately 50% at the OSC_IN inputs. Note that the maximum output frequency of the 2× frequency multipliers must not exceed the maximum PFD rate that is specified in Table 12.

PLL2 Feedback Divider

PLL2 has a feedback divider (N divider) that enables it to provide integer frequency up-conversion. The PLL2 N divider is a combination of a prescaler (P) and two counters, A and B. The total divider value is

$$N = (P \times B) + A$$

where $P = 4$.

The feedback divider is a dual modulus prescaler architecture, with a nonprogrammable P that is equal to 4. The value of the B counter can be from 4 to 63, and the value of the A counter can be from 0 to 3. However, due to the architecture of the divider, there are constraints, as listed in Table 46.

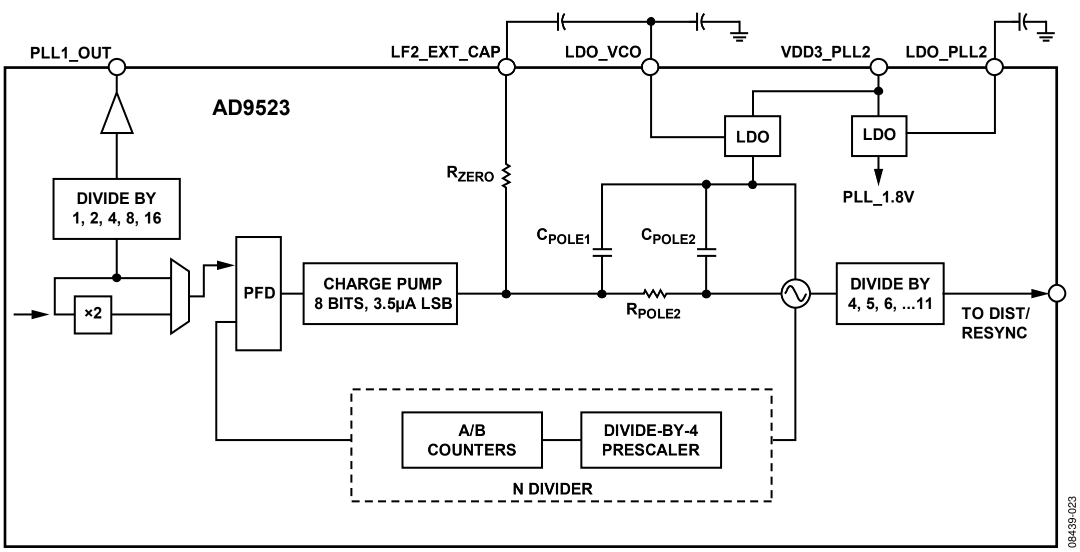


Figure 25. Output PLL (PLL2) Block Diagram

PLL2 Loop Filter

The PLL2 loop filter requires the connection of an external capacitor from LF2_EXT_CAP (Pin 11) to LDO_VCO (Pin 14), as illustrated in Figure 25. The value of the external capacitor depends on the operating mode and the desired phase noise performance. For example, a loop bandwidth of approximately 500 kHz produces the lowest integrated jitter. A lower bandwidth produces lower phase noise at 1 MHz but increases the total integrated jitter.

Table 21. PLL2 Loop Filter Programmable Values

R_{ZERO} (Ω)	C_{POLE1} (pF)	R_{POLE2} (Ω)	C_{POLE2} (pF)	LF2_EXT_CAP[1] (pF)
3250	48	900	Fixed at 16	Typical at 1000
3000	40	450		
2750	32	300		
2500	24	225		
2250	16			
2100	8			
2000	0			
1850				

[1] External loop filter capacitor.

VCO Divider

The VCO divider provides frequency division between the internal VCO and the clock distribution. The VCO divider can be set to divide by 4, 5, 6, 7, 8, 9, 10, or 11.

VCO and VCO Calibration

The AD9523 on-chip VCO must be manually calibrated to ensure proper operation over process and temperature. A VCO calibration is accomplished by transitioning the calibrate VCO bit (Register 0x0F3[1]) from 0 to 1 (this bit is not self clearing). The setting can be performed as part of the initial setup before executing the IO_UPDATE bit (Register 0x234[1] = 1b). A readback bit, VCO calibration in progress (Register 0x22D[0]), indicates when a VCO calibration is in progress by returning a logic true (Register 0x22D[1] = 1b). If the EEPROM is in use, setting the calibrate VCO bit to 1 before saving the register settings to the EEPROM ensures that the VCO calibrates automatically after the EEPROM has loaded. After calibration, it is recommended to initiate a distribution sync (see the Clock Distribution Synchronization section).

Note that the calibrate VCO bit defaults to 0. This bit must change from 0 to 1 to initiate a calibration sequence. Therefore, any subsequent calibrations require the following sequence:

1. Register 0x0F3[1] = 0b (calibrate VCO bit)
2. Register 0x234[0] = 1b (IO_UPDATE bit)
3. Register 0x0F3[1] = 1b (calibrate VCO bit)
4. Register 0x234[0] =1b (IO_UPDATE bit)

VCO calibration is controlled by a calibration controller that runs off the OSC_IN input clock. The calibration requires that PLL2 be set up properly to lock the PLL2 loop and that the OSC_IN clock be present.

During power-up or reset, the distribution section is automatically held in sync until the first VCO calibration is finished. Therefore, no outputs can occur until VCO calibration is complete and PLL2 is locked. This default functionality can be overwritten using Register 0x0F3[4].

Initiate a VCO calibration under the following conditions:

- After changing any of the PLL2 B counter and A counter settings or after a change in the PLL2 reference clock frequency. This means that a VCO calibration should be initiated any time that a PLL2 register or reference clock changes such that a different VCO frequency is the result.
- Whenever system calibration is desired. The VCO is designed to operate properly over extremes of temperature even when it is first calibrated at the opposite extreme. However, a VCO calibration can be initiated at any time, if desired.

CLOCK DISTRIBUTION

The clock distribution block provides an integrated solution for generating multiple clock outputs based on frequency dividing the PLL2 VCO divider output. The distribution output consists of 14 channels (OUT0 to OUT13). Each of the output channels has a dedicated divider and output driver, as shown in Figure 27. The AD9523 also has the capability to route the VCXO output to four of the outputs (OUT0 to OUT3).

Clock Dividers

The output clock distribution dividers are referred to as D0 to D13, corresponding to output channels OUT0 through OUT13, respectively. Each divider is programmable with 10 bits of division depth that is equal to 1 to 1024. Dividers have duty cycle correction to always give a 50% duty cycle, even for odd divides.

Output Power-Down

Each of the output channels offers independent control of the power-down functionality via the Channel 0 to Channel 13 control registers (see Table 51). Each output channel has a dedicated power-down bit for powering down the output driver. However, if all 14 outputs are powered down, the entire distribution output enters a deep sleep mode. Although each channel has a channel power-down control signal, it may sometimes be desirable to power down an output driver while maintaining the divider's synchronization with the other channel dividers. This is accomplished by placing the output in tristate mode (this works in CMOS mode, as well).

Multimode Output Drivers

The user has independent control of the operating mode of each of the fourteen output channels via the Channel 0 to Channel 13 control registers (see Table 51). The operating mode control includes the following:

- Logic family and pin functionality
- Output drive strength
- Output polarity

The four least significant bits (LSBs) of each of the 14 Channel 0 to Channel 13 control registers comprise the driver mode bits. The mode value selects the desired logic family and pin functionality of an output channel, as listed in Table 51. This driver design allows a common 100 Ω external resistor for all the different driver modes of operation that are illustrated in Figure 26.

If the output channel is ac-coupled to the circuit to be clocked, changing the mode varies the voltage swing to determine sensitivity to the drive level. For example, in LVDS mode, a current of 3.5 mA causes a 350 mV peak voltage. Likewise, in LVPECL mode, a current of 8 mA causes an 800 mV peak voltage at the 100 Ω load resistor. Using any termination other than those specified in the Input/Output Termination Recommendations section may results in damage or decrease end of life performance.

In addition to the four mode bits, each of the 14 Channel 0 to Channel 13 control registers includes the following control bits:

- Invert divider output. Enables the user to choose between normal polarity and inverted polarity. Normal polarity is the default state. Inverted polarity reverses the representation of Logic 0 and Logic 1, regardless of the logic family.
- Ignore sync. Makes the divider ignore the SYNC signal from any source.
- Power down channel. Powers down the entire channel.
- Lower power mode.
- Driver mode.
- Channel divider.
- Divider phase.

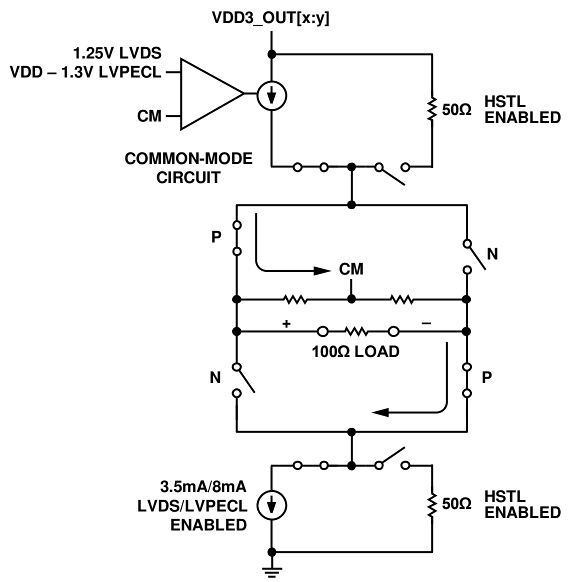


Figure 26. Multimode Driver

Clock Distribution Synchronization

A block diagram of the clock distribution synchronization functionality is shown in Figure 27. The synchronization sequence begins with the primary synchronization signal, which ultimately results in delivery of a synchronization strobe to the clock distribution logic.

As indicated, the primary synchronization signal originates from one of the following sources:

- Direct synchronization source via the sync dividers bit (see Register 0x232[0] in Table 55)
- Device pin, SYNC (Pin 17)

An automatic synchronization of the divider is initiated the first time that PLL2 locks after a power-up or reset event. Subsequent lock/unlock events do not initiate a resynchronization of the distribution dividers unless they are preceded by a power-down or reset of the part. Both sources of the primary synchronization signal are logic OR'd; therefore, any one of them can synchronize the clock distribution output at any time.