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Low Jitter Clock Generator with Eight LVPECL Outputs

Data Sheet

AD9525

FEATURES

- Integrated ultralow noise synthesizer
- 8 differential 3.6 GHz LVPECL outputs and 1 LVPECL SYNC output or 2 CMOS SYNC outputs
- 2 differential reference inputs and 1 single-ended reference input

APPLICATIONS

- LTE and multicarrier GSM base stations
- Clocking high speed ADCs, DACs
- ATE and high performance instrumentation
- 40/100 Gb/sec OTN line side clocking
- Cable/DOCSIS CMTS clocking
- Test and measurement

FUNCTIONAL BLOCK DIAGRAM

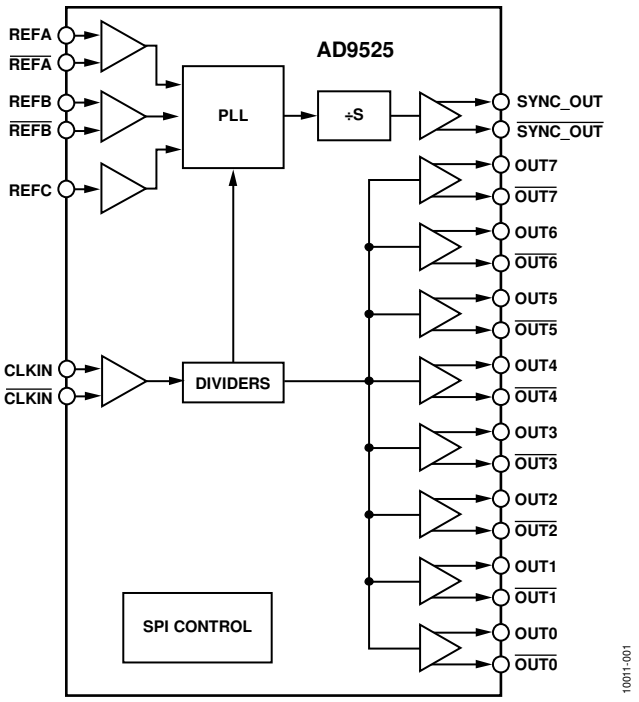

Figure 1.

GENERAL DESCRIPTION

The AD9525 is designed to support converter clock requirements for long-term evolution (LTE) and multicarrier GSM base station designs.

The AD9525 provides a low power, multioutput, clock distribution function with low jitter performance, along with an on-chip PLL that can be used with an external VCO or VCXO. The VCO input and eight LVPECL outputs can operate up to a frequency of 3.6 GHz. All outputs share a common divider that can provide a division of 1 to 6.

The AD9525 offers a dedicated output that can be used to provide a programmable signal for resetting or synchronizing a data converter. The output signal is activated by a SPI write.

The AD9525 is available in a 48-lead LFCSP and can be operated from a single 3.3 V supply. The external VCXO or VCO can have an operating voltage of up to 5.5 V.

The AD9525 operates over the extended industrial temperature range of −40°C to +85°C.

Rev. A

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COMPARABLE PARTS

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EVALUATION KITS

- AD9525 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9525: Low Jitter Clock Generator with Eight LVPECL Outputs Data Sheet

TOOLS AND SIMULATIONS

- ADIsimCLK Design and Evaluation Software
- AD9525 IBIS Models

REFERENCE MATERIALS

Press

- RF Clock IC Achieves Industry's Best Jitter Performance and Fastest Output Speed to Meet Demands of High-Speed Data Converters

Product Selection Guide

- RF Source Booklet

Technical Articles

- Clocking Wideband GSPS JESD204B ADCs

DESIGN RESOURCES

- AD9525 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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Changes to Register 0x01A, Table 28 ... 31
Change to Register 0x000, Bit 6, Table 28 ... 33
Changes to Table 35 ... 38
Changes to Table 38 ... 40

10/12—Revision 0: Initial Version

SPECIFICATIONS

Typical is given for VDD3 = 3.3 V ± 5%; VDD3 ≤ VDD_CP ≤ 5.25 V; T_A = 25°C; OUT_RSET resistor = 4.12 kΩ; CP_RSET resistor (CPRSET) = 5.1 kΩ, unless otherwise noted. Minimum and maximum values are given over full VDD3 and T_A (−40°C to +85°C) variation as listed in Table 1. REFA at 122.88 MHz, CLKIN frequency = 2949.12 MHz.

CONDITIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
VDD3		3.3		V	3.3 V ± 5%
VDD_CP	VDD3		5.25	V	Nominally 3.3 V to 5.0 V ± 5%
OUT_RSET PIN RESISTOR		4.12		kΩ	Sets internal biasing currents; connect to ground
CP_RSET PIN RESISTOR (CPRSET RESISTOR)		5.1		kΩ	Sets internal CP current range, nominally 4.8 mA (CP_LSB = 600 µA); actual current calculated by CP_LSB = 3.06/CPRSET, connect to ground; CPRSET range = 2.7 kΩ to10 kΩ
TEMPERATURE RANGE, T_A	−40	+25	+85	°C	

SUPPLY CURRENT

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT FOR VDD3 and VDD_CP PINS					f_{CLK} = 2949.12 MHz; REFA and REFB enabled at 122.88 MHz; R dividers = 2; M divider = 2; PFD = 61.44 MHz; eight LVPECL outputs at 1474.56 MHz; LVPECL 780 mV mode
VDD3 (Pin 3, Pin 36, Pin 41, Pin 46), Total Supply Voltage for Outputs		310	369	mA	Outputs terminated with 50 Ω to VDD3 − 2 V
VDD3 (Pin 9), Supply Voltage for M Divider, CLK Inputs and Distribution		98	107	mA	
VDD_CP (Pin 13), Supply Voltage for Charge Pump		6.6	7.6	mA	
VDD3 (Pin 20), Supply Voltage for PLL		53	63.4	mA	
VDD3 (Pin 32), Supply Voltage for SYNC_OUT		45	54	mA	

POWER DISSIPATION

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION, CHIP					Does not include power dissipated in external resistors; all LVPECL outputs terminated with 50 Ω to VDD3 − 2 V; LVPECL 780 mV mode
Power-On Default		782	871	mW	No programming; default register values
Typical Operation 1		1.15	1.23	W	f_{CLK} = 2949.12 MHz; REFA and REFB enabled at 122.88 MHz; R dividers = 2; M divider = 2; PFD = 61.44 MHz; eight LVPECL outputs at 1474.56 MHz
Typical Operation 2		1.17	1.25	W	f_{CLK} = 2949.12 MHz; PLL on; REFA enabled at 122.88 MHz; M divider = 1; PFD = 122.88MHz; eight LVPECL outputs at 2949.12 MHz
$\overline{PD}$ Power-Down		51	56.4	mW	$\overline{PD}$ pin pulled low
$\overline{PD}$ Power-Down, Maximum Sleep		13.2	19.1	mW	$\overline{PD}$ pin pulled low; power-down distribution reference, Reg. 0x230[1] = 1b; note that powering down distribution reference disables safe power-down mode (see Power-Down Modes section)
VDD_CP Supply		22	25	mW	PLL operating; typical closed-loop configuration

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DELTAS, INDIVIDUAL FUNCTIONS					Power delta when a function is enabled/disabled
M Divider On/Off		5	8.7	mW	M divider bypassed
P Divider On/Off		3	5.7	mW	P divider bypassed
B Divider On/Off		16	23.1	mW	B divider bypassed
REFB On		15	25	mW	Delta from powering down REFB differential input
PLL On/Off		254	300.5	mW	PLL off to PLL on, normal operation; no reference enabled
One Channel, One Driver		107	132	mW	No LVPECL output on to one LVPECL output on at 2949.12 MHz; same output pair
One Channel, Two Drivers		184	233	mW	No LVPECL output on to two LVPECL outputs on at 2949.12 MHz; same output pair

REFA AND REFB INPUT CHARACTERISTICS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL MODE (REFA, $\overline{\text{REFA}}$; REFB, $\overline{\text{REFB}}$)					Differential mode (can accommodate single-ended input by ac grounding unused input)
Input Frequency	0		500	MHz	Frequencies below ~1 MHz should be dc-coupled; be careful to match self-bias voltage
Input Sensitivity	200			mV p-p	Frequency at 122.88 MHz
Self-Bias Voltage, REFA and REFB	1.52	1.65	1.78	V	Self-bias voltage of REFA and REFB inputs[1]
Self-Bias Voltage, $\overline{\text{REFA}}$ and $\overline{\text{REFB}}$	1.38	1.50	1.61	V	Self-bias voltage of $\overline{\text{REFA}}$ and $\overline{\text{REFB}}$ inputs[1]
Input Resistance, REFA and REFB	4.5	4.7	4.9	kΩ	Self-biased[1]
Input Resistance, $\overline{\text{REFA}}$ and $\overline{\text{REFB}}$	4.9	5.2	5.4	kΩ	Self-biased[1]
DUTY CYCLE					Duty cycle bounds are set by pulse width high and pulse width low
Pulse Width Low	500			ps	
Pulse Width High	500			ps	

[1] The differential pairs of REFA and $\overline{\text{REFA}}$, REFB and $\overline{\text{REFB}}$ self-bias points are offset slightly to avoid chatter on an open input condition.

REFC INPUT CHARACTERISTICS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFC INPUT					
Input Frequency Range			300	MHz	DC-coupled input (not self-biased)
Input High Voltage	2.0			V	
Input Low Voltage			0.8	V	
Input Current		1		µA	
Duty Cycle					Duty cycle bounds are set by pulse width high and pulse width low
Pulse Width Low	1			ns	
Pulse Width High	1			ns	

CLOCK INPUTS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Input Frequency	0		3.6	GHz	Frequencies below ~1 MHz should be dc-coupled; be careful to match self-bias voltage
Input Sensitivity	150			mV p-p	Measured at 3.1 GHz
Input Level			2	V p-p	Larger voltage swings can turn on the protection diodes and can degrade jitter performance
Input Common-Mode Voltage, V_{CM}	1.55	1.64	1.74	V	Self-biased; enables ac coupling
Input Common-Mode Range, V_{CMR}	1.3		1.8	V	With 200 mV p-p signal applied; dc-coupled
Input Resistance	6.7	7	7.4	kΩ	Self-biased
Input Capacitance		2		pF	

PLL CHARACTERISTICS

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PHASE/FREQUENCY DETECTOR (PFD)					
PFD Input Frequency			125	MHz	Antibacklash pulse width = 1.3 ns, 2.9 ns
			45	MHz	Antibacklash pulse width = 6.0 ns
CHARGE PUMP (CP)					VDD_CP (Pin 13); V_{CP} is the voltage of the charge pump pin (CP, Pin 14)
I_{CP} Sink/Source					Programmable
High Value	4.5	4.9	5.4	mA	With CPRSET = 5.1 kΩ; higher I_{CP} is possible by changing CPRSET; V_{CP} = VDD_CP/2 V
Low Value	0.57	0.61	0.67	mA	With CPRSET = 5.1 kΩ; lower I_{CP} is possible by changing CPRSET, V_{CP} = VDD_CP/2 V
Absolute Accuracy		2.5		%	V_{CP} = VDD_CP/2 V
CPRSET Range	2.7		10	kΩ	
I_{CP} High Impedance Mode Leakage		3.5		µA	VDD_CP = 5 V
Sink-and-Source Current Matching		2		%	0.5 V < V_{CP} < VDD_CP − 0.5 V
I_{CP} vs. V_{CP}		1.5		%	0.5 V < V_{CP} < VDD_CP − 0.5 V
I_{CP} vs. Temperature		2		%	V_{CP} = VDD_CP/2 V
P DIVIDER (PART OF N DIVIDER)					
Input Frequency P = 1			1500	MHz	
Input Frequency P = 2			3000	MHz	
Input Frequency P = 3			3600	MHz	
Input Frequency P = 4			3600	MHz	
Input Frequency P = 5			3600	MHz	
Input Frequency P = 6			3600	MHz	
B DIVIDER (PART OF N DIVIDER)					
Input Frequency			1500	MHz	B counter input frequency (N Divider input frequency divided by P)
M DIVIDER					
Input Frequency			3600	MHz	
NOISE CHARACTERISTICS					
In-Band Phase Noise of the Charge Pump/ Phase Frequency Detector (In-Band Means Within the LBW of the PLL)					PLL in-band phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log(N) (where N is the value of the N divider)
At 61.44 MHz PFD Frequency		−144		dBc/Hz	
At 122.88 MHz PFD Frequency		−141		dBc/Hz	
PLL Figure of Merit (FOM)		−222		dBc/Hz	Reference slew rate > 0.25 V/ns; FOM +10 log (f_{PFD}) is an approximation of the PFD/CP in-band phase noise (in the flat region) inside the PLL loop bandwidth; when running closed loop, the phase noise, as observed at the VCO output, is increased by 20 log(N)

PLL DIGITAL LOCK DETECT

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PLL DIGITAL LOCK DETECT WINDOW[1]					Signal available at the STATUS and REF_MON pins when selected by appropriate register settings; lock detect window settings can be varied by changing the CPRSET resistor
Lock Threshold (Coincidence of Edges)					Selected by Reg. 0x010[1:0] and Reg. 0x019[1], which is the threshold for transitioning from unlock to lock
Low Range (ABP 1.3 ns, 2.9 ns)		4		ns	Reg. 0x010[1:0] = 00b, 01b,11b; Reg. 0x019[1] = 1b
High Range (ABP 1.3 ns, 2.9 ns)		7		ns	Reg. 0x010[1:0] = 00b, 01b, 11b; Reg. 0x019[1] = 0b
High Range (ABP 6.0 ns)		3.5		ns	Reg. 0x010[1:0] = 10b; Reg. 0x019[1] = 0b
Unlock Threshold (Hysteresis)[1]					Selected by Reg. 0x017[1:0] and Reg. 0x019[1], which is the threshold for transitioning from unlock to lock
Low Range (ABP 1.3 ns, 2.9 ns)		8.3		ns	Reg. 0x010[1:0] = 00b, 01b, 11b; Reg. 0x019[1] = 1b
High Range (ABP 1.3 ns, 2.9 ns)		16.9		ns	Reg. 0x010[1:0] = 00b, 01b, 11b; Reg. 0x019[1] = 0b
High Range (ABP 6.0 ns)		11		ns	Reg. 0x010[1:0] = 10b; Reg. 0x019[1] = 0b

[1] For reliable operation of the digital lock detect, the period of the PFD frequency must be greater than the unlock-after-lock time.

CLOCK OUTPUTS

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL CLOCK OUTPUTS					
Output Frequency, Maximum	3.6			GHz	
Rise Time/Fall Time (20% to 80%)		105	162	ps	
Duty Cycle					Input duty cycle = 50/50
M = 1	47	50	53	%	FOUT = 2800 MHz
	45	50	55	%	FOUT < 3000 MHz
M = 2, 4, 6	47	49	51	%	FOUT = 1400 MHz
	45	49	55	%	FOUT < 1500 MHz
M = 3, 5	32	32	33	%	FOUT = 933.33 MHz
Output Differential Voltage, Magnitude	750	830	984	mV	Voltage across pins, output driver static; Termination = 50 Ω to VDD3 − 2 V
Common-Mode Output Voltage	VDD3 − 1.42	VDD3 − 1.37	VDD3 − 1.32	V	Output driver static; VDD3 (Pin 3, Pin 36, Pin 41, Pin 46); Termination = 50 Ω to VDD3 − 2 V

TIMING CHARACTERISTICS

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PROPAGATION DELAY, t_{PECL}, CLKIN TO LVPECL OUTPUT					Termination as shown in Figure 35
For All M Divider Values	461	522	600	ps	High frequency clock distribution configuration
Variation with Temperature		388		fs/°C	
OUTPUT SKEW, LVPECL OUTPUTS[1]					
All LVPECL Outputs		13.5	25.2	ps	Across temperature and VDD per device
Temperature Coefficient		14		fs/°C	
All LVPECL Outputs Across Multiple Parts			144	ps	
OUTPUT SKEW, LVPECL-TO-SYNC_OUT[1]					
SYNC_OUT LVPECL Mode					
All LVPECL Outputs		189	298	ps	Across temperature and VDD per device
Temperature Coefficient		543		fs/°C	
All LVPECL Outputs Across Multiple Parts			417	ps	
SYNC_OUT CMOS Mode					
All LVPECL Outputs		1.64	2.34	ns	Across temperature and VDD per device
All LVPECL Outputs Across Multiple Parts			2.46	ns	
PROPAGATION DELAY, REF TO LVPECL OUTPUT	267	581	924	ps	REF refers to either REFA/$\overline{\text{REFA}}$ or REFB/$\overline{\text{REFB}}$ pairs

[1] The output skew is the difference between any two paths while operating at the same voltage and temperature.

Timing Diagrams

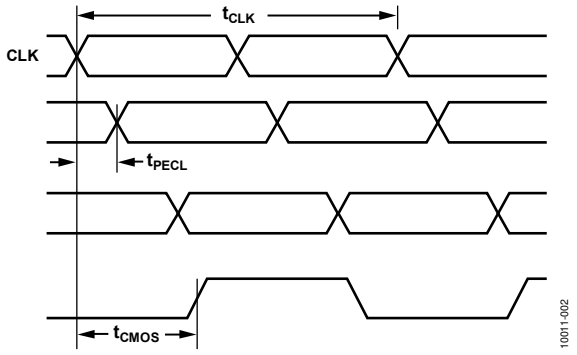


Figure 2. CLK/$\overline{\text{CLK}}$ to Clock Output Timing, M Divider = 1

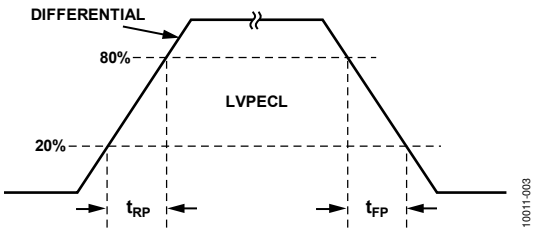


Figure 3. LVPECL Timing, Differential

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING EXTERNAL 122.88 MHZ VCXO)

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup using an external 122.88 MHz VCXO (Crystek CVHD-950); reference = 122.88 MHz; R divider = 1; LBW = 40 Hz
FOUT = 122.88 MHz		107		fs rms	Integration BW = 1 kHz to 40 MHz
		69		fs rms	Integration BW = 12 kHz to 20 MHz
FOUT = 61.44 MHz		108		fs rms	Integration BW = 1 kHz to 20 MHz
		107		fs rms	Integration BW = 12 kHz to 20 MHz

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING EXTERNAL 1475 MHZ VCO)

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup using an external 1475 MHz VCO (Bowei Model MVCO-1475); reference = 122.88 MHz; R divider = 1; PLL LBW = 18 kHz
FOUT = 1474.56 MHz		99		fs rms	Integration BW = 1 kHz to 100 MHz
		77		fs rms	Integration BW = 10 kHz to 100 MHz
		74		fs rms	Integration BW = 10 kHz to 40 MHz
		68		fs rms	Integration BW = 12 kHz to 20 MHz
Reference Sideband Spurs		−93		dBc	±122.88 MHz
FOUT = 245.76 MHz		104		fs rms	Integration BW = 1 kHz to 100 MHz
		87		fs rms	Integration BW = 10 kHz to 100 MHz
		75		fs rms	Integration BW = 12 kHz to 20 MHz
Reference Sideband Spurs		−98		dBc	±122.88 MHz

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup using an external 1475 MHz VCO (Z-Communications CRO1474-LF); reference = 122.88 MHz; R divider = 1; PLL LBW = 8 kHz
FOUT = 1474.56 MHz		72		fs rms	Integration BW = 1 kHz to 100 MHz
		40		fs rms	Integration BW = 10 kHz to 100 MHz
		33		fs rms	Integration BW = 10 kHz to 40 MHz
		28		fs rms	Integration BW = 12 kHz to 20 MHz
Reference Sideband Spurs		−94		dBc	±122.88 MHz
FOUT = 245.76 MHz		83		fs rms	Integration BW = 1 kHz to 100 MHz
		61		fs rms	Integration BW = 10 kHz to 40 MHz
		46		fs rms	Integration BW = 12 kHz to 20 MHz
Reference Sideband Spurs		−93		dBc	±122.88 MHz

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING EXTERNAL 2.05 GHZ VCO)

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup using an external 2.05 MHz VCO (Bowei Model MVCO-2050A); reference = 122.054215 MHz; R divider = 12; PLL LBW = 5 kHz
FOUT = 2048.867 MHz		19		fs rms	Integration BW = 200 kHz to 5 MHz
		21		fs rms	Integration BW = 200 kHz to 10 MHz
		87		fs rms	Integration BW = 12 kHz to 20 MHz
Reference Sideband Spurs		−105		dBc	±10.671MHz

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING EXTERNAL 3 GHZ VCO)

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup using an external 2950 MHz VCO (Z-Communications Model CRO-2950); reference = 122.88 MHz; R divider = 1
FOUT = 2949.12 MHz; PLL LBW = 7 kHz		63		fs rms	Integration BW = 1 kHz to 100 MHz
		38		fs rms	Integration BW = 10 kHz to 100 MHz
		34		fs rms	Integration BW = 10 kHz to 40 MHz
		28		fs rms	Integration BW = 12 kHz to 20 MHz
Reference Sideband Spurs		−99		dBc	±122.88 MHz
FOUT = 1474.56 MHz; PLL LBW = 7 kHz		62		fs rms	Integration BW = 1 kHz to 100 MHz
		36		fs rms	Integration BW = 10 kHz to 100 MHz
		31		fs rms	Integration BW = 10 kHz to 40 MHz
		25		fs rms	Integration BW = 12 kHz to 20 MHz
Reference Sideband Spurs		−100		dBc	±122.88 MHz
FOUT = 491.52 MHz; PLL LBW = 7 kHz		78		fs rms	Integration BW = 1 kHz to 100 MHz
		60		fs rms	Integration BW = 10 kHz to 100 MHz
		44		fs rms	Integration BW = 10 kHz to 40 MHz
		33		fs rms	Integration BW = 12 kHz to 20 MHz
Reference Sideband Spurs		−96		dBc	±122.88 MHz

CLOCK OUTPUT ADDITIVE PHASE NOISE (DISTRIBUTION ONLY; CLOCK INPUT TO DISTRIBUTION OUTPUT, INCLUDING VCO DIVIDER)

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK-TO-LVPECL ADDITIVE PHASE NOISE					Distribution section only; does not include PLL and VCO
CLK = 2949.12 MHz, FOUT = 2949.12 MHz					
Divider = 1					
At 10 Hz Offset		−112		dBc/Hz	
At 100 Hz Offset		−122		dBc/Hz	
At 1 kHz Offset		−133		dBc/Hz	
At 10 kHz Offset		−141		dBc/Hz	
At 100 kHz Offset		−146		dBc/Hz	
At 800 kHz Offset		−148		dBc/Hz	
At 1 MHz Offset		−148		dBc/Hz	
At 10 MHz Offset		−149		dBc/Hz	
At 100 MHz Offset		−151		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK = 1474.56 MHz, FOUT = 1474.56 MHz					
Divider = 1					
At 10 Hz Offset		−114		dBc/Hz	
At 100 Hz Offset		−125		dBc/Hz	
At 1 kHz Offset		−134		dBc/Hz	
At 10 kHz Offset		−144		dBc/Hz	
At 100 kHz Offset		−149		dBc/Hz	
At 800 kHz Offset		−151		dBc/Hz	
At 1 MHz Offset		−151		dBc/Hz	
At 10 MHz Offset		−154		dBc/Hz	
CLK = 122.88 MHz, FOUT = 122.88 MHz					
Divider = 1					
At 10 Hz Offset		−134		dBc/Hz	
At 100 Hz Offset		−145		dBc/Hz	
At 1 kHz Offset		−153		dBc/Hz	
At 10 kHz Offset		−159		dBc/Hz	
At 100 kHz Offset		−161		dBc/Hz	
At 800 kHz Offset		−161		dBc/Hz	
At 1 MHz Offset		−161		dBc/Hz	
At 10 MHz Offset		−161		dBc/Hz	

$\overline{PD}$, $\overline{RESET}$, AND REF_SEL PINS

Table 17.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT CHARACTERISTICS					
Logic 1 Voltage	2.0			V	
Logic 0 Voltage			0.8	V	
Logic 1 Current		1		µA	
Logic 0 Current $\overline{PD}$, $\overline{RESET}$		−112		µA	The minus sign indicates that current is flowing out of the AD9525, which is due to the internal pull-up resistor
Logic 0 Current REF_SEL		1		µA	
Capacitance		2		pF	
RESET TIMING					
Pulse Width Low	50			ns	
$\overline{RESET}$ Inactive to Start of Register Programming	100			ns	

STATUS AND REF_MON PINS

Table 18.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS					1 mA output load
Output Voltage High, V_{OH}	2.7			V	
Output Voltage Low, V_{OL}			0.4	V	
MAXIMUM TOGGLE RATE		200		MHz	Applies when mux is set to any divider or counter output or PFD up/down pulse; usually debug mode only; beware that spurs can couple to output when any of these pins is toggling

SERIAL CONTROL PORT

Table 19.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{CS}$ (INPUT)					$\overline{CS}$ has an internal 30 kΩ pull-up resistor
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current			2.5	μA	
Input Logic 0 Current		−112		μA	The minus sign indicates that current is flowing out of the AD9525, which is due to the internal pull-up resistor
Input Capacitance		2		pF	
SCLK (INPUT)					SCLK has an internal 30 kΩ pull-down resistor
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		112		μA	
Input Logic 0 Current			1	μA	
Input Capacitance		2		pF	
SDIO (WHEN INPUT)					
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		10		nA	
Input Logic 0 Current		20		nA	
Input Capacitance		2		pF	
SDIO, SDO (OUTPUTS)					1 mA load current
Output Logic 1 Voltage	2.7			V	
Output Logic 0 Voltage			0.4	V	
TIMING					
Clock Rate (SCLK, $1/t_{SCLK}$)			31	MHz	
Pulse Width High, t_{HIGH}	16			ns	
Pulse Width Low, t_{LOW}	16			ns	
SDIO to SCLK Setup, t_{DS}	2			ns	
SCLK to SDIO Hold, t_{DH}	1.1			ns	
SCLK to Valid SDIO and SDO, t_{DV}			12	ns	
$\overline{CS}$ to SCLK Setup and Hold, t_S, t_H	2			ns	
$\overline{CS}$ Minimum Pulse Width High, t_{PWH}	3.6			ns	

ABSOLUTE MAXIMUM RATINGS

Table 20.

Parameter	Rating
VDD3 to GND	−0.3 V to +3.6 V
VDD_CP, CP to GND	−0.3 V to +5.8 V
REFA, $\overline{\text{REFA}}$, REFB, $\overline{\text{REFB}}$, REFC to GND	−0.3 V to VDD3 + 0.3 V
OUT_RSET to GND	−0.3 V to VDD3 + 0.3 V
CP_RSET to GND	−0.3 V to VDD3 + 0.3 V
CLKIN, $\overline{\text{CLKIN}}$ to GND	−0.3 V to VDD3 + 0.3 V
CLKIN to $\overline{\text{CLKIN}}$	−1.2 V to +1.2 V
SCLK, SDIO, SDO, $\overline{\text{CS}}$ to GND	−0.3 V to VDD3 + 0.3 V
OUT0, $\overline{\text{OUT0}}$, OUT1, $\overline{\text{OUT1}}$, OUT2, $\overline{\text{OUT2}}$, OUT3, $\overline{\text{OUT3}}$, OUT4, $\overline{\text{OUT4}}$, OUT5, $\overline{\text{OUT5}}$, OUT6, $\overline{\text{OUT6}}$, OUT7, $\overline{\text{OUT7}}$, SYNC_OUT, $\overline{\text{SYNC\_OUT}}$ to GND	−0.3 V to VDD3 + 0.3 V
$\overline{\text{RESET}}$, $\overline{\text{PD}}$, STATUS, REF_MON to GND	−0.3 V to VDD3 + 0.3 V
Junction Temperature[1]	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 sec)	300°C

[1] See Table 21 for θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 21. Thermal Resistance (Simulated)

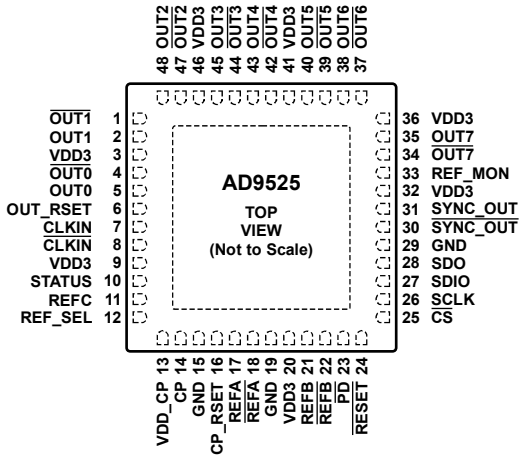
Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JC}[1, 3]	θ_{JB}[1, 4]	Ψ_{JT}[1, 2]	Unit
48-Lead LFCSP	0	27.3	2.1	14.7	0.2	°C/W
	1.0	23.9			0.3	°C/W
	2.5	21.4			0.4	°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD IS A GROUND CONNECTION ON THE CHIP THAT MUST BE SOLDERED TO THE ANALOG GROUND OF THE PCB TO ENSURE PROPER FUNCTIONALITY AND HEAT DISSIPATION, NOISE, AND MECHANICAL STRENGTH BENEFITS.

10011-004

Figure 4. Pin Configuration

Table 22. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	$\overline{\text{OUT1}}$	O	LVPECL Complementary Output 1.
2	OUT1	O	LVPECL Output 1.
3	VDD3	P	3.3 V Power Supply for Channel OUT0 and Channel OUT1.
4	$\overline{\text{OUT0}}$	O	LVPECL Complementary Output 0.
5	OUT0	O	LVPECL Output 0.
6	OUT_RSET	O	Clock Distribution Current Set Resistor. Connect a 4.12 kΩ resistor from this pin to GND.
7	CLKIN	I	Along with $\overline{\text{CLKIN}}$, this pin is the differential input for the clock distribution section.
8	$\overline{\text{CLKIN}}$	I	Along with CLKIN, this pin is the differential input for the clock distribution section. If a single-ended input is connected to the CLKIN pin, connect a 0.1 µF bypass capacitor from $\overline{\text{CLKIN}}$ to ground.
9	VDD3	P	3.3 V Power Supply for CLK Inputs, M Divider, and Output Distribution.
10	STATUS	O	Lock Detect and Other Status Signals.
11	REFC	I	Reference Clock Input C. This pin is a CMOS input for the PLL reference.
12	REF_SEL	I	Reference Input Select. Logic high = REFB. No internal pull-up or pull-down resistor on this pin.
13	VDD_CP	P	Power Supply for Charge Pump (CP). VDD3 < VDD_CP < 5.0 V. VDD_CP must still be connected to 3.3 V if the PLL is not used.
14	CP	O	Charge Pump (Output). This pin connects to an external loop filter. This pin can be left unconnected if the PLL is not used.
15	GND	GND	Ground for Charge Pump VDD_CP Supply. Connect to ground.
16	CP_RSET	O	Charge Pump Current Set Resistor. Connect a 5.1 kΩ resistor from this pin to GND. This resistor can be omitted if the PLL is not used.
17	REFA	I	Reference Clock Input A. Along with $\overline{\text{REFA}}$, this pin is the differential input for the PLL reference.
18	$\overline{\text{REFA}}$	I	Reference Clock Input A. Along with REFA, this pin is the differential input for the PLL reference.
19	GND	GND	Ground for PLL Power Supply. Connect to ground.
20	VDD3	P	3.3 V Power Supply for PLL.
21	REFB	I	Reference Clock Input B. Along with $\overline{\text{REFB}}$, this pin is the differential input for the PLL reference.
22	$\overline{\text{REFB}}$	I	Reference Clock Input B. Along with REFB, this pin is the differential input for the PLL reference.
23	$\overline{\text{PD}}$	I	Chip Power-Down, Active Low. This pin has an internal 30 kΩ pull-up resistor.
24	$\overline{\text{RESET}}$	I	Chip Reset, Active Low. This pin has an internal 30 kΩ pull-up resistor.
25	$\overline{\text{CS}}$	I	Serial Control Port Chip Select; Active Low. This pin has an internal 30 kΩ pull-up resistor.
26	SCLK	I	Serial Control Port Clock Signal. This pin has an internal 30 kΩ pull-down resistor.
27	SDIO	I	Serial Control Port Bidirectional Serial Data In/Out.

Pin No.	Mnemonic	Type	Description
28	SDO	I	Serial Control Port Unidirectional Serial Data Out.
29	GND	GND	Connect to ground.
30	$\overline{\text{SYNC\_OUT}}$	O	LVPECL Complementary Output for Programmable Sync Signal.
31	SYNC_OUT	O	LVPECL Output for Programmable Sync Signal.
32	VDD3	P	Power Supply for SYNC_OUT Driver.
33	REF_MON	O	Reference Monitor (Output). This pin has multiple selectable outputs.
34	$\overline{\text{OUT7}}$	O	LVPECL Complementary Output 7.
35	OUT7	O	LVPECL Output 7.
36	VDD3	P	3.3 V Power Supply for Channel OUT6 and Channel OUT7.
37	$\overline{\text{OUT6}}$	O	LVPECL Complementary Output 6.
38	OUT6	O	LVPECL Output 6.
39	$\overline{\text{OUT5}}$	O	LVPECL Complementary Output 5.
40	OUT5	O	LVPECL Output 5.
41	VDD3	P	3.3 V Power Supply for Channel OUT4 and Channel OUT5.
42	$\overline{\text{OUT4}}$	O	LVPECL Complementary Output 4.
43	OUT4	O	LVPECL Output 4.
44	$\overline{\text{OUT3}}$	O	LVPECL Complementary Output 3.
45	OUT3	O	LVPECL Output 3.
46	VDD3	P	3.3 V Power Supply for Channel OUT2 and Channel OUT3.
47	$\overline{\text{OUT2}}$	O	LVPECL Complementary Output 2.
48	OUT2	O	LVPECL Output 2.
EP	EP, GND	GND	Exposed Paddle. The exposed pad is a ground connection on the chip that must be soldered to the analog ground of the PCB to ensure proper functionality and heat dissipation, noise, and mechanical strength benefits.

TYPICAL PERFORMANCE CHARACTERISTICS

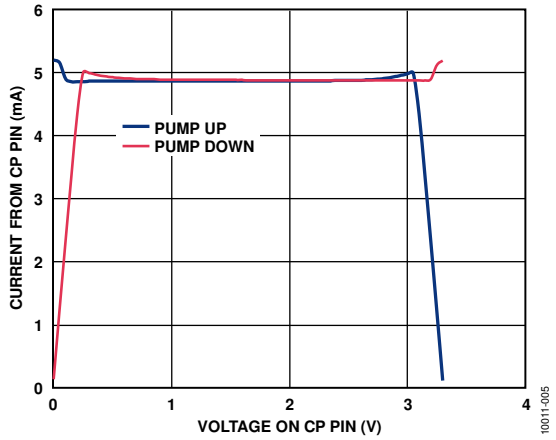


Figure 5. Charge Pump Characteristics at VDD_CP = 3.3 V

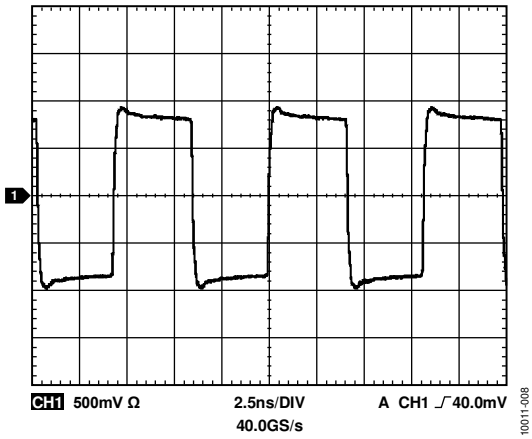


Figure 8. LVPECL Output (Differential) at 122.88 MHz

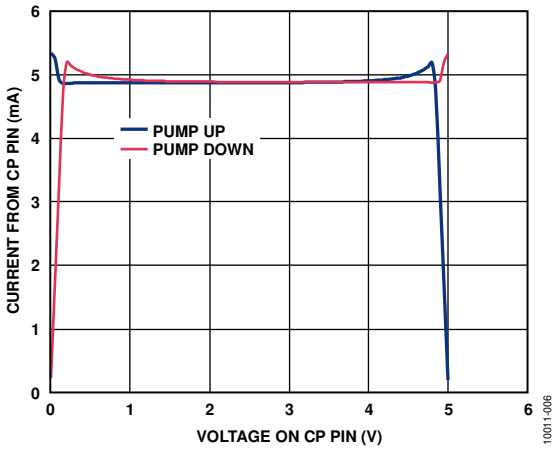


Figure 6. Charge Pump Characteristics at VDD_CP = 5.0 V

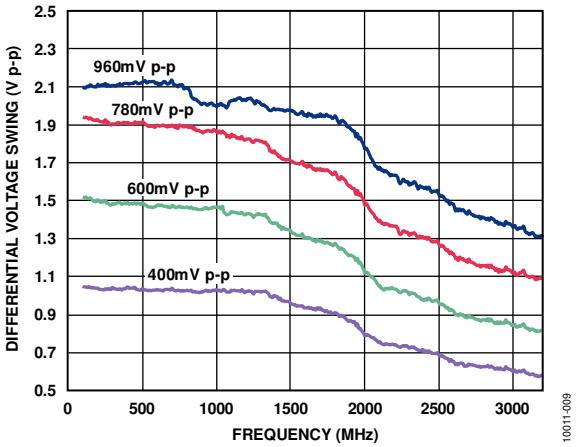


Figure 9. LVPECL Differential Voltage Swing vs. Frequency

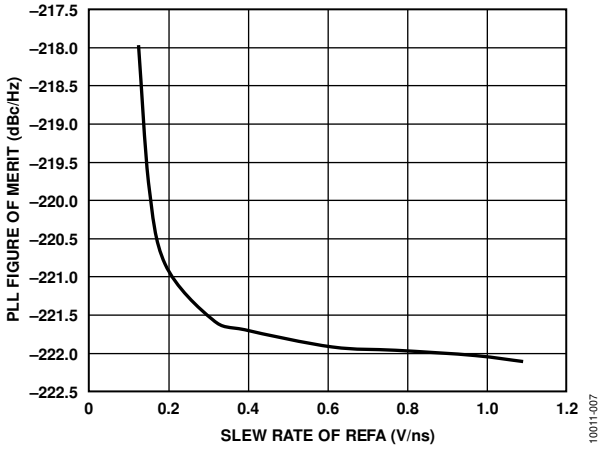


Figure 7. PLL Figure of Merit (FOM) vs. Slew Rate at REFA

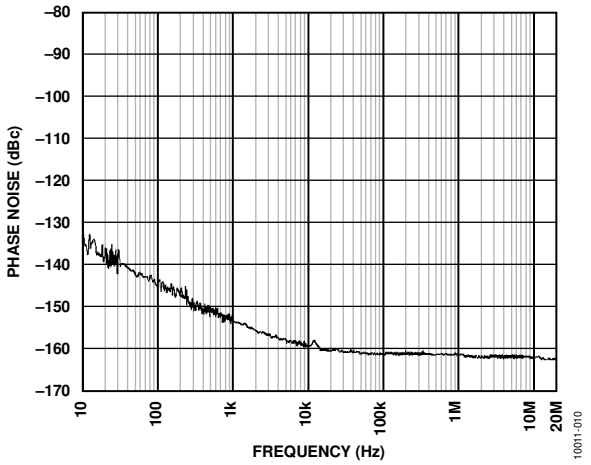


Figure 10. Additive (Residual) Phase Noise, CLK-to-LVPECL at 122.88 MHz, Divide-by-1

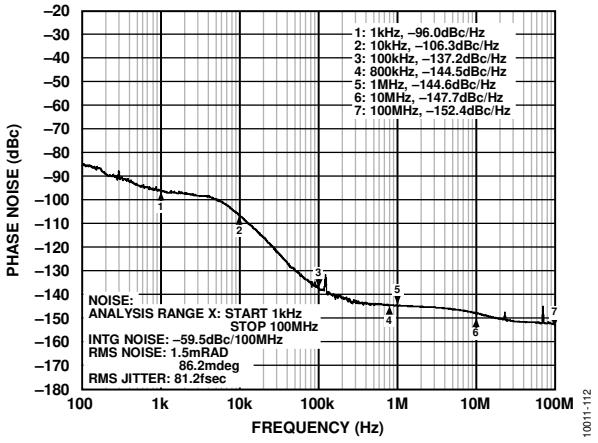


Figure 13. Phase Noise (Absolute), External VCO (Z-Communications Model CRO-2950) at 2949.12 MHz; PFD = 122.88 MHz; LBW = 8 kHz; LVPECL Output = 2949.12 MHz

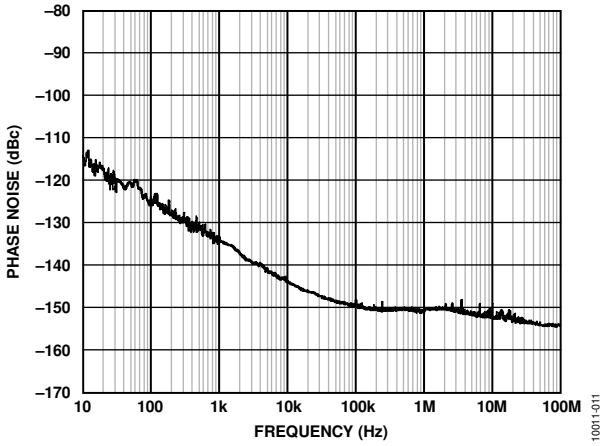


Figure 11. Additive (Residual) Phase Noise, CLK-to-LVPECL at 1500 MHz, Divide-by-1

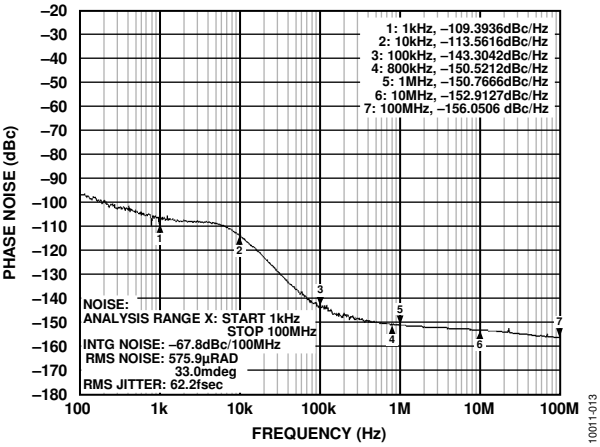


Figure 14. Phase Noise (Absolute), External VCO (Z-Communications Model CRO-2950) at 2949.12 MHz; PFD = 122.88 MHz; LBW = 8k Hz; LVPECL Output = 1474.56 MHz

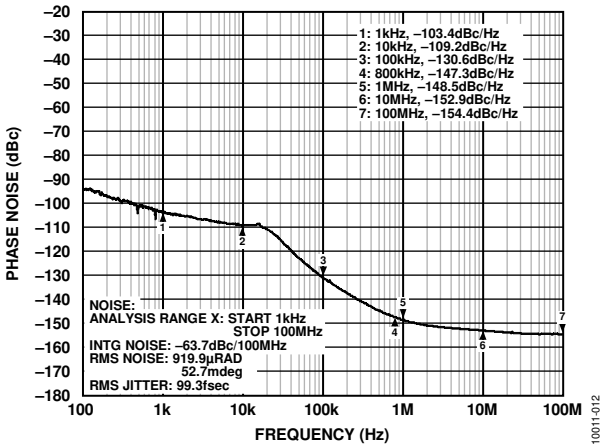


Figure 12. Phase Noise (Absolute), External VCO (Bowei Model MVCO-1475) at 1474.56 MHz; PFD = 122.88 MHz; LBW = 18 kHz; LVPECL Output = 1474.56 MHz

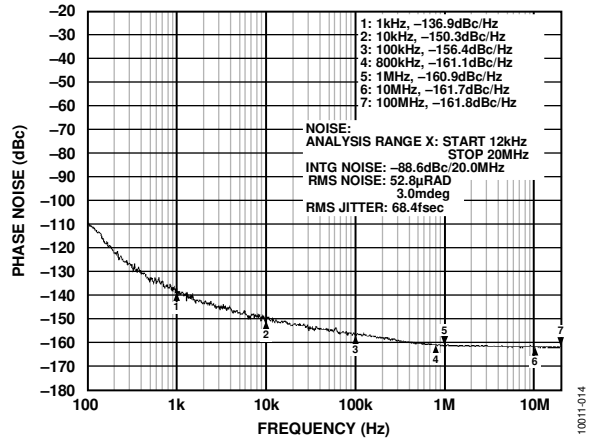


Figure 15. Phase Noise (Absolute), External VCXO (122.88 MHz VCXO) (Crystek CVHD-950); Reference = 122.88 MHz; R Divider = 1); LBW = 40 Hz; LVPECL Output = 122.88 MHz

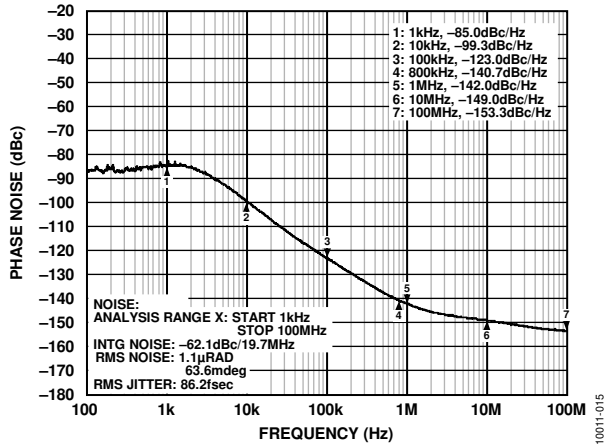


Figure 16. Phase Noise (Absolute), External VCO 2.05 GHz VCO (Bowei Model MVCO-2050A); at 2050 MHz; Reference = 122.054215 MHz; R Divider = 12

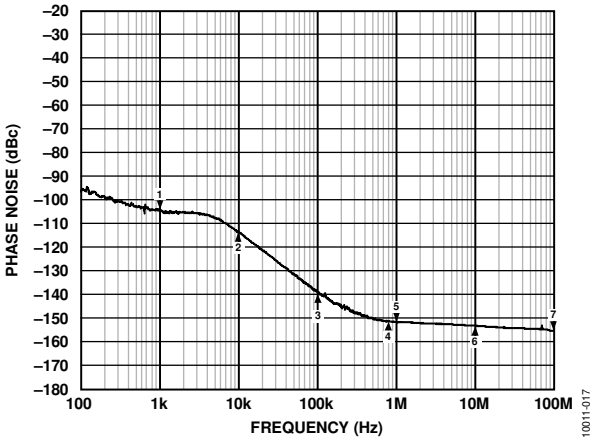


Figure 17. Phase Noise (Absolute), External VCO (Z-Communications CRO1474-LF) at 1474.56 MHz; PFD = 122.88 MHz; LBW = 15 kHz; LVPECL Output = 1474.56 MHz

TERMINOLOGY

Phase Jitter and Phase Noise

An ideal sine wave can be thought of as having a continuous and even progression of phase with time from 0° to 360° for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time. This phenomenon is called phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, which is characterized statistically as being Gaussian (normal) in distribution.

This phase jitter leads to a spreading out of the energy of the sine wave in the frequency domain, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in decibels) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

It is meaningful to integrate the total power contained within some interval of offset frequencies (for example, 10 kHz to 10 MHz). This is called the integrated phase noise over that frequency offset interval; it can be readily related to the time jitter due to the phase noise within that offset frequency interval.

Phase noise has a detrimental effect on the performance of ADCs, DACs, and RF mixers. It lowers the achievable dynamic range of the converters and mixers, although they are affected in somewhat different ways.

Time Jitter

Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings varies. In a square wave, the time jitter is a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in seconds root mean square (rms) or 1 sigma of the Gaussian distribution.

Time jitter that occurs on a sampling clock for a DAC or an ADC decreases the signal-to-noise ratio (SNR) and dynamic range of the converter. A sampling clock with the lowest possible jitter provides the highest performance from a given converter.

Additive Phase Noise

Additive phase noise is the amount of phase noise that can be attributed to the device or subsystem being measured. The phase noise of any external oscillators or clock sources is subtracted, making it possible to predict the degree to which the device impacts the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contributes its own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise. When there are multiple contributors to phase noise, the total is the square root of the sum of squares of the individual contributors.

Additive Time Jitter

Additive time jitter is the amount of time jitter that can be attributed to the device or subsystem being measured. The time jitter of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device impacts the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contributes its own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.

DETAILED BLOCK DIAGRAM

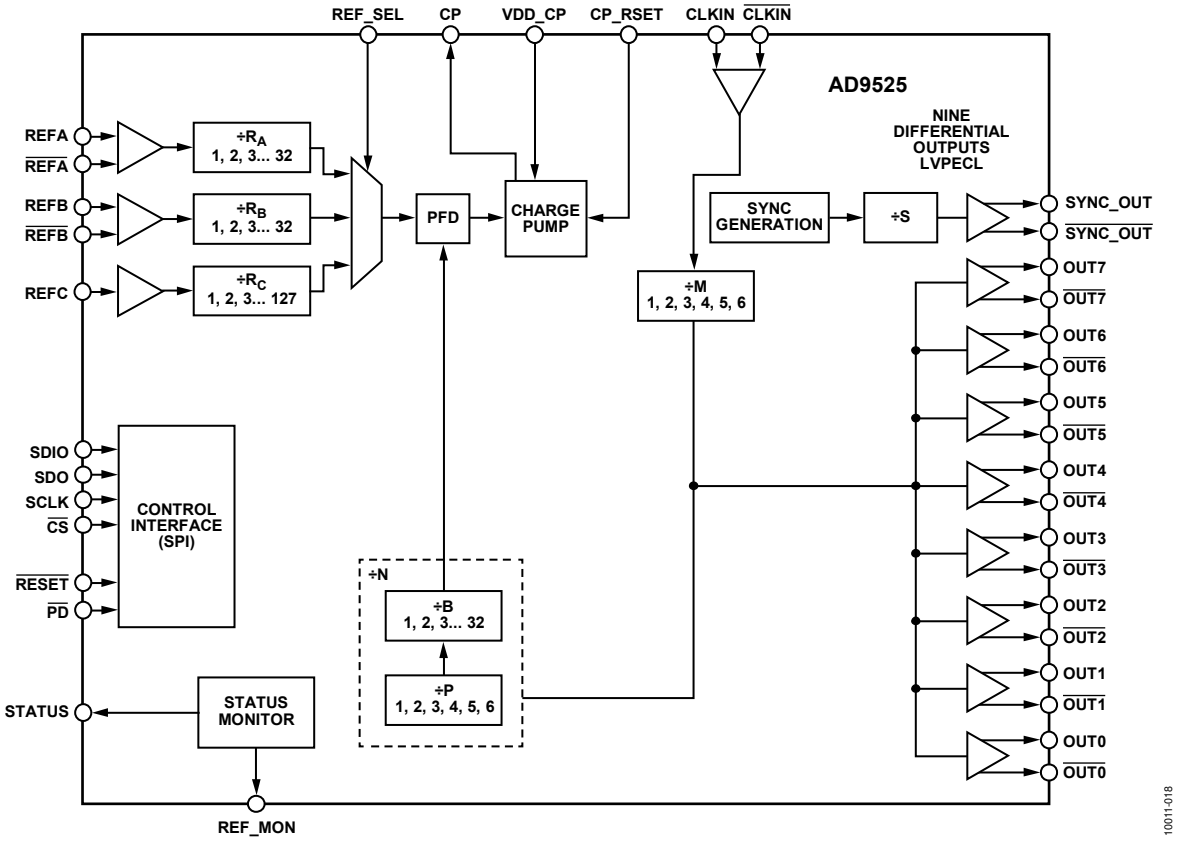


Figure 18. Detailed Block Diagram

THEORY OF OPERATION

The AD9525 PLL is useful for generating clock frequencies from a supplied reference frequency. In addition, the PLL can be used to clean up jitter and phase noise on a noisy reference. The exact choice of PLL parameters and loop dynamics is application specific. The flexibility and depth of the AD9525 PLL allow the part to be tailored to function in many different applications and signal environments.

The AD9525 includes on-chip PLL blocks that can be used with an external VCO or VCXO to create a complete phase-locked loop. The PLL requires an external loop filter, which usually consists of a small number of capacitors and resistors. The configuration and components of the loop filter help to establish the loop bandwidth and stability of the PLL. The external loop filter that must be connected between CP and the tuning pin of the VCO/VCXO. This loop filter determines the loop bandwidth and stability of the PLL. Make sure to select the proper PFD polarity for the VCO/VCXO being used.

The AD9525 can also be configured as a clock distribution by shutting down the PLL and using CLKIN and $\overline{\text{CLKIN}}$ as the input. The M divider can be used to divide the input frequency down to the desired output frequency to each of the eight LVPECL outputs.

CONFIGURATION OF THE PLL

Configuration of the PLL is accomplished by programming the various settings for the R divider, N divider, PFD polarity, and charge pump current. The combination of these settings and the loop filter determines the PLL loop bandwidth and PLL stability. These are managed through programmable register settings and by the design of the external loop filter.

Successful PLL operation and satisfactory PLL loop performance are highly dependent on proper configuration of the PLL settings, and the design of the external loop filter is crucial to the proper operation of the PLL.

ADIsimCLK™ is a free program that can help with the design and exploration of the capabilities and features of the AD9525, including the design of the PLL loop filter. The AD9516 model found in ADIsimCLK Version 1.2 can also be used for modeling the AD9525 loop filter. It is available at www.analog.com/clocks.

Phase Frequency Detector (PFD)

The PFD takes inputs from the R divider and the N divider and produces an output proportional to the phase and frequency difference between them. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. The antibacklash pulse width is set by Register 0x010[1:0].

An important limit to keep in mind is the maximum frequency allowed into the PFD. The maximum input frequency into the PFD is a function of the antibacklash pulse setting, as specified in the phase/frequency detector (PFD) parameter in Table 7.

Charge Pump (CP)

The charge pump is controlled by the PFD. The PFD monitors the phase and frequency relationship between its two inputs and tells the CP to pump up or pump down to charge or discharge the integrating node (part of the loop filter). The integrated and filtered CP current is transformed into a voltage that drives the tuning node of the external VCO to move the VCO frequency up or down. The CP can be set for high impedance (allows holdover operation), for normal operation (attempts to lock the PLL loop), for pump-up, or for pump-down (test modes). The CP current is programmable in eight steps. The exact value of the CP current LSB is set by the CPRSET resistor, which is nominally 5.1 kΩ. The actual LSB current can be calculated by CP_LSB = 3.06/CPRSET.

PLL External Loop Filter

An example of an external loop filter for the PLL is shown in Figure 19. A loop filter must be calculated for each desired PLL configuration. The values of the components depend on the VCO frequency, the K_{VCO}, the PFD frequency, the charge pump current, the desired loop bandwidth, and the desired phase margin. The loop filter affects the phase noise, the loop settling time, and the loop stability. A basic knowledge of PLL theory is necessary for understanding loop filter design. ADIsimCLK can help with the calculation of a loop filter according to the application requirements.

PLL Reference Inputs

The AD9525 features two fully differential PLL reference input circuits. The differential inputs are self-biased, allowing for easy ac coupling of input signals. All PLL reference inputs are off by default. The self-bias level of the two sides is offset slightly to prevent chattering of the input buffer when the reference is ac coupled and is slow or missing. The input offset increases the voltage swing required of the driver to overcome the offset. The input frequency range and common-mode voltages for the reference inputs are specified in Table 4.

The reference input receiver is powered down when the PLL is powered down. It is possible to dc couple to these inputs. If the differential reference input is driven by a single-ended signal, the unused side ($\overline{\text{REFA}}$ or $\overline{\text{REFB}}$) should be decoupled via a suitable capacitor to a quiet ground.

The AD9525 provides a third single-ended CMOS reference input referred to as REFC.

Reference Switchover

The AD9525 supports two separate differential reference inputs. Manual switchover is performed between these inputs either through Register 0x01A or by using the REF_SEL pin. This feature supports networking and other applications that require redundant references.

Manual switchover requires that a clock be present on the reference input that is being switched to or that the switchover deglitching feature be disabled (Register 0x01A[4]).

Reference Dividers R

The reference inputs are routed to their respective divider, R. R can be set to any value from 1 to 32 (Both R = 0 and R = 1 give divide-by-1.).

The division is set by the values of R_{LOW} and R_{HIGH}. The divider can be bypassed (equivalent to divide-by-1, divider circuit is powered down) by setting the bypass bit.

For each R divider, the frequency division (R_X) is set by the values of R_{LOW} and R_{HIGH} (four bits each, representing Decimal 0 to Decimal 15), where

$$Number\ of\ Low\ Cycles = R_{LOW} + 1$$

$$Number\ of\ High\ Cycles = R_{HIGH} + 1$$

The high and low cycles are cycles of the clock signal currently routed to the input of the R.

When a divider is bypassed, $R_X = 1$.

Otherwise, $R_X = (R_{HIGH} + 1) + (R_{LOW} + 1) = R_{HIGH} + R_{LOW} + 2$. This allows each reference divider to divide by any integer from 1 to 32.

The output of the R divider goes to a mux to select one of the references to the PFD inputs. The frequency applied to the PFD must not exceed the maximum allowable frequency, which depends on the antibacklash pulse setting (see Table 7).

The R divider has its own reset. The R divider can also be reset using the shared reset bit of the R and B counters. This reset bit is not self-clearing.

The R divider in the REFC path has a division ratio programmable from 1 to 127.

VCO/VCXO, M and N Feedback Dividers

The feedback division is the product of the M divider and the N divider. The N divider is a combination of a prescaler (P) and a B divider.

$$f_{VCO} = (f_{REF}/R) \times N \times M$$

where:
M =1, 2, 3, 4, 5, or 6.
$N = (P \times B)$.
P =1, 2, 3, 4, 5, or 6.
B = 1, 2, 3, … or 32.

M Divider

The M divider is a fixed divide (FD) of 1, 2, 3, 4, 5, or 6.

The maximum input frequency to the M counter is reflected in the maximum CLKIN input frequency specified in Table 6.

The M divider provides frequency division between the CLKIN input and the N feedback divider and clock distribution output channels.

The M divider can also be set to static, which is useful for applications where the only desired output frequency is the CLK input frequency.

P Divider

The P divider is a fixed divide (FD) of 1, 2, 3, 4, 5 or 6.

The maximum input frequency to the P counter is reflected in the maximum CLKIN input frequency specified in Table 6.

B Divider

The B divider is a fixed divide (FD) of 1, 2, 3, …or 32.

The maximum input frequency to the B counter is ~1500 MHz, as specified in Table 7. This is the prescaler input frequency (external VCO or CLKIN) divided by the P and M counters. For example, M = 1 and P = 1 mode is not allowed if the external VCO frequency is greater than 1500 MHz because the frequency going to the B divider is too high.

The division is set by the values of B_{LOW} and B_{HIGH}. The divider can be bypassed (equivalent to divide-by-1, divider circuit is powered down) by setting the bypass bit.

The frequency division, B_X, is set by the values of B_{LOW} and B_{HIGH} (four bits each, representing Decimal 0 to Decimal 15), where

$$Number\ of\ Low\ Cycles = B_{LOW} + 1$$

$$Number\ of\ High\ Cycles = B_{HIGH} + 1$$

The high and low cycles are cycles of the clock signal currently routed to the input of the B divider.

When a divider is bypassed, $B_X = 1$.

Otherwise, $B_X = (B_{HIGH} + 1) + (B_{LOW} + 1) = B_{HIGH} + B_{LOW} + 2$.

Although manual reset is not normally required, the B counter has its own reset bit. Note that this reset bit is not self-clearing.

Digital Lock Detect (DLD)

By selecting the proper output through the mux on each pin, the DLD function is available at the STATUS and REF_MON pins. The digital lock detect circuit indicates a lock when the time difference of the rising edges at the PFD inputs is less than a specified value (the lock threshold). The loss of a lock is indicated when the time difference exceeds a specified value (the unlock threshold). Note that the unlock threshold is wider than the lock threshold, which allows some phase error in excess of the lock window to occur without chattering on the lock indicator.

The lock detect window timing depends on the value of the CPRSET resistor, as well as three settings: the digital lock detect window bit (Register 0x019[1]), the antibacklash pulse width bits (Register 0x010[1:0], see Table 8), and the lock detect counter bits (Register 0x019[3:2]). The lock and unlock detection values in Table 8 are for the nominal value of CPRSET = 5.11 kΩ. Doubling the CPRSET value to 10 kΩ doubles the values in Table 8.

A lock is not indicated until there is a programmable number of consecutive PFD cycles with a time difference that is less than the lock detect threshold. The lock detect circuit continues to indicate a lock until a time difference greater than the unlock threshold occurs on a single subsequent cycle. For the lock detect to work properly, the period of the PFD frequency must be greater than the unlock threshold. The number of consecutive PFD cycles required for a lock is programmable (Register 0x018[6:5]).

Note that, in certain low (<500 Hz) loop bandwidth, high phase margin cases, it is possible that the DLD can chatter during acquisition. This is normal and occurs because the PFD inputs are moving slowly in and out of the lock/unlock window during PLL loop settling. Adjustment of the lock detect counter setting (Register 0x019[3:2]) can suppress this behavior.

External VCXO/VCO Clock Input (CLKIN/$\overline{\text{CLKIN}}$)

This differential input is used to drive the AD9525 clock distribution section. The pins are internally self-biased, and the input signal should be ac-coupled via capacitors.

The CLKIN/$\overline{\text{CLKIN}}$ input can be used either as a distribution only input (with the PLL off) or as a feedback input for an external VCO/VCXO using the internal PLL. Sample configurations are illustrated in Figure 19 through Figure 21. Refer to the manufacturer's recommendation for VCO terminations; a T or PI attenuator is often recommended, as illustrated in Figure 19.

For operation using a CMOS input, an external resistive divider is required to limit the swing on CLKIN (see Table 6 for the maximum input rating).

Status Monitor

The AD9525 contains three frequency status monitors that are used to indicate if the PLL reference (or references, in the case of single-ended mode) and the VCO have fallen below a threshold.

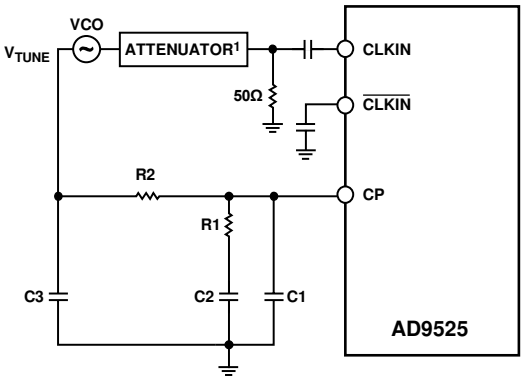


Figure 19. CLKIN Configured as Single-Ended VCO

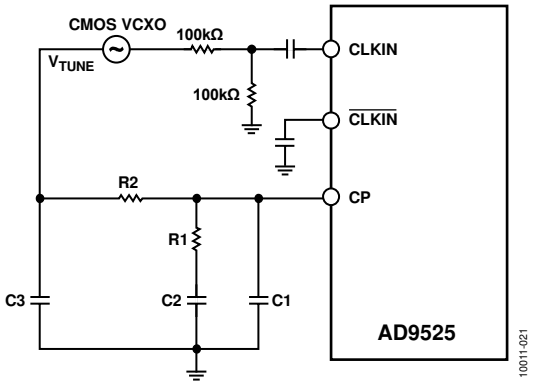


Figure 20. CLKIN Configured as Single-Ended CMOS VCXO

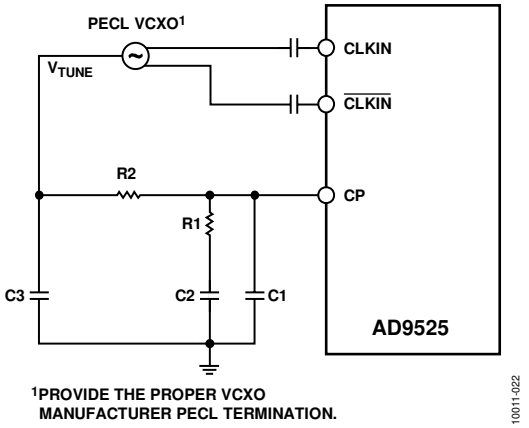


Figure 21. CLKIN Configured as Differential LVPECL VCXO

CLOCK DISTRIBUTION

The AD9525 can be used only as a clock fan out buffer by disabling the PLL circuit blocks except for the clock distribution section. The clock distribution consists of eight LVPECL clock output drivers that share a common M divider. See the M Divider section for more information on the common M divider.

Duty Cycle and Duty-Cycle Correction

The duty cycle of the clock signal at the output of a driver is a result of either or both of the following conditions:

- The CLKIN, $\overline{\text{CLKIN}}$ input duty cycle. If the CLKIN, $\overline{\text{CLKIN}}$ input is routed directly to the output, the duty cycle of the output is the same as the CLKIN, $\overline{\text{CLKIN}}$ input.
- The M divider value. An odd M divider value results in a non-50% duty cycle.

Table 23.Typical Output Duty Cycle with M Divider ≠ 1

M Divider	Output Duty Cycle (%)
Even	50
Odd = 3	33.3
Odd = 5	40

LVPECL Output Drivers

The LVPECL differential voltage (V_{OD}) is selectable (from ~400 mV to 960 mV (see Bit 2 and Bit 1 in Register 0x0F0 to Register 0x0F7).

The LVPECL output polarity can be set as noninverting or inverting, which allows for the adjustment of the relative polarity of outputs within an application without requiring a board layout change. Each LVPECL output can be powered down or powered up, as needed. Because of the architecture of the LVPECL output stages, there is the possibility of electrical overstress and breakdown under certain power-down conditions.

For this reason, the LVPECL outputs have two power-down modes: total power-down and safe power-down. The primary power-down mode is the safe power-down mode. This mode continues to protect the output devices while powered down. There are three ways to activate safe power-down mode: individually set the power-down bit for each driver, power down an individual output channel, or activate sleep mode.

In total power-down mode 0x0230[1] = 1 (power down distribution reference). This mode must not be used if there is an external voltage bias network (such as Thevenin equivalent termination) on the output pins that will cause a dc voltage to appear at the powered down outputs. However, total power-down mode is allowed when the LVPECL drivers are terminated using only pull-down resistors.

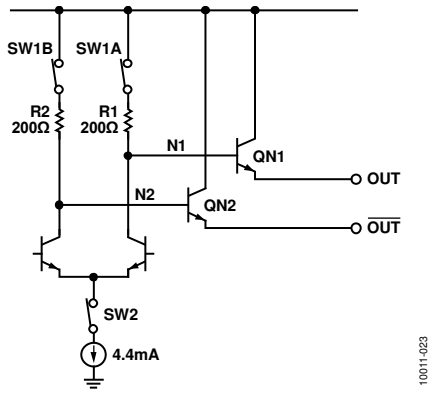


Figure 22. LVPECL Output Simplified Equivalent Circuit

SYNC_OUT

SYNC_OUT provides one LVPECL output or two CMOS output signal that can used to reset or synchronize a converter. SYNC_OUT functionality block diagram is shown in Figure 23. The SYNC_OUT signal is derived from the PLL phase detector reference input clock or feedback (N-divider) clock. A programmable 16-bit S divider further divides the selected reference clock. There are three different modes of operation for SYNC_OUT: single shot, periodic, or pseudorandom. SYNC_OUT is retimed to the high speed clock.

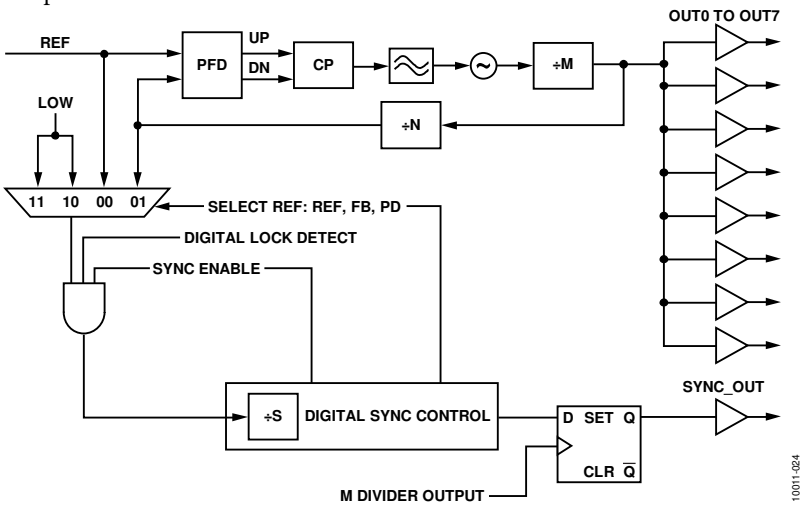


Figure 23. SYNC_OUT Functional Diagram

Single Shot Mode

In single shot mode one sync pulse occurs after writing SYNC ENABLE 0x192[4] = 1. An IO_UPDATE is required to complete a register write. The width of the sync pulse is determined by the value of the S divider. A divider value of 0x0000 allows a pulse whose width is equal to one half period of the phase detector rate. A divider value of 0x0001 allows a pulse whose width is equal to two half periods of the phase detector rate. In single shot mode, the sync enable bit is self-clearing and the sync circuits are ready to receive another sync enable.

Periodic Mode

In periodic mode, the pulse is continuous until SYNC ENABLE is cleared by a register writing SYNC ENABLE 0x192[4] = 0. An IO_UPDATE is required to complete a register write. The width of the sync pulse is equal to one half period of the phase detector rate. The pulse repetition rate is determined by the value of the S divider. A divider value of 0x0000 allows a pulse rate equal to the phase detector rate. A divider value of 0x0001 allows a pulse rate equal to two half periods of the phase detector rate. The SYNC_OUT signal is resampled with the OUT clock to ensure time alignment and minimum output skew. There is a possibility in periodic mode that the SYNC_OUT could slip one half cycle of the OUT clock period.

Pseudorandom Mode

Pseudorandom mode is similar to periodic mode but the pulse is a PN17 sequence that is continuous until SYNC ENABLE is cleared by a register writing SYNC ENABLE 0x192[4] = 0. An IO_UPDATE is required to complete a register write. The width of the sync pulse is equal to one half period the phase detector rate. The pulse repetition rate is determined by the value of the S divider. A divider value of 0x0000 allows a pulse rate equal to the phase detector rate. A divider value of 0x0001 allows pulse rate equal to two half the phase detector rate.

SYNC_OUT Programming

The procedure to configure the SYNC_OUT depends on the logic requirement of the converters that require synchronization. Analog Devices, Inc., converters are synchronized on the rise edge of the SYNC pulse.

SYNC_OUT CMOS Driver

The user can also configure the LVPECL SYNC_OUT as a pair of CMOS outputs. When the output is configured as CMOS, CMOS Output A and CMOS Output B are automatically turned on. Either CMOS Output A or Output B can be turned on or off independently. The user can also select the relative polarity of the CMOS outputs for any combination of inverting and noninverting (see Register 0x0F9). The user can power down each CMOS output as needed to save power. The CMOS driver is in tristate when it is powered down.

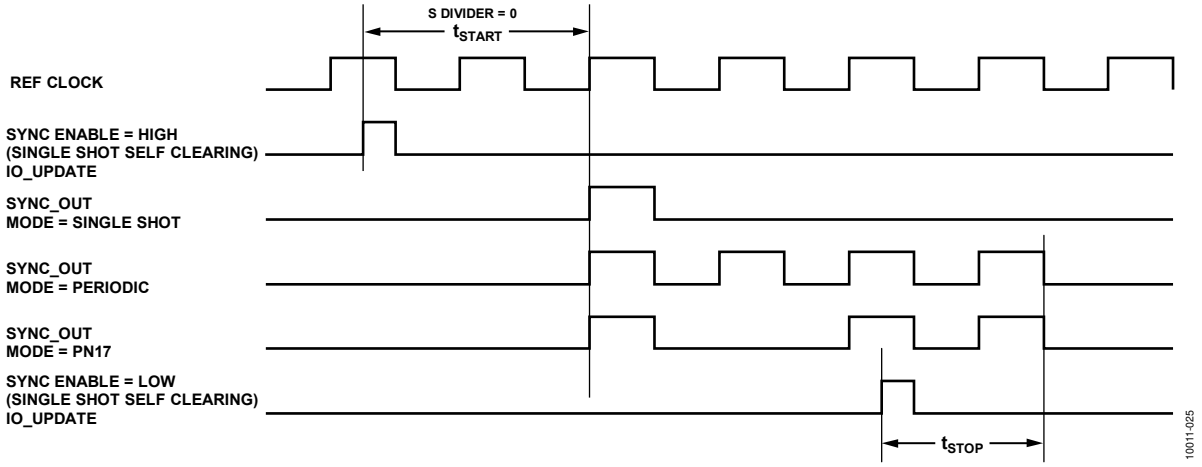


Figure 24. SYNC Output Timing