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JESD204B Clock Generator with 14 LVDS/HSTL Outputs

Data Sheet **AD9528**

FEATURES

- 14 outputs configurable for HSTL or LVDS
- Maximum output frequency
  - 2 outputs up to 1.25 GHz
  - 12 outputs up to 1 GHz
- Dependent on the voltage controlled crystal oscillator (VCXO) frequency accuracy (start-up frequency accuracy: <±100 ppm)
- Dedicated 8-bit dividers on each output
  - Coarse delay: 63 steps at 1/2 the period of the RF VCO divider output frequency with no jitter impact
  - Fine delay: 15 steps of 31 ps resolution
- Typical output to output skew: 20 ps
- Duty cycle correction for odd divider settings
- Output 12 and Output 13, VCXO output at power up
- Absolute output jitter: <160 fs at 122.88 MHz, 12 kHz to 20 MHz integration range
- Digital frequency lock detect
- SPI- and I^2C-compatible serial control port
- Dual PLL architecture
  - PLL1
    - Provides reference input clock cleanup with external VCXO
    - Phase detector rate up to 110 MHz
    - Redundant reference inputs
    - Automatic and manual reference switchover modes
      - Revertive and nonrevertive switching
    - Loss of reference detection with holdover mode
    - Low noise LVDS/HSTL outputs from VCXO used for radio frequency/intermediate frequency (RF/IF) synthesizers
  - PLL2
    - Phase detector rate of up to 275 MHz
    - Integrated low noise VCO

APPLICATIONS

- High performance wireless transceivers
- LTE and multicarrier GSM base stations
- Wireless and broadband infrastructure
- Medical instrumentation
- Clocking high speed ADCs, DACs, DDSs, DDCs, DUCs, MxFEs; supports JESD204B
- Low jitter, low phase noise clock distribution
- ATE and high performance instrumentation

FUNCTIONAL BLOCK DIAGRAM

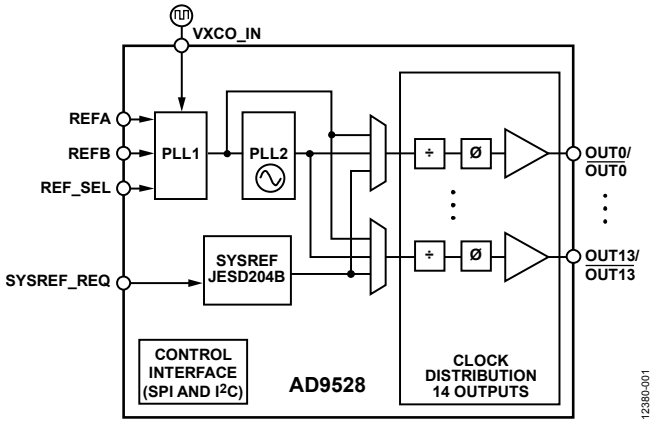

Figure 1.

GENERAL DESCRIPTION

The AD9528 is a two-stage PLL with an integrated JESD204B SYSREF generator for multiple device synchronization. The first stage phase-locked loop (PLL) (PLL1) provides input reference conditioning by reducing the jitter present on a system clock. The second stage PLL (PLL2) provides high frequency clocks that achieve low integrated jitter as well as low broadband noise from the clock output drivers. The external VCXO provides the low noise reference required by PLL2 to achieve the restrictive phase noise and jitter requirements necessary to achieve acceptable performance. The on-chip VCO tunes from 3.450 GHz to 4.025 GHz. The integrated SYSREF generator outputs single shot, N-shot, or continuous signals synchronous to the PLL1 and PLL2 outputs to time align multiple devices.

The AD9528 generates two outputs (Output 1 and Output 2) with a maximum frequency of 1.25 GHz, and 12 outputs up to 1 GHz. Each output can be configured to output directly from PLL1, PLL2, or the internal SYSREF generator. Each of the 14 output channels contains a divider with coarse digital phase adjustment and an analog fine phase delay block that allows complete flexibility in timing alignment across all 14 outputs. The AD9528 can also be used as a dual input flexible buffer to distribute 14 device clock and/or SYSREF signals. At power-up, the AD9528 sends the VCXO signal directly to Output 12 and Output 13 to serve as the power-up ready clocks.

Note that, throughout this data sheet, the dual function pin names are referenced by the relevant function where applicable.

Rev. C
Document Feedback

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- AD9528: JESD204B Clock Generator with 14 LVDS/HSTL Outputs Data Sheet

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SPECIFICATIONS

The AD9528 is configured for dual loop mode. The REFA differential input is enabled at 122.88 MHz, f_{VCXO} = 122.88 MHz and single-ended, f_{VCO} = 3686.4 MHz, VCO divider = 3. Doubler and analog delay are off, SYSREF generation is on, unless otherwise noted. Typical is given for VDDx = 3.3 V ± 5%, and T_A = 25°C, unless otherwise noted. Minimum and maximum values are given over the full VDDx and T_A (−40°C to +85°C) variation, as listed in Table 1.

CONDITIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
VDDx[1]	3.135	3.3	3.465	V	3.3 V ± 5%
TEMPERATURE					
Ambient Temperature Range, T_A	−40	+25	+85	°C	
Junction Temperature, T_J			+115	°C	Refer to the Power Dissipation and Thermal Considerations section to calculate the junction temperature

[1] VDDx includes the VDD pins (Pin 1, Pin 10, Pin 16, Pin 20, and Pin 72) and the VDD13 pin through the VDD0 pin, unless otherwise noted. See the Pin Configuration and Function Descriptions for details.

SUPPLY CURRENT

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT					Excludes clock distribution section; clock distribution outputs running as follows: 7 HSTL device clocks at 122.88 MHz, 7 LVDS SYSREF clocks (3.5 mA) at 960 kHz
Dual Loop Mode					PLL1 and PLL2 enabled
VDD (Pin 1, Pin 72)		19	21	mA	
VDD (Pin 10)		29	32	mA	
VDD (Pin 16)		34	37	mA	
VDD (Pin 20)		64	71	mA	
Single Loop Mode					PLL1 off and REFA and REFB inputs off
VDD (Pin 1, Pin 72)		7	9	mA	122.88 MHz reference source applied to the VCXO inputs (input to PLL2)
VDD (Pin 10)		29	32	mA	
VDD (Pin 16)		34	37	mA	
VDD (Pin 20)		64	71	mA	
Buffer Mode					PLL1 and PLL2 off, REFA and REFB inputs disabled; 122.88 MHz reference source applied to VCXO differential inputs to drive 7 of 14 outputs, internal SYSREF generator off, 960 kHz input source applied to SYSREF differential inputs to drive the other 7 outputs, dividers in clock distribution path bypassed in clock distribution channel
VDD (Pin 1, Pin 72)		17	19	mA	
VDD (Pin 10)		23	25	mA	
VDD (Pin 16)		2	3	mA	
VDD (Pin 20)		15	19	mA	
Chip Power-Down Mode					
VDD (Pin 1, Pin 10, Pin 16, Pin 20, and Pin 72)		15		mA	Chip power-down bit enabled (Register 0x0500, Bit 0 = 1)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT FOR EACH CLOCK DISTRIBUTION CHANNEL					Each clock output channel has a dedicated VDD pin. The current draw for each VDD pin includes the divider, fine delay, and output driver, fine delay is off; see the Pin Configuration and Function Descriptions section for pin assignment
LVDS Mode, 3.5 mA					
		21	23	mA	Output = 122.88 MHz, channel divider = 10
		24	26	mA	Output = 409.6 MHz, channel divider = 3
		28	30	mA	Output = 737.28 MHz, channel divider = 1, VCO divider = 5, LVDS boost mode of 4.5 mA recommended
LVDS Boost Mode, 4.5 mA					
		22	24	mA	Output = 122.88 MHz, channel divider =10
		25	27	mA	Output = 409.6 MHz, channel divider = 3
		29	31	mA	Output = 737.28 MHz, channel divider = 1, VCO divider = 5
HSTL Mode, 9 mA					
		25	27	mA	Output = 122.88 MHz, channel divider =10
		26	28	mA	Output = 409.6 MHz, channel divider = 3
		29	31	mA	Output = 983.04 MHz, channel divider = 1, VCO divider = 5, VCO = 3932.16 MHz
		37	41	mA	Output = 1228.8 MHz, channel divider = 1, only output channels OUT1 and OUT2 support output frequencies greater than ~1 GHz
Chip Power-Down Mode		2.5	4	mA	For each channel VDD pin, chip power-down bit enabled (Register 0x0500, Bit 0 = 1)

POWER DISSIPATION

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TOTAL POWER DISSIPATION					Does not include power dissipated in termination resistors
Typical Dual Loop Mode Configuration		1675	1780	mW	Differential REFA input at 122.88 MHz; f_{VCXO} = 122.88 MHz, f_{VCO} = 3686.4 MHz, VCO divider at 3 clock distribution outputs running as follows: 7 HSTL at 122.88 MHz, 7 LVDS (3.5 mA) at 960 kHz
Typical Single Loop Mode Configuration		1635	1810	mW	PLL1 off, differential VCXO input at 122.88 MHz, clock distribution outputs running as follows: 7 HSTL at 122.88 MHz, 7 LVDS (3.5 mA) at 960 kHz
Typical Buffer Mode		1030	1200	mW	PLL1 and PLL2 off, differential VCXO input at 122.88 MHz. SYSREF generator off, differential SYSREF input at 960 kHz; clock distribution outputs running as follows: 7 HSTL at 122.88 MHz, 7 LVDS (3.5 mA) at 960 kHz
Chip Power-Down Mode		65		mW	Chip power-down bit enabled (Register 0x0500, Bit 0 = 1)
$\overline{\text{RESET}}$ Enabled		1015	1200	mW	$\overline{\text{RESET}}$ pin low
INCREMENTAL POWER DISSIPATION					Does not include power dissipated in termination resistors
Low Power Base Configuration		590		mW	Dual loop mode, SYSREF generation and fine delay off; total power with 1 LVDS output running at 122.88 MHz, single-ended REFA at 122.88 MHz; REFB off, VCXO = 122.88 MHz, VCO = 3686.4 MHz
PLL1 OFF		0		mW	Define settings to power off PLL1
Output Distribution					Incremental power increase for each additional enable output
LVDS Mode, 3.5 mA		70		mW	Single 3.5 mA LVDS output at 122.88 MHz, channel divider = 10
		78		mW	Single 3.5 mA LVDS output at 409.6 MHz, channel divider = 3
		92		mW	Single 3.5 mA LVDS output at 737.28 MHz, VCO divider = 5, channel divider = 1
LVDS Mode, 4.5 mA		73		mW	Single 4.5 mA LVDS output at 122.88 MHz, channel divider = 10
		81		mW	Single 4.5 mA LVDS output at 409.6 MHz, channel divider = 3
		95		mW	Single 4.5 mA LVDS output at 737.28 MHz, VCO divider = 5

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL Mode, 9 mA		80		mW	Single 9 mA HSTL output at 122.88 MHz, channel divider = 10
		85		mW	Single 9 mA HSTL output at 409.6 MHz, channel divider = 3
		95		mW	Single 9 mA HSTL output at 983.04 MHz, VCO divider = 5, channel divider = 1
		125		mW	Single 9 mA HSTL output at 1228.8 MHz, channel divider = 1
REFA					
Differential On		72		mW	REFA and REFB running at 122.88 MHz, REF_SEL = REFB
Single-Ended		72		mW	REFA and REFB running at 122.88 MHz, REF_SEL = REFB
SYSREF Generator Enabled		5		mW	Single 3.5 mA LVDS output at 960 kHz
Fine Delay On		1		mW	Maximum delay setting

INPUT CHARACTERISTICS—REFA, $\overline{\text{REFA}}$, REFB, $\overline{\text{REFB}}$, VCXO_IN, $\overline{\text{VCXO\_IN}}$, SYSREF_IN, AND $\overline{\text{SYSREF\_IN}}$

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL MODE					
Input Frequency Range			400	MHz	
Input Frequency Range (VCXO_IN)			1250	MHz	For buffer mode
Input Slew Rate (VCXO_IN)	500			V/µs	Minimum limit imposed for jitter performance
Common-Mode Internally Generated Input Voltage	0.6	0.7	0.8	V	
Input Common-Mode Range	0.4		1.4	V	DC-coupled LVDS mode and HSTL mode supported
Differential Input Voltage, Sensitivity Frequency < 250 MHz	200			mV p-p	Can accommodate single-ended inputs via ac grounding of unused inputs; instantaneous voltage on either pin must not exceed 1.8 V dc
Differential Input Voltage, Sensitivity Frequency > 250 MHz	250			mV p-p	Can accommodate single-ended inputs via ac grounding of unused inputs; instantaneous voltage on either pin must not exceed 1.8 V dc
Differential Input Resistance		4.8		kΩ	
Differential Input Capacitance		4		pF	
Duty Cycle					Duty cycle limits are set by pulse width high and pulse width low
Pulse Width Low	1			ns	
Pulse Width High	1			ns	
CMOS MODE, SINGLE-ENDED INPUT					
Input Frequency Range			250	MHz	
Input High Voltage	1.4			V	
Input Low Voltage			0.65	V	
Input Capacitance		2		pF	
Duty Cycle					Duty cycle limits are set by pulse width high and pulse width low
Pulse Width Low	1.6			ns	
Pulse Width High	1.6			ns	

PLL1 CHARACTERISTICS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PFD FREQUENCY			110	MHz	
Charge Pump Current LSB Size		0.5		µA	7-bit resolution
Reference Frequency Detector Threshold	950			kHz	Do not use automatic holdover if the reference frequency is less than the minimum value

VCXO_VT OUTPUT CHARACTERISTICS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT VOLTAGE					
High	VDD − 0.15			V	R_{LOAD} > 20 kΩ
Low			150	mV	

PLL2 CHARACTERISTICS

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VCO (ON CHIP)					
Frequency Range	3450		4025	MHz	
Gain		48		MHz/V	
PLL2 FIGURE OF MERIT (FOM)		−226		dBc/Hz	
MAXIMUM PFD FREQUENCY			275	MHz	

CLOCK DISTRIBUTION OUTPUT CHARACTERISTICS

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL MODE					
Output Frequency			1000	MHz	All outputs
			1250	MHz	Outputs OUT1 and OUT2 only
Rise Time/Fall Time (20% to 80%)		60	160	ps	100 Ω termination across output pair
Duty Cycle					
f < 500 MHz	48	50	53	%	
f = 500 MHz to 800 MHz	46	51	54	%	
f = 800 MHz to 1.25 GHz	44	50	62	%	
f = 800 MHz to 1.25 GHz	50		57	%	If using PLL2
Differential Output Voltage Swing	900	1000	1100	mV	$V_{OH} - V_{OL}$ for each leg of a differential pair for default amplitude setting with the driver not toggling; the peak-to-peak amplitude measured using a differential probe across the differential pair with the driver toggling is roughly 2× these values (see Figure 5 for variation over frequency)
Common-Mode Output Voltage	0.88	0.9	0.94	V	
LVDS MODE, 3.5 mA					3.5 mA
Output Frequency			1000	MHz	All outputs
			1250	GHz	Outputs OUT1 and OUT2 only
Rise Time/Fall Time (20% to 80%)		50	216	ps	100 Ω termination across output pair
Duty Cycle					
f < 500 MHz	47	50	53	%	
f = 500 MHz to 800 MHz	46	51	54	%	
f = 800 MHz to 1.25 GHz	48	54	58	%	
Balanced, Differential Output Swing (VOD)	345		390	mV	Voltage swing between output pins; output driver static (see Figure 6 for variation over frequency)
Unbalanced, ΔVOD			3	mV	Absolute difference between voltage swing of normal pin and inverted pin; output driver static
Common-Mode Output Voltage	1.15		1.35	V	
Common-Mode Difference			1.2	mV	Voltage difference between output pins; output driver static
Short-Circuit Output Current		15	19	mA	Output driver static

OUTPUT TIMING ALIGNMENT CHARACTERISTICS

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT TIMING SKEW					Delay off on all outputs, maximum deviation between rising edges of outputs; all outputs are on and in HSTL mode, unless otherwise noted
PLL1 Outputs					
PLL1 to PLL1		17	100	ps	PLL1 clock to PLL1 clock
PLL1 to SYSREF		17	100	ps	SYSREF retimed by PLL1 clock
PLL1 to SYSREF		361	510	ps	SYSREF not retimed by any clock
PLL1 to SYSREF		253	1150	ps	SYSREF retimed by PLL2 clock
PLL1 to PLL2		257	1000	ps	PLL1 clock to PLL2 clock
PLL2 Outputs					
PLL2 to PLL2		20	165	ps	PLL2 clock to PLL2 clock
PLL2 to SYSREF		20	165	ps	SYSREF retimed by PLL2 clock
PLL2 to SYSREF		620	750	ps	SYSREF not retimed by any clock
PLL2 to SYSREF		253	1150	ps	SYSREF retimed by PLL1 clock
PLL2 to PLL1		257	1000	ps	PLL2 clock to PLL1 clock
OUTPUT DELAY ADJUST					Enables digital and analog delay capability
Coarse Adjustable Delay		32		Steps	Resolution step is the period of VCO RF divider (M1) output/2
Fine Adjustable Delay		15		Steps	Resolution step
Resolution Step		31		ps	
Insertion Delay		425		ps	Analog delay enabled and delay setting equal to zero

SYSREF_IN, $\overline{\text{SYSREF\_IN}}$, VCXO_IN, AND $\overline{\text{VCXO\_IN}}$ TIMING CHARACTERISTICS

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PROPAGATION LATENCY OF VCXO PATH	1.92	2.3	2.7	ns	VCXO input to device clock output, not retimed
PROPAGATION LATENCY OF SYSREF PATH	1.83	2.2	2.6	ns	SYSREF input to SYSREF output, not retimed
RETIMED WITH DEVICE CLOCK					
Setup Time of External SYSREF Relative to Device Clock Output	−1.13			ns	Given a SYSREF input clock rate equal to 122.88 MHz
Hold Time of External SYSREF Relative to Device Clock Output	0.7			ns	
RETIMED WITH VCXO					
Setup Time of External SYSREF Relative to VCXO Input	−0.21			ns	
Hold Time of External SYSREF Relative to VCXO	0.09			ns	

CLOCK OUTPUT ABSOLUTE PHASE NOISE—DUAL LOOP MODE

Application examples are based on a typical setups (see Table 2) using an external 122.88 MHz VCXO (Crystek CVHD-950); reference = 122.88 MHz; channel divider = 10 or 1; PLL2 loop bandwidth (LBW) = 450 kHz.

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL OUTPUT					
f_{OUT} = 122.88 MHz					
10 Hz Offset		−87		dBc/Hz	
100 Hz Offset		−106		dBc/Hz	
1 kHz Offset		−126		dBc/Hz	
10 kHz Offset		−135		dBc/Hz	
100 kHz Offset		−139		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
800 kHz Offset		−147		dBc/Hz	
1 MHz Offset		−149		dBc/Hz	
10 MHz Offset		−161		dBc/Hz	
40 MHz Offset		−162		dBc/Hz	
f_{OUT} = 1228.8 MHz					OUT1 and OUT2 only, channel divider = 1
10 Hz Offset		−62		dBc/Hz	
100 Hz Offset		−85		dBc/Hz	
1 kHz Offset		−106		dBc/Hz	
10 kHz Offset		−115		dBc/Hz	
100 kHz Offset		−119		dBc/Hz	
800 kHz Offset		−127		dBc/Hz	
1 MHz Offset		−129		dBc/Hz	
10 MHz Offset		−147		dBc/Hz	
100 MHz Offset		−153		dBc/Hz	
LVDS OUTPUT					
f_{OUT} = 122.88 MHz					
10 Hz Offset		−86		dBc/Hz	
100 Hz Offset		−106		dBc/Hz	
1 kHz Offset		−126		dBc/Hz	
10 kHz Offset		−135		dBc/Hz	
100 kHz Offset		−139		dBc/Hz	
800 kHz Offset		−147		dBc/Hz	
1 MHz Offset		−148		dBc/Hz	
10 MHz Offset		−157		dBc/Hz	
40 MHz Offset		−158		dBc/Hz	
f_{OUT} = 1228.8 MHz					OUT1 and OUT2 only, channel divider = 1
10 Hz Offset		−66		dBc/Hz	
100 Hz Offset		−86		dBc/Hz	
1 kHz Offset		−106		dBc/Hz	
10 kHz Offset		−115		dBc/Hz	
100 kHz Offset		−119		dBc/Hz	
800 kHz Offset		−127		dBc/Hz	
1 MHz Offset		−129		dBc/Hz	
10 MHz Offset		−147		dBc/Hz	
100 MHz Offset		−152		dBc/Hz	

CLOCK OUTPUT ABSOLUTE PHASE NOISE—SINGLE LOOP MODE

Single loop mode is based on the typical setup (see Table 2) using an external 122.88 MHz reference (SMA100A generator); reference = 122.88 MHz; channel divider = 10; PLL2 LBW = 450 kHz.

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL OUTPUT					
f_{OUT} = 122.88 MHz					
10 Hz Offset		−104		dBc/Hz	
100 Hz Offset		−113		dBc/Hz	
1 kHz Offset		−123		dBc/Hz	
10 kHz Offset		−135		dBc/Hz	
100 kHz Offset		−140		dBc/Hz	
800 kHz Offset		−147		dBc/Hz	
1 MHz Offset		−149		dBc/Hz	
10 MHz Offset		−161		dBc/Hz	
40 MHz Offset		−162		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
f_{OUT} = 1228.8 MHz					OUT1 and OUT2 only, channel divider = 1
10 Hz Offset		−85		dBc/Hz	
100 Hz Offset		−95		dBc/Hz	
1 kHz Offset		−103		dBc/Hz	
10 kHz Offset		−114		dBc/Hz	
100 kHz Offset		−120		dBc/Hz	
800 kHz Offset		−126		dBc/Hz	
1 MHz Offset		−128		dBc/Hz	
10 MHz Offset		−147		dBc/Hz	
100 MHz Offset		−153		dBc/Hz	
LVDS OUTPUT					
f_{OUT} = 122.88 MHz					
10 Hz Offset		−111		dBc/Hz	
100 Hz Offset		−113		dBc/Hz	
1 kHz Offset		−123		dBc/Hz	
10 kHz Offset		−135		dBc/Hz	
100 kHz Offset		−140		dBc/Hz	
800 kHz Offset		−147		dBc/Hz	
1 MHz Offset		−148		dBc/Hz	
10 MHz Offset		−157		dBc/Hz	
40 MHz Offset		−157		dBc/Hz	
f_{OUT} = 1228.8 MHz					OUT1 and OUT2 only, channel divider = 1
10 Hz Offset		−85		dBc/Hz	
100 Hz Offset		−95		dBc/Hz	
1 kHz Offset		−103		dBc/Hz	
10 kHz Offset		−114		dBc/Hz	
100 kHz Offset		−120		dBc/Hz	
800 kHz Offset		−126		dBc/Hz	
1 MHz Offset		−128		dBc/Hz	
10 MHz Offset		−146		dBc/Hz	
100 MHz Offset		−152		dBc/Hz	

CLOCK OUTPUT ABSOLUTE TIME JITTER

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT ABSOLUTE RMS TIME JITTER					Application examples are based on typical setups (see Table 2) using an external 122.88 MHz VCXO (Crystek CVHD-950); reference = 122.88 MHz; channel divider = 10 or 1; PLL2 LBW = 450 kHz
Dual Loop Mode					
HSTL Output		117		fs	Integrated BW = 200 kHz to 5 MHz
f_{OUT} = 122.88 MHz		123		fs	Integrated BW = 200 kHz to 10 MHz
		159		fs	Integrated BW = 12 kHz to 20 MHz
		172		fs	Integrated BW = 10 kHz to 40 MHz
		177		fs	Integrated BW = 1 kHz to 40 MHz
		109		fs	Integrated BW = 1 MHz to 40 MHz
f_{OUT} = 1228.8 MHz, Channel Divider = 1		114		fs	Integrated BW = 200 kHz to 5 MHz
		116		fs	Integrated BW = 200 kHz to 10 MHz
		147		fs	Integrated BW = 12 kHz to 20 MHz
		154		fs	Integrated BW = 10 kHz to 100 MHz
		160		fs	Integrated BW = 1 kHz to 100 MHz
		74		fs	Integrated BW = 1 MHz to 100 MHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS Output		124		fs	Integrated BW = 200 kHz to 5 MHz
f_{OUT} = 122.88 MHz		136		fs	Integrated BW = 200 kHz to 10 MHz
		179		fs	Integrated BW = 12 kHz to 20 MHz
		209		fs	Integrated BW = 10 kHz to 40 MHz
		213		fs	Integrated BW = 1 kHz to 40 MHz
		160		fs	Integrated BW = 1 MHz to 40 MHz
f_{OUT} = 1228.8 MHz, Channel Divider = 1		116		fs	Integrated BW = 200 kHz to 5 MHz
		118		fs	Integrated BW = 200 kHz to 10 MHz
		150		fs	Integrated BW = 12 kHz to 20 MHz
		157		fs	Integrated BW = 10 kHz to 100 MHz
		163		fs	Integrated BW = 1 kHz to 100 MHz
		76		fs	Integrated BW = 1 MHz to 100 MHz
Single Loop Mode					
HSTL Output		115		fs	Integrated BW = 200 kHz to 5 MHz
f_{OUT} = 122.88 MHz		122		fs	Integrated BW = 200 kHz to 10 MHz
		156		fs	Integrated BW = 12 kHz to 20 MHz
		171		fs	Integrated BW = 10 kHz to 40 MHz
		179		fs	Integrated BW = 1 kHz to 40 MHz
		110		fs	Integrated BW = 1 MHz to 40 MHz
f_{OUT} = 1228.8 MHz, Channel Divider = 1		116		fs	Integrated BW = 200 kHz to 5 MHz
		118		fs	Integrated BW = 200 kHz to 10 MHz
		146		fs	Integrated BW = 12 kHz to 20 MHz
		153		fs	Integrated BW = 10 kHz to 100 MHz
		163		fs	Integrated BW = 1 kHz to 100 MHz
		81		fs	Integrated BW = 1 MHz to 100 MHz
LVDS Output		123		fs	Integrated BW = 200 kHz to 5 MHz
f_{OUT} = 122.88 MHz		135		fs	Integrated BW = 200 kHz to 10 MHz
		177		fs	Integrated BW = 12 kHz to 20 MHz
		207		fs	Integrated BW = 10 kHz to 40 MHz
		214		fs	Integrated BW = 1 kHz to 40 MHz
		160		fs	Integrated BW = 1 MHz to 40 MHz
f_{OUT} = 1228.8 MHz, Channel Divider = 1		117		fs	Integrated BW = 200 kHz to 5 MHz
		119		fs	Integrated BW = 200 kHz to 10 MHz
		147		fs	Integrated BW = 12 kHz to 20 MHz
		155		fs	Integrated BW = 10 kHz to 100 MHz
		164		fs	Integrated BW = 1 kHz to 100 MHz
		83		fs	Integrated BW = 1 MHz to 100 MHz

CLOCK OUTPUT ADDITIVE TIME JITTER (BUFFER MODE)

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT ADDITIVE RMS TIME JITTER					Application examples are based on typical performance (see Table 2) using an external 122.88 MHz source driving VCXO inputs (distribution section only, does not include PLL and VCO)
Buffer Mode					
HSTL Output		66		fs	Integrated BW = 200 kHz to 5 MHz
f_{OUT} = 122.88 MHz		81		fs	Integrated BW = 200 kHz to 10 MHz
		112		fs	Integrated BW = 12 kHz to 20 MHz
		145		fs	Integrated BW = 10 kHz to 40 MHz
		146		fs	Integrated BW = 1 kHz to 40 MHz
		132		fs	Integrated BW = 1 MHz to 40 MHz
LVDS Output		79		fs	Integrated BW = 200 kHz to 5 MHz
f_{OUT} = 122.88 MHz		101		fs	Integrated BW = 200 kHz to 10 MHz
		140		fs	Integrated BW = 12 kHz to 20 MHz
		187		fs	Integrated BW = 10 kHz to 40 MHz
		189		fs	Integrated BW = 1 kHz to 40 MHz
		176		fs	Integrated BW = 1 MHz to 40 MHz

LOGIC INPUT PINS—$\overline{\text{RESET}}$, REF_SEL, AND SYSREF_REQ

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE					
Input High	1.3			V	
Input Low			0.6	V	
INPUT LOW CURRENT		13	14	µA	
CAPACITANCE		4		pF	
$\overline{\text{RESET}}$ TIMING					
Pulse Width Low	1.0			ns	
Inactive to Start of Register Programming	2.5			ns	

STATUS OUTPUT PINS—STATUS0 AND STATUS1

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT VOLTAGE					
High	3			V	
Low			0.02	V	

SERIAL CONTROL PORT—SERIAL PORT INTERFACE (SPI) MODE

Table 17.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{CS}$ (INPUT)						$\overline{CS}$ has an internal 40 kΩ pull-up resistor
Voltage						
Input Logic 1			1.37		V	
Input Logic 0			1.33		V	
Current						
Input Logic 1			−52		µA	
Input Logic 0			−82		µA	
Input Capacitance			2		pF	
SCLK (INPUT) IN SPI MODE						SCLK has an internal 40 kΩ pull-down resistor in SPI mode but not in I^2C mode
Voltage						
Input Logic 1			1.76		V	
Input Logic 0			1.22		V	
Current						
Input Logic 1			0.0037		µA	
Input Logic 0			0.0012		µA	
Input Capacitance			2		pF	
SDIO						Input is in bidirectional mode
Voltage						
Input Logic 1			1.76		V	
Input Logic 0			1.22		V	
Current						
Input Logic 1			0.0037		µA	
Input Logic 0			0.0012		µA	
Input Capacitance			3.5		pF	
SDIO, SDO (OUTPUTS)						
Voltage						
Output Logic 1		3.11			V	
Output Logic 0				0.0018	V	
TIMING						
Clock Rate (SCLK, $1/t_{SCLK}$)				50	MHz	
Pulse Width High	t_{HIGH}	4			ns	
Pulse Width Low	t_{LOW}	2			ns	
SDIO to SCLK Setup	t_{DS}	2.2			ns	
SCLK to SDIO Hold	t_{DH}	−0.9			ns	
SCLK to Valid SDIO and SDO	t_{DV}			6	ns	
$\overline{CS}$ to SCLK Setup	t_S	1.25			ns	
$\overline{CS}$ to SCLK Hold	t_C	0			ns	
$\overline{CS}$ Minimum Pulse Width High	t_{PWH}	0.9			ns	

SERIAL CONTROL PORT—I²C MODE

Table 18.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SDA, SCL VOLTAGE						When inputting data
Input Logic 1		0.7 × VDD			V	
Input Logic 0				0.3 × VDD	V	
Input Current		−10		+10	µA	Input voltage between 0.1 × VDD and 0.9 × VDD
Hysteresis of Schmitt Trigger Inputs		0.015 × VDD			V	
SDA						When outputting data
Output Logic 0 Voltage at 3 mA Sink Current				0.2	V	
Output Fall Time from VIH_{MIN} to VIL_{MAX}		20 + 0.1 C_B[1]		250	ns	Bus capacitance from 10 pF to 400 pF
TIMING						All I²C timing values are referred to VIH_{MIN} (0.3 × VDD) and VIL_{MAX} levels (0.7 × VDD)
Clock Rate (SCL, f_{I2C})				400	kHz	
Bus Free Time Between a Stop and Start Condition	t_{IDLE}	1.3			µs	
Setup Time for a Repeated Start Condition	$t_{SET;\ STR}$	0.6			µs	
Hold Time (Repeated) Start Condition	$t_{HLD;\ STR}$	0.6			µs	After this period, the first clock pulse is generated
Setup Time for a Stop Condition	$t_{SET;\ STP}$	0.6			µs	
Low Period of the SCL Clock	t_{LOW}	1.3			µs	
High Period of the SCL Clock	t_{HIGH}	0.6			µs	
SCL, SDA Rise Time	t_{RISE}	20 + 0.1 C_B[1]		300	ns	
SCL, SDA Fall Time	t_{FALL}	20 + 0.1 C_B[1]		300	ns	
Data Setup Time	$t_{SET;\ DAT}$	100			ns	
Data Hold Time	$t_{HLD;\ DAT}$	0			ns	
Capacitive Load for Each Bus Line	C_B[1]			400	pF	

[1] C_B is the capacitance of one bus line in picofarads (pF).

ABSOLUTE MAXIMUM RATINGS

Table 19.

Parameter	Rating
VDD	−0.3 V to +3.6 V
REFA, $\overline{\text{REFA}}$, REFB, $\overline{\text{REFB}}$, VCXO_IN, $\overline{\text{VCXO\_IN}}$, SYSREF_IN, $\overline{\text{SYSREF\_IN}}$, SYSREF_REQ to GND	−0.3 V to +3.6 V
SCLK/SCL, SDIO/SDA, SDO, $\overline{\text{CS}}$ to GND	−0.3 V to +3.6 V
$\overline{\text{RESET}}$, REF_SEL, SYSREF_REQ to GND	−0.3 V to +3.6 V
STATUS0/SP0, STATUS1/SP1 to GND	−0.3 V to +3.6 V
Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 20. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JC}[1, 3]	θ_{JB}[1, 4]	Ψ_{JT}[1, 2]	Unit
72-Lead LFCSP, 10 mm × 10 mm	0	21.3	1.7	12.6	0.1	°C/W
	1.0	20.1			0.2	°C/W
	2.5	18.1			0.3	°C/W

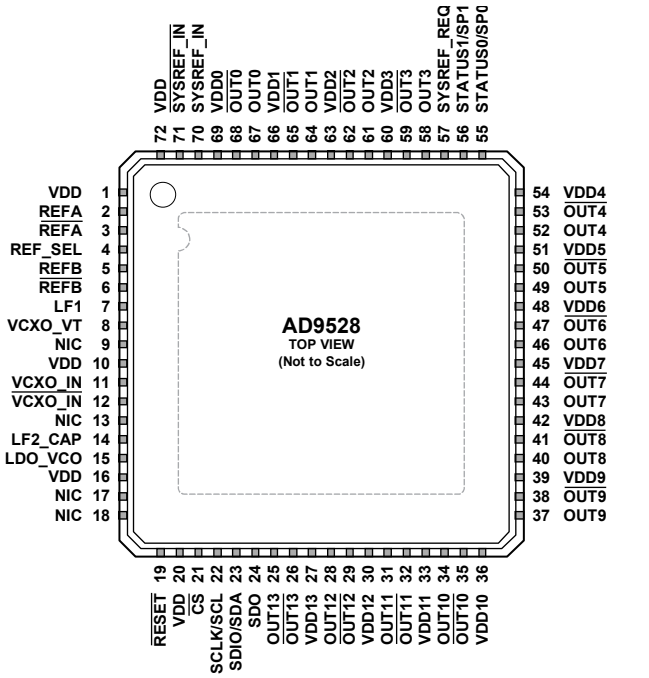
[1] Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Additional power dissipation information can be found in the Power Dissipation and Thermal Considerations section.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NO INTERNAL CONNECTION. THIS PIN CAN BE LEFT FLOATING.
2. THE EXPOSED PAD IS THE GROUND CONNECTION ON THE CHIP. IT MUST BE SOLDERED TO THE ANALOG GROUND OF THE PCB TO ENSURE PROPER FUNCTIONALITY AND HEAT DISSIPATION, NOISE, AND MECHANICAL STRENGTH BENEFITS.

12380-002

Figure 2. Pin Configuration

Table 21. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	VDD	P	3.3 V Supply for the PLL1 Input Section.
2	REFA	I	Reference Clock Input A. Along with $\overline{\text{REFA}}$, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
3	$\overline{\text{REFA}}$	I	Complementary Reference Clock Input A. Along with REFA, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
4	REF_SEL	I	Reference Input Select. The reference input selection function defaults to software control via internal Register 0x010A, Bits[2:0]. When the REF_SEL pin is active, a logic low selects REFA and logic high selects REFB.
5	REFB	I	Reference Clock Input B. Along with $\overline{\text{REFB}}$, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
6	$\overline{\text{REFB}}$	I	Complementary Reference Clock Input B. Along with REFB, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
7	LF1	O	PLL1 External Loop Filter.
8	VCXO_VT	O	VCXO Control Voltage. Connect this pin to the voltage control pin of the external VCXO.
9	NIC	NIC	No Internal Connection. The pin can be left floating.
10	VDD	P	3.3 V Supply for the PLL2 Section.
11	VCXO_IN	I	PLL1 Oscillator Input. Along with $\overline{\text{VCXO\_IN}}$, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
12	$\overline{\text{VCXO\_IN}}$	I	Complementary PLL1 Oscillator Input. Along with VCXO_IN, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
13	NIC	NIC	No Internal Connection. The pin can be left floating.
14	LF2_CAP	O	PLL2 External Loop Filter Capacitor Connection. Connect capacitor between this pin and the LDO_VCO pin.

Pin No.	Mnemonic	Type[1]	Description
15	LDO_VCO	P/O	2.5 V LDO Internal Regulator Decoupling for the VCO. Connect a 0.47 µF decoupling capacitor from this pin to ground. Note that, for best performance, the LDO bypass capacitor must be placed in close proximity to the device.
16	VDD	P	3.3 V Supply for the PLL2 Internal Regulator.
17	NIC	NIC	No Internal Connection. The pin can be left floating.
18	NIC	NIC	No Internal Connection. The pin can be left floating.
19	$\overline{\text{RESET}}$	I	Digital Input, Active Low. Resets internal logic to default states.
20	VDD	P	3.3 V Supply for the PLL2 Internal Regulator.
21	$\overline{\text{CS}}$		Serial Control Port Chip Select, Active Low. This pin has an internal 30 kΩ pull-up resistor.
22	SCLK/SCL	I	Serial Control Port Clock Signal for SPI Mode (SCLK) or I²C Mode (SCL). Data clock for serial programming.
23	SDIO/SDA	I/O	Serial Control Port Bidirectional Serial Data In/Data Out for SPI Mode (SDIO) or I²C Mode (SDA).
24	SDO	O	Serial Data Output. Use this pin to read data in 4-wire mode (high impedance in 3-wire mode). There is no internal pull-up or pull-down resistor on this pin.
25	OUT13	O	Square Wave Clocking Output 13.
26	$\overline{\text{OUT13}}$	O	Complementary Square Wave Clocking Output 13.
27	VDD13	P	3.3 V Supply for the Output 13 Clock Driver.
28	OUT12	O	Square Wave Clocking Output 12.
29	$\overline{\text{OUT12}}$	O	Complementary Square Wave Clocking Output 12.
30	VDD12	P	3.3 V Supply for the Output 12 Clock Divider.
31	OUT11	O	Square Wave Clocking Output 11.
32	$\overline{\text{OUT11}}$	O	Complementary Square Wave Clocking Output 11.
33	VDD11	P	3.3 V Supply for the Output 11 Clock Driver.
34	OUT10	O	Square Wave Clocking Output 10.
35	$\overline{\text{OUT10}}$	O	Complementary Square Wave Clocking Output 10.
36	VDD10	P	3.3 V Supply for the Output 10 Clock Divider.
37	OUT9	O	Square Wave Clocking Output 9.
38	$\overline{\text{OUT9}}$	O	Complementary Square Wave Clocking Output 9.
39	VDD9	P	3.3 V Supply for the Output 9 Clock Driver.
40	OUT8	O	Square Wave Clocking Output 8.
41	$\overline{\text{OUT8}}$	O	Complementary Square Wave Clocking Output 8.
42	VDD8	P	3.3 V Supply for the Output 8 Clock Divider.
43	OUT7	O	Square Wave Clocking Output 7.
44	$\overline{\text{OUT7}}$	O	Complementary Square Wave Clocking Output 7.
45	VDD7	P	3.3 V Supply for the Output 7 Clock Driver.
46	OUT6	O	Square Wave Clocking Output 6.
47	$\overline{\text{OUT6}}$	O	Complementary Square Wave Clocking Output 6.
48	VDD6	P	3.3 V Supply for the Output 6 Clock Divider.
49	OUT5	O	Square Wave Clocking Output 5.
50	$\overline{\text{OUT5}}$	O	Complementary Square Wave Clocking Output 5.
51	VDD5	P	3.3 V Supply for the Output 5 Clock Driver.
52	OUT4	O	Square Wave Clocking Output 4.
53	$\overline{\text{OUT4}}$	O	Complementary Square Wave Clocking Output 4.
54	VDD4	P	3.3 V Supply for the Output 4 Clock Divider.
55	STATUS0/SP0	I/O	Lock Detect and Other Status Signals/I²C Address. This pin has an internal 30 kΩ pull-down resistor.
56	STATUS1/SP1	I/O	Lock Detect and Other Status Signals/I²C Address. This pin has an internal 30 kΩ pull-down resistor.
57	SYSREF_REQ	I	SYSREF Request Input Logic Control.
58	OUT3	O	Square Wave Clocking Output 3.
59	$\overline{\text{OUT3}}$	O	Complementary Square Wave Clocking Output 3.
60	VDD3	P	3.3 V Supply for the Output 3 Clock Driver.
61	OUT2	O	Square Wave Clocking Output 2. High speed output up to 1.25 GHz.
62	$\overline{\text{OUT2}}$	O	Complementary Square Wave Clocking Output 2. High speed output up to 1.25 GHz.
63	VDD2	P	3.3 V Supply for the Output 2 Clock Divider.

Pin No.	Mnemonic	Type[1]	Description
64	OUT1	O	Square Wave Clocking Output 1. High speed output up to 1.25 GHz.
65	$\overline{\text{OUT1}}$	O	Complementary Square Wave Clocking Output 1. High speed output up to 1.25 GHz.
66	VDD1	P	3.3 V Supply for the Output 1 Clock Driver.
67	OUT0	O	Square Wave Clocking Output 0.
68	$\overline{\text{OUT0}}$	O	Complementary Square Wave Clocking Output 0.
69	VDD0	P	3.3 V Supply for the Output 0 Clock Divider.
70	SYSREF_IN	I	External SYSREF Input Clock. Along with $\overline{\text{SYSREF\_IN}}$, this pin is the differential input for an external SYSREF signal. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
71	$\overline{\text{SYSREF\_IN}}$	I	Complementary External SYSREF Input Clock. Along with SYSREF_IN, this pin is the differential input for an external SYSREF signal. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
72	VDD	P	3.3 V Supply for the PLL1 Input Section.
EP	EP, GND	GND	Exposed Pad. The exposed pad is the ground connection on the chip. It must be soldered to the analog ground of the printed circuit board (PCB) to ensure proper functionality and heat dissipation, noise, and mechanical strength benefits.

[1] P means power, I means input, O means output, I/O means input/output, P/O means power/output, and GND means ground.

TYPICAL PERFORMANCE CHARACTERISTICS

f_{VCXO} = 122.88 MHz, REFA differential at 122.88 MHz, f_{VCO} = 3686.4 MHz, and doubler is off, unless otherwise noted. External PLL1 loop filter component values are as follows: R_{ZERO} = 10 kΩ, C_{ZERO} = 1 µF, C_{POLE} = 200 pF. External PLL2 external capacitor C_{ZERO} = 1 nF. PLL1 charge pump = 5 µA and PLL2 charge pump = 805 µA.

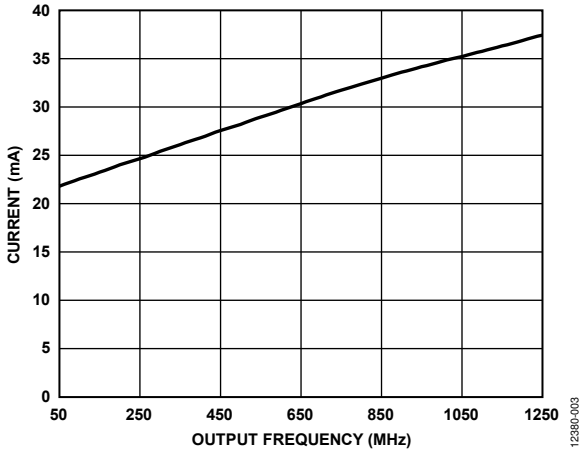


Figure 3. VDDx Current (Typical) vs. Output Frequency, HSTL Mode

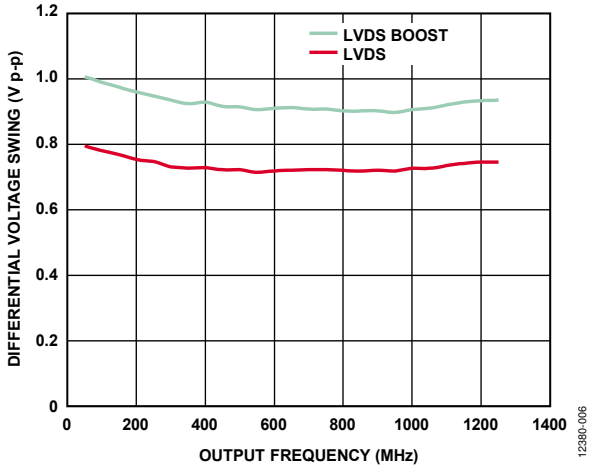


Figure 6. Differential Voltage Swing vs. Output Frequency, LVDS Mode and LVDS Boost Mode

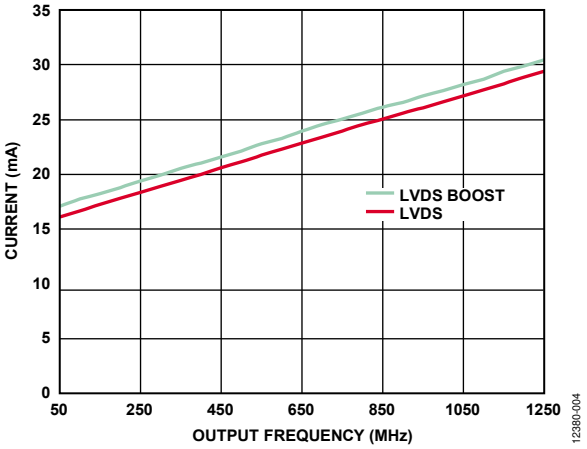


Figure 4. VDDx Current (Typical) vs. Output Frequency, LVDS Mode and LVDS Boost Mode

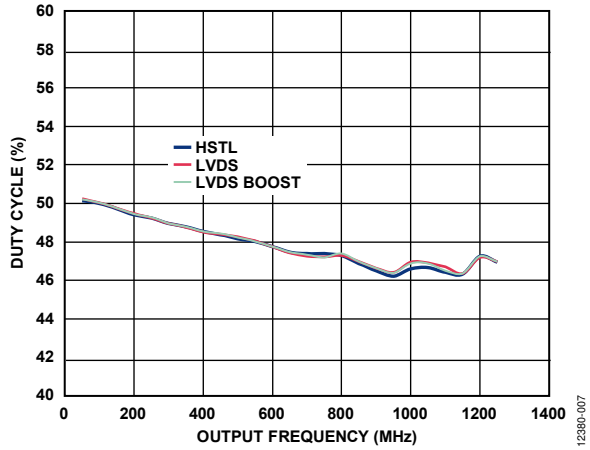


Figure 7. Positive Duty Cycle vs. Output Frequency, HSTL, LVDS, and LVDS Boost Modes

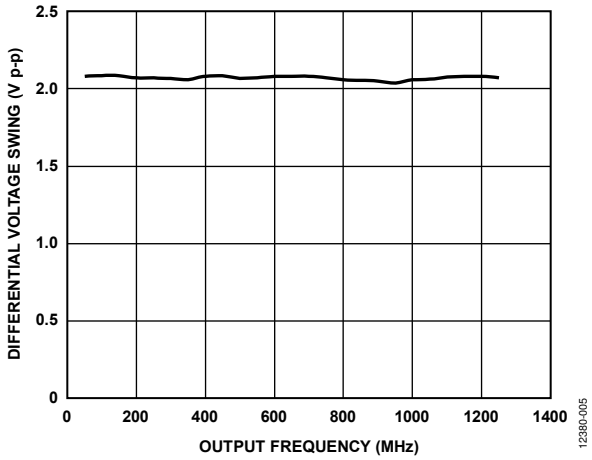


Figure 5. Differential Voltage Swing vs. Output Frequency, HSTL Mode

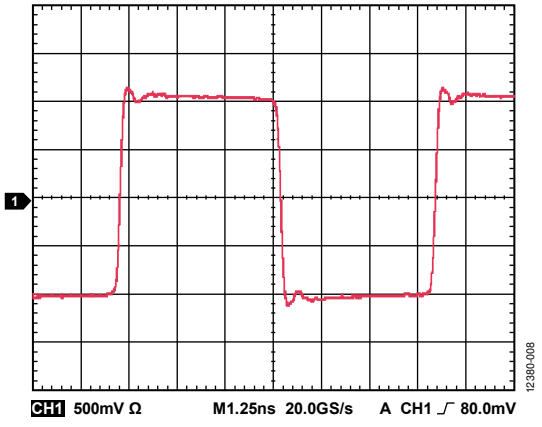


Figure 8. Output Waveform (Differential), HSTL at 122.88 MHz

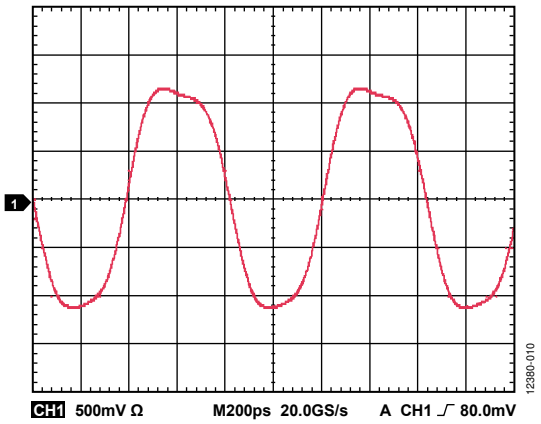


Figure 9. Output Waveform (Differential), HSTL at 1228.8 MHz

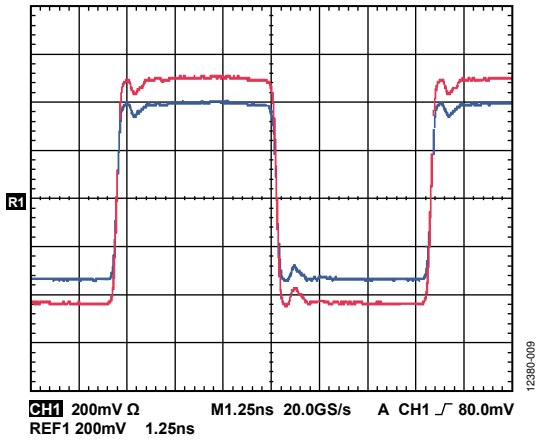


Figure 10. Output Waveform (Differential), LVDS and LVDS Boost Mode at 122.88 MHz

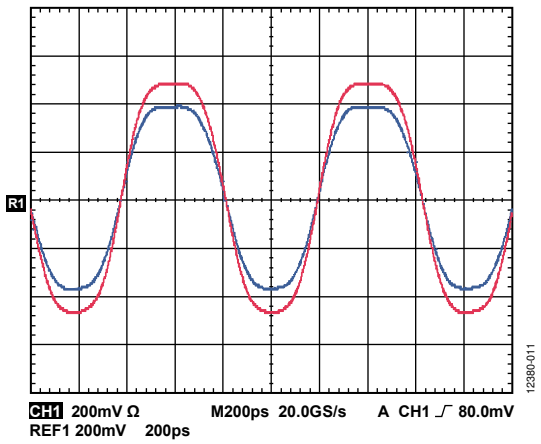


Figure 11. Output Waveform (Differential), LVDS and LVDS Boost Mode at 1228.8 MHz

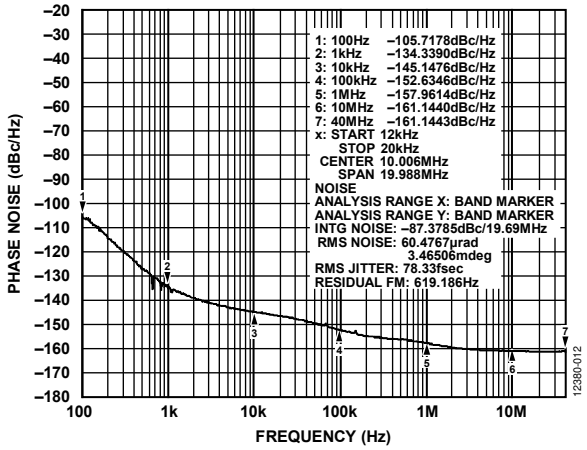


Figure 12. Phase Noise, Output = 122.88 MHz, HSTL Mode, PLL1 Output Sent Directly to Clock Distribution, PLL2 Off (VCXO = 122.88 MHz, Crystek VCXO CVHD-950)

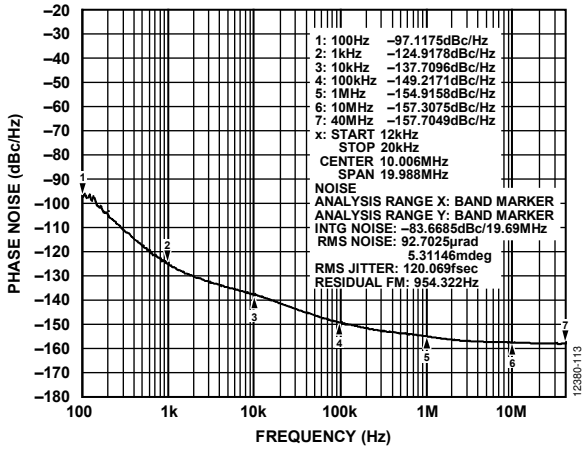


Figure 13. Phase Noise, Output = 122.88 MHz, HSTL Mode, PLL1 Output Sent Directly to Clock Distribution, PLL2 Off (VCXO = 122.88 MHz, TAITEN VCXO (A0145-0-011-3)

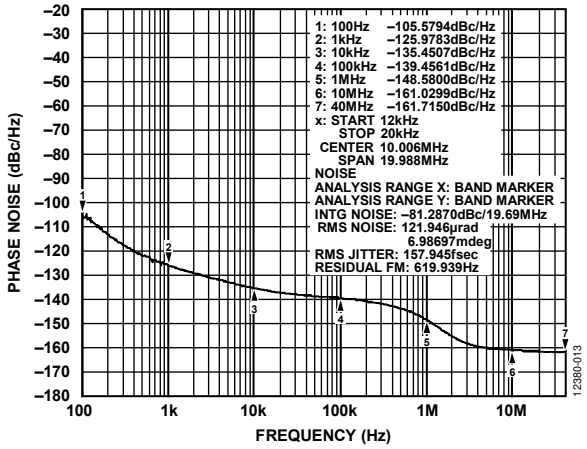


Figure 14. Phase Noise, Output = 122.88 MHz, HSTL Mode, Dual Loop Mode (VCXO = 122.88 MHz, Crystek VCXO CVHD-950, VCO = 3686.4 MHz)

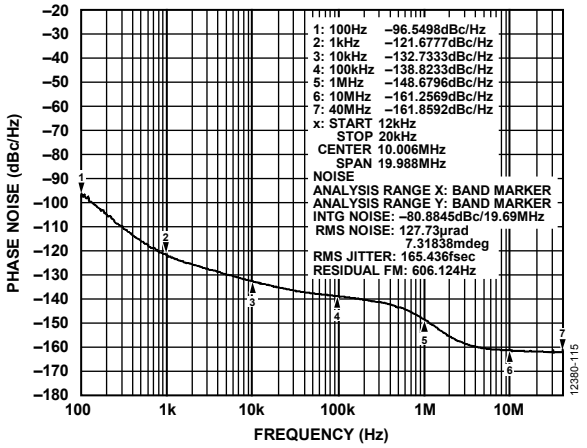


Figure 15. Phase Noise, Output = 122.88 MHz, HSTL Mode, Dual Loop Mode (VCXO = 122.88 MHz, TAITEN VCXO (A0145-0-011-3), VCO = 3686.4 MHz)

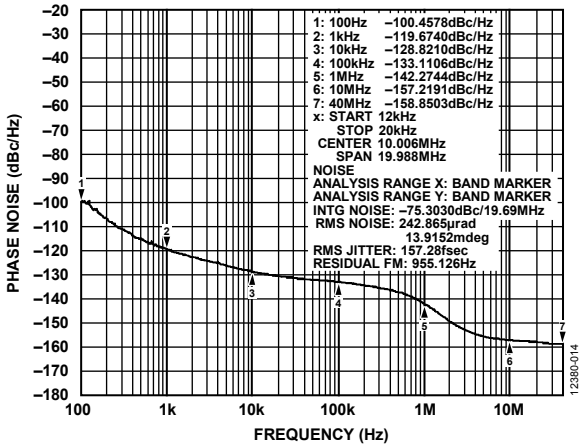


Figure 16. Phase Noise, Output = 245.76 MHz, HSTL Mode, Dual Loop Mode (VCXO = 122.88 MHz, Crystek VCXO CVHD-950, VCO = 3686.4 MHz)

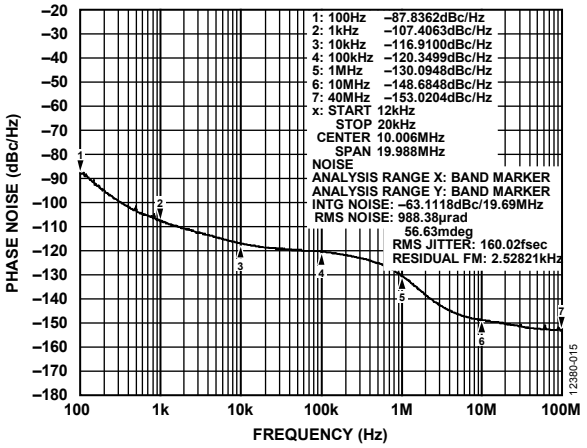


Figure 17. Phase Noise, Output = 983.04 MHz, HSTL Mode, Dual Loop Mode (VCXO = 122.88 MHz, Crystek VCXO CVHD-950, VCO = 3932.16 MHz)

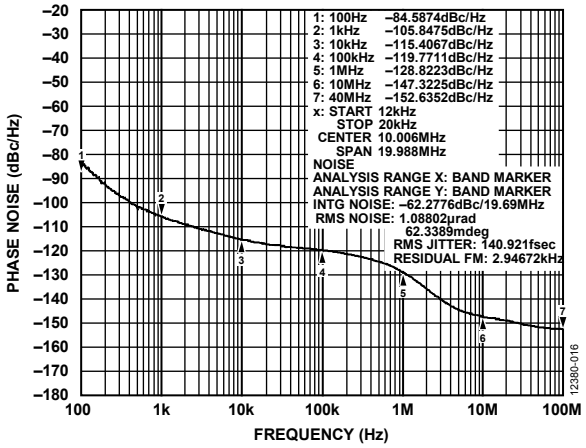


Figure 18. Phase Noise, Output = 1228.8 MHz, HSTL Mode, Dual Loop Mode (VCXO = 122.88 MHz, Crystek VCXO CVHD-950, VCO = 3686.4 MHz)

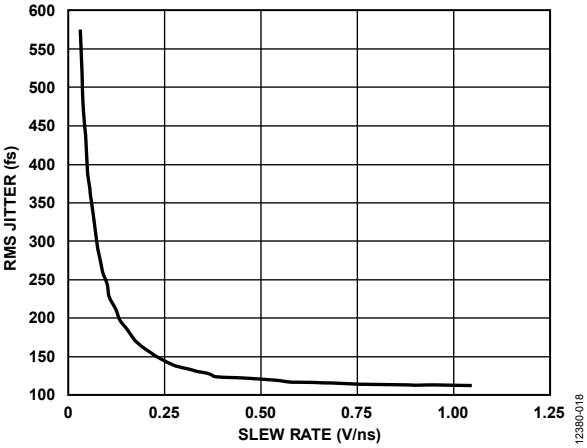


Figure 19. RMS Jitter in Buffer Mode with Both PLL1 and PLL2 Off vs. Slew Rate; Input Applied to the VCXO Input and Output Taken from Clock Distribution, Phase Noise Integration Range from 12 kHz to 20 MHz to Derive Jitter Number

INPUT/OUTPUT TERMINATION RECOMMENDATIONS

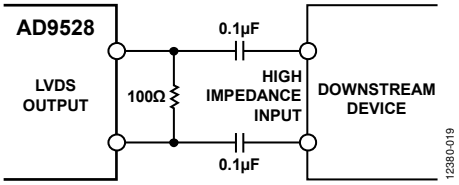


Figure 20. AC-Coupled LVDS Output Driver

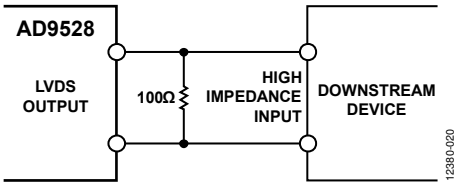


Figure 21. DC-Coupled LVDS Output Driver

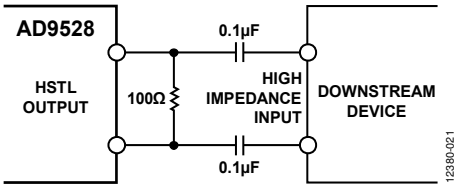


Figure 22. AC-Coupled HSTL Output Driver

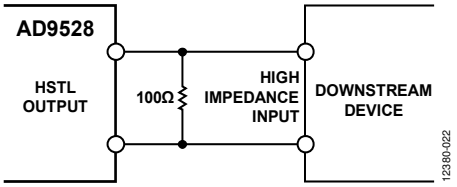


Figure 23. DC-Coupled HSTL Output Driver

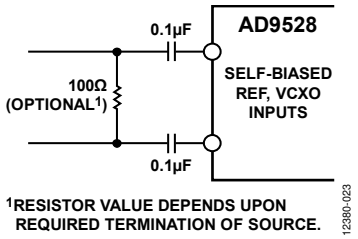


Figure 24. REFx, VCXO Input Differential Mode Receiver

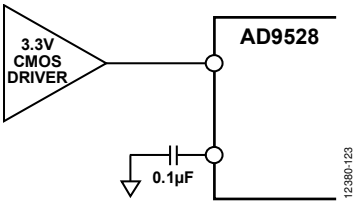


Figure 25. REFx, VCXO Input, Single-Ended Mode Receiver

TYPICAL APPLICATION CIRCUIT

The AD9528 is capable of synchronizing multiple devices designed to the JESD204B JEDEC standard. Figure 26 illustrates the AD9528 synchronizing to the system reference clock. The AD9528 first jitter cleans the system reference clock and multiples up to a higher frequency in dual loop mode. The clock distribution of the AD9528 is used to clock and synchronize all the surrounding JESD204B devices together in the system.

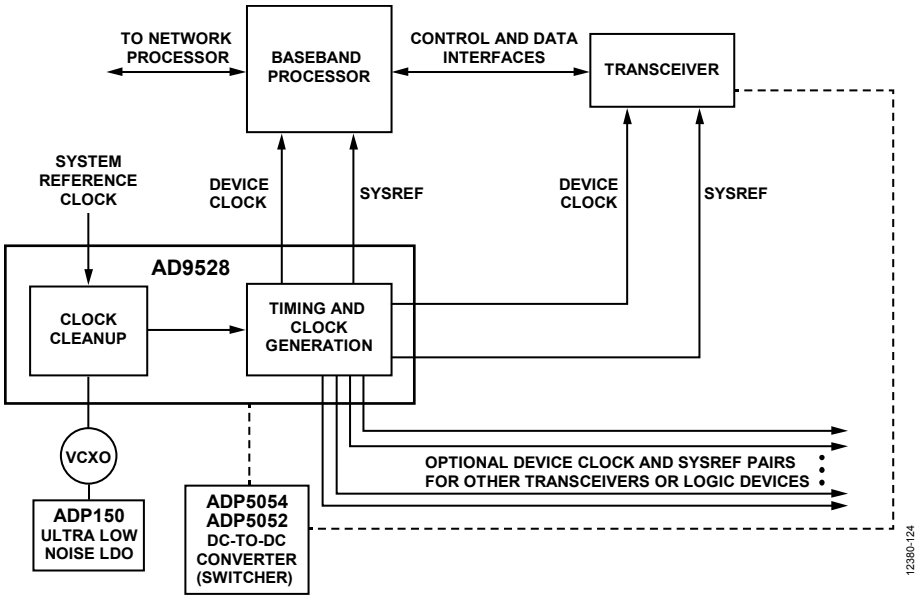


Figure 26. Synchronizing Multiple JESD204B Devices

TERMINOLOGY

Phase Jitter

An ideal sine wave has a continuous and even progression of phase with time from 0° to 360° for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time. This phenomenon is called phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, which is characterized statistically as being Gaussian (normal) in distribution.

Phase jitter leads to a spreading out of the energy of the sine wave in the frequency domain, producing a continuous power spectrum. This power spectrum is usually reported as a series of values with the units dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in decibels) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

In some applications, it is meaningful to integrate only the total power contained within some interval of offset frequencies (for example, 10 kHz to 10 MHz). This is called the integrated phase noise over that frequency offset interval and can be readily related to the time jitter due to the phase noise within that offset frequency interval.

Phase Noise

Phase noise has a detrimental effect on the performance of analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and radio frequency (RF) mixers. It lowers the achievable dynamic range of the converters and mixers, although they are affected in somewhat different ways.

Time Jitter

Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings varies. In a square wave, the time jitter is a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in seconds root mean square (rms) or 1 sigma of the Gaussian distribution.

Time jitter that occurs on a sampling clock for a DAC or an ADC decreases the SNR and dynamic range of the converter. A sampling clock with the lowest possible jitter provides the highest performance from a given converter.

Additive Phase Noise

Additive phase noise is the amount of phase noise that is attributable to the device or subsystem being measured. The phase noise of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device impacts the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contributes its own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise. When there are multiple contributors to phase noise, the total is the square root of the sum of squares of the individual contributors.

Additive Time Jitter

Additive time jitter is the amount of time jitter that is attributable to the device or subsystem being measured. The time jitter of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device impacts the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contributes its own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.