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4 CML Output, Low Jitter Clock Generator with an Integrated 5.4 GHz VCO

Data Sheet

AD9530

FEATURES

Fully integrated, ultralow noise phase-locked loop (PLL)
4 differential, 2.7 GHz common-mode logic (CML) outputs
2 differential reference inputs with programmable internal termination options
<232 fs rms absolute jitter (12 kHz to 20 MHz) with a non-ideal reference and 8 kHz loop bandwidth
<100 fs rms absolute jitter (12 kHz to 20 MHz) with an 80 kHz loop bandwidth and low jitter input reference clock
Supports low loop bandwidths for jitter attenuation
Manual switchover
Single 2.5 V typical supply voltage
48-lead, 7 mm × 7 mm LFCSP

APPLICATIONS

40 Gbps/100 Gbps optical transport network (OTN) line side clocking
Clocking of high speed analog-to-digital converters (ADCs) and digital-to-analog converters (DACs)
Data communications

GENERAL DESCRIPTION

The AD9530 is a fully integrated PLL and distribution supporting, clock cleanup, and frequency translation device for 40 Gbps/ 100 Gbps OTN applications. The internal PLL can lock to one of two reference frequencies to generate four discrete output frequencies up to 2.7 GHz.

The AD9530 features an internal 5.11 GHz to 5.4 GHz, ultralow noise voltage controlled oscillator (VCO). All four outputs are individually divided down from the internal VCO using two high speed VCO dividers (the Mx dividers) and four individual 8-bit channel dividers (the Dx dividers). The high speed VCO dividers offer fixed divisions of 2, 2.5, 3, and 3.5 for wide coverage of possible output frequencies. The AD9530 is configurable for loop bandwidths <15 kHz to attenuate reference noise.

The AD9530 is available in a 48-lead LFCSP and operates from a single 2.5 V typical supply voltage.

The AD9530 operates over the extended industrial temperature range of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

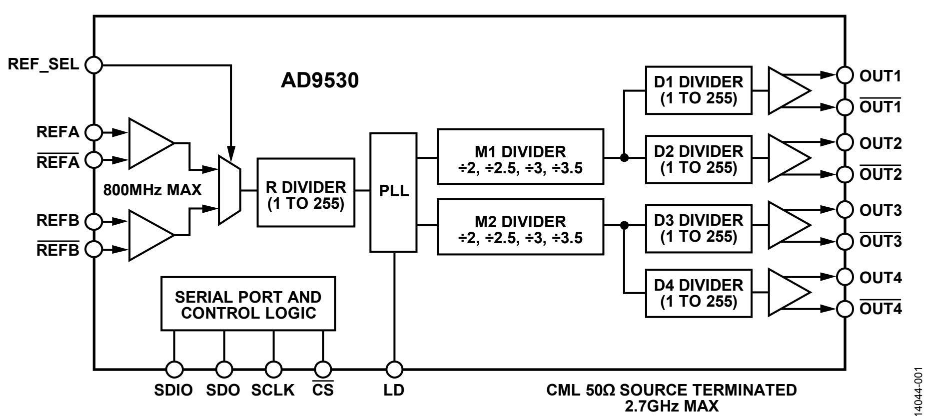

Figure 1.

Rev. 0 Document Feedback

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DOCUMENTATION

Data Sheet

- AD9530: 4 CML Output, Low Jitter Clock Generator with an Integrated 5.4 GHz VCO Data Sheet

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- AD9530 Material Declaration
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REVISION HISTORY

4/16—Revision 0: Initial Version

SPECIFICATIONS

Typical values are given for V_{DD} = 2.5 V ± 5%, T_A = 25°C, unless otherwise noted. Minimum and maximum values are given over the full V_{DD} range and T_A (−40°C to +85°C) variations listed in Table 1.

SUPPLY VOLTAGE AND TEMPERATURE RANGE SPECIFICATIONS

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE	V_{DD}	2.375	2.5	2.625	V	2.5 V ± 5%
TEMPERATURE						
Ambient Temperature Range	T_A	−40	+25	+85	°C	
Junction Temperature[1]	T_J			115	°C	

[1] The is the maximum junction temperature for which device performance is guaranteed. Note that the Absolute Maximum Ratings section may have a higher maximum junction temperature, but device operation or performance is not guaranteed above the number that appears here. To calculate the junction temperature, see the Power Dissipation and Thermal Considerations section.

SUPPLY CURRENT SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT OTHER THAN CLOCK THE DISTRIBUTION CHANNEL					Current listed in the Typ column is at nominal V_{DD} at 25°C; current listed in the Max column is at maximum V_{DD} and worst case temperature
Typical Operation 1					f_{RTWO} = 5300.16 MHz; VCO mode = low power; REFA enabled at 110.42 MHz; REFB disabled; R divider = 1; M1 and M3 divider = 3; M2 divider = powered down; phase frequency detector (PFD) = 110.42 MHz; OUT1 CML output at 1766.72 MHz; OUT2, OUT3, and OUT4 outputs and dividers powered down; single-ended output swing level = 800 mV; outputs terminated externally with 50 Ω to V_{DD}
Reference Input VDD (Pin 3 and Pin 7)		8.2	10.7	mA	Combined current of Pin 3 and Pin 7
PLL VDD (Pin 12)		18.2	24	mA	
Rotary Travelling Wave Oscillator (RTWO) VDD (Pin 20 to Pin 23)		747	860	mA	Combined current of Pin 20 to Pin 23
SUPPLY CURRENT FOR AN INDIVIDUAL CLOCK DISTRIBUTION CHANNEL					Each output channel has a dedicated VDD pin; all current values are listed for a single driver supply pin operating at 1766.72 MHz; output terminated externally, 50 Ω to VDD; these specifications include the current required for the external load resistors
CML					
Internal Termination Disabled					
800 mV		28.8	35.5	mA	
900 mV		30.7	37.6	mA	
1000 mV		32.6	39.8	mA	
1100 mV		34.5	41.8	mA	
Internal Termination Enabled					
800 mV		47.6	57.2	mA	
900 mV		51.5	61.5	mA	
1000 mV		55.3	65.8	mA	
1100 mV		59.0	70.1	mA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT DELTAS, INDIVIDUAL FUNCTIONS					Current delta when a function is enabled/disabled from Typical Operation 1
VCO High Performance Mode Enabled		133.5	160.0	mA	Current increase when the VCO mode is changed from low power mode to high performance mode; combined current delta of Pin 20 to Pin 23
REFx/$\overline{\text{REFx}}$ Receiver[1]		2.5	3.3	mA	Current increase when REFB is enabled with a 110.42 MHz reference input; combined current delta of Pin 3 and Pin 7
Reference Divider	−0.55	−0.39		mA	Delta from bypassing reference divider to using reference divider = 2; total feedback division doubled to preserve lock; combined current delta of Pin 3 and Pin 7
Output Channel		28.4	33.3	mA	One output channel enabled by powering up M2 divider = 3; D3 and D4 divider = 1; OUT3 and OUT4 enabled to 800 mV; no internal termination; associated low-dropout regulators (LDOs) enabled; includes the current required by the external termination; both outputs at 1766.72 MHz
Mx Divider On/Off		33.2	36.2	mA	This is the current consumption delta between an Mx (where x is 0, 1, or 2) divider powered up and powered down; these dividers are a part of the RTWO VDD (Pin 20 to Pin 23) power domain
Single Output Plus Associated Channel Divider (OUT1: Pin 31, OUT2: Pin 35, OUT3: Pin 41, OUT4: Pin 45)		28.4	33.4	mA	One output driver enabled by powering up the driver and channel divider (does not include power on the extra M2 divider); includes the current required by the external termination; output = 1766.72 MHz

[1] Where x is either A or B.

POWER DISSIPATION SPECIFICATIONS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TOTAL POWER DISSIPATION					Does not include power dissipated in external resistors; all CML outputs terminated with 50 Ω to VDD; internal output termination is disabled; output amplitude set to 1.0 V; reference inputs set to ac-coupled mode
Power-On Default		2.284	2.750	W	
Power-Down Mode		0.338	0.480	W	
Typical Operation 2		2.344	2.82	W	f_{RTWO} = 5302.5 MHz; VCO mode = high performance; REFA enabled at 101 MHz, ac-coupled; REFB disabled; R divider = 1; M1 divider and M3 divider = 2.5; PFD = 101 MHz; OUT1 and OUT2 CML outputs at 2121 MHz; OUT3 and OUT4 disabled; output swing level = 800 mV; outputs terminated externally to 50 Ω to VDD and internal termination disabled; M2 divider and LDO powered down; D3 and D4 dividers and associated LDOs disabled
All Blocks Running					f_{RTWO} = 5400 MHz; VCO mode = high performance; REFA and REFB enabled at 100 MHz; ac-coupled mode; R divider = 1; M divider = 2; PFD = 100 MHz; four CML outputs at 2700 MHz
800 mV Output Swing, Without Internal Output Termination		2.536	3.02	W	Single-ended output swing level = 800 mV and internal termination off
1100 mV Output Swing with Internal Output Termination		2.796	3.326	W	Single-ended output swing level = 1100 mV and internal termination on

REFA/$\overline{REFA}$ AND REFB/$\overline{REFB}$ INPUT CHARACTERISTICS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC-COUPLED LVDS MODE (REFA, $\overline{REFA}$; REFB, $\overline{REFB}$)					DC-coupled LVDS mode (REFx_TERM_SEL = 00); includes an internal 100 Ω differential termination; inputs are not self biased in this setting
Input Frequency	6		800	MHz	Assumes a minimum of 494 mV p-p differential amplitude as measured with a differential probe at the REFx input pins
Input Sensitivity	494			mV p-p	Peak-to-peak differential voltage swing across the pins to ensure switching between logic levels as measured with a differential probe
Common-Mode Input Voltage	0.4		1.4	V	Allowable common-mode voltage for dc coupling
Differential Input Resistance		110		Ω	Differential input resistance measured across the REFx and $\overline{REFx}$ pins
Input Capacitance		3		pF	Input capacitance measured from each REFx pin to GND
DC-COUPLED CML MODE (REFA, $\overline{REFA}$, REFB, $\overline{REFB}$)					DC-coupled (REFx_TERM_SEL = 01); includes an internal termination of 50 Ω from each REFx input to GND; inputs are not self biased in this setting
Input Frequency	6		800	MHz	Assumes a minimum of 494 mV p-p differential amplitude as measured with a differential probe at the REFx input pins
Input Sensitivity	494			mV p-p	Peak-to-peak differential voltage swing across pins to ensure switching between logic levels as measured with a differential probe
Common-Mode Input Voltage	0.3		0.4	V	Allowable common-mode voltage for dc coupling
Single-Ended Input Resistance		55		Ω	Input resistance measured from each REFx pin to GND
Input Capacitance		3		pF	Input capacitance measured from each REFx pin to GND
AC-COUPLED CML MODE (REFA, $\overline{REFA}$, REFB, $\overline{REFB}$)					AC-coupled mode (REFx_TERM_SEL = 10); includes an internal termination of 50 Ω from each REFx input to a nominal dc bias of 0.35 V
Input Frequency	6		800	MHz	Assumes a minimum of 494 mV p-p differential amplitude as measured with a differential probe at the REFx input pins
Input Sensitivity	494			mV p-p	Peak-to-peak differential voltage swing across pins to ensure switching between logic levels as measured with a differential probe
Input Self Bias Voltage (VTT) (Internally Generated)	0.32	0.355	0.39	V	Self bias voltage of the REFx and $\overline{REFx}$ inputs in ac-coupled mode (REFx_TERM_SEL = 10)
Differential Input Resistance		105		Ω	Differential input resistance measured across the REFx and $\overline{REFx}$ pins
Input Capacitance		3		pF	Input capacitance measured from each REFx pin to GND
DC-COUPLED HIGH-Z MODE (REFA, $\overline{REFA}$, REFB, $\overline{REFB}$)					DC-coupled high-Z mode (REFx_TERM_SEL = 11) places the REFx inputs into a high impedance state; inputs are not self biased in this setting
Input Frequency	6		800	MHz	Assumes a minimum of 500 mV p-p differential amplitude as measured with a differential probe at the REFx input pins
Input Sensitivity	494			mV p-p	Peak-to-peak differential voltage swing across pins to ensure switching between logic levels as measured with a differential probe
Common-Mode Input Voltage	0.4		1.4	V	
Differential Input Resistance		10.3		kΩ	Differential input resistance measured across the REFx and $\overline{REFx}$ pins
Input Capacitance		3		pF	Input capacitance measured from each REFx pin to GND

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DUTY CYCLE					Duty cycle bounds are set by pulse width high and pulse width low
Pulse Width					
Low	600			ps	
High	600			ps	

PLL CHARACTERISTICS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RTWO					
Frequency Range	5.11		5.4	GHz	
VCO Gain (K_{VCO})		180		MHz/V	
PHASE FREQUENCY DETECTOR (PFD)					
PFD Input Frequency	6		800	MHz	Antibacklash pulse width disabled (Register 0x026, Bit 1 = 0)
	6		500	MHz	Antibacklash pulse width enabled (Register 0x026, Bit 1 = 1)
CHARGE PUMP (CP)					
Sink/Source Current (I_{CP})	0.05		2.6	mA	Register 0x025, Bits[5:0] controls the charge pump current (see Table 56)
LOOP FILTER					
External Loop Filter Capacitor			3.2	µF	Maximum value for the C2 capacitor in Figure 16; using a loop filter capacitor value larger than the maximum may affect device functionality
POWER-ON RESET (POR) TIMER					
Internal Wait Time	2			sec	Minimum wait time implemented before issuing the first RTWO calibration after a POR

PLL DIGITAL LOCK DETECT SPECIFICATIONS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PLL DIGITAL LOCK DETECT WINDOW[1]					Signal available at the LD pin and in Register 0x01F, Bit 2
Lock Threshold	±0.020		±300	ppm	Lock threshold is selected by Register 0x01D, Bits[3:1], which is the threshold for transitioning from unlock to lock and vice versa

[1] For reliable operation of the digital lock detect, the period of the PFD frequency must be greater than the lock detector update interval (see Table 48).

CLOCK OUTPUTS (INTERNAL TERMINATION DISABLED) SPECIFICATIONS

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CML MODE					All outputs are externally terminated with 50 Ω to VDD
800 mV					
Output Frequency	5.725		2700	MHz	
Rise Time/Fall Time (20% to 80%)		78	107	ps	
Duty Cycle	47		53	%	Any Mx divider, output divider ≠ 1
	48	51	54	%	Mx divider = 2, output divider = 1
	45	51	57	%	Mx divider = 2.5, output divider = 1
	48	50	53	%	Mx divider = 3, output divider = 1
Output Differential Voltage, Magnitude	600	845	1090	mV	Voltage difference between the output pins; output driver is static; in normal operation, the peak-to-peak amplitude is approximately 2× this value if measured with a differential probe
Common-Mode Output Voltage	1.82	2.075	2.32	V	Measured with output driver static

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
900 mV					All outputs are externally terminated with 50 Ω to VDD
Output Frequency	5.725		2700	MHz	
Rise Time/Fall Time (20% to 80%)		77	98	ps	
Duty Cycle	47		53	%	Any Mx divider, output divider ≠ 1
	48	51	54	%	Mx divider = 2, output divider = 1
	45	51	57	%	Mx divider = 2.5, output divider = 1
	49	51	53	%	Mx divider = 3, output divider = 1
Output Differential Voltage, Magnitude	675	950	1340	mV	Voltage difference between the output pins; output driver is static; in normal operation, the peak-to-peak amplitude is approximately 2× this value if measured with a differential probe
Common-Mode Output Voltage	1.76	2.03	2.29	V	Measured with output driver static
1000 mV					All outputs are externally terminated with 50 Ω to VDD
Output Frequency	5.725		2700	MHz	
Rise Time/Fall Time (20% to 80%)		76	105	ps	
Duty Cycle	47		53	%	Any Mx divider, output divider ≠ 1
	48	51	54	%	Mx divider = 2, output divider = 1
	45	51	57	%	Mx divider = 2.5, output divider = 1
	49	51	52	%	Mx divider = 3, output divider = 1
Output Differential Voltage, Magnitude	730	1040	1340	mV	Voltage difference between the output pins; output driver is static; in normal operation, the peak-to-peak amplitude is approximately 2× this value if measured with a differential probe
Common-Mode Output Voltage	1.69	1.97	2.25	V	
1100 mV					All outputs are externally terminated with 50 Ω to VDD
Output Frequency	5.725		2700	MHz	
Rise Time/Fall Time (20% to 80%)		76	104	ps	
Duty Cycle	47		53	%	Any Mx divider, output divider ≠ 1
	48	51	54	%	Mx divider = 2, output divider = 1
	45	51	57	%	Mx divider = 2.5, output divider = 1
	49	50	52	%	Mx divider = 3, output divider = 1
Output Differential Voltage, Magnitude	815	1140	1480	mV	Voltage difference between the output pins; output driver is static; in normal operation, the peak-to-peak amplitude is approximately 2× this value if measured with a differential probe
Common-Mode Output Voltage	1.61	1.92	2.22	V	Measured with output driver static

CLOCK OUTPUTS (INTERNAL TERMINATION ENABLED) SPECIFICATIONS

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CML MODE					All outputs are externally terminated with 50 Ω to VDD
800 mV					
Output Frequency	5.725		2700	MHz	
Rise Time/Fall Time (20% to 80%)		55	75	ps	
Duty Cycle	47		53	%	Any Mx divider, output divider ≠ 1
	48	52	56	%	Mx divider = 2, output divider = 1
	43	51	60	%	Mx divider = 2.5, output divider = 1
	48	51	53	%	Mx divider = 3, output divider = 1
Output Differential Voltage, Magnitude	590	830	1070	mV	Voltage difference between the output pins; output driver is static; in normal operation, the peak-to-peak amplitude is approximately 2× this value if measured with a differential probe
Common-Mode Output Voltage	1.9	2.08	2.26	V	Measured with output driver static

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
900 mV					All outputs are externally terminated with 50 Ω to VDD
Output Frequency	5.725		2700	MHz	
Rise Time/Fall Time (20% to 80%)		53	70	ps	
Duty Cycle	47		53	%	Any Mx divider, output divider ≠ 1
	48	52	56	%	Mx divider = 2, output divider = 1
	43	51	60	%	Mx divider = 2.5, output divider = 1
	48	51	53	%	Mx divider = 3, output divider = 1
Output Differential Voltage, Magnitude	660	930	1200	mV	Voltage difference between the output pins; output driver is static; in normal operation, the peak-to-peak amplitude is approximately 2× this value if measured with a differential probe
Common-Mode Output Voltage	1.83	2.03	2.23	V	Measured with output driver static
1000 mV					All outputs are externally terminated with 50 Ω to VDD
Output Frequency	5.725		2700	MHz	
Rise Time/Fall Time (20% to 80%)		53	71	ps	
Duty Cycle	47		53	%	Any Mx divider, output divider ≠ 1
	47	52	56	%	Mx divider = 2, output divider = 1
	43	52	60	%	Mx divider = 2.5, output divider = 1
	48	51	53	%	Mx divider = 3, output divider = 1
Output Differential Voltage, Magnitude	735	1025	1335	mV	Voltage difference between the output pins; output driver is static; in normal operation, the peak-to-peak amplitude is approximately 2× this value if measured with a differential probe
Common-Mode Output Voltage	1.83	2.03	2.23	V	Measured with output driver static
1100 mV					All outputs are externally terminated with 50 Ω to VDD
Output Frequency	5.725		2700	MHz	
Rise Time/Fall Time (20% to 80%)		53	72	ps	
Duty Cycle	47		53	%	Any Mx divider, output divider ≠ 1
	47	52	56	%	Mx divider = 2, output divider = 1
	43	52	60	%	Mx divider = 2.5, output divider = 1
	48	51	54	%	Mx divider = 3, output divider = 1
Output Differential Voltage, Magnitude	810	1125	1455	mV	Voltage difference between the output pins; output driver is static; in normal operation, the peak-to-peak amplitude is approximately 2× this value if measured with a differential probe
Common-Mode Output Voltage	1.71	1.93	2.23	V	Measured with output driver static
INTERNAL OUTPUT TERMINATION RESISTANCE		53.7		Ω	Measured with output driver static

CLOCK OUTPUT ABSOLUTE TIME JITTER (LOW LOOP BANDWIDTH) SPECIFICATIONS

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CML OUTPUT ABSOLUTE TIME JITTER					REFA enabled and ac-coupled; R divider = 1; Mx divider value varies; loop bandwidth = 8 kHz; output divider bypassed unless otherwise noted; single-ended output swing level = 1000 mV; no internal termination; VCO in high power mode, integration bandwidth = 12 kHz to 20 MHz
f_{OUT} = 2700 MHz		219		fs rms	Reference frequency = 100 MHz, Mx divider = 2
f_{OUT} = 2100 MHz		220		fs rms	Reference frequency = 100 MHz, Mx divider = 2.5
f_{OUT} = 2050 MHz		214		fs rms	Reference frequency = 102.5 MHz, Mx divider = 2.5
f_{OUT} = 1768 MHz		219		fs rms	Reference frequency = 104 MHz, Mx divider = 3
f_{OUT} = 1500 MHz		210		fs rms	Reference frequency = 100 MHz, Mx divider = 3.5
f_{OUT} = 100 MHz		232		fs rms	Reference frequency = 100 MHz, Mx divider = 3, output divider (Dx divider) = 17

CLOCK OUTPUT ABSOLUTE TIME JITTER (HIGH LOOP BANDWIDTH) SPECIFICATIONS

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CML OUTPUT ABSOLUTE TIME JITTER		93		fs rms	REFA enabled and ac-coupled; R divider = 1; Mx divider value = 2; loop bandwidth = 80 kHz; output divider bypassed; single-ended output swing level = 1000 mV; no internal termination; VCO in high power mode; reference frequency = 860 MHz; output frequency = 2.58 GHz; integration bandwidth = 12 kHz to 20 MHz; absolute jitter value also depends on the noise of the input clock in the 12 kHz to 80 kHz range

$\overline{\text{RESET}}$ AND REF_SEL PINS SPECIFICATIONS

Table 11.

Parameter	Min	Typ	Max	Unit
INPUT CHARACTERISTICS				
Voltage				
Logic 1	V_{DD} − 0.5		V_{DD}	V
Logic 0			0.5	V
Current				
Logic 1		1		µA
Logic 0		36		µA
Capacitance		3		pF
RESET TIMING				
Pulse Width Low	100			ns
$\overline{\text{RESET}}$ Inactive to Start of Register Programming	50			ms

LD PIN SPECIFICATIONS

Table 12.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS						1 mA output load
Output Voltage						
High	V_{OH}	V_{DD} − 0.5			V	
Low	V_{OL}			0.5	V	

SERIAL CONTROL PORT SPECIFICATIONS

Table 13.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{\text{CS}}$ (INPUT)						$\overline{\text{CS}}$ has an internal 75 kΩ pull-up resistor
Input Voltage						
Logic 1		V_{DD} − 0.4			V	
Logic 0				0.4	V	
Input Current						
Logic 1			1		µA	
Logic 0			32		µA	
Input Capacitance			3		pF	
SCLK (INPUT)						SCLK has an internal 75 kΩ pull-down resistor
Input Voltage						
Logic 1		V_{DD} − 0.4			V	
Logic 0				0.4	V	
Input Current						
Logic 1			45		µA	
Logic 0			1		µA	
Input Capacitance			3		pF	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SDIO (INPUT)						
Input Voltage						
Logic 1		V_{DD} − 0.4			V	
Logic 0				0.4	V	
Input Current						
Logic 1			1		µA	
Logic 0			1		µA	
Input Capacitance			3		pF	
SDIO, SDO (OUTPUTS)						1 mA load current
Output Voltage						
Logic 1		V_{DD} − 0.2			V	
Logic 0				0.2	V	
TIMING						See Figure 26 through Figure 30 and Table 21
Clock Rate (SCLK)	$1/t_{SCLK}$			40	MHz	
Pulse Width High	t_{HIGH}	6			ns	
Pulse Width Low	t_{LOW}	6			ns	
SDIO to SCLK Setup	t_{DS}	1.8			ns	
SCLK to SDIO Hold	t_{DH}	0.6			ns	
SCLK to Valid SDIO and SDO	t_{DV}			10	ns	
$\overline{CS}$ to SCLK Setup	t_S	0.6			ns	
$\overline{CS}$ to SCLK Hold	t_H	3.5			ns	
$\overline{CS}$ Minimum Pulse Width High	t_{PWH}	1.5			ns	

ABSOLUTE MAXIMUM RATINGS

Table 14.

Parameter	Rating
VDD, BP_CAP_1, BP_CAP_2, BP_CAP_3, REFA, $\overline{\text{REFA}}$, REFB, $\overline{\text{REFB}}$, SCLK, SDIO, SDO, $\overline{\text{CS}}$, OUT1, $\overline{\text{OUT1}}$, OUT2, $\overline{\text{OUT2}}$, OUT3, $\overline{\text{OUT3}}$, OUT4, $\overline{\text{OUT4}}$, $\overline{\text{RESET}}$, and REF_SEL to GND	2.625 V
Junction Temperature[1]	150°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (10 sec)	300°C

[1] See Table 15 for θ_{JA}.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

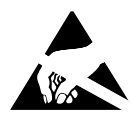
THERMAL RESISTANCE

Table 15. Thermal Resistance (Simulated)

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1,2]	θ_{JC}[1,3,4]	θ_{JB}[1,4,5]	Ψ_{JT}[1,2,4]	Unit
48-Lead LFCSP	0	25.8	2.8	7.5	0.20	°C/W
	1.0	22.2	N/A	N/A	N/A	°C/W
	2.5	19.7	N/A	N/A	N/A	°C/W

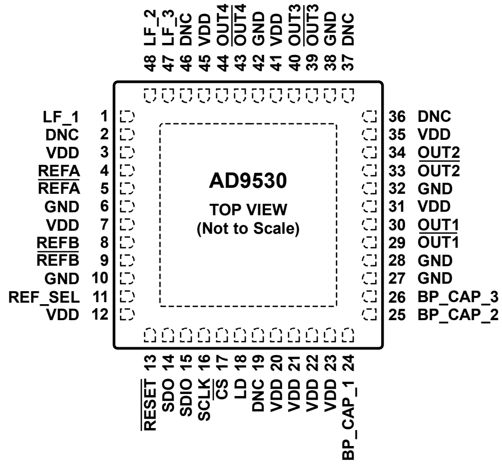
[1] Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] N/A means not applicable.
[5] Per JEDEC JESD51-8 (still air).

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THESE PINS.
2. THE EXPOSED PAD IS A GROUND CONNECTION ON THE CHIP THAT MUST BE SOLDERED TO THE ANALOG GROUND OF THE PCB TO ENSURE PROPER FUNCTIONALITY AND HEAT DISSIPATION, NOISE, AND MECHANICAL STRENGTH BENEFITS.

14044-003

Figure 2. Pin Configuration

Table 16. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	LF_1	O	Loop Filter Connection, Negative Output Side of the Active Loop Filter Op Amp. Connect the PLL active loop filter components (R1, C1, and C2) to this pin and LF_2 (Pin 48).
2, 19, 36, 37, 46	DNC	N/A	Do Not Connect. Do not connect to this pin.
3	VDD	P	Power Supply for REFA.
4	REFA	I	Reference Clock Input A. This pin, along with $\overline{\text{REFA}}$, is the first differential reference input for the PLL.
5	$\overline{\text{REFA}}$	I	Complimentary Reference Clock Input A. This pin, along with REFA, is the first differential reference input for the PLL.
6	GND	GND	Ground for the REFA Power Supply. Connect this pin to ground.
7	VDD	P	Power Supply for REFB.
8	REFB	I	Reference Clock Input B. This pin, along with $\overline{\text{REFB}}$, is the second differential reference input for the PLL.
9	$\overline{\text{REFB}}$	I	Complimentary Reference Clock Input B. This pin, along with REFB, is the second differential reference input for the PLL.
10	GND	GND	Ground for the REFB Power Supply. Connect this pin to ground.
11	REF_SEL	I	Reference Input Select. This pin is the digital input to select REFA or REFB as the active reference to the PLL. This pin has an internal 75 kΩ pull-up resistor. Logic high (default) selects REFA. Logic low selects REFB.
12	VDD	P	Power Supply for the Serial Port Interface (SPI) and the PFD.
13	$\overline{\text{RESET}}$	I	Chip Reset, Active Low. This pin has an internal 75 kΩ pull-up resistor.
14	SDO	O	Serial Control Port Unidirectional Serial Data Output. This pin is high impedance during 3-wire SPI mode.
15	SDIO	I/O	Serial Control Port Bidirectional Serial Data Input/Output.
16	SCLK	I	Serial Control Port Clock Signal. This pin has an internal 75 kΩ pull-down resistor.
17	$\overline{\text{CS}}$	I	Serial Control Port Chip Select, Active Low. This pin has an internal 75 kΩ pull-up resistor.
18	LD	O	PLL Lock Detect Output.
20 to 23	VDD	P	2.5 V Power Supply for the RTWO Internal LDO.
24	BP_CAP_1	O	RTWO LDO Op Amp Bypass Capacitor. Connect an external 0.01 µF capacitor from this pin to GND.
25	BP_CAP_2	O	RTWO LDO Bypass Capacitor. Connect an external 1 µF capacitor from this pin to GND.
26	BP_CAP_3	O	RTWO Bias Supply Bypass Capacitor. This pin can be left unconnected (floating).
27	GND	GND	Ground for RTWO Power Supply. Connect this pin to ground.
28	GND	GND	Ground for OUT1 Power Supply. Connect this pin to ground.

Pin No.	Mnemonic	Type[1]	Description
29	$\overline{\text{OUT1}}$	O	CML Complementary Output 1. This pin requires a 50 Ω to VDD termination even if the output is unused. See the CML Output Drivers section for more information.
30	OUT1	O	CML Output 1. This pin requires a 50 Ω termination to VDD, even if the output is unused. See the CML Output Drivers section for more information.
31	VDD	P	Power Supply for OUT1.
32	GND	GND	Ground for OUT2 Power Supply. Connect this pin to ground.
33	$\overline{\text{OUT2}}$	O	CML Complementary Output 2.
34	OUT2	O	CML Output 2.
35	VDD	P	Power Supply for OUT2.
38	GND	GND	Ground for OUT3 Power Supply. Connect this pin to ground.
39	$\overline{\text{OUT3}}$	O	CML Complementary Output 3.
40	OUT3	O	CML Output 3.
41	VDD	P	Power Supply for OUT3.
42	GND	GND	Ground for OUT4 Power Supply. Connect this pin to ground.
43	$\overline{\text{OUT4}}$	O	CML Complementary Output 4.
44	OUT4	O	CML Output 4.
45	VDD	P	Power Supply for OUT4.
47	LF_3	O	Loop Filter Connection. Connect an external capacitor (C_A) between this pin and ground.
48	LF_2	O	Loop Filter Connection. This pin is the output side of the active loop filter op amp. Connect the PLL active loop filter components (R1, C1, and C2) to this pin and LF_1 (Pin 1).
	EP	GND	Exposed Pad. The exposed pad is a ground connection on the chip that must be soldered to the analog ground of the printed circuit board (PCB) to ensure proper functionality and heat dissipation, noise, and mechanical strength benefits.

[1] O means output, N/A means not applicable, P means power, I means input, GND means ground, and I/O means input/output.

TYPICAL PERFORMANCE CHARACTERISTICS

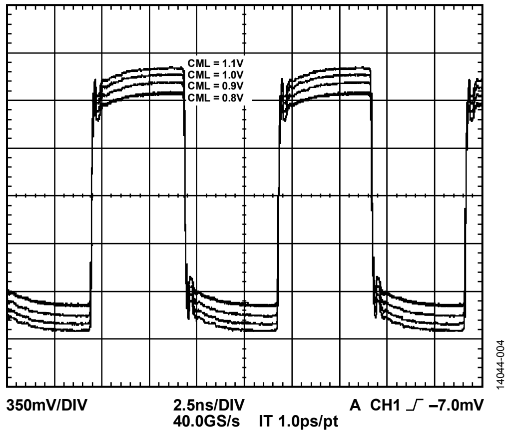


Figure 3. CML Output Waveform (Differential) at 101 MHz, Internal Termination Disabled

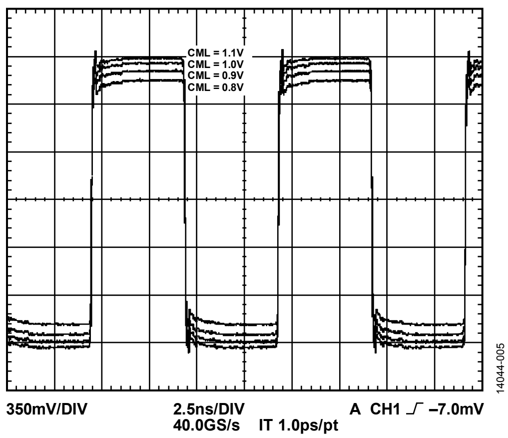


Figure 4. CML Output Waveform (Differential) at 101 MHz, Internal Termination Enabled

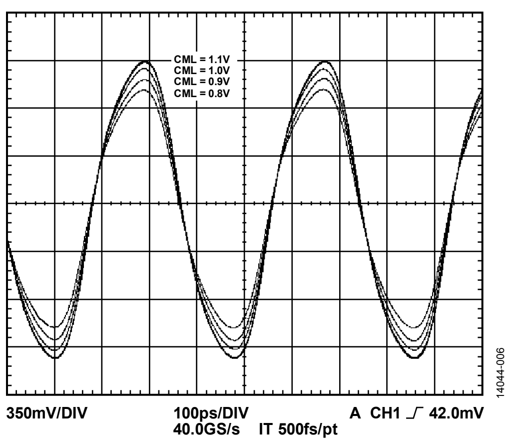


Figure 5. CML Output Waveform (Differential) at 2650 MHz, Internal Termination Disabled

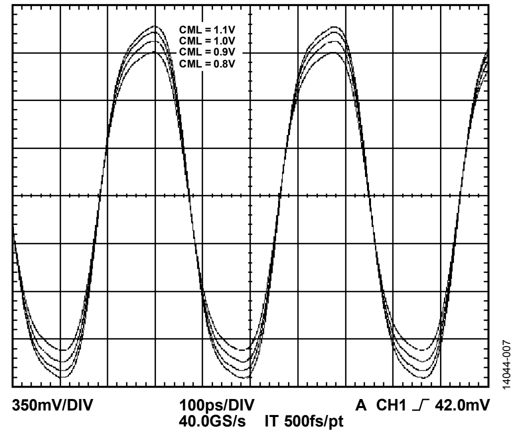


Figure 6. CML Output Waveform (Differential) at 2650 MHz, Internal Termination Enabled

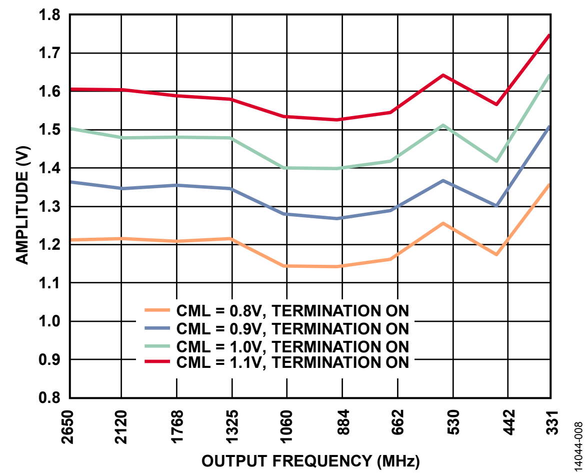


Figure 7. Differential Voltage Amplitude vs. Output Frequency, Internal Termination Enabled

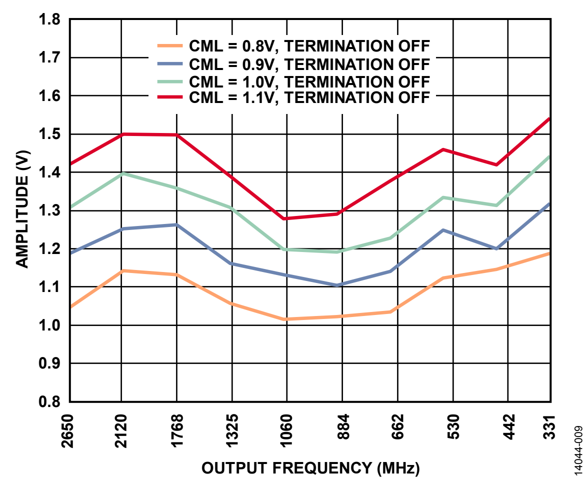


Figure 8. Differential Voltage Amplitude vs. Output Frequency, Internal Termination Disabled

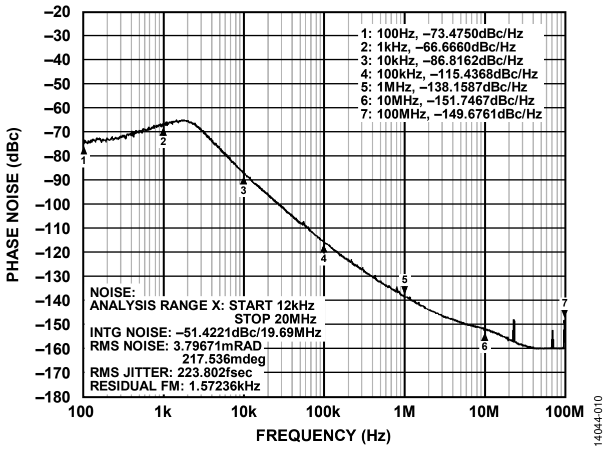


Figure 9. Phase Noise, f_{OUT} = 2.7 GHz, Loop Bandwidth = 8 kHz

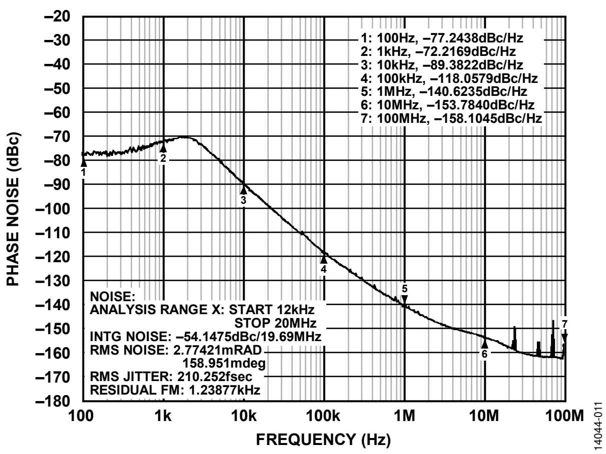


Figure 10. Phase Noise, f_{OUT} = 2.1 GHz, Loop Bandwidth = 8 kHz

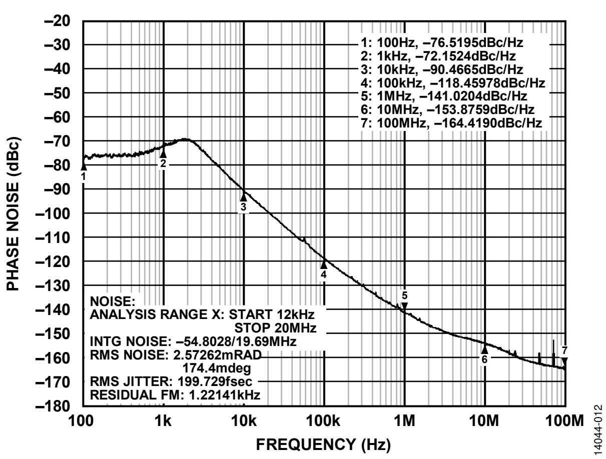


Figure 11. Phase Noise, f_{OUT} = 2.05 GHz, Loop Bandwidth = 8 kHz

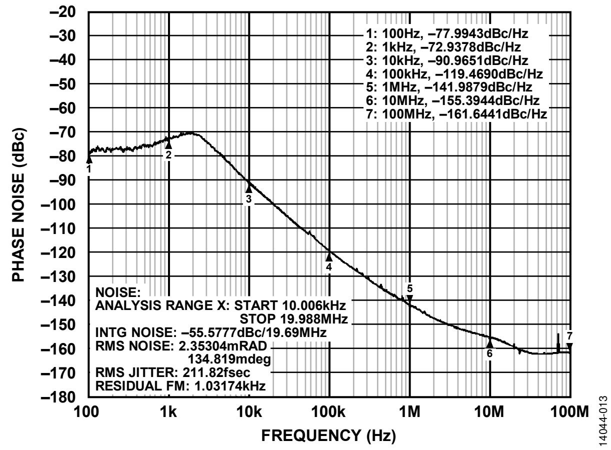


Figure 12. Phase Noise, f_{OUT} = 1.768 GHz, Loop Bandwidth = 8 kHz

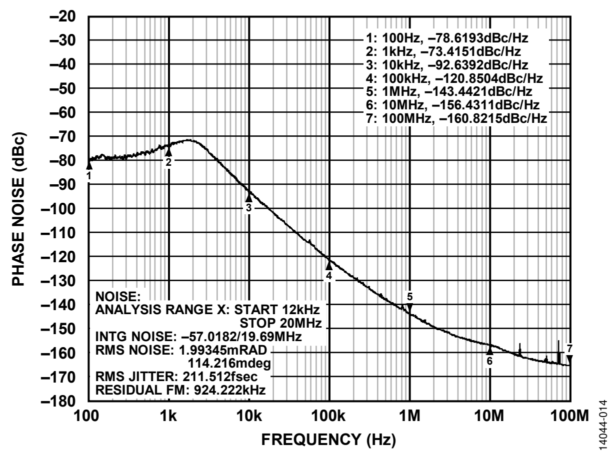


Figure 13. Phase Noise, f_{OUT} = 1.5 GHz, Loop Bandwidth = 8 kHz, High Performance Mode

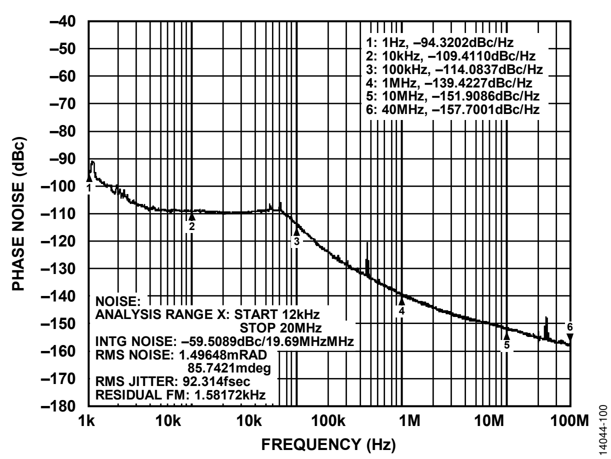


Figure 14. Phase Noise, f_{IN} = 860 MHz, f_{OUT} = 2.58 GHz, Loop Bandwidth = 80 kHz, I_{CP} = 2.4 mA, High Performance Mode

TERMINOLOGY

Phase Jitter

An ideal sine wave can be thought of as having a continuous and even progression of phase with time from 0° to 360° for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time, and this phenomenon is called phase jitter. Although many factors can contribute to phase jitter, one major factor is random noise, which is characterized statistically as being Gaussian (normal) in distribution.

Phase jitter leads to a spreading out of the energy of the sine wave in the frequency domain, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in decibels) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

Absolute Phase Noise

It is meaningful to integrate the total power contained within some interval of offset frequencies (for example, 10 kHz to 10 MHz). This is called the integrated phase noise over that frequency offset interval; it is related to the time jitter due to the phase noise within that offset frequency interval.

Phase noise has a detrimental effect on the performance of ADCs, DACs, and RF mixers. It lowers the achievable dynamic range of the converters and mixers, although they are affected in somewhat different ways. Absolute phase noise is the actual measured noise from the AD9530, and includes the input reference and power supply noise.

Time Jitter

Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings varies. In a square wave, the time jitter is a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in seconds root mean square (rms) or 1 sigma of the Gaussian distribution.

Time jitter that occurs on a sampling clock for a DAC or an ADC decreases the signal-to-noise ratio (SNR) and dynamic range of the converter. A sampling clock with the lowest possible jitter provides the highest performance from a given converter.

Additive Phase Noise

Additive phase noise is the amount of phase noise that can be attributed to the device or subsystem being measured. The phase noise of any external oscillators or clock sources is subtracted, making it possible to predict the degree to which the device impacts the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contributes its own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise. When there are multiple contributors to phase noise, the total is the square root of the sum of squares of the individual contributors.

Additive Time Jitter

Additive time jitter is the amount of time jitter that can be attributed to the device or subsystem being measured. The time jitter of any external oscillators or clock sources is not a part of this jitter number. This makes it possible to predict the degree to which the device impacts the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contributes its own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.

THEORY OF OPERATION

DETAILED FUNCTIONAL BLOCK DIAGRAM

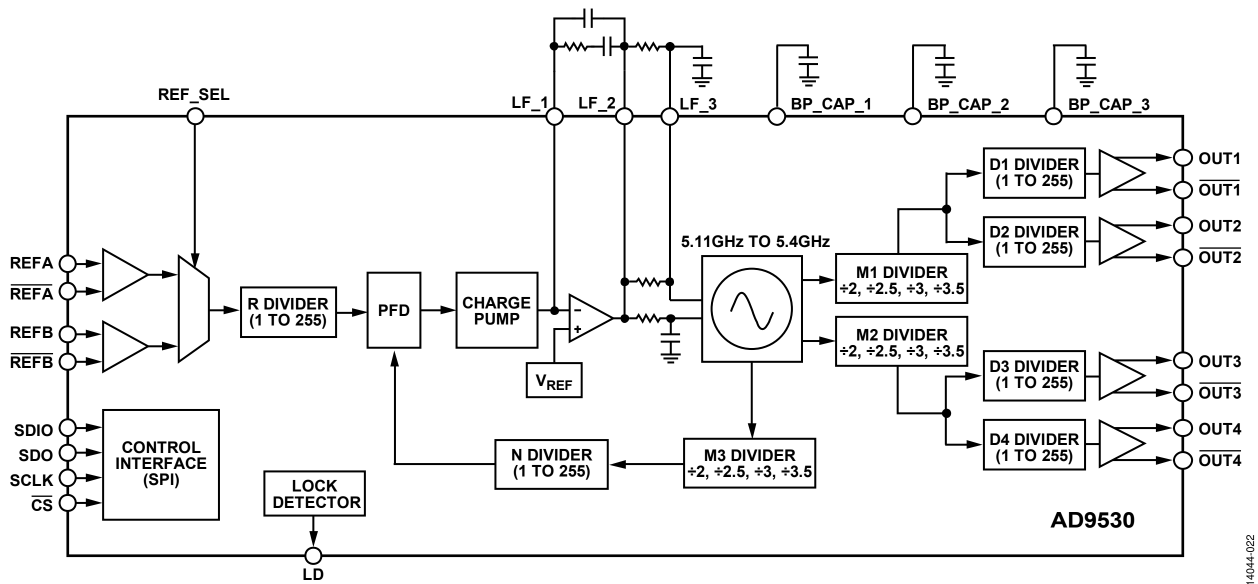


Figure 15. Detailed Functional Block Diagram

OVERVIEW

The AD9530 is a fully integrated, integer-N PLL with an ultralow noise, internal 5.11 GHz to 5.4 GHz RTWO capable of generating <232 fs rms, (12 kHz to 20 MHz) jitter clocking signals with a nonideal reference. The AD9530 is tailored for 40 Gbps and 100 Gbps OTN applications with stringent converter and ASIC clocking specifications.

The AD9530 includes an on-chip PLL, an internal RTWO, and four output channels with integrated dividers and CML drivers. The PLL contains a partially internal active loop filter, which requires a small number of external components to obtain loop bandwidths lower than 15 kHz for reference phase noise attenuation.

The four outputs of the AD9530 feature individual dividers to generate four separate frequencies up to 2.7 GHz.

CONFIGURATION OF THE PLL

Configuration of the PLL is accomplished by programming the various settings for the R divider, N divider, M3 divider, charge pump current, and a calibration of the RTWO. The combination of these settings and the loop filter determine the PLL loop bandwidth and stability.

Successful PLL operation and satisfactory PLL loop performance are highly dependent on proper configuration of the internal PLL settings and loop filter. ADIsimCLK™ is a free program that helps the design and exploration of the capabilities and features of the AD9530, including the design of the PLL loop filter.

Phase Frequency Detector (PFD)

The PFD takes inputs from the R divider output and the feedback divider path to produce an output proportional to the phase and frequency difference between them. The PFD includes an adjustable delay element that controls the width of the anti-backlash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs.

The maximum allowable input frequency into the PFD is specified in the PFD parameter in Table 5.

Charge Pump (CP)

The CP is controlled by the PFD. The PFD monitors the phase and frequency relationship between its two inputs and causes the CP to pump up or pump down to charge or discharge, respectively, the integrating node, which is part of the loop filter. The integrated and filtered CP current is transformed into a voltage that drives the tuning node of the RTWO to move the RTWO frequency up or down. The CP current is programmable in 52 steps, where each step corresponds to a current increase of 50 µA. Calculate the CP current (I_{CP}) by

$$I_{CP}\ (\mu A) = 50 \times (1 + x)$$

where x is the value written to Register 0x025, Bits[5:0].

PLL Active Loop Filter

The AD9530 active loop filter consists of an internal op amp, internal passive components, and external passive components. Proper loop filter configuration is application dependent. An example of a second-order loop filter is shown in Figure 16.

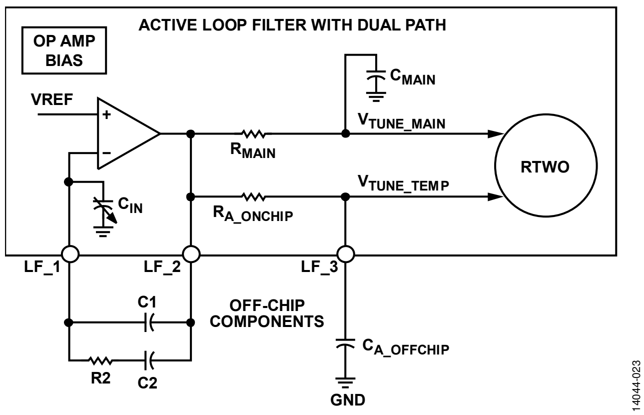


Figure 16. External Second-Order Loop Filer Configuration

C1, C2, $C_{A\_OFFCHIP}$, and R2 are external components required for proper loop filter operation. All internal loop filter components (R_{MAIN}, R_{A_ONCHIP}, C_{MAIN}) are fixed with the exception of C_{IN}, which has available settings of 5 pF to 192.5 pF by programming Register 0x027, Bits[5:2]. This capacitance setting alters the bandwidth of the loop filter op amp. C_{IN} is composed of a fixed 5 pF capacitor and a bank of 15 selectable 12.5 pF capacitors. Calculate the C_{IN} value by

$$C_{IN} = 5\text{ pF} + 12.5\text{ pF} \times \textit{Register 0x027, Bits[5:2]}$$

Note that R_{MAIN} and C_{MAIN} in Figure 16 form a pole at approximately 2 MHz.

Table 17 shows the typical loop filter component values and CP settings for an 8 kHz loop bandwidth.

The maximum allowable capacitance value for the external loop filter design is shown in Table 5. Exceeding this value may cause various functions of the AD9530 to become unstable.

Use the ADIsimCLK design tool to design and simulate loop filters with varying bandwidths.

PLL Reference Inputs

The AD9530 features two fully differential PLL reference inputs that are routed through a 2:1 mux to a common R divider. The differential reference input receiver has four internal termination/biasing options to accommodate many input logic types. A functional diagram of the reference input receiver is shown in Figure 17. Table 18 details the four possible reference input termination and common-mode settings achievable by writing to Register 0x012, Bits[3:2] and Register 0x013, Bits[3:2]. The input frequency specifications for the reference inputs are listed in Table 4.

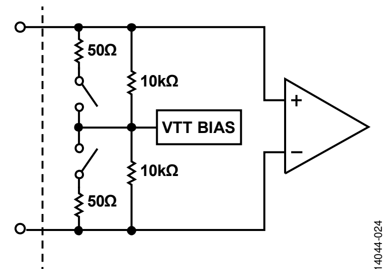


Figure 17. Reference Input Receiver Functional Diagram

Each REFx/$\overline{\text{REFx}}$ receiver can be disabled by setting the associated reference enable bit to 0.

RTWO

The internal RTWO tunes from 5.11 GHz to 5.4 GHz and is powered by the VDD supply pins (Pin 20 to Pin 23). The RTWO has two modes: high performance mode and low power mode. These modes are set by Register 0x01C, Bit 0. These modes enable optimization between the phase noise performance and power consumption. See the Power Supply Recommendations section for a recommended power supply configuration for Pin 20 to Pin 23.

Table 17. Typical Loop Filter Components and I_{CP} Settings for 8 kHz Loop Bandwidth

Reference (MHz)	R Divider	Feedback Divider (N × M3)	C1 (nF)	C2 (µF)	R2 (Ω)	$C_{A\_OFFCHIP}$ (µF)	I_{CP} (mA)
181.5	÷1	÷30	10	0.47	255	0.1	0.3

Table 18. Possible Reference Input Termination Settings

Mode Name	REFx/$\overline{\text{REFx}}$ Input Termination Select Settings	On-Chip Termination	Common-Mode Bias
DC-Coupled LVDS	00	100 Ω differential	High-Z
DC-Coupled, Internally Biased	01 (default)	50 Ω to GND	GND
AC-Coupled	10	50 Ω to 0.35 V	0.35 V
DC-Coupled High-Z	11	10 kΩ to GND	GND

RTWO Calibration

The RTWO calibration function selects the appropriate RTWO frequency band for a given configuration. A calibration is performed by toggling Register 0x001, Bit 2 from 0 to 1. The command sequence to issue a VCO calibration is as follows:

1. Write the desired AD9530 configuration, including the divider and output driver settings.
2. Set Register 0x001, Bit 2 = 0 (CALIBRATE VCO bit). Note that this is a self clearing bit.

A calibration is required after initial power-up, after subsequent resets, and after any changes to the input reference frequency or the divide settings that affect the RTWO operating frequency. A 2 sec wait timer is activated at power-up to gate the first calibration. This wait time is not enforced for subsequent calibrations after power-on. See the CML Output Drivers section for more details. The PLL reference must be active and stable and the PLL must be configured to a valid operational state prior to issuing a calibration. After a calibration, all of the internal dividers are synchronized automatically to ensure proper phase alignment of the PLL and distribution.

Reference Switchover

The AD9530 supports two separate differential reference inputs. Manual switchover is performed between these inputs by either writing to Register 0x011, Bit 2 and Bit 1, or by using the REF_SEL pin. Register 0x011, Bit 2 sets whether the REF_SEL pin or the reference select register controls the reference input mux. Default operation ignores the REF_SEL pin setting and uses the value of Register 0x011, Bit 1.

Dividers (R, Mx, N, and Dx)

The AD9530 contains multiple dividers that configure the PLL for a given frequency plan. Each divider has an associated reset bit that is self clearing. Resetting a divider is required every time the divide value of that driver is changed. Issuing a reset of a single divider does not clear the current divide value.

Reference Divider (R Divider)

The reference inputs are routed through a 2:1 mux into a common 8-bit R divider. R can be set to any value from 1 to 255 (Register 0x010, Bits[7:0]). Setting Register 0x010 = 0x0A is equivalent to an R divider setting of 10.

The frequency out of the R divider must not exceed the maximum allowable frequency of the PFD listed in Table 5.

The R divider has its own reset located in Register 0x011. This reset bit is self clearing.

M3 and N Feedback Dividers

The total feedback division from the RTWO to the PFD is the product of the M3 and N dividers. The N divider (Register 0x023, Bits[7:0]) functions identically to the R divider described in the Reference Divider (R Divider) section. The M3 divider (Register 0x022, Bits[3:2]) is limited to fixed divide values of 2, 2.5, 3, and 3.5 and acts as a prescaler to the N divider. The M3 and N dividers have individual resets located at Register 0x022, Bit 0, and Register 0x024, Bit 0, respectively.

M1 and M2 Dividers (M1 and M2)

The M1 and M2 dividers (Register 0x020, Bits[4:3] and Register 0x021, Bits[4:3], respectively) have fixed divide values of 2, 2.5, 3, and 3.5.

The M1 and M2 dividers provide frequency division between the RTWO output and the clock distribution channel dividers (Dx).

The M1 and M2 dividers have individual resets located at Register 0x020, Bit 0, and Register 0x021, Bit 0, respectively.

Channel Dividers (Dx)

The AD9530 has four 8-bit channel dividers (Dx) which are identical to the R and N dividers. Dx can be set to any value from 1 to 255. Setting the divide value for D1 through D4 is accomplished by writing Register 0x014, Register 0x016, Register 0x018, and Register 0x01A, respectively. The D1 through D4 reset bits that reset D1 through D4 are located in Bit 0 of Register 0x015, Register 0x017, Register 0x019, and Register 0x01B, respectively. A setting of 0 disables the divider.

Dividers Sync

Use a sync to phase align all of the AD9530 internal dividers to a common point in time. A global sync of all dividers is performed after a VCO calibration. To perform a VCO calibration, write a 1 to Bit 2 of Register 0x001. A VCO calibration must be performed after power up, as well as any time a different VCO frequency is selected.

To sync all of the dividers after programming them, without the VCO frequency, write a 1 to Bit 1 of Register 0x001.

Lock Detector

The AD9530 features a frequency lock detect signal that corresponds to whether the PLL reference and feedback edges are within a certain frequency of one another. The exact frequency lock threshold to indicate a PLL lock is user programmable in Register 0x01D, Bits[3:1]. The three register bits allow the frequency lock threshold to span ±20 ppb to ±300 ppm.

If the frequency error between the reference and feedback edges is lower than the specified lock threshold, the LD pin goes high and the PLL_LOCKED bit = 1. The LD pin and the PLL_LOCKED bit go low when the error between the reference and feedback edges is greater than the frequency lock threshold.

The lock detector also outputs an 11-bit word located in Register 0x01E, Bits[7:0] and Register 0x01F, Bits[1:0]. Bit 10 through Bit 0 contain a binary value representative of the measured frequency lock error, and Bit 11 indicates whether the 10-bit value is expressed in ppm (parts per million) or ppb (parts per billion). Note that this 11^{th} bit is found in Register 0x01F, Bit 3.

CML Output Drivers

The AD9530 has four CML output drivers that are operable up to 2.7 GHz. Each output driver must be externally terminated as shown in the Input/Output Termination Recommendations section. The output voltage swing, internal termination, and power-down of each CML driver are configurable by writing to the appropriate registers. An initial calibration of the internal termination and voltage swing is performed after a POR event. This calibration requires that OUT1 is terminated, regardless of whether the driver is needed in a specific design. A functional diagram of the output driver is shown in Figure 18.

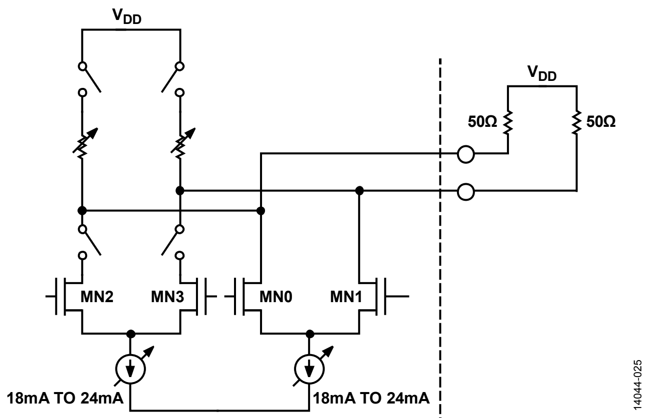


Figure 18. CML Output Simplified Equivalent Circuit

The CML differential voltage (V_{OD}) is selectable from 0.8 V to 1.1 V via Bits[5:4] of Register 0x015, Register 0x017, Register 0x019, and Register 0x01B.

The AD9530 has optional internal termination for cases where transmission line impedance mismatch between the CML output and the receiver causes increased reflections at high output frequencies. These terminations improve impedance match traces at high frequency at the expense of drawing twice as much current as the default operating condition.

For Register 0x015 (for OUT1), Register 0x017 (for OUT2), Register 0x019 (for OUT3), and Register 0x01B (for OUT4), setting the OUTx_TERM_EN (Bit 3) = 1 enables the on-chip termination and is configurable for each driver.

Each CML output can be enabled as needed by altering the appropriate OUTx_ENABLE bit.

RESET MODES

The AD9530 has a POR and several other ways to apply a reset condition to the chip.

Power-On Reset (POR)

During chip power-up, a POR pulse is issued when VDD reaches ~2 V and restores the chip to the default on-chip setting. At this point, a 2 sec counter is started to allow all the user device settings to load and the RTWO to stabilize. After the 2 sec counter finishes, the user can issue a VCO calibration and outputs begin toggling ~500 ns later.

2 sec Wait Timer

The 2 sec wait timer ensures that all internal supplies are stable before allowing the user to issue a VCO calibration. This timer only starts after a POR. The user may program all the necessary registers during this time, including the VCO calibration bit. After the timer times out and a reference input is applied, the calibration issues, allowing the PLL to lock and the outputs to toggle. The maximum internal wait time is shown in Table 5.

Hardware Reset via the $\overline{\text{RESET}}$ Pin

Driving the $\overline{\text{RESET}}$ pin to a Logic 0 and then back to a Logic 1 restores the chip to the on-chip default register settings.

Soft Reset via the Serial Port

The serial port control register allows a soft reset by setting Register 0x000, Bit 7 and Bit 1. When these bits are set, the chip restores to the on-chip default settings, except for Register 0x000 and Register 0x001. Register 0x000 and Register 0x001 retain the values prior to reset, except for the self clearing bits. However, the self clearing operation does not complete until an additional serial port SCLK cycle occurs; the AD9530 is held in reset until this additional SCLK cycle.

Individual Divider Reset via the Serial Port

Every divider in the AD9530 has the ability to reset individually by using the appropriate reset bit. This reset does not clear the value written in the specific divider register but restarts the divider count to 0, which results in a phase adjustment. See the associated divider section or the register map for the location of these bits.

POWER-DOWN MODES

Sleep Mode via the Serial Port

Place the AD9530 in sleep mode by writing Register 0x002, Bits[1:0] = 11. This mode powers down the following blocks:

- All OUTx drivers
- All REFx inputs
- All Mx dividers
- RTWO power set to minimum
- CP current set to minimum
- PFD
- Loop filter op amp

Individual Clock Input and Output Power-Down

Power down any of the reference inputs or clock distribution outputs by individually writing to the appropriate registers. The register map details the individual power-down settings for each input and output.

INPUT/OUTPUT TERMINATION RECOMMENDATIONS

Figure 19 through Figure 24 illustrate the recommended input and output connections for connecting the AD9530 to other devices.

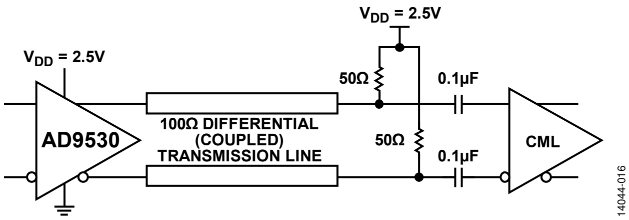


Figure 19. CML AC-Coupled Output Driver (External Termination Required When Using the Internal Termination Option)

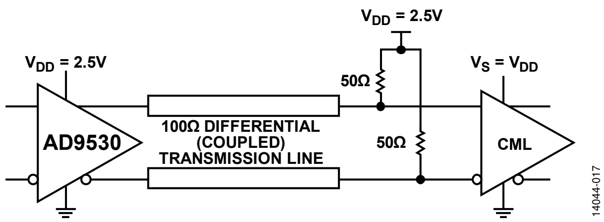


Figure 20. CML DC-Coupled Output Driver (External Termination Required When Using the Internal Termination Option)

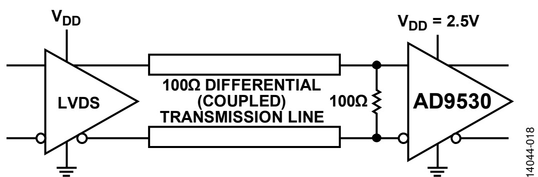


Figure 21. REFx Input Termination Recommendation for LVDS Drivers

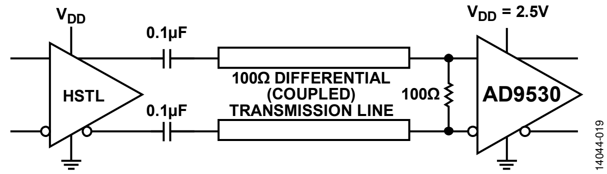


Figure 22. REFx Input Termination Recommendation for High Speed Transceiver Logic (HSTL) Drivers

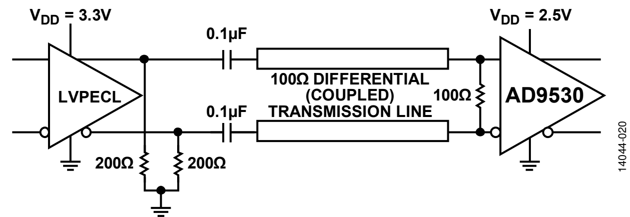


Figure 23. REFx Input Termination Recommendation for 3.3V LVPECL Drivers

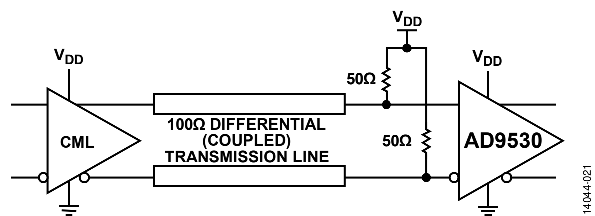


Figure 24. REFx Input Termination Recommendation for 2.5V CML Drivers

SERIAL CONTROL PORT

The AD9530 serial control port is a flexible, synchronous serial communications port that provides a convenient interface to many industry-standard microcontrollers and microprocessors. The serial control port allows read/write access to the AD9530 register map.

The AD9530 uses the Analog Devices, Inc., unified SPI protocol. The unified SPI protocol guarantees that all new Analog Devices products using the unified protocol have consistent serial port characteristics. The SPI port configuration is programmable via Register 0x0000. This register is a part of the SPI control logic rather than in the register map.

SPI SERIAL PORT OPERATION

Pin Descriptions

The SCLK (serial clock) pin serves as the serial shift clock. This pin is an input. SCLK synchronizes serial control port read and write operations. The rising edge SCLK registers write data bits, and the falling edge registers read data bits. The SCLK pin supports a maximum clock rate of 40 MHz.

The SPI port supports both 3-wire (bidirectional) and 4-wire (unidirectional) hardware configurations and both MSB-first and LSB-first data formats. Both the hardware configuration and data format features are programmable. The 3-wire mode uses the SDIO (serial data input/output) pin for transferring data in both directions. The 4-wire mode uses the SDIO pin for transferring data to the AD9530, and the SDO pin for transferring data from the AD9530.

The $\overline{CS}$ (chip select) pin is an active low control that gates read and write operations. Assertion (active low) of the $\overline{CS}$ pin initiates a write or read operation to theAD9530 SPI port. Any number of data bytes can be transferred in a continuous stream. The register address is automatically incremented or decremented based on the setting of the address ascension bit (Register 0x0000). $\overline{CS}$ must be deasserted at the end of the last byte transferred, thereby ending the stream mode. This pin is internally connected to a 10 kΩ pull-up resistor. When $\overline{CS}$ is high, the SDIO and SDO pins go into a high impedance state.

Implementation Specific Details

A detailed description of the unified SPI protocol can be found at www.analog.com/ADISPI, which covers items such as timing, command format, and addressing.

The following product specific items are defined in the unified SPI protocol:

- Analog Devices unified SPI protocol Revision: 1.0.
- Chip type: 0x05 (0x05 indicates a clock chip).
- Product ID: 10011b (in this case) uniquely identifies the device as AD9530. No other Analog Devices clock IC supporting unified SPI has this identifier.
- Physical layer: 3-wire and 4-wire supported and 2.5 V operation supported.
- Optional single-byte instruction mode: not supported.
- Data link: not used.
- Control: not used.

Communication Cycle—Instruction Plus Data

The unified SPI protocol consists of a two part communication cycle. The first part is a 16-bit instruction word that is coincident with the first 16 SCLK rising edges and a payload. The instruction word provides the AD9530 serial control port with information regarding the payload. The instruction word includes the R/$\overline{W}$ bit that indicates the direction of the payload transfer (that is, a read or write operation). The instruction word also indicates the starting register address of the first payload byte.

Write

If the instruction word indicates a write operation, the payload is written into the serial control port buffer of the AD9530. Data bits are registered on the rising edge of SCLK. Generally, it does not matter what data is written to blank registers; however, it is customary to use 0s. Note that there may be reserved registers with default values not equal to 0x00; however, every effort was made to avoid this.

Most of the serial port registers are buffered (see the Buffered/ Active Registers section for details on the difference between buffered and active registers). Therefore, data written into buffered registers does not take effect immediately. An additional operation is needed to transfer buffered serial control port contents to the registers that actually control the device. This transfer is accomplished with an IO_UPDATE operation, which is performed in one of two ways. One method is to write a Logic 1 to Register 0x00F, Bit 0 (this bit is an autoclearing bit). The user can change as many register bits as desired before executing an IO_UPDATE command. The IO_UPDATE operation transfers the buffer register contents to their active register counterparts.

Read

If the instruction word indicates a read operation, the next N × 8 SCLK cycles clock out the data starting from the address specified in the instruction word. N is the number of data bytes read. The readback data is driven to the pin on the falling edge and must be latched on the rising edge of SCLK. Blank registers are not skipped over during readback.

A readback operation takes data from either the serial control port buffer registers or the active registers, as determined by Register 0x001, Bit 5.

SPI Instruction Word (16 Bits)

The MSB of the 16-bit instruction word is R/$\overline{W}$, which indicates whether the instruction is a read or a write. The next 15 bits are the register address (A14 to A0), which indicates the starting register address of the read/write operation (see Table 20). Note that, because there are no registers that require more than 13 address bits, A14 and A13 are ignored and treated as zeros.

SPI MSB/LSB First Transfers

The AD9530 instruction word and payload can be MSB first or LSB first. The default for the AD9530 is MSB first. The LSB first mode can be set by writing a 1 to Register 0x000, Bit 6 and Bit 1. Immediately after the LSB first bit is set, subsequent serial control port operations are LSB first.

Address Ascension

If the address ascension bit (Register 0x000, Bit 5 and Bit 2) = 0, the serial control port register address decrements from the specified starting address toward Address 0x0000.

If the address ascension bit (Register 0x0000, Bit 5 and Bit 2) = 1, the serial control port register address increments from the starting address toward Address 0x0FF. Reserved addresses are not skipped during multibyte input/output operations; therefore, write the default value to a reserved register and 0s to unmapped registers. Note that it is more efficient to issue a new write command than to write the default value to more than two consecutive reserved (or unmapped) registers.

Table 19. Streaming Mode (No Addresses Skipped)

Address Ascension	Stop Sequence
Increment	0x0000 … 0x1FFF
Decrement	0x1FFF … 0x0000

Table 20. Serial Control Port, 16-Bit Instruction Word

MSB **LSB**

I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
R/$\overline{W}$	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

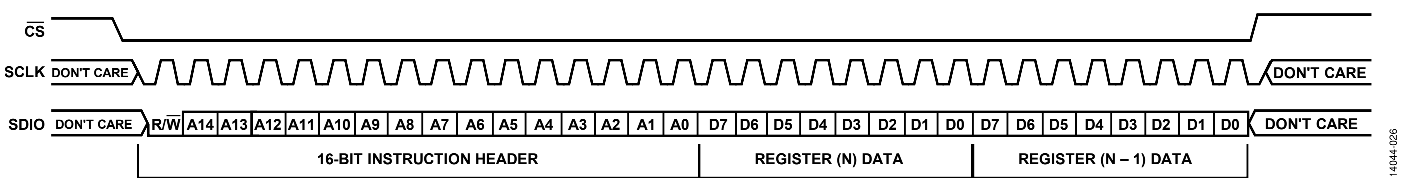


Figure 25. Serial Control Port Write—MSB First, Address Decrement, Two Bytes of Data

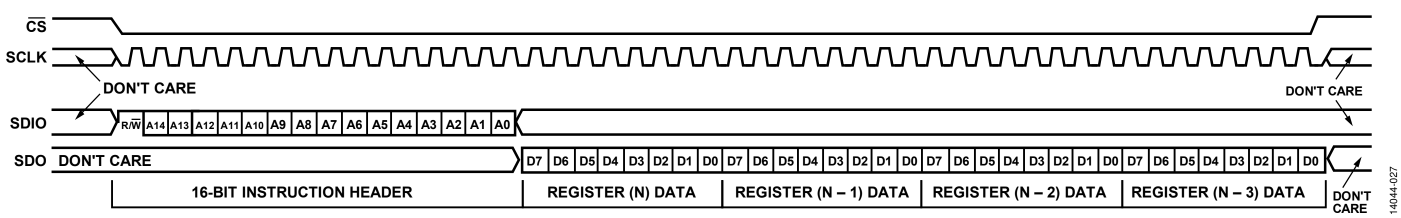


Figure 26. Serial Control Port Read—MSB First, Address Decrement, Four Bytes of Data

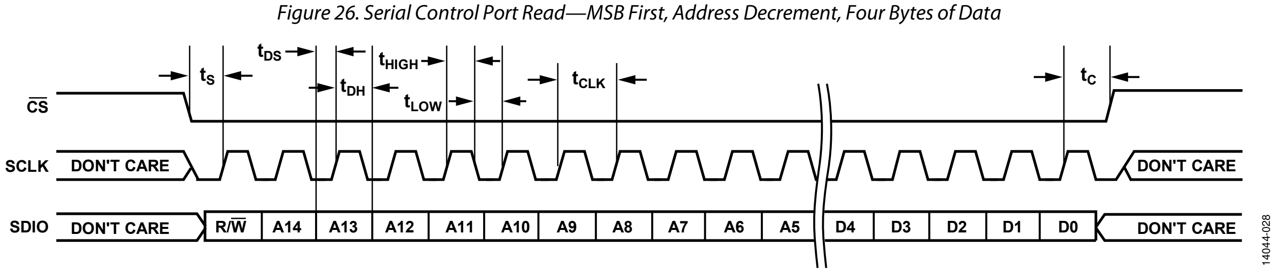


Figure 27. Timing Diagram for Serial Control Port Write—MSB First