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ANALOG DEVICES

3-Channel Clock Generator, 24 Outputs

Data Sheet

AD9531

FEATURES

3 fully integrated PLL/VCO cores (PLL1, PLL2, and PLL3)
Jitter performance: 0.462 ps rms typical
   PLL1, fractional-N mode, 12 kHz to 20 MHz bandwidth
Loss of reference and lock detection for each PLL
Pin-configurable common frequency translations
Automatic synchronization of all outputs on power-up
Manual output synchronization capability
Package available in an 88-lead LFCSP
PLL1 details
   Fractional-N/integer-N modes
   Optional external VCXO
   Fixed delay mode for constant static phase offset
   2 reference clock inputs
      Input format: differential/single-ended
      Frequency range: 9.5 MHz to 260 MHz
      Reference switching: manual/automatic
   10 ultralow jitter HSTL/CMOS outputs up to 400 MHz
PLL2 details
   Integer-N mode (1 reference clock input)
      Input format: differential/single-ended/crystal[1]
      Frequency range: 9.5 MHz to 250 MHz
   12 HSTL/CMOS outputs up to 400 MHz
PLL3 details
   Integer-N mode (1 reference clock input)
      Frequency range: 9.5 MHz to 100 MHz
Input format: differential/crystal (supports a 25 MHz to
   50 MHz AT-cut quartz crystal resonator)
   2 HSTL/LVDS/CMOS outputs to 400 MHz/150 MHz
      (differential/CMOS)

APPLICATIONS

Radio equipment controller clocking
Low jitter/phase noise clock generation and distribution
Clock generation and translation for SONET, 10GE, 10G FC,
   and other 10 Gbps protocols
40 Gbps/100 Gbps networking line cards, including SONET,
   synchronous ethernet, OTU2/3/4
Forward error correction (G.710)
High performance wireless transceivers
ATE and high performance instrumentation
Broadband infrastructures
Ethernet line cards, switches, and routers
SATA and PCI-express

GENERAL DESCRIPTION

The AD9531 provides a multioutput clock generator function and three on-chip phase-locked loop (PLL) cores with SPI programmable output frequencies and formats.

PLL1 provides two reference inputs and 10 outputs and includes four user selectable loop configurations. The PLL has a fully integrated loop filter requiring only a single external capacitor (or a series RC network). PLL1 provides a wide range of output frequencies up to 400 MHz and is capable of operating with an external voltage controlled crystal oscillator (VCXO) and loop filter, instead of the integrated voltage controlled oscillator (VCO) and loop filter.

PLL2 is an integer-N PLL providing a single reference input and 12 outputs. PLL2 synthesizes output frequencies up to 400 MHz from the REF2_x source and synchronizes the output clocks to the input reference.

PLL3 provides a single reference input and two outputs. PLL3 synthesizes output frequencies up to 400 MHz from the REF3_x source and synchronizes the output clocks to input reference.

The AD9531 is available in an 88-lead LFCSP and is specified over the −40°C to +85°C operating temperature range.

Throughout this data sheet, multifunction pins, such as LOR/M4, are referred to either by the entire pin name or by a single function of the pin (for example, LOR, when only that function is relevant). In other cases, the text and figures of this data sheet contain references to a channel rather than a pin. For example, REF_A refers to the REF_A channel rather than the REF_AP and REF_AN pins. Likewise, OUT3_1 refers to Channel 1 of PLL3 rather than the OUT3_1P and OUT3_1N pins. Additionally, an abbreviated notation for a pin pair replaces an explicit reference to a each pin (for example, REF_Ax signifies the REF_AN and REF_AP pins.).

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1/16—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM
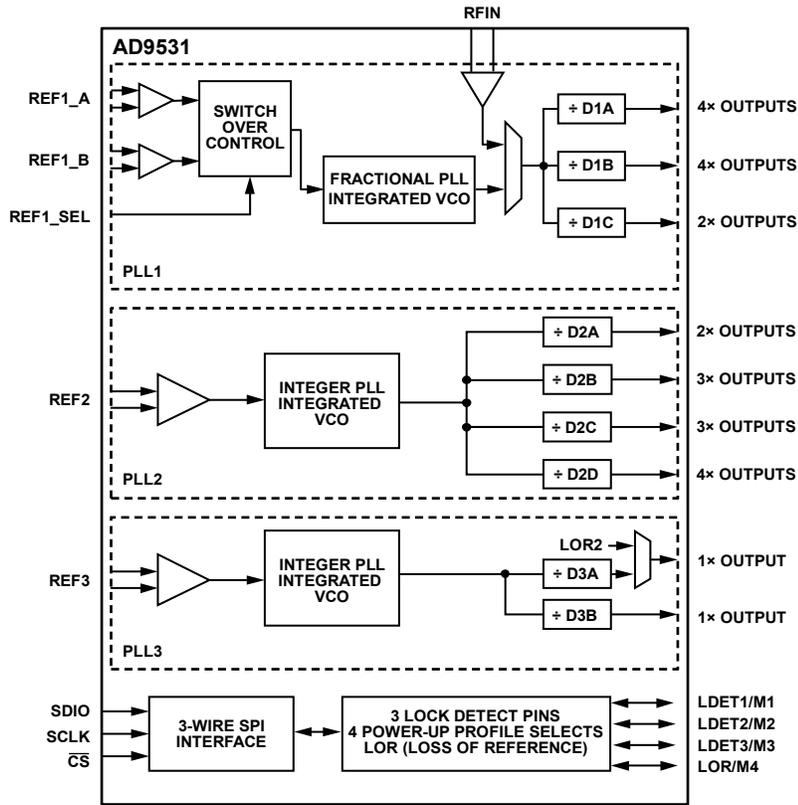
Figure 1.

SPECIFICATIONS

Typical values are given for 3.3 V supplies at 3.3 V ± 5% and 1.8 V supplies at 1.8 V ± 5%; T_A = 25°C. Minimum and maximum values apply over the full variation of supply voltage and T_A (−40°C to +85°C) as listed in Table 1, unless otherwise specified.

CONDITIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
3 V Supply Pins		3.3		V	3.3 V ± 5%
1.8 V Supply Pins		1.8		V	1.8 V ± 5%
TEMPERATURE RANGE, T_A	−40	+25	+85	°C	

SUPPLY CURRENT

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT					
Case 1					PLL1: off; PLL2: off; PLL3: off
1.8 V Supply					
PLL1 Pins		6		mA	
PLL2 Pins		19		mA	
PLL3 Pins		1.5		mA	
DVDD		3		mA	
3.3 V Supply					
PLL1 Pins		3.2		mA	
PLL2 Pins		1.3		mA	
PLL3 Pins		0.1		mA	
Case 2					PLL1: differential input at 122.88 MHz, HSTL output at 122.88 MHz, all outputs active, internal VCO; PLL2: off; PLL3: off
1.8 V Supply					
PLL1 Pins		270		mA	
PLL2 Pins		19		mA	
PLL3 Pins		1.5		mA	
DVDD		0.3		mA	
3.3 V Supply					
PLL1 Pins		34		mA	
PLL2 Pins		1.3		mA	
PLL3 Pins		0.1		mA	
Case 3					PLL1: off; PLL2: 3.3 V, CMOS input at 50 MHz, HSTL output at 156.25 MHz, all outputs active; PLL3: off
1.8 V Supply					
PLL1 Pins		6		mA	
PLL2 Pins		280		mA	
PLL3 Pins		1.5		mA	
DVDD Pin		0.3		mA	
3.3 V Supply					
PLL1 Pins		3.2		mA	
PLL2 Pins		22		mA	
PLL3 Pins		0.1		mA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Case 4					PLL1: off; PLL3: 3.3 V, CMOS input at 25 MHz, OUT3_0 and OUT3_1 at 125 MHz (1.8 V CMOS and HSTL, respectively); PLL2: off
1.8 V Supply					
PLL1 Pins		6		mA	
PLL2 Pins		19		mA	
PLL3 Pins		72		mA	
DVDD Pin		0.3		mA	
3.3 V Supply					
PLL1 Pins		3.2		mA	
PLL2 Pins		1.3		mA	
PLL3 Pins		0.1		mA	
Case 5					PLL1: differential input at 122.88 MHz, HSTL output at 122.88 MHz, all outputs active, internal VCO; PLL2: 3.3 V, CMOS input at 50 MHz, HSTL output at 156.25 MHz, all outputs active; PLL3: 3.3 V, CMOS input at 25 MHz, OUT3_0 and OUT3_1 at 125 MHz (1.8 V CMOS and HSTL, respectively)
1.8 V Supply					
PLL1 Pins		270		mA	
PLL2 Pins		280		mA	
PLL3 Pins		72		mA	
DVDD Pin		0.3		mA	
3.3 V Supply					
PLL1 Pins		34		mA	
PLL2 Pins		23		mA	
PLL3 Pins		0.1		mA	
INCREMENTAL SUPPLY CURRENT					
PLL1, External VCXO Configuration					
1.8 V Supply (PLL1 Pins)		−22		mA	
3.3 V Supply (PLL1 Pins)		−27		mA	
PLL3, Dual Loop Configuration					
1.8 V Supply (PLL3 Pins)		36		mA	
3.3 V Supply (PLL3 Pins)		0		mA	

POWER DISSIPATION

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER CONSUMPTION					Does not include power dissipated in the external resistors
Case 1					PLL1: off; PLL2: off; PLL3 off
1.8 V Supply					
PLL1 Pins		11		mW	
PLL2 Pins		35		mW	
PLL3 Pins		2.5		mW	
DVDD Pin		0.5		mW	
3.3 V Supply					
PLL1 Pins		11		mW	
PLL2 Pins		4.0		mW	
PLL3 Pins		0.3		mW	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Case 2					PLL1: differential input at 122.88 MHz, HSTL output at 122.88 MHz, all outputs active, internal VCO; PLL2: off; PLL3: off
1.8 V Supply					
PLL1 Pins		480		mW	
PLL2 Pins		35		mW	
PLL3 Pins		2.5		mW	
DVDD Pins		0.5		mW	
3.3 V Supply					
PLL1 Pins		112		mW	
PLL2 Pins		4.0		mW	
PLL3 Pins		0.3		mW	
Case 3					PLL1: off; PLL2: 3.3 V, CMOS input at 50 MHz, HSTL output at 156.25 MHz, all outputs active; PLL3: off
1.8 V Supply					
PLL1 Pins		11		mW	
PLL2 Pins		500		mW	
PLL3 Pins		2.5		mW	
DVDD Pins		0.5		mW	
3.3 V Supply					
PLL1 Pins		11		mW	
PLL2 Pins		73		mW	
PLL3 Pins		0.3		mW	
Case 4					PLL1: off; PLL2: off; PLL3: 3.3 V, CMOS input at 25 MHz, OUT3_0 and OUT3_1 at 125 MHz (1.8 V CMOS and HSTL, respectively)
1.8 V Supply					
PLL1 Pins		11		mW	
PLL2 Pins		35		mW	
PLL3 Pins		130		mW	
DVDD Pins		0.5			
3.3 V Supply					
PLL1 Pins		11		mW	
PLL2 Pins		4.0		mW	
PLL3 Pins		0.3		mW	
Case 5					PLL1: differential input at 122.88 MHz, HSTL output at 122.88 MHz, all outputs active, internal VCO; PLL2: 3.3 V, CMOS input at 50 MHz, HSTL output at 156.25 MHz, all outputs active; PLL3: 3.3 V, CMOS input at 25 MHz, OUT3_0 and OUT3_1 at 125 MHz (1.8 V CMOS and HSTL, respectively)
1.8 V Supply					
PLL1 Pins		480		mW	
PLL2 Pins		500		mW	
PLL3 Pins		130		mW	
DVDD Pins		0.5		mW	
3.3 V Supply					
PLL1 Pins		112		mW	
PLL2 Pins		73		mW	
PLL3 Pins		0.3		mW	
INCREMENTAL POWER CONSUMPTON					Change in power consumption when a specific circuit block or function is made active (or inactive)
PLL1, External VCXO Configuration					
1.8 V Supply (PLL1 Pins)		−39		mW	
3.3 V Supply (PLL1 Pins)		−89		mW	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PLL3, Dual Loop Configuration				mW	
1.8 V Supply (PLL3 Pins)		65		mW	
3.3 V Supply (PLL3 Pins)		0		mW	

LDET1/M1, LDET2/M2, LDET3/M3, AND LOR/M4 PINS

In addition to the LOR/M4 pin, a secondary LOR indicator pin is possible via OUT3_0 (see the OUT3_0 Driver section).

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT SPECIFICATIONS					Load current: 1 mA
1.8 V Operating Mode					The 3.3 V mode bit in Register 0x0083 or Register 0x0084 is Logic 0 for the associated pin
Output Voltage					
High	$V_{DD} - 0.2$			V	Relative to the supply pins (Pin 49, Pin 78, Pin 61, and Pin 6) for LDET1/M1, LDET2/M2, LDET3/M3, and LOR/M4, respectively
Low			0.2	V	
3.3 V Operating Mode					The 3.3 V mode bit in Register 0x0083 or Register 0x0084 is Logic 1 for the associated pin
Output Voltage					
High	2.7			V	
Low			0.2	V	
INPUT SPECIFICATIONS					Applies during a power-on/reset sequence (see the Power-On Reset (POR) section and the Multifunction Pins (LDET1/M1, LDET2/M2, LDET3/M3, LOR/M4) section)
Input High Voltage (V_{IH})	1.2			V	
Input Low Voltage (V_{IL})			0.7	V	
External Resistive Load	3	10	100	kΩ	Required termination to ground or 1.8 V for Logic 0 or Logic 1, respectively
Input Capacitance (C_{IN})		3		pF	

REF1_SEL PIN

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT SPECIFICATIONS					
Input High Voltage (V_{IH})	1.4			V	
Input Low Voltage (V_{IL})			1.0	V	
Input Current (I_{INH}, I_{INL})	−2		+2	μA	
Input Capacitance (C_{IN})		3		pF	

PLL1 CHARACTERISTICS

PLL1 Reference Inputs (REF1_A and REF1_B)

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL MODE					Capacitive coupling required
Input Frequency Range					
×2 Frequency Multiplier					
Bypassed	9.5		260	MHz	
Enabled	9.5		100	MHz	
Input Sensitivity	200			mV p-p	
Input Slew Rate	100			V/μs	Minimum limit imposed for jitter performance

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Common-Mode Internally Generated Bias Voltage		1.0		V	
Hysteresis		20		mV	
Differential Input Resistance		19		kΩ	
Differential Input Capacitance		3		pF	
Duty Cycle	40		60	%	Required for input frequencies below 20 MHz; limited by spurious performance when ×2 frequency multiplier is in use
CMOS MODE SINGLE-ENDED INPUT					Single-ended operation is only applicable to the REF1_AP and REF1_BP pins; for both of these inputs, the 2.5 V or 3.3 V mode is selectable via Register 0x0103
Input Frequency Range					
×2 Frequency Multiplier					
Bypassed	9.5		260	MHz	
Enabled	9.5		100	MHz	
Hysteresis		430		mV	
Input Resistance		46		kΩ	
Input Capacitance		3		pF	
Duty Cycle	40		60	%	Required for input frequencies below 20 MHz; limited by spurious performance when ×2 frequency multiplier is in use.
3.3 V Operating Mode					
Input Voltage					
Bias		1.65		V	50% of 3.3 V supply, Pin 23 (VDD1_3V3)
High	2.0			V	
Low			1.3	V	
2.5 V Operating Mode					
Input Voltage					
Bias		1.25		V	38% of 3.3 V supply, Pin 23 (VDD1_3V3)
High	1.5			V	
Low			0.9	V	

PLL1 Distribution Clock Outputs (OUT1_0x to OUT1_9x)

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL MODE					Specifications assume a 100 Ω termination across the differential output pins
Output Frequency			400	MHz	
Rise/Fall Time (20% to 80%)		120	170	ps	Listed values are for the edge (rising or falling) with the lesser rate of change ($|\delta v/\delta t|$)
Duty Cycle					
Up to f_{OUT} = 400 MHz	45	50	55	%	
Differential Output Voltage Swing		950		mV	Magnitude of voltage across pins; output driver static
Common-Mode Output Voltage		870		mV	Output driver static
CMOS MODE					
Output Frequency			150	MHz	10 pF load
Rise/Fall Time (20% to 80%)		1.0		ns	10 pF load; listed value is for the edge (rising or falling) with the lesser rate of change ($|\delta v/\delta t|$)
Duty Cycle		50		%	10 pF load
Output Voltage High (V_{OH})	V_{DD} − 0.2			V	Relative to the VDD1_03, VDD1_47, and VDD1_89 pins, with the output driver static and I_{OH} = 1 mA
Output Voltage Low (V_{OL})			0.2	V	Output driver static and I_{OL} = 1 mA

PLL1 Output Timing Skew Matrix (HSTL Mode)

Entries in Table 8 are typical with units of pico seconds (ps) and only apply with a channel divider input frequency less than 650 MHz. Any blank cell shown in Table 8 indicates an empty space in the matrix.

Table 8.

OUT1_x[1]	Group 1A				Group 1B				Group 1C	
	0	1	2	3	4	5	6	7	8	9
0		20	20	20	100	100	100	100	100	100
1			20	20	100	100	100	100	100	100
2				20	100	100	100	100	100	100
3					100	100	100	100	100	100
4						20	20	20	100	100
5							20	20	100	100
6								20	100	100
7									100	100
8										20
9										

[1] OUT1_x refers to one of the 10 output channels associated with PLL1.

PLL1 Output Timing Skew Matrix (CMOS Mode)

Entries in Table 9 are typical with units of pico seconds (ps) and only apply with a channel divider input frequency less than 650 MHz. The typical pin load is 10 pF. Any blank cell shown in Table 9 indicates an empty space in the matrix.

Table 9.

OUT1_x[1]	Group 1A				Group 1B				Group 1C	
	0	1	2	3	4	5	6	7	8	9
0		20	20	20	100	100	100	100	100	100
1			20	20	100	100	100	100	100	100
2				20	100	100	100	100	100	100
3					100	100	100	100	100	100
4						20	20	20	100	100
5							20	20	100	100
6								20	100	100
7									100	100
8										20
9										

[1] OUT1_x refers to one of the 10 output channels associated with PLL1.

PLL1 Output Isolation, Group to Group

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
GROUP TO GROUP ISOLATION					Indicates the worst spur occurring in any channel of the noninterferer groups; all outputs of all groups are active and configured as HSTL
Group 1A Interferer		65		dB	Group 1A = 153.6 MHz, Group 1B = 122.88 MHz, Group 1C = 122.88 MHz
Group 1B Interferer		64		dB	Group 1A = 122.88 MHz, Group 1B = 153.6 MHz, Group 1C = 122.88 MHz
Group 1C Interferer		66		dB	Group 1A = 122.88 MHz, Group 1B = 122.88 MHz, Group 1C = 153.6 MHz

PLL1, Fixed Delay Mode

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RELATIVE INPUT/OUTPUT DELAY					
External VCXO					f_{VCXO} = 122.88 MHz, f_R = 15.36 MHz, f_{OUT} = 15.36 MHz
Group 1A Feedback					From REF1_A/REF1_B to any Group 1A output
Differential Reference	1.60		2.45	ns	
3.3 V CMOS Reference	0.82		1.48	ns	
2.5 V CMOS Reference	0.64		1.37	ns	
Group 1B Feedback					From REF1_A/REF1_B to any Group 1B output
Differential Reference	1.56		2.38	ns	
3.3 V CMOS Reference	0.76		1.41	ns	
2.5 V CMOS Reference	0.64		1.31	ns	
Group 1C Feedback					From REF1_A/REF1_B to any Group 1C output
Differential Reference	1.79		2.60	ns	
3.3 V CMOS Reference	0.94		1.58	ns	
2.5 V CMOS Reference	0.84		1.41	ns	
Internal VCO					f_R = 122.88 MHz, f_{OUT} = 122.88 MHz
Group 1A Feedback					From REF1_A/REF1_B to any Group 1A output
Differential Reference	1.09		2.23	ns	
3.3 V CMOS Reference	0.36		1.64	ns	
2.5 V CMOS Reference	0.27		1.51	ns	
Group 1B Feedback					From REF1_A/REF1_B to any Group 1B output
Differential Reference	1.01		2.16	ns	
3.3 V CMOS Reference	0.28		1.57	ns	
2.5 V CMOS Reference	0.20		1.43	ns	
Group 1C Feedback					From REF1_A/REF1_B to any Group 1C output
Differential Reference	1.14		2.32	ns	
3.3 V CMOS Reference	0.44		1.70	ns	
2.5 V CMOS Reference	0.37		1.56	ns	

PLL1 Internal VCO

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INTERNAL VCO					
Frequency Range	3500	3686	3900	MHz	
Gain		53		MHz/V	

PLL1 PFD and Charge Pump

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MAXIMUM PFD FREQUENCY					
1.8 V Charge Pump (Internal VCO)					
Integer Mode			260	MHz	
Fractional Mode			60	MHz	
3.3 V Charge Pump (for External VCXO)			40	MHz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
3.3 V CHARGE PUMP CURRENT					These charge pump specifications are only applicable to the 3.3 V charge pump, which draws its power from Pin 23 (VDD1_3V3)
I_{CP} Sink/Source					Programmable via Register 0x0101, Bits[D4:D2]
Highest Programmable Value		±5.0		mA	
Lowest Programmable Value		±0.625		mA	
I_{CP} High Impedance Mode Leakage		0.5		nA	
Sink and Source Current Matching		10		%	$0.8 V < V_{CP} < V_{DD} - 0.8 V$
I_{CP} vs. V_{CP}		11		%	$0.8 V < V_{CP} < V_{DD} - 0.8 V$
I_{CP} vs. Temperature		2		%	$V_{CP} = V_{DD}/2$
PLL FIGURE OF MERIT (FOM)		−221		dBc/Hz	Applies to wide loop bandwidth mode (see the PLL1 Loop 2 Wide Bandwidth Configuration section) measured at 500 kHz offset relative to the output frequency under the following conditions: f_R = 245.76 MHz (differential input), f_{OUT} = 122.88 MHz (HSTL output), integer-N PLL mode, internal VCO, and loop bandwidth = 500 kHz

PLL1 RFIN1_x Inputs

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL MODE					
Input Frequency Range			400	MHz	
Input Sensitivity	200			mV p-p	Capacitive coupling recommended
Input Slew Rate	100			V/µs	Minimum limit imposed for jitter performance (when using a sinusoidal source, for example)
Common-Mode Internally Generated Bias Voltage		0.65		V	
Differential Input Resistance		5.6		kΩ	
Differential Input Capacitance		3		pF	
CMOS MODE, SINGLE-ENDED INPUT					
Input Frequency Range			400	MHz	
Input Voltage					
High	1.2			V	
Low			0.6	V	
Hysteresis		300		mV	
Input Resistance		5		MΩ	
Input Capacitance		3		pF	

PLL1 Jitter Generation

The jitter integration bandwidth is from 12 kHz to 20 MHz.

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ABSOLUTE TIME JITTER					
Fractional Mode		0.462		ps rms	f_R = 10 MHz, f_{OUT} = 122.88 MHz, f_{LOOP} = 90 kHz
Integer Mode		0.360		ps rms	f_R = 15.36 MHz, f_{OUT} = 122.88 MHz, f_{LOOP} = 100 kHz
Wide Loop Bandwidth Integer Mode[1]		0.204		ps rms	f_R = 122.88 MHz, f_{OUT} = 122.88 MHz, f_{LOOP} = 300 kHz
External VCXO Mode		0.145		ps rms	f_R = 10 MHz, f_{OUT} = 122.88 MHz, f_{LOOP} = 100 Hz
ADDITIVE TIME JITTER					Additive jitter contribution is from the RFIN1_x input to the OUT_x output, excluding the VCXO contribution
External VCXO Mode		0.125		ps rms	f_{VCXO} = 122.88 MHz, f_{OUT} = 122.88 MHz

[1] See the PLL1 Loop 2 Wide Bandwidth Configuration section.

PLL1 Spurious Performance

Entries in Table 16 indicate the worst spur measured between dc and 1 GHz on any PLL1 output for the given conditions.

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SPURIOUS PERFORMANCE					
ROM Profile 4		−85		dBc	PLL1: f_R = 122.88 MHz, f_{LOOP} = 300 kHz; PLL2: f_R = 50 MHz
ROM Profile 5		−85		dBc	PLL1: f_R = 10 MHz, f_{VCXO} = 122.88 MHz, f_{LOOP} = 100 Hz; PLL2: f_R = 50 MHz

PLL1 Start-Up Time

Table 17.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
START-UP TIME—INTERNAL VCO					Time from application of power (90% of nominal) to first output clock edge after PLL1 is locked and the outputs are synchronized
f_R = 122.88 MHz, f_{OUT} = 122.88 MHz, f_{PFD} = 122.88 MHz, f_{LOOP} = 300 kHz		25		ms	
f_R = 10 MHz, f_{OUT} = 122.88 MHz, f_{PFD} = 10 MHz, f_{LOOP} = 90 kHz, Fractional-N PLL Mode		35		ms	
START-UP TIME—EXTERNAL VCXO					Time from application of power (90% of nominal) to first output clock edge after PLL1 is locked
f_R = 10 MHz, f_{OUT} = 122.88 MHz, f_{PFD} = 80 kHz, f_{LOOP} = 130 Hz		840		ms	

PLL2 CHARACTERISTICS

PLL2 Reference Input (REF2_x)

Table 18.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE CLOCK INPUT PATH					
Input Frequency Range	9.5		250	MHz	
Input Sensitivity	200			mV p-p	
Input Slew Rate	100			V/µs	Minimum limit imposed for jitter performance
Common-Mode Internally Generated Bias Voltage		1.1		V	
Hysteresis		95		mV	
Differential Input Capacitance		3		pF	
Differential Input Resistance	1			kΩ	
Duty Cycle	45		55	%	Required for input frequencies below 20 MHz when ×2 frequency multiplier is in use
CRYSTAL MOTIONAL RESISTANCE			100	Ω	Use a fundamental mode AT-cut crystal when operating REF2_x as a crystal resonator input

PLL2 Distribution Clock Outputs (OUT2_0x to OUT2_11x)

Table 19.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL MODE					Specifications assume a 100 Ω termination across differential output pins
Output Frequency			400	MHz	
Rise/Fall Time (20% to 80%)		120	170	ps	Listed values are for the edge (rising or falling) with the lesser rate of change ($|δv/δt|$)
Duty Cycle					
Up to f_{OUT} = 400 MHz	45	50	55	%	
Differential Output Voltage Swing		950		mV	Magnitude of voltage across pins; output driver static
Common-Mode Output Voltage		870		mV	Output driver static
CMOS MODE					
Output Frequency			150	MHz	10 pF load
Rise/Fall Time (20% to 80%)		1.0		ns	10 pF load; listed value is for the edge (rising or falling) with the lesser rate of change ($|δv/δt|$)
Duty Cycle		50		%	10 pF load
Output Voltage High (V_{OH})	V_{DD} − 0.2			V	Relative to the VDD2_01, VDD2_24, VDD2_57, and VDD2_811 pins, with output driver static and I_{OH} = 1 mA
Output Voltage Low (V_{OL})			0.2	V	Output driver static and I_{OL} = 1 mA

PLL2 Output Timing Skew Matrix (HSTL Mode)

Entries in Table 20 are typical with units of picoseconds (ps) and only apply with a channel divider input frequency less than 650 MHz. Any blank cell shown in Table 20 indicates an empty space in the matrix.

Table 20.

OUT2_x[1]	Group 2A		Group 2B			Group 2C			Group 2D			
	0	1	2	3	4	5	6	7	8	9	10	11
0		20	100	100	100	100	100	100	100	100	100	100
1			100	100	100	100	100	100	100	100	100	100
2				20	20	100	100	100	100	100	100	100
3					20	100	100	100	100	100	100	100
4						100	100	100	100	100	100	100
5							20	20	100	100	100	100
6								20	100	100	100	100
7									100	100	100	100
8										20	20	20
9											20	20
10												20
11												

[1] OUT2_x refers to one of the 12 output channels associated with PLL2.

PLL2 Output Timing Skew Matrix (CMOS Mode)

Entries in Table 21 are typical with units of picoseconds (ps) and only apply with a channel divider input frequency less than 650 MHz. The typical pin load is 10 pF. Any blank cell shown in Table 21 indicates an empty space in the matrix.

Table 21.

OUT2_x[1]	Group 2A		Group 2B			Group 2C			Group 2D			
	0	1	2	3	4	5	6	7	8	9	10	11
0		20	100	100	100	100	100	100	100	100	100	100
1			100	100	100	100	100	100	100	100	100	100
2				20	20	100	100	100	100	100	100	100
3					20	100	100	100	100	100	100	100
4						100	100	100	100	100	100	100
5							20	20	100	100	100	100
6								20	100	100	100	100
7									100	100	100	100
8										20	20	20
9											20	20
10												20
11												

[1] OUT2_x refers to one of the 12 output channels associated with PLL2.

PLL2 Output Isolation, Group to Group

Table 22.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
GROUP TO GROUP ISOLATION					Indicates the worst spur occurring in any channel of the noninterferer groups; all outputs of all groups active and configured as HSTL
Group 2A Interferer		70		dB	Group 2A = 125 MHz, Group 2B = 156.25 MHz, Group 2C = 156.25 MHz, Group 2D = 156.25 MHz
Group 2B Interferer		66		dB	Group 2A = 156.25 MHz, Group 2B = 125 MHz, Group 2C = 156.25 MHz, Group 2D = 156.25 MHz
Group 2C Interferer		65		dB	Group 2A = 156.25 MHz, Group 2B = 156.25 MHz, Group 2C = 125 MHz, Group 2D = 156.25 MHz
Group 2D Interferer		63		dB	Group 2A = 156.25 MHz, Group 2B = 156.25 MHz, Group 2C = 156.25 MHz, Group 2D = 125 MHz

PLL2 VCO and PFD Characteristics

Table 23.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VCO FREQUENCY RANGE	2400		2500	MHz	An additional 200 ppm margin is allowed beyond these limits to accommodate input reference drift
PLL FIGURE OF MERIT (FOM)		−222		dBc/Hz	Measured at 500 kHz offset from the output frequency under the following conditions: f_R = 50 MHz, 3.3 V CMOS (single-ended input), f_{OUT} = 156.25 MHz, (HSTL output)
PFD FREQUENCY RANGE			125	MHz	

PLL2 Jitter Generation

The jitter integration bandwidth is from 12 kHz to 20 MHz.

Table 24.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
JITTER GENERATION					
f_R = 25 MHz, f_{OUT} = 156.25 MHz		0.566		ps rms	
f_R = 50 MHz, f_{OUT} = 156.25 MHz		0.337		ps rms	

PLL2 Spurious Performance

Entries in Table 25 indicate the worst spur measured between dc and 1 GHz on any PLL2 output for the given conditions.

Table 25.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SPURIOUS PERFORMANCE					
ROM Profile 4					PLL1: f_R = 122.88 MHz, f_{LOOP} = 300 kHz; PLL2: f_R = 50 MHz
OUT2_0 to OUT2_4		−61		dBc	
OUT2_5 to OUT2_7		−69		dBc	
OUT2_8 to OUT2_11		−78		dBc	
ROM Profile 5					PLL1: f_R = 10 MHz, f_{VCXO} = 122.88 MHz, f_{LOOP} = 100 Hz; PLL2: f_R = 50 MHz; PLL3: f_R = 10 MHz, C_{LOAD} = 10 pF on OUT3_1P
OUT2_0		−76		dBc	
OUT2_1		−65		dBc	
OUT2_2 to OUT2_3		−69		dBc	
OUT2_4 to OUT2_11		−79		dBc	

PLL2 Start-Up Time

Table 26.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
START-UP TIME					The time from the application of power (90% of nominal) to the first output clock edge (PLL2 is locked and outputs are synchronized)
f_R = 25 MHz, f_{OUT} = 156.25 MHz, f_{PFD} = 25 MHz		50		ms	

PLL3 CHARACTERISTICS

PLL3 Reference Input (REF3_x)

Table 27.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE INPUT PATH					
Input Frequency Range	9.5		100	MHz	
Input Sensitivity	200			mV p-p	
Minimum Input Slew Rate	100			V/μs	Minimum limit imposed for jitter performance
Common-Mode, Internally Generated Bias Voltage		1.16		V	
Hysteresis		70		mV	
Differential Input Capacitance		3		pF	
Differential Input Resistance		4.1		kΩ	
Duty Cycle	47		53	%	Required for input frequencies below 20 MHz when using a frequency scale factor of either 2 or 2/3
CRYSTAL MOTIONAL RESISTANCE			100	Ω	Use a fundamental mode AT-cut crystal when operating REF3_x as a crystal resonator input

PLL3 Outputs OUT3_0

Table 28.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
1.8 V SUPPLY (CMOS)					
Output Frequency			150	MHz	10 pF load
Rise/Fall Time (20% to 80%)		1.0		ns	10 pF load; listed value is for the edge (rising or falling) with the lesser rate of change ($|\delta v/\delta t|$)
Duty Cycle		50		%	10 pF load
Output Voltage High (V_{OH})	$V_{DD} - 0.2$			V	Relative to VDD3_01 (Pin 66) with output driver static and I_{OH} = 1 mA
Output Voltage Low (V_{OL})			0.2	V	Output driver static and I_{OL} = 1 mA
3.3 V SUPPLY (CMOS)					
Output Frequency			200	MHz	10 pF load
Rise/Fall Time (20% to 80%)		0.7		ns	10 pF load; listed value is for the edge (rising or falling) with the lesser rate of change ($|\delta v/\delta t|$)
Duty Cycle		50		%	10 pF load
Output Voltage High (V_{OH})	$V_{DD} - 0.2$			V	Relative to VDD3_3V3 (Pin 67) with output driver static and I_{OH} = 1 mA
Output Voltage Low (V_{OL})			0.2	V	Output driver static and I_{OL} = 1 mA

PLL3 Outputs (OUT3_1x)

Table 29.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL MODE					
Output Frequency			400	MHz	
Rise/Fall Time (20% to 80%)		120	170	ps	100 Ω termination across the output pins; listed values are for the edge (rising or falling) with the lesser rate of change ($|\delta v/\delta t|$)
Duty Cycle	45	50	55	%	
Differential Output Voltage Swing		925		mV	Magnitude of voltage across the pins; output driver static
Common-Mode Output Voltage		850		mV	Output driver static

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS MODE					
Output Frequency			400	MHz	
Rise/Fall Time (20% to 80%)		160		ps	100 Ω termination across the output pair; listed value is for the edge (rising or falling) with the lesser rate of change ($|\delta v/\delta t|$)
Duty Cycle	45	50	55	%	
Differential Output Voltage Swing					
Balanced, V_{OD}	247		454	mV	Voltage swing between the output pins; output driver static
Unbalanced, ΔV_{OD}			50	mV	Absolute difference between the voltage swing of the OUT3_xP pin and the OUT3_xN pin; output driver static
Offset Voltage					
Common-Mode, V_{OS}	1.125	1.26	1.375	V	Output driver static
Common-Mode Difference, ΔV_{OS}			50	mV	Voltage difference between the OUT3_xP pin and the OUT3_xN pin; output driver static
Short-Circuit Output Current		13	24	mA	Output driver static
CMOS MODE					
1.8 V Supply					
Output Frequency			150	MHz	10 pF load
Rise/Fall Time (20% to 80%)		1.0		ns	10 pF load; listed value is for the edge (rising or falling) with the lesser rate of change ($|\delta v/\delta t|$)
Duty Cycle		50		%	10 pF load
Output Voltage High (V_{OH})	$V_{DD} - 0.2$			V	Relative to VDD3_01 (Pin 66) with output driver static and $I_{OH} = 1$ mA
Output Voltage Low (V_{OL})			0.2	V	Output driver static and $I_{OL} = 1$ mA
3.3 V Supply					
Output Frequency			200	MHz	10 pF load
Rise/Fall Time (20% to 80%)		0.7		ns	10 pF load; listed value is for the edge (rising or falling) with the lesser rate of change ($|\delta v/\delta t|$)
Duty Cycle		50		%	10 pF load
Output Voltage High (V_{OH})	$V_{DD} - 0.2$			V	Relative to VDD3_3V3 (Pin 67) with output driver static and $I_{OH} = 1$ mA
Output Voltage Low (V_{OL})			0.2	V	Output driver static and $I_{OL} = 1$ mA

PLL3 VCO and PFD Characteristics

The specifications in Table 30 apply to both the input and output PLLs of PLL3.

Table 30.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VCO FREQUENCY RANGE	720		805	MHz	An additional 200 ppm margin is allowed beyond these limits to accommodate input reference drift
PLL FIGURE OF MERIT (FOM)		−215		dBc/Hz	Measured at 100 kHz offset from the output frequency under the following conditions: $f_R = 10$ MHz (3.3 V CMOS single-ended input), $f_{OUT} = 125$ MHz (HSTL output)
PFD FREQUENCY RANGE	9.5		100	MHz	

PLL3 Spurious Performance

Entries in Table 31 indicate the worst spur measured between dc and 600 MHz on OUT3_1P for the given conditions.

Table 31.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SPURIOUS PERFORMANCE					
ROM Profile 4					PLL1: f_R = 122.88 MHz, f_{LOOP} = 300 kHz; PLL2: f_R = 50 MHz
OUT2_0 to OUT2_4		−61		dBc	
OUT2_5 to OUT2_7		−69		dBc	
OUT2_8 to OUT2_11		−78		dBc	
ROM Profile 5					PLL1: f_R = 10 MHz, f_{VCXO} = 122.88 MHz, f_{LOOP} = 100 Hz; PLL2: f_R = 50 MHz; PLL3: f_R = 10 MHz, C_{LOAD} = 10 pF on OUT3_1P
OUT2_0		−76		dBc	
OUT2_1		−65		dBc	
OUT2_2 to OUT2_3		−69		dBc	
OUT2_4 to OUT2_11		−79		dBc	

PLL3 Jitter Generation

Unless otherwise specified the following test conditions apply: PLL1 configured with OUT1_0 to OUT1_9 operating at 122.88 MHz in HSTL mode; PLL2 configured with f_{REF} = 50 MHz, f_{VCO} = 2.5 GHz, and OUT2_0 to OUT2_11 operating at 125 MHz in HSTL mode; PLL3 configured for single loop operation with OUT3_0 disabled. Measurements are valid with the PLL2 input reference locked to an integer multiple of the PLL3 input reference frequency to within 4.8 ppm.

Table 32.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
JITTER GENERATION					
f_R = 25 MHz; f_{OUT} = 100 MHz					
OUT1_8x and OUT1_9x Disabled		1.78		ps rms	
OUT1_8x and OUT1_9x Active		3.17		ps rms	
f_R = 10 MHz; f_{OUT} = 125 MHz					
PLL1 and PLL2 Powered Down		2.69		ps rms	
OUT1_8x and OUT1_9x Disabled		2.95		ps rms	
OUT1_8x and OUT1_9x Active		5.20		ps rms	

PLL3 Start-Up Time

The PPL3 start-up time is the time from the application of power (90% of nominal) to the first output clock edge (PLL3 is locked and the outputs are synchronized).

Table 33.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
START-UP TIME					
f_R = 10 MHz, f_{OUT} = 25 MHz, f_{PFD} = 10 MHz		20		ms	

SERIAL CONTROL PORT

Table 34.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT (SCLK, SDIO, $\overline{CS}$)					
1.8 V Supply					DVDD_IO (Pin 18) powered with 1.8 V
Input Voltage					
Logic 1	1.3			V	
Logic 0			0.6	V	
Input Current (I_{INH}, I_{INL})	−2		+2	μA	
Input Capacitance		3		pF	
3.3 V Supply					DVDD_IO (Pin 18) powered with 3.3 V
Input Voltage					
Logic 1	1.3			V	
Logic 0			0.6	V	
Input Current (I_{INH}, I_{INL})	−2		+2	μA	
Input Capacitance		3		pF	
OUTPUT (SDIO)					
1.8 V Supply					DVDD_IO (Pin 18) powered with 1.8 V
Output Voltage					
Logic 1	V_{DD} − 0.2			V	1 mA load current
Logic 0			0.2	V	1 mA load current
3.3 V Supply					DVDD_IO (Pin 18) powered with 3.3 V
Output Voltage					
Logic 1	V_{DD} − 0.2			V	1 mA load current
Logic 0			0.2	V	1 mA load current

Serial Control Port Timing

Table 35.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
1.8 V SUPPLY					DVDD_IO (Pin 18) powered with 1.8 V
SCLK					
Clock Rate, $1/t_{SCLK}$			50	MHz	
Pulse Width High, t_{HIGH}	2.1			ns	
Pulse Width Low, t_{LOW}	1.7			ns	
SDIO to SCLK Setup, t_{DS}	0.3			ns	
SCLK to SDIO Hold, t_{DH}	1.0			ns	
SCLK to Valid SDIO, t_{DV}	6.5			ns	
$\overline{CS}$ to SCLK Setup (t_S) and Hold (t_H)	1.1			ns	
$\overline{CS}$ Minimum Pulse Width High	1.4			ns	
3.3 V SUPPLY					DVDD_IO (Pin 18) powered with 3.3 V
SCLK					
Clock Rate, $1/t_{SCLK}$			50	MHz	
Pulse Width High, t_{HIGH}	0.8			ns	
Pulse Width Low, t_{LOW}	2.5			ns	
SDIO to SCLK Setup, t_{DS}	1.8			ns	
SCLK to SDIO Hold, t_{DH}	0.4			ns	
SCLK to Valid SDIO, t_{DV}	6.5			ns	
$\overline{CS}$ to SCLK Setup (t_S) and Hold (t_H)	2.4			ns	
$\overline{CS}$ Minimum Pulse Width High	3.0			ns	

ABSOLUTE MAXIMUM RATINGS

Table 36.

| Parameter	Rating
Analog Supply Voltage	
3.3 V Supply Pins	3.6 V
1.8 V Supply Pins	2 V
Maximum Digital Input Voltage	−0.5 V to VDD3 + 0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS
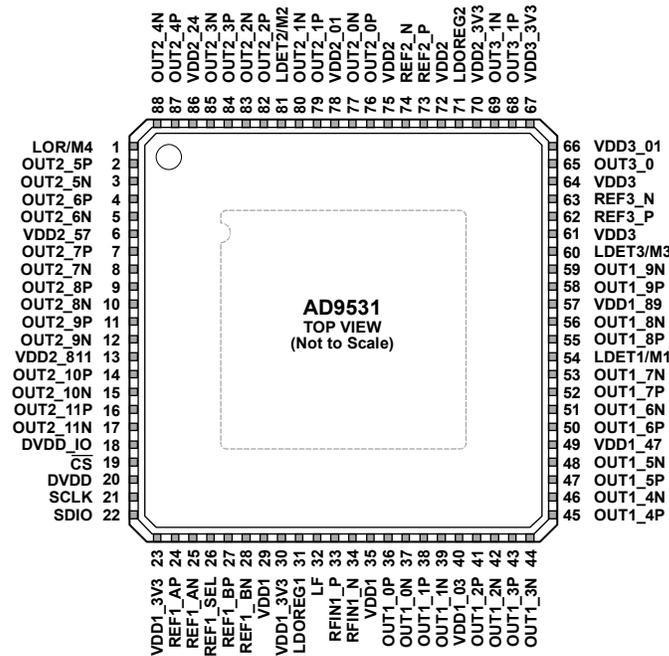
NOTES
1. THE EXPOSED PAD ON THE BOTTOM OF THE PACKAGE MUST BE SOLDERED
   TO GROUND TO ACHIEVE THE SPECIFIED THERMAL PERFORMANCE.

Figure 2. Pin Configuration

Table 37. Pin Function Descriptions

Pin No.	Mnemonic	Supply Domain	Description
1	LOR/M4	1.8 V/3.3 V	Loss of Reference Pin. This is a multifunction pin.
2	OUT2_5P	1.8 V	PLL2 Output 5 (Positive).
3	OUT2_5N	1.8 V	PLL2 Output 5 (Negative).
4	OUT2_6P	1.8 V	PLL2 Output 6 (Positive).
5	OUT2_6N	1.8 V	PLL2 Output 6 (Negative).
6	VDD2_57	1.8 V	PLL2 Power Supply for Channel Outputs OUT2_5 Through OUT2_7.
7	OUT2_7P	1.8 V	PLL2 Output 7 (Positive).
8	OUT2_7N	1.8 V	PLL2 Output 7 (Negative).
9	OUT2_8P	1.8 V	PLL2 Output 8 (Positive).
10	OUT2_8N	1.8 V	PLL2 Output 8 (Negative).
11	OUT2_9P	1.8 V	PLL2 Output 9 (Positive).
12	OUT2_9N	1.8 V	PLL2 Output 9 (Negative).
13	VDD2_811	1.8 V	PLL2 Power Supply for Channel Outputs OUT2_8 Through OUT2_11.
14	OUT2_10P	1.8 V	PLL2 Output 10 (Positive).
15	OUT2_10N	1.8 V	PLL2 Output 10 (Negative).
16	OUT2_11P	1.8 V	PLL2 Output 11 (Positive).
17	OUT2_11N	1.8 V	PLL2 Output 11 (Negative).
18	DVDD_IO	1.8 V/3.3 V	Power Supply for Serial Input/Output Pins.
19	$\overline{CS}$	1.8 V/3.3 V	Chip Select Pin.
20	DVDD	1.8 V	Power Supply for SPI Registers and PLL1 Digital Σ-Δ Modulator (SDM).
21	SCLK	1.8 V/3.3 V	Serial Programming Clock.
22	SDIO	1.8 V/3.3 V	Serial Data Input/Output.
23	VDD1_3V3	3.3 V	PLL1 REF_A/REF_B Input Receiver Power Supply.
24	REF1_AP	3.3 V	PLL1 REF_A Input (Positive). Use this pin when operating the REF_A input in single-ended mode.

Pin No.	Mnemonic	Supply Domain	Description
25	REF1_AN	3.3 V	PLL1 REF_A Input (Negative). When operating the REF_A input in single-ended mode, this pin becomes inoperative (internally disconnected) and must be connected to ground or left floating.
26	REF1_SEL	3.3 V	PLL1 Manual REF_A/REF_B Input Select.
27	REF1_BP	3.3 V	PLL1 REF_B Input (Positive). Use this pin when operating the REF_B input in single-ended mode.
28	REF1_BN	3.3 V	PLL1 REF_B Input (Negative). When operating the REF_B input in single-ended mode, this pin becomes inoperative (internally disconnected) and must be connected to ground or left floating.
29	VDD1	1.8 V	PLL1 Power Supply for the Input Circuitry Following the REF1_A/REF1_B Receivers.
30	VDD1_3V3	3.3 V	PLL1 Power Supply for the Low Dropout (LDO) Input.
31	LDOREG1	3.3 V	PLL1 LDO Regulated Supply for the VCO Core. Connect a 220 nF capacitor between this pin and ground.
32	LF	3.3 V	Loop Filter.
33	RFIN1_P	3.3 V	PLL1 External VCO/VCXO Input (Positive).
34	RFIN1_N	3.3 V	PLL1 External VCO/VCXO Input (Negative).
35	VDD1	1.8 V	PLL1 Power Supply for the Output Distribution Circuitry.
36	OUT1_0P	1.8 V	PLL1 Output 0 (Positive).
37	OUT1_0N	1.8 V	PLL1 Output 0 (Negative).
38	OUT1_1P	1.8 V	PLL1 Output 1 (Positive).
39	OUT1_1N	1.8 V	PLL1 Output 1 (Negative).
40	VDD1_03	1.8 V	PLL1 Power Supply for Channel Outputs OUT1_0 Through OUT1_3.
41	OUT1_2P	1.8 V	PLL1 Output 2 (Positive).
42	OUT1_2N	1.8 V	PLL1 Output 2 (Negative).
43	OUT1_3P	1.8 V	PLL1 Output 3 (Positive).
44	OUT1_3N	1.8 V	PLL1 Output 3 (Negative).
45	OUT1_4P	1.8 V	PLL1 Output 4 (Positive).
46	OUT1_4N	1.8 V	PLL1 Output 4 (Negative).
47	OUT1_5P	1.8 V	PLL1 Output 5 (Positive).
48	OUT1_5N	1.8 V	PLL1 Output 5 (Negative).
49	VDD1_47	1.8 V	PLL1 Power Supply for Channel Outputs OUT1_4 Through OUT1_7.
50	OUT1_6P	1.8 V	PLL1 Output 6 (Positive).
51	OUT1_6N	1.8 V	PLL1 Output 6 (Negative).
52	OUT1_7P	1.8 V	PLL1 Output 7 (Positive).
53	OUT1_7N	1.8 V	PLL1 Output 7 (Negative).
54	LDET1/M1	1.8 V/3.3 V	PLL1 Lock Detect. This is a multifunction pin.
55	OUT1_8P	1.8 V	PLL1 Output 8 (Positive).
56	OUT1_8N	1.8 V	PLL1 Output 8 (Negative).
57	VDD1_89	1.8 V	PLL1 Power Supply for Channel Outputs OUT1_8 Through OUT1_9.
58	OUT1_9P	1.8 V	PLL1 Output 9 (Positive).
59	OUT1_9N	1.8 V	PLL1 Output 9 (Negative).
60	LDET3/M3	1.8 V/3.3 V	PLL3 Lock Detect. This is a multifunction pin.
61	VDD3	1.8 V	PLL3 Power Supply for Input Circuitry of the First PLL in the 2 PLL Cascade of PLL3.
62	REF3_P	1.8 V	PLL3 Reference Input (Positive).
63	REF3_N	1.8 V	PLL3 Reference Input (Negative).
64	VDD3	1.8 V	PLL3 Power Supply for the Output Circuitry of PLL3A and Input Circuitry of PLL3B.
65	OUT3_0	1.8 V/3.3 V	PLL3 Output 0.
66	VDD3_01	1.8 V	PLL3 Power Supply for Channel Outputs OUT3_0 Through OUT3_1.
67	VDD3_3V3	3.3 V	PLL3 Power Supply for the Output Circuitry.
68	OUT3_1P	1.8 V/3.3 V	PLL3 Output 1 (Positive).
69	OUT3_1N	1.8 V/3.3 V	PLL3 Output 1 (Negative).
70	VDD2_3V3	3.3 V	PLL2 Power Supply for the LDO Input.
71	LDOREG2	1.8 V	PLL2 LDO Regulated Supply for the VCO Core. Connect a 220 nF capacitor between this pin and ground.

Pin No.	Mnemonic	Supply Domain	Description
72	VDD2	1.8 V	PLL2 Power Supply for the Input Circuitry.
73	REF2_P	1.8 V	PLL2 Reference Input (Positive).
74	REF2_N	1.8 V	PLL2 Reference Input (Negative).
75	VDD2	1.8 V	PLL2 Power Supply for the Output Circuitry.
76	OUT2_0P	1.8 V	PLL2 Output 0 (Positive).
77	OUT2_0N	1.8 V	PLL2 Output 0 (Negative).
78	VDD2_01	1.8 V	PLL2 Power Supply for Outputs OUT2_0 Through OUT2_1.
79	OUT2_1P	1.8 V	PLL2 Output 1 (Positive).
80	OUT2_1N	1.8 V	PLL2 Output 1 (Negative).
81	LDET2/M2	1.8 V/3.3 V	PLL2 Lock Detect. This is a multifunction pin.
82	OUT2_2P	1.8 V	PLL2 Output 2 (Positive).
83	OUT2_2N	1.8 V	PLL2 Output 2 (Negative).
84	OUT2_3P	1.8 V	PLL2 Output 3 (Positive).
85	OUT2_3N	1.8 V	PLL2 Output 3 (Negative).
86	VDD2_24	1.8 V	PLL2 Power Supply for Outputs OUT2_2 Through OUT2_4.
87	OUT2_4P	1.8 V	PLL2 Output 4 (Positive).
88	OUT2_4N	1.8 V	PLL2 Output 4 (Negative).
	EP		Exposed Pad. The exposed pad on the bottom of the package must be soldered to ground to achieve the specified thermal performance.