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Quad Input, 10-Output, Dual DPLL, 1 pps Synchronizer and Jitter Cleaner

Data Sheet **AD9544**

FEATURES

- Dual DPLL synchronizes 1 Hz to 750 MHz physical layer clocks providing frequency translation with jitter cleaning of noisy references
- Complies with ITU-T G.8262 and Telcordia GR-253
- Supports Telcordia GR-1244, ITU-T G.812, G.813, G.823, G.824, and G.825
- Continuous frequency monitoring and reference validation for frequency deviation as low as 50 ppb
- Both DPLLs feature a 24-bit fractional divider with 24-bit programmable modulus
- Programmable digital loop filter bandwidth: 10^{-4} Hz to 1850 Hz
- Automatic and manual holdover and reference switchover, providing zero delay, hitless, or phase buildout operation
- Programmable priority-based reference switching with manual, automatic revertive, and automatic nonrevertive modes supported
- 5 pairs of clock output pins with each pair useable as differential LVDS/HCSL/CML or as 2 single-ended outputs (1 Hz to 500 MHz)
- 2 differential or 4 single-ended input references
- Crosspoint mux interconnects reference inputs to PLLs
- Supports embedded (modulated) input/output clock signals
- Fast DPLL locking modes
- Provides internal capability to combine the low phase noise of a crystal resonator or crystal oscillator with the frequency stability and accuracy of a TCXO or OCXO
- External EEPROM support for autonomous initialization
- Single 1.8 V power supply operation with internal regulation
- Built in temperature monitor/alarm and temperature compensation for enhanced zero delay performance

APPLICATIONS

- SyncE and GPS synchronization and jitter cleanup
- Optical transport networks (OTN), SDH, and macro and small cell base stations
- OTN mapping/demapping with jitter cleaning
- Small base station clocking, including baseband and radio
- Stratum 2, Stratum 3e, and Stratum 3 holdover, jitter cleanup, and phase transient control
- JESD204B support for analog-to-digital converter (ADC) and digital-to-analog converter (DAC) clocking
- Cable infrastructures
- Carrier Ethernet

GENERAL DESCRIPTION

The 10 clock outputs of the AD9544 are synchronized to any one of up to four input references. The digital phase-locked loops (DPLLs) reduce timing jitter associated with the external references. The digitally controlled loop and holdover circuitry continuously generate a low jitter output signal, even when all reference inputs fail.

The AD9544 is available in a 48-lead LFCSP (7 mm × 7 mm) package and operates over the −40°C to +85°C temperature range.

Note that throughout this data sheet, multifunction pins, such as SDO/M5, are referred to either by the entire pin name or by a single function of the pin, for example, M5, when only that function is relevant.

Rev. 0 Document Feedback

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REVISION HISTORY

10/2017—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

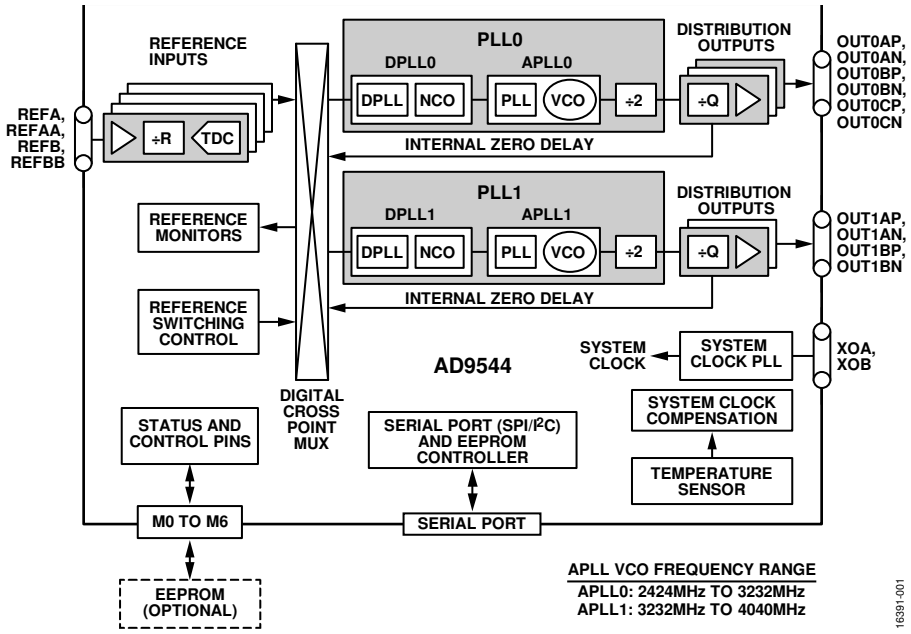

Figure 1.

SPECIFICATIONS

The minimum and maximum values apply for the full range of the supply voltage and operating temperature variations. The typical values apply for VDD = 1.8 V and T_A = 25°C, unless otherwise noted.

SUPPLY VOLTAGE

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
VDDIOA, VDDIOB	1.71	1.8	3.465	V	1.8 V, 2.5 V, and 3.3 V operation supported
VDD	1.71	1.8	1.89	V	

SUPPLY CURRENT

The maximum supply voltage values given in Table 1 are the basis for the maximum supply current specifications. The typical supply voltage values given in Table 1 are the basis for the typical supply current specifications. The minimum supply voltage values given in Table 1 are the basis for the minimum supply current specifications.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT FOR TYPICAL CONFIGURATION					The Typical Configuration specification in Table 3 is the basis for the values shown in this section
I_{VDDIOx}		5	8	mA	Aggregate current for all VDDIOx pins (where x = A or B)
I_{VDD}	260	310	355	mA	Aggregate current for all VDD pins
SUPPLY CURRENT FOR ALL BLOCKS RUNNING CONFIGURATION					The All Blocks Running condition in Table 3 is the basis for the values shown in this section
I_{VDDIOx}		5	8	mA	Aggregate current for all VDDIOx pins (where x = A or B)
I_{VDD}	321	390	430	mA	Aggregate current for all VDD pins

POWER DISSIPATION

The typical values apply for VDD = 1.8 V, and the maximum values apply for VDD = 1.89 V.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION					
Typical Configuration	445	560	671	mW	System clock = 49.152 MHz crystal; two DPLLs active; two 19.44 MHz input references in differential mode; two ac-coupled PLL0 CML output drivers at 245.76 MHz; and two PLL1 CML output drivers at 156.25 MHz
All Blocks Running	548	700	813	mW	System clock = 49.152 MHz crystal; two DPLLs active; two 19.44 MHz input references in differential mode; three ac-coupled PLL0 HCSL output drivers at 400 MHz; and two PLL1 HCSL output drivers at 400 MHz
Full Power-Down		125		mW	Based on the Typical Configuration specification with the power down all bit set to Logic 1
Incremental Power Dissipation					Based on the Typical Configuration specification; the values in this section indicate the change in power due to the indicated operation relative to the Typical Configuration specification
Complete DPLL/APLL On/Off		200		mW	Change in dissipated power relative to the Typical Configuration specification; the blocks, powered down, consist of one reference input, one DPLL, one APLL, two channel dividers, and two output drivers
Incremental Power Dissipation					
Complete DPLL/APLL On/Off		200		mW	Based on the Typical Configuration specification; the values in this section indicate the change in power due to the indicated operation relative to the Typical Configuration specification; the blocks, powered down, consist of one reference input, one DPLL, one APLL, two channel dividers, and two output drivers

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Input Reference On/Off					
Differential (Normal Mode)		20		mW	f_{REF} = 19.44 MHz
Differential (DC-Coupled LVDS)		21		mW	f_{REF} = 19.44 MHz
Single-Ended		13		mW	f_{REF} = 19.44 MHz
Output Distribution Driver On/Off					At 156.25 MHz
15 mA Mode		30		mW	
12 mA Mode		23		mW	
7.5 mA Mode		15		mW	
Auxiliary DPLL On/Off		1		mW	

SYSTEM CLOCK INPUTS, XOA AND XOB

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SYSTEM CLOCK MULTIPLIER					
Output Frequency Range	2250		2415	MHz	The frequency range of the internal voltage controlled oscillator (VCO) places limits on the choice of the system clock input frequency
Phase Frequency Detector (PFD) Rate	20		300	MHz	
SYSTEM CLOCK REFERENCE INPUT PATH					System clock input must be ac-coupled
Input Frequency Range					
System Clock Input Doubler					
Disabled	20		300	MHz	Support of oven controlled crystal oscillators (OCXOs) < 20 MHz is possible using the auxiliary DPLL for system clock frequency compensation
Enabled	16		150	MHz	
Self Biased Common-Mode Voltage		0.75		V	Internally generated
Input Voltage					For dc-coupled, single-ended operation
High	0.9			V	
Low			0.5	V	
Differential Input Voltage Sensitivity	250			mV p-p	Minimum voltage swing required (as measured with a differential probe) across the XOA/XOB pins to ensure switching between logic states; the instantaneous voltage on either pin must not exceed 1.2 V; accommodate the single-ended input by ac grounding the complementary input; 800 mV p-p recommended for optimal jitter performance
Slew Rate for Sinusoidal Input	50			V/µs	Minimum input slew rate for device operation; oscillators with square wave outputs are recommended if not using a crystal
System Clock Input Divider (J Divider) Frequency	100			MHz	
System Clock Input Doubler Duty Cycle					Tolerable duty cycle variation on the system clock input when using the frequency doubler
20 MHz to 150 MHz	43	50	57	%	
16 MHz to 20 MHz	47	50	53	%	
Input Resistance		5		kΩ	
QUARTZ CRYSTAL RESONATOR PATH					
Resonator Frequency Range	25		60	MHz	Fundamental mode, AT cut crystal
Crystal Motional Resistance			100	Ω	A maximum motional resistance of 50 Ω , and maximum C_{LOAD} of 8 pF is strongly recommended for crystals >52 MHz

REFERENCE INPUTS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL MODE					Differential mode specifications assume ac coupling of the input signal to the reference input pins
Frequency Range					
Sinusoidal Input			750	MHz	Lower limit dependent on input slew rate
LVPECL Input	1		750×10^6	Hz	Lower limit dependent on ac coupling; 1 Hz is equivalent to 1 pulse per second (pps)
LVDS Input	1		500×10^6	Hz	Assumes an LVDS minimum of 494 mV p-p differential amplitude; lower limit dependent on ac coupling
Slew Rate for Sinusoidal input	20			V/µs	Minimum input slew rate for device operation; jitter degradation may occur for slew rates < 35 V/µs
Common-Mode Input Voltage		0.64		V	Internally generated self bias voltage
Differential Input Amplitude					Peak-to-peak differential voltage swing across pins required to ensure switching between logic levels as measured with a differential probe; instantaneous voltage on either pin must not exceed 1.3 V
f_{IN} < 500 MHz	350		2100	mV p-p	
f_{IN} = 500 MHz to 750 MHz	500		2100	mV p-p	
Differential Input Voltage Hysteresis		55	100	mV	
Input Resistance		16		kΩ	Equivalent differential input resistance
Input Pulse Width					
LVPECL	600			ps	
LVDS	900			ps	
DC-COUPLED, LVDS-COMPATIBLE MODE					Applies for dc-coupling to an LVDS source
Frequency Range	1		450×10^6	Hz	
Common-Mode Input Voltage	1.125		1.375	V	
Differential Input Amplitude	400		1200	mV p-p	Differential voltage across pins required to ensure switching between logic levels; instantaneous voltage on either pin must not exceed the supply rails
Differential Input Voltage Hysteresis		55	100	mV	
Input Resistance		16		kΩ	
Input Pulse Width	1			ns	
SINGLE-ENDED MODE					Single-ended mode specifications assume dc coupling of the input signal to the reference input pins
Frequency Range					
1.2 V AC-Coupled	1		500×10^6	Hz	Lower limit dependent on ac-coupling
1.2 V and 1.8 V CMOS	1		500×10^6	Hz	CMOS specifications assume dc coupling of the input signal to the reference input pins
1.2 V AC-Coupled Common-Mode Voltage		610		mV	Internally generated self-bias voltage
Input Amplitude (Single-Ended, AC-Coupled Mode)	360		1200	mV p-p	Peak-to-peak single-ended voltage swing; instantaneous voltage must not exceed 1.3 V
1.2 V and 1.8 V CMOS Input Voltage					
High, V_{IH}	$0.65 \times V_{REF}$		$1.15 \times V_{REF}$	V	V_{REF} is determined by operating mode of the CMOS input receiver, 1.2 V or 1.8 V
Low, V_{IL}			$0.35 \times V_{REF}$	V	
Input Resistance					
DC-Coupled Single-Ended Mode		30		kΩ	
AC-Coupled Single-Ended Mode		15		kΩ	
Input Pulse Width	900			ps	

REFERENCE MONITORS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE MONITORS					
Reference Monitor					
Loss of Reference Detection Time		$4.9 + 0.13 \times t_{PFD}$		µs	t_{PFD} is the nominal phase detector period, R/f_{REF}, where R is the frequency division factor determined by the R divider, and f_{REF} is the frequency of the active reference
Frequency Out of Range Limits	50		1.5×10^7	ppb	Parts per billion (ppb) is defined as $\Delta f/f_{REF}$, where Δf is the frequency deviation, and f_{REF} is the reference input frequency; programmable with the lower bound, subject to quality of the system clock (or the source of system clock compensation); 1.5×10^7 is equivalent to 1.5%
Validation Timer	0.001		1048	sec	Programmable in 1 ms increments
Excess Jitter Alarm Threshold	1		65535	ns	Programmable in 1 ns increments

DPLL PHASE CHARACTERISTICS

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MAXIMUM OUTPUT PHASE PERTURBATION					Assumes a jitter free reference; satisfies Telcordia GR-1244-CORE requirements; 0 ppm frequency difference between references; reference switch initiated via register map (see the AD9544 Register Map Reference Manual) by faulting the active reference input
Phase Refinement Disabled					50 Hz DPLL loop bandwidth; normal phase margin mode; frequency translation = 19.44 MHz to 155.52 MHz; 49.152 MHz signal generator used for system clock source
Peak		±20	±140	ps	
Steady State					
Phase Buildout Operation		±18	±125	ps	
Hitless Operation		0		ps	
Phase Refinement Enabled					50 Hz DPLL loop bandwidth; high phase margin mode; phase refinement iterations = 4; frequency translation = 19.44 MHz to 155.52 MHz; 49.152 MHz signal generator used for system clock source
Peak		±5	±40	ps	
Steady State					
Phase Buildout Operation		±4	±35	ps	
Hitless Operation		0		ps	
PHASE SLEW LIMITER	0.001		250	µs/sec	See the AN-1420 Application Note, *Phase Buildout and Hitless Switchover with Digital Phase-Locked Loops (DPLLs)*

DISTRIBUTION CLOCK OUTPUTS

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL MODE					All testing is both ac-coupled and dc-coupled
Output Frequency					Frequency range determined by driver functionality; actual frequency synthesis may be limited by the APLL VCO frequency range
CML	1		500×10^6	Hz	Terminated per Figure 33
HCSL	1		500×10^6	Hz	Terminated per Figure 32
Differential Output Voltage Swing					Voltage between output pins measured with output driver static; peak-to-peak differential output amplitude is twice that shown when driver is toggling and measured using a differential probe
Output Current = 7.5 mA					
HCSL	312	368	402	mV	Terminated per Figure 32
CML	257	348	408	mV	Terminated to VDD (nominal 1.8 V) per Figure 33
Output Current = 15 mA					
HCSL	631	745	809	mV	Terminated per Figure 32
CML	578	729	818	mV	Terminated to VDD (nominal 1.8 V) per Figure 33
Common-Mode Output Voltage					
Output Current = 7.5 mA					
HCSL	155	184	201	mV	Terminated per Figure 32
CML	VDD − 208	VDD − 188	VDD − 169	mV	Terminated to VDD (nominal 1.8 V) per Figure 33 (maximum common-mode voltage case occurs at the minimum amplitude)
Output Current = 15 mA					
HCSL	316	372	405	mV	Terminated per Figure 32
CML	VDD − 416	VDD − 371	VDD − 327	mV	Terminated to VDD (nominal 1.8 V) per Figure 33 (maximum common-mode voltage case occurs at the minimum amplitude)
SINGLE-ENDED MODE					
Output Frequency	1		500×10^6	Hz	Frequency range determined by driver functionality; actual frequency synthesis may be limited by the APLL VCO frequency range
Output Current = 12 mA					
Voltage Swing (Peak-to-Peak)					
HCSL Driver Mode	509	584	634	mV	Each output terminated per Figure 37 with $R_L = 50\ \Omega$
CML Driver Mode	456	565	644	mV	Each output terminated per Figure 37 with $R_L = 50\ \Omega$ connected to VDD (nominal 1.8 V) instead of GND
Voltage Swing Midpoint					
HCSL Driver Mode	255	292	317	mV	Each output terminated per Figure 37 with $R_L = 50\ \Omega$
CML Driver Mode	VDD − 325	VDD − 291	VDD − 266	mV	Each output terminated per Figure 37 with $R_L = 50\ \Omega$ connected to VDD (nominal 1.8 V) instead of GND
Output Current = 15 mA					
Voltage Swing (Peak-to-Peak)					
HCSL Driver Mode	645	734	796	mV	Each output terminated per Figure 37 with $R_L = 50\ \Omega$
CML Driver Mode	589	721	815	mV	Each output terminated per Figure 37 with $R_L = 50\ \Omega$ connected to VDD (nominal 1.8 V) instead of GND
Voltage Swing Midpoint					
HCSL Driver Mode	322	367	398	mV	Each output terminated per Figure 37 with $R_L = 50\ \Omega$
CML Driver Mode	VDD − 411	VDD − 367	VDD − 334	mV	Each output terminated per Figure 37 with $R_L = 50\ \Omega$ connected to VDD (nominal 1.8 V) instead of GND

TIME DURATION OF DIGITAL FUNCTIONS

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TIME DURATION OF DIGITAL FUNCTIONS					
EEPROM to Register Download Time		10		ms	Using the Typical Configuration from Table 3
Power-On Reset (POR)			25	ms	Time from power supplies > 80% to release of internal reset
Mx Pin to RESETB Rising Edge Setup Time			1	ns	Mx refers to Pin M0 through Pin M6
Mx Pin to RESETB Rising Edge Hold Time			2	ns	
Multiple Mx Pin Timing Skew			39	ns	Applies only to multibit Mx pin functions
RESETB Falling Edge to Mx Pin High-Z Time			14	ns	
TIME FROM START OF DPLL ACTIVATION TO ACTIVE PHASE DETECTOR OUTPUT					
Untagged Operation			10	t_{PFD}	t_{PFD} is the nominal phase detector period given by R/f_{REF}, where R is the frequency division factor determined by the R divider, and f_{REF} is the frequency of the active reference
Tagged Operation			10	Tag period	Tag period = (tag ratio/f_{TAG}), where f_{TAG} is either f_{REF} (for tagged reference mode) or $f_{FEEDBACK}$ (for all other tagged modes); the tag ratio corresponds to the selection of f_{TAG}

DIGITAL PLL (DPLL0, DPLL1) SPECIFICATIONS

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL PLL					
Digital Phase Detector (DPD) Input Frequency Range	1		2×10^5	Hz	
Loop Filter					
Profile 0					
Bandwidth	0.0001		1850	Hz	Programmable design parameter; (f_{PFD}/bandwidth) ≥ 20
Phase Margin		70		Degrees	
Closed-Loop Peaking		1.1		dB	
Profile 1					
Bandwidth	0.0001		305	Hz	Programmable design parameter; (f_{PFD}/bandwidth) ≥ 20
Phase Margin		88.5		Degrees	
Closed-Loop Peaking			0.1	dB	In accordance with Telcordia GR-253-CORE jitter transfer specifications
DIGITAL PLL NCO Division Ratio					These specifications cover limitations on the DPLLx frequency tuning word (FTW0); the AD9544 evaluation software frequency planning wizard sets these values automatically for the user, and the AD9544 evaluation software is available for download from the AD9544 product page; NCO division = 2^{48}/FTW0, which takes the form INT.FRAC, where INT is the integer portion, and FRAC is the fractional portion
NCO Integer	7		13		This is the integer portion of NCO division ratio
NCO Fraction	0.05		0.95		This is the fractional portion of NCO division ratio

DIGITAL PLL LOCK DETECTION SPECIFICATIONS

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PHASE LOCK DETECTOR					
Threshold Programming Range	10		$2^{24} - 1$	ps	
Threshold Resolution		1		ps	
FREQUENCY LOCK DETECTOR					
Threshold Programming Range	10		$2^{24} - 1$	ps	
Threshold Resolution		1		ps	
PHASE STEP DETECTOR					
Threshold Programming Range	100		$2^{32} - 1$	ps	Setting this value too low causes false triggers
Threshold Resolution		1		ps	

HOLDOVER SPECIFICATIONS

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HOLDOVER SPECIFICATIONS					
Initial Frequency Accuracy		±0.01	±0.1	ppb	AD9544 is configured using Configuration 1 from Table 21; excludes frequency drift of system clock (SYSCLK) source; excludes frequency drift of input reference prior to entering holdover; 160 ms history timer; history holdoff setting of 8; three holdover history features (bits) are enabled: delay history until frequency lock bit, delay history until phase lock bit, and delay holdover history accumulation until not phase slew limited bit
Relative Frequency Accuracy Between Channels					
Cascaded Operation		0		ppb	
History Averaging Window	0.001		268435	sec	

ANALOG PLL (APLL0, APLL1) SPECIFICATIONS

Table 13.

Parameter	Min	Typ	Max	Unit
VCO FREQUENCY RANGE				
Analog PLL0 (APLL0)	2424		3232	MHz
Analog PLL1 (APLL1)	3232		4040	MHz
PHASE FREQUENCY DETECTOR (PFD) INPUT FREQUENCY RANGE	162		350	MHz
LOOP BANDWIDTH		260		kHz
PHASE MARGIN		68		Degrees

OUTPUT CHANNEL DIVIDER SPECIFICATIONS

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT PHASE ADJUST STEP SIZE	1			t_{VCO}	t_{VCO} = 1/(APLLx VCO frequency), where x = 0, 1

SYSTEM CLOCK COMPENSATION SPECIFICATIONS

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIRECT COMPENSATION					
Resolution		0.028		ppt	ppt is parts per trillion (10^{-12})
CLOSED-LOOP COMPENSATION (AUXILIARY DPLL)					
Phase Detector Frequency	2		200	kHz	
Loop Bandwidth	0.1		2×10^3	Hz	
Reference Monitor Threshold		5		%	

TEMPERATURE SENSOR SPECIFICATIONS

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE					
Accuracy					T_A = −50°C to +110°C
Absolute		5		°C	
Relative		1.7		%	
Resolution		0.0078		°C	16-bit (signed) resolution
Conversion Time		0.18		ms	
REPEATABILITY		±0.02		°C	T_A = 25°C
DRIFT		0.1		°C	500 hour stress test at 100°C

SERIAL PORT SPECIFICATIONS

Serial Port Interface (SPI) Mode

Table 17.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CSB					Valid for VDDIOA = 3.3 V, 1.8 V, and 2.5 V
Input Logic 1 Voltage	VDDIOA – 0.4			V	
Input Logic 0 Voltage			0.4	V	
Input Logic 1 Current		1		µA	
Input Logic 0 Current		1		µA	
SCLK					
Input Logic 1 Voltage	VDDIOA – 0.4			V	
Input Logic 0 Voltage			0.4	V	
Input Logic 1 Current		1		µA	
Input Logic 0 Current		1		µA	
SDIO					
As an Input					
Input Logic 1 Voltage	VDDIOA – 0.4			V	
Input Logic 0 Voltage			0.4	V	
Input Logic 1 Current		1		µA	
Input Logic 0 Current		1		µA	
As an Output					
Output Logic 1 Voltage	VDDIOA – 0.2			V	1 mA load current
Output Logic 0 Voltage			0.2	V	1 mA load current
SDO					
Output Logic 1 Voltage	VDDIOA – 0.2			V	1 mA load current
Output Logic 0 Voltage			0.2	V	1 mA load current
Leakage Current			±1	µA	SDO inactive (high impedance)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TIMING					Valid for VDDIOA = 3.3 V, 1.8 V, and 2.5 V
SCLK					
Clock Rate, $1/t_{CLK}$			50	MHz	
Pulse Width High, t_{HIGH}	5			ns	
Pulse Width Low, t_{LOW}	9			ns	
SDIO to SCLK Setup, t_{DS}	2.2			ns	
SCLK to SDIO Hold, t_{DH}	0			ns	
SCLK to Valid SDIO and SDO, t_{DV}			9	ns	
CSB to SCLK Setup, t_S	1.5			ns	
CSB to SCLK Hold, t_C	0			ns	
CSB Minimum Pulse Width High	1			t_{CLK}	

I²C Mode

Table 18.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDA, SCL (AS INPUTS)					Valid for VDDIOA = 3.3 V, 1.8 V, and 2.5 V
Input Logic 1 Voltage	70			% of VDDIOA	
Input Logic 0 Voltage			0.3 × VDDIOA	V	
Input Current	−10		+10	µA	For V_{IN} = 10% to 90% of VDDIOA
Hysteresis of Schmitt Trigger Inputs	1.5			% of VDDIOA	
SDA (AS OUTPUT)					
Output Logic 0 Voltage			0.2	V	I_{OUT} = 3 mA
Output Fall Time from V_{IH} Minimum to V_{IL} Maximum	$20 + 0.1 \times C_B$		250	ns	10 pF ≤ C_B ≤ 400 pF
TIMING					
SCL Clock Rate			400	kHz	
Bus Free Time Between a Stop and Start Condition, t_{BUF}	1.3			µs	
Repeated Start Condition Setup Time, $t_{SU;STA}$	0.6			µs	
Repeated Hold Time Start Condition, $t_{HD;STA}$	0.6			µs	After this period, the first clock pulse is generated
Stop Condition Setup Time, $t_{SU;STO}$	0.6			µs	
Low Period of the SCL Clock, t_{LOW}	1.3			µs	
High Period of the SCL Clock, t_{HIGH}	0.6			µs	
SCL/SDA Rise Time, t_R	$20 + 0.1 \times C_B$		300	ns	
SCL/SDA Fall Time, t_F	$20 + 0.1 \times C_B$		300	ns	
Data Setup Time, $t_{SU;DAT}$	100			ns	
Data Hold Time, $t_{HD;DAT}$	100			ns	
Capacitive Load for Each Bus Line, C_B			400	pF	

LOGIC INPUT SPECIFICATIONS (RESETB, M0 TO M6)

Table 19.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RESETB					Valid for 3.3 V ≥ VDDIOA ≥ 1.8 V; internal 100 kΩ pull-up resistor
Input High Voltage (V_{IH})	VDDIOA − 0.4			V	
Input Low Voltage (V_{IL})			0.4	V	
Input Current High (I_{INH})		1		µA	
Input Current Low (I_{INL})		±15	±125	µA	
LOGIC INPUTS (M0 to M6)					Valid for 3.3 V ≥ VDDIOx ≥ 1.8 V; VDDIOA applies to the M5 pin and the M6 pin; VDDIOB applies to the M0, M1, M2, M3, and M4 pins; the M3 and M4 pins have internal 100 kΩ pull-down resistors
Frequency Range			51	MHz	
Input High Voltage (V_{IH})	VDDIOx − 0.4			V	
Input Low Voltage (V_{IL})			0.4	V	
Input Current (I_{INH}, I_{INL})		±15	±125	µA	

LOGIC OUTPUT SPECIFICATIONS (M0 TO M6)

Table 20.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS (M0 to M6)					Valid for 3.3 V ≥ VDDIOx ≥ 1.8 V; VDDIOA applies for the M5 and M6 pins; VDDIOB applies for M0 to M4; normal (default) output drive current setting for M0 through M6
Frequency Range			26	MHz	
Output High Voltage (V_{OH})	VDDIOx − 0.6			V	Load current = 10 mA
	VDDIOx − 0.2			V	Load current = 1 mA
Output Low Voltage (V_{OL})			0.6	V	Load current = 10 mA
			0.2	V	Load current = 1 mA

JITTER GENERATION (RANDOM JITTER)

Table 21.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
JITTER GENERATION					System clock doubler enabled; high phase margin mode enabled; there is not a significant jitter difference between driver modes
Channel 0—DPLL0, APLL0					Channel 1 powered down
RMS Jitter (12 kHz to 20 MHz)					
Configuration 1—155.52 MHz		223		fs	Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{REF} = 38.88 MHz, f_{VCO} = 2488.32 MHz, f_{OUT} = 155.52 MHz, BW_{DPLL} = 50 Hz, phase buildout operation
Configuration 2—245.76 MHz		220		fs	Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{REF} = 30.72 MHz, f_{VCO} = 2457.6 MHz, f_{OUT} = 245.76 MHz, BW_{DPLL} = 50 Hz, internal zero delay operation
Configuration 3—491.52 MHz		235		fs	Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{COMP} = 19.2 MHz temperature compensated crystal oscillator (TCXO), BW_{COMP} = 50 Hz, f_{REF} = 1 Hz, f_{VCO} = 2949.12 MHz, f_{OUT} = 491.52 MHz, BW_{DPLL} = 50 mHz, phase buildout operation
Configuration 4—125 MHz		213		fs	Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{COMP} = 19.2 MHz TCXO, BW_{COMP} = 50 Hz, f_{REF} = 125 MHz, f_{VCO} = 2500 MHz, f_{OUT} = 125 MHz, BW_{DPLL} = 0.1 Hz, phase buildout operation
Configuration 5—312.5 MHz		217		fs	Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{REF} = 25 MHz, f_{VCO} = 2500 MHz, f_{OUT} = 312.5 MHz, BW_{DPLL} = 50 Hz, phase buildout operation
Configuration 6—174.7030837 MHz		230		fs	Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{REF} = 155.52 MHz, f_{VCO} = 2620.5463 MHz, f_{OUT} = (155.52 × 255/227) MHz, BW_{DPLL} = 50 Hz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Channel 1—DPLL1, APLL1					Channel 0 powered down
RMS Jitter (12 kHz to 20 MHz)					
Configuration 1—155.52 MHz		247		fs	Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{REF} = 38.88 MHz, f_{VCO} = 3265.92 MHz, f_{OUT} = 155.52 MHz, BW_{DPLL} = 50 Hz, phase buildout operation, half divide enabled
Configuration 2—245.76 MHz		280		fs	Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{REF} = 30.72 MHz, f_{VCO} = 3686.4 MHz, f_{OUT} = 245.76 MHz, BW_{DPLL} = 50 Hz, half divide enabled, internal zero delay operation
Configuration 3—491.52 MHz		323		fs	Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{COMP} = 19.2 MHz TCXO, BW_{COMP} = 50 Hz, f_{REF} = 1 Hz, f_{VCO} = 3932.16 MHz, f_{OUT} = 491.52 MHz, BW_{DPLL} = 50 mHz, phase buildout operation
Configuration 4—125 MHz		243		fs	Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{COMP} = 19.2 MHz TCXO, BW_{COMP} = 50 Hz, f_{REF} = 125 MHz, f_{VCO} = 3250 MHz, f_{OUT} = 125 MHz, BW_{DPLL} = 0.1 Hz, phase buildout operation
Configuration 5—312.5 MHz		266		fs	Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{REF} = 25 MHz, f_{VCO} = 3750 MHz, f_{OUT} = 312.5 MHz, BW_{DPLL} = 50 Hz, phase buildout operation
Configuration 6—174.7030837 MHz		264		fs	Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{REF} = 155.52 MHz, f_{VCO} = 3319.3586 MHz, f_{OUT} = (155.52 × 255/227) MHz, BW_{DPLL} = 50 Hz, phase buildout operation

PHASE NOISE

Table 22.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PHASE NOISE					System clock doubler enabled; high phase margin mode enabled; there is not a significant jitter difference between driver modes
Channel 0—DPLL0, APLL0					Channel 1 powered down
RMS Jitter (12 kHz to 20 MHz)					
Configuration 1—155.52 MHz					Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{REF} = 38.88 MHz, f_{VCO} = 2488.32 MHz, f_{OUT} = 155.52 MHz, BW_{DPLL} = 50 Hz, phase buildout operation
10 Hz Offset		−81		dBc/Hz	
100 Hz Offset		−98		dBc/Hz	
1 kHz Offset		−118		dBc/Hz	
10 kHz Offset		−128		dBc/Hz	
100 kHz Offset		−134		dBc/Hz	
1 MHz Offset		−144		dBc/Hz	
10 MHz Offset		−158		dBc/Hz	
Floor		−161		dBc/Hz	
Configuration 2—245.76 MHz					Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{REF} = 30.72 MHz, f_{VCO} = 2457.6 MHz, f_{OUT} = 245.76 MHz, BW_{DPLL} = 50 Hz, internal zero delay operation
10 Hz Offset		−77		dBc/Hz	
100 Hz Offset		−93		dBc/Hz	
1 kHz Offset		−114		dBc/Hz	
10 kHz Offset		−125		dBc/Hz	
100 kHz Offset		−130		dBc/Hz	
1 MHz Offset		−140		dBc/Hz	
10 MHz Offset		−156		dBc/Hz	
Floor		−161		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Configuration 3—491.52 MHz					Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{COMP} = 19.2 MHz TCXO, BW_{COMP} = 50 Hz, f_{REF} = 1 Hz, f_{VCO} = 2949.12 MHz, f_{OUT} = 491.52 MHz, BW_{DPLL} = 50 mHz, phase buildout operation
10 Hz Offset		−74		dBc/Hz	
100 Hz Offset		−89		dBc/Hz	
1 kHz Offset		−108		dBc/Hz	
10 kHz Offset		−119		dBc/Hz	
100 kHz Offset		−123		dBc/Hz	
1 MHz Offset		−134		dBc/Hz	
10 MHz Offset		−152		dBc/Hz	
Floor		−159			
Configuration 4—125 MHz					Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{COMP} = 19.2 MHz TCXO, BW_{COMP} = 50 Hz, f_{REF} = 125 MHz, f_{VCO} = 2500 MHz, f_{OUT} = 125 MHz, BW_{DPLL} = 0.1 Hz, phase buildout operation
10 Hz Offset		−84		dBc/Hz	
100 Hz Offset		−106		dBc/Hz	
1 kHz Offset		−120		dBc/Hz	
10 kHz Offset		−131		dBc/Hz	
100 kHz Offset		−136		dBc/Hz	
1 MHz Offset		−147		dBc/Hz	
10 MHz Offset		−160		dBc/Hz	
Floor		−163		dBc/Hz	
Configuration 5—312.5 MHz					Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{REF} = 25 MHz, f_{VCO} = 2500 MHz, f_{OUT} = 312.5 MHz, BW_{DPLL} = 50 Hz, phase buildout operation
10 Hz Offset		−74		dBc/Hz	
100 Hz Offset		−91		dBc/Hz	
1 kHz Offset		−112		dBc/Hz	
10 kHz Offset		−123		dBc/Hz	
100 kHz Offset		−128		dBc/Hz	
1 MHz Offset		−138		dBc/Hz	
10 MHz Offset		−154		dBc/Hz	
Floor		−161		dBc/Hz	
Configuration 6—174.7030837 MHz					Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{REF} = 155.52 MHz, f_{VCO} = 2620.5463 MHz, f_{OUT} = (155.52 × 255/227) MHz, BW_{DPLL} = 50 Hz
10 Hz Offset		−82		dBc/Hz	
100 Hz Offset		−99		dBc/Hz	
1 kHz Offset		−117		dBc/Hz	
10 kHz Offset		−127		dBc/Hz	
100 kHz Offset		−133		dBc/Hz	
1 MHz Offset		−143		dBc/Hz	
10 MHz Offset		−157		dBc/Hz	
Floor		−160		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Channel 1—DPLL1, APLL1					Channel 0 powered down
RMS Jitter (12 kHz to 20 MHz)					
Configuration 1—155.52 MHz					Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{REF} = 38.88 MHz, f_{VCO} = 3265.92 MHz, f_{OUT} = 155.52 MHz, BW_{DPLL} = 50 Hz, phase buildout operation, half divide enabled
10 Hz Offset		−81		dBc/Hz	
100 Hz Offset		−98		dBc/Hz	
1 kHz Offset		−118		dBc/Hz	
10 kHz Offset		−128		dBc/Hz	
100 kHz Offset		−132		dBc/Hz	
1 MHz Offset		−144		dBc/Hz	
10 MHz Offset		−158		dBc/Hz	
Floor		−162		dBc/Hz	
Configuration 2—245.76 MHz					Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{REF} = 30.72 MHz, f_{VCO} = 3686.4 MHz, f_{OUT} = 245.76 MHz, BW_{DPLL} = 50 Hz, half divide enabled; internal zero delay operation
10 Hz Offset		−76		dBc/Hz	
100 Hz Offset		−93		dBc/Hz	
1 kHz Offset		−114		dBc/Hz	
10 kHz Offset		−124		dBc/Hz	
100 kHz Offset		−127		dBc/Hz	
1 MHz Offset		−138		dBc/Hz	
10 MHz Offset		−156		dBc/Hz	
Floor		−161		dBc/Hz	
Configuration 3—491.52 MHz					Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{COMP} = 19.2 MHz TCXO, BW_{COMP} = 50 Hz, f_{REF} = 1 Hz, f_{VCO} = 3932.16 MHz, f_{OUT} = 491.52 MHz, BW_{DPLL} = 50 mHz, phase buildout operation
10 Hz Offset		−74		dBc/Hz	
100 Hz Offset		−90		dBc/Hz	
1 kHz Offset		−108		dBc/Hz	
10 kHz Offset		−118		dBc/Hz	
100 kHz Offset		−120		dBc/Hz	
1 MHz Offset		−131		dBc/Hz	
10 MHz Offset		−150		dBc/Hz	
Floor		−160		dBc/Hz	
Configuration 4—125 MHz					Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{COMP} = 19.2 MHz TCXO, BW_{COMP} = 50 Hz, f_{REF} = 125 MHz, f_{VCO} = 3250 MHz, f_{OUT} = 125 MHz, BW_{DPLL} = 0.1 Hz, phase buildout operation
10 Hz Offset		−83		dBc/Hz	
100 Hz Offset		−106		dBc/Hz	
1 kHz Offset		−120		dBc/Hz	
10 kHz Offset		−131		dBc/Hz	
100 kHz Offset		−135		dBc/Hz	
1 MHz Offset		−145		dBc/Hz	
10 MHz Offset		−160		dBc/Hz	
Floor		−163		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Configuration 5—312.5 MHz					Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{REF} = 25 MHz, f_{VCO} = 3750 MHz, f_{OUT} = 312.5 MHz, BW_{DPLL} = 50 Hz, phase buildout operation
10 Hz Offset		−73		dBc/Hz	
100 Hz Offset		−91		dBc/Hz	
1 kHz Offset		−112		dBc/Hz	
10 kHz Offset		−122		dBc/Hz	
100 kHz Offset		−125		dBc/Hz	
1 MHz Offset		−137		dBc/Hz	
10 MHz Offset		−154		dBc/Hz	
Floor		−161		dBc/Hz	
Configuration 6—174.7030837 MHz					Device configuration: f_{SYSCLK} = 52 MHz XTAL, f_{REF} = 155.52 MHz, f_{VCO} = 3319.3586 MHz, f_{OUT} = (155.52 × 255/227) MHz, BW_{DPLL} = 50 Hz
10 Hz Offset		−77		dBc/Hz	
100 Hz Offset		−99		dBc/Hz	
1 kHz Offset		−117		dBc/Hz	
10 kHz Offset		−127		dBc/Hz	
100 kHz Offset		−131		dBc/Hz	
1 MHz Offset		−142		dBc/Hz	
10 MHz Offset		−158		dBc/Hz	
Floor		−161		dBc/Hz	

ABSOLUTE MAXIMUM RATINGS

Table 23.

Parameter	Rating
1.8 V Supply Voltage (VDD)	2 V
Input/Output Supply Voltage (VDDIOA, VDDIOB)	3.6 V
Input Voltage Range (XOA, XOB, REFA, REFAA, REFB, REFBB)	−0.5 V to VDD + 0.5 V
Digital Input Voltage Range	
SDO/M5, SCLK/SCL, SDIO/SDA, CSB/M6	−0.5 V to VDDIOA + 0.5 V
M0, M1, M2, M3, M4	−0.5 V to VDDIOB + 0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range[1]	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C

[1] See the Thermal Resistance section for additional information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the junction to ambient thermal resistance, 0.0 m/sec airflow per JEDEC JESD51-2 (still air).

θ_{JMA} is the junction to ambient thermal resistance, 1.0 m/sec airflow or 2.5 m/sec airflow per JEDEC JESD51-6 (moving air).

θ_{JC} is the junction to case thermal resistance (die to heat sink) per MIL-STD 883, Method 1012.1.

Values of θ_{JA} are for package comparison and PCB design considerations. θ_{JA} provides for a first-order approximation of T_J per the following equation:

$$T_J = T_A + (\theta_{JA} \times PD)$$

where T_A is the ambient temperature (°C).

Values of θ_{JC} are for package comparison and PCB design considerations when an external heat sink is required.

Table 24. Thermal Resistance

Package Type	θ_{JA}	θ_{JMA}[1]	θ_{JC}	Unit
CP-48-13[2, 3]	23.9	19.4, 18.2	1.5	°C/W

[1] θ_{JMA} is 19.4°C/W at 1.0 m/sec airflow and 18.2°C/W at 2.5 m/sec airflow.
[2] Thermal characteristics derived using a JEDEC51-7 plus JEDEC51-5 2S2P test board. The exposed pad on the bottom of the package must be soldered to ground to achieve the specified thermal performance.
[3] Results are from simulations. The PCB is a JEDEC multilayer type. Thermal performance for actual applications requires careful inspection of the conditions in the application to determine if they are similar to those assumed in these calculations.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

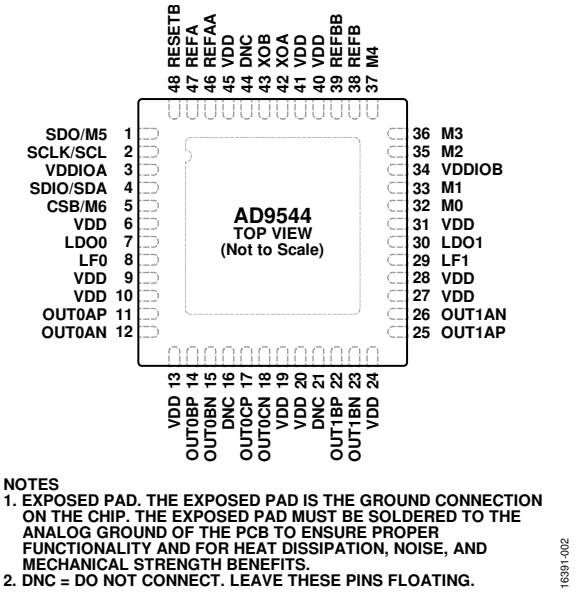

Figure 2. Pin Configuration

Table 25. Pin Function Descriptions

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
1	SDO/M5	Output	CMOS	Serial Data Output (SDO). This pin is for reading serial data in 4-wire SPI mode. Changes to the VDDIOA supply voltage affect the V_{IH} and V_{OH} values for this pin. Configurable Input/Output (M5).This pin is a status and control pin when the device is not in 4-wire SPI mode.
2	SCLK/SCL	Input	CMOS	Serial Programming Clock (SCLK) Pin in SPI Mode. Changes to the VDDIOA supply voltage affect the V_{IH} and V_{OH} values for this pin. Serial Clock Pin (SCL) in I^2C Mode. Changes to the VDDIOA supply voltage affect the V_{IH} and V_{OH} values for this pin.
3	VDDIOA	Input	Power	Serial Port Power Supply. The valid supply voltage is 1.8 V, 2.5 V, or 3.3 V. The VDDIOA pin can be connected to the VDD supply bus if 1.8 V operation is desired.
4	SDIO/SDA	Input/ output	CMOS	Serial Data Input/Output in SPI Mode (SDIO). Write data to this pin in 4-wire SPI mode. This pin has no internal pull-up or pull-down resistor. Changes to the VDDIOA supply voltage affect the V_{IH} and V_{OH} values for this pin. Serial Data Pin in I^2C Mode (SDA).
5	CSB/M6	Input/ output	CMOS	Chip Select in SPI Mode (CSB). Active low input. Maintain a Logic 0 level on this pin when programming the device in SPI mode. This pin has an internal 10 kΩ pull-up resistor. Changes to the VDDIOA supply voltage affect the V_{IH} and V_{OH} values for this pin. Configurable Input/Output (M6). This pin is a status and control pin when the device is not in SPI mode.
6, 9, 10, 13, 19, 20, 24, 27, 28, 31, 40, 41, 45	VDD	Input	Power	1.8 V Power Supply.
7	LDO0	Input	LDO bypass	APLL0 Loop Filter Voltage Regulator. Connect a 0.22 µF capacitor from this pin to ground. This pin is the ac ground reference for the integrated APLL0 loop filter.
8	LF0	Input/ output	Loop filter for APLL0	Loop Filter Node for APLL0. Connect a 3.9 nF capacitor from this pin to Pin 7 (LDO0).
11	OUT0AP	Output	HCSL, LVDS, CML, CMOS	PLL0 Output 0A.
12	OUT0AN	Output	HCSL, LVDS, CML, CMOS	PLL0 Complementary Output 0A.

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
14	OUT0BP	Output	HCSL, LVDS, CML, CMOS	PLL0 Output 0B.
15	OUT0BN	Output	HCSL, LVDS, CML, CMOS	PLL0 Complementary Output 0B.
16, 21, 44	DNC	DNC	No Connect	Do Not Connect. Leave these pins floating.
17	OUT0CP	Output	HCSL, LVDS, CML, CMOS	PLL0 Output 0C.
18	OUT0CN	Output	HCSL, LVDS, CML, CMOS	PLL0 Complementary Output 0C.
22	OUT1BP	Output	HCSL, LVDS, CML, CMOS	PLL1 Output 1B.
23	OUT1BN	Output	HCSL, LVDS, CML, CMOS	PLL1 Complementary Output 1B.
25	OUT1AP	Output	HCSL, LVDS, CML, CMOS	PLL1 Output 1A.
26	OUT1AN	Input/ Output	HCSL, LVDS, CML, CMOS	PLL1 Complementary Output 1A.
29	LF1	Input/ output	Loop filter for APLL1	Loop Filter Node for APLL1. Connect a 3.9 nF capacitor from this pin to Pin 30 (LDO1).
30	LDO1	Input	LDO bypass	APLL1 Loop Filter Voltage Regulator. Connect a 0.1 µF capacitor from this pin to ground. This pin is the ac ground reference for the integrated APLL1 loop filter.
32, 33, 35, 36, 37	M0, M1, M2, M3, M4	Input/ output	CMOS	Configurable Input/Output Pins. These are status and control pins. Changes to the VDDIOB supply voltage affect the V_{IH} and V_{OH} values for these pins. M3 and M4 have internal 100 kΩ pull-down resistors. M0, M1, and M2 do not have internal resistors.
34	VDDIOB	Input	Power	Mx Pin Power Supply. This power supply powers the digital section that controls the M0 to M4 pins. Valid supply voltages are 1.8 V, 2.5 V, or 3.3 V. The VDDIOB pin can be connected to the VDD supply bus if 1.8 V operation is desired.
38	REFB	Input	1.8 V single-ended or differential input	Reference B Input. This internally biased input is typically ac-coupled; when configured in this manner, it can accept any differential signal with a single-ended swing up to the VDD power supply. If dc-coupled, the input can be LVDS or single-ended 1.8 V CMOS.
39	REFBB	Input	1.8 V single-ended or differential input	Reference BB Input or Complementary Reference B Input. If REFB is in differential mode, the REFB complementary signal is on this pin. No connection is necessary to this pin if REFB is a single-ended input and REFBB is not used.
42	XOA	Input	Differential input	System Clock Input. XOA contains internal dc biasing and is ac-coupled with a 0.01 µF capacitor except when using a crystal. When a crystal is used, connect the crystal across XOA and XOB. A single-ended CMOS input is also an option, but it can produce spurious spectral content when the duty cycle is not 50%. When using XOA as a single-ended input, connect a 0.1 µF capacitor from XOB to ground.
43	XOB	Input	Differential input	Complementary System Clock Input. Complementary signal to XOA. XOB contains internal dc biasing and is ac-coupled with a 0.1 µF capacitor except when using a crystal. When a crystal is used, connect the crystal across XOA and XOB.
46	REFAA	Input	1.8 V single-ended or differential input	Reference AA input or Complementary REFA Input. If REFA is in differential mode, the REFA complementary signal is on this pin. No connection is necessary to this pin if REFA is a single-ended input and REFAA is not used. If dc-coupled, the input is single-ended 1.8 V CMOS.
47	REFA	Input	1.8 V single-ended or differential input	Reference A Input. This internally biased input is typically ac-coupled; when configured in this manner, it can accept any differential signal with a single-ended swing up to the VDD power supply. If dc-coupled, the input can be LVDS or single-ended 1.8 V CMOS.
48	RESETB	Input	1.8 V CMOS logic	Active Low Chip Reset. This pin has an internal 100 kΩ pull-up resistor. When asserted, the chip goes into reset. Changes to the VDDIOA supply voltage affect the V_{IH} values for this pin.
EP	EPAD	Output	Exposed pad	Exposed Pad. The exposed pad is the ground connection on the chip. The exposed pad must be soldered to the analog ground of the PCB to ensure proper functionality and for heat dissipation, noise, and mechanical strength benefits.

TYPICAL PERFORMANCE CHARACTERISTICS

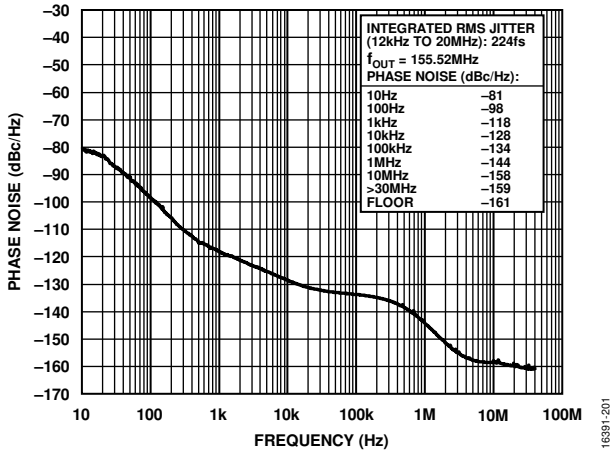

Figure 3. Absolute Phase Noise (PLL0, Configuration 1, HCSL Mode, f_{REF} = 38.88 MHz, f_{OUT} = 155.52 MHz, f_{SYS} = 52 MHz Crystal, BW_{DPLL} = 50 Hz)

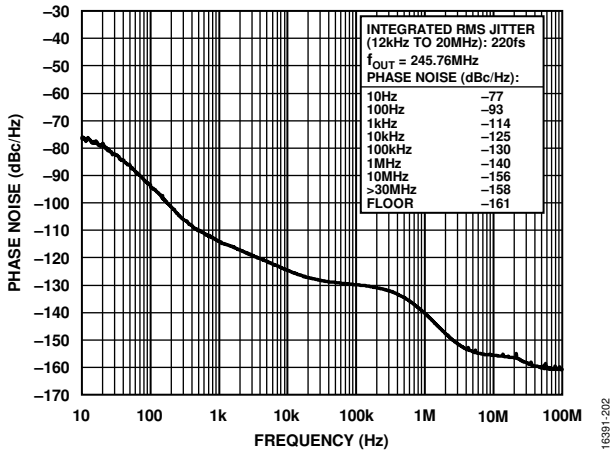

Figure 4. Absolute Phase Noise (PLL0, Configuration 2, HCSL Mode, f_{REF} = 30.72 MHz, f_{OUT} = 245.76 MHz, f_{SYS} = 52 MHz Crystal, BW_{DPLL} = 50 Hz)

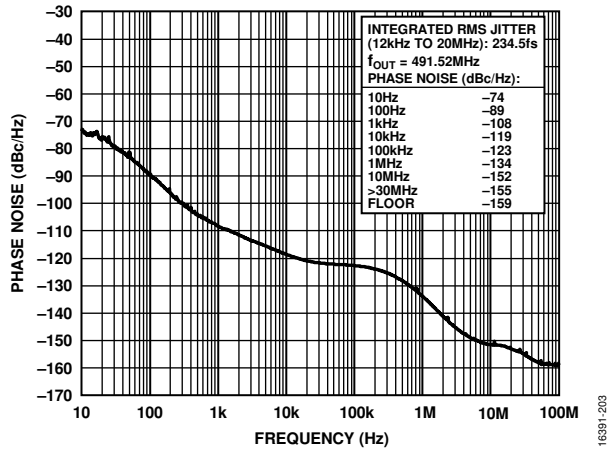

Figure 5. Absolute Phase Noise (PLL0, Configuration 3, HCSL Mode, f_{REF} = 1 Hz, f_{OUT} = 491.52 MHz, f_{COMP} = 19.2 MHz TCXO, f_{SYS} = 52 MHz Crystal, BW_{DPLL} = 50 Hz)

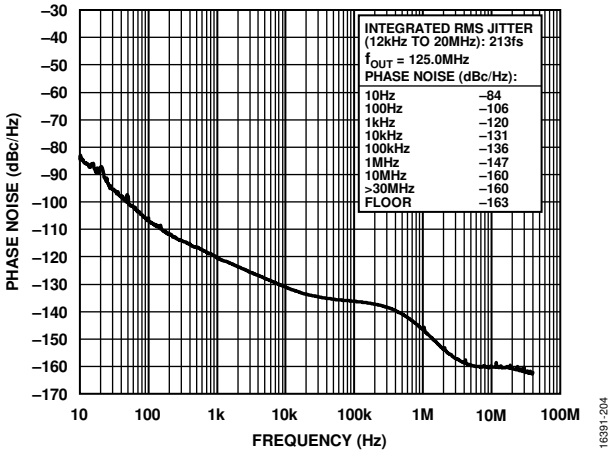

Figure 6. Absolute Phase Noise (PLL0, Configuration 4, HCSL Mode, f_{REF} = 125 MHz, f_{OUT} = 125.0 MHz, f_{COMP} = 19.2 MHz TCXO, f_{SYS} = 52 MHz Crystal, BW_{DPLL} = 0.1 Hz, Phase Buildout Mode)

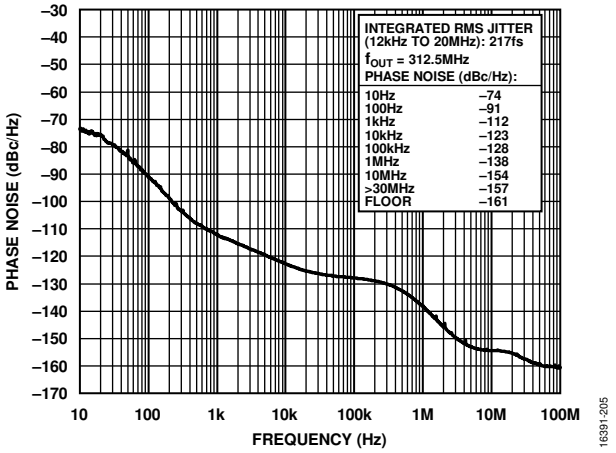

Figure 7. Absolute Phase Noise (PLL0, Configuration 5, HCSL Mode, f_{REF} = 25 MHz, f_{OUT} = 312.5 MHz, f_{SYS} = 52 MHz Crystal, BW_{DPLL} = 50 Hz, Phase Buildout Mode)

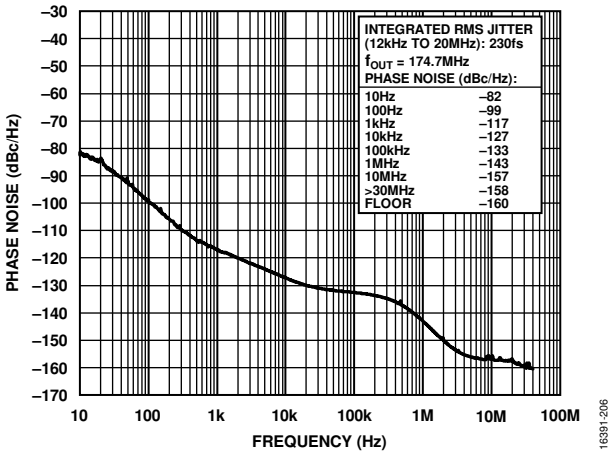

Figure 8. Absolute Phase Noise (PLL0, Configuration 6, HCSL Mode, f_{REF} = 155.52 MHz, f_{OUT} = 174.7 MHz, f_{SYS} = 52 MHz Crystal, BW_{DPLL} = 50 Hz, Phase Buildout Mode)

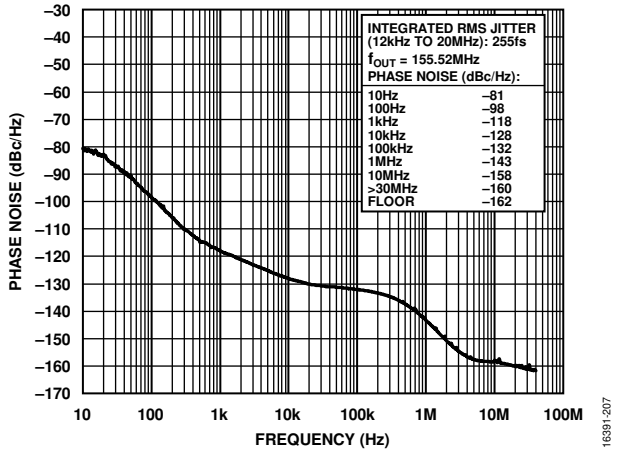

Figure 9. Absolute Phase Noise (PLL1, Configuration 1, HCSL Mode, f_{REF} = 38.88 MHz, f_{OUT} = 155.52 MHz, f_{SYS} = 52 MHz Crystal, BW_{DPLL} = 50 Hz)

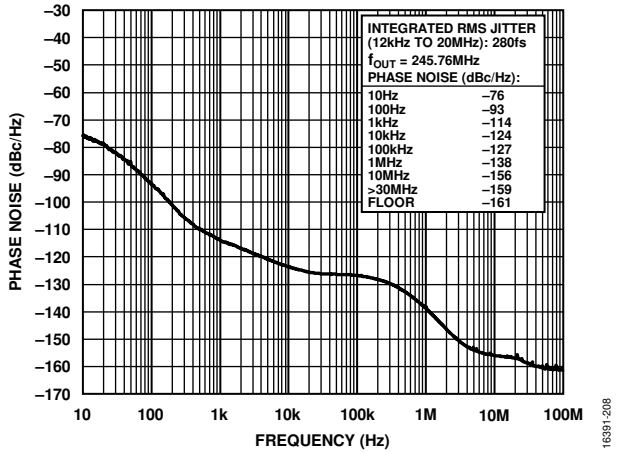

Figure 10. Absolute Phase Noise (PLL1, Configuration 2, HCSL Mode, f_{REF} = 30.72 MHz, f_{OUT} = 245.76 MHz, f_{SYS} = 52 MHz Crystal, 50 Hz DPLL BW)

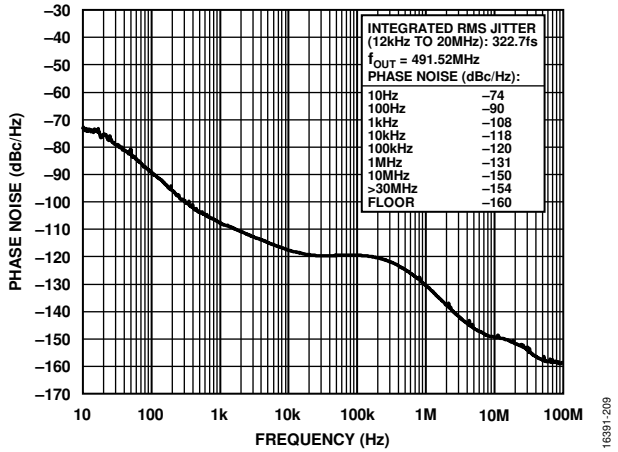

Figure 11. Absolute Phase Noise (PLL1, Configuration 3, HCSL Mode, f_{REF} = 1 Hz, f_{OUT} = 491.52 MHz, f_{COMP} = 19.2 MHz TCXO, f_{SYS} = 52 MHz Crystal, 50 MHz DPLL BW)

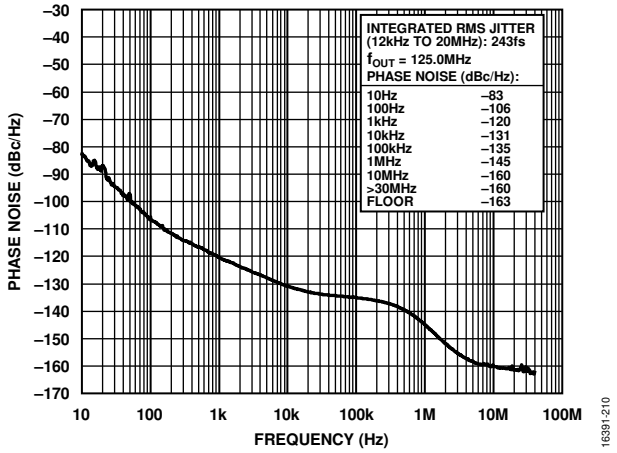

Figure 12. Absolute Phase Noise (PLL1, Configuration 4, HCSL Mode, f_{REF} = 125 MHz, f_{OUT} = 125 MHz, f_{COMP} = 19.2 MHz TCXO, f_{SYS} = 52 MHz Crystal, BW_{DPLL} = 0.1 Hz, Phase Buildout Mode)

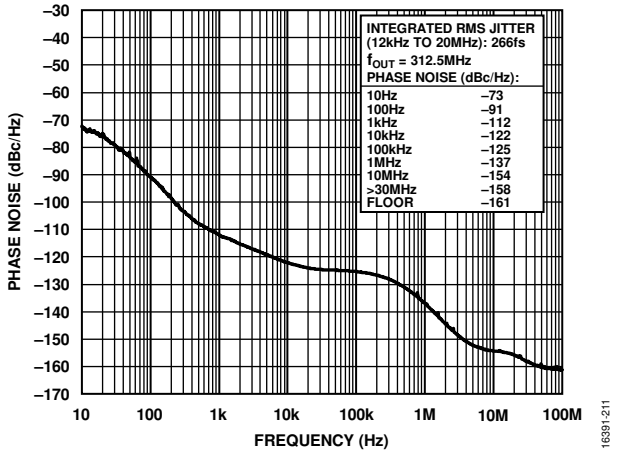

Figure 13. Absolute Phase Noise (PLL1, Configuration 5, HCSL Mode, f_{REF} = 25 MHz, f_{OUT} = 312.5 MHz, f_{SYS} = 52 MHz Crystal, BW_{DPLL} = 50 Hz, Phase Buildout Mode)

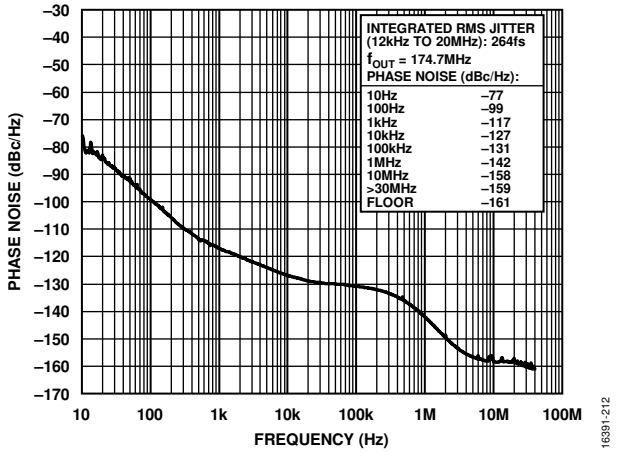

Figure 14. Absolute Phase Noise (PLL1, Configuration 6, HCSL Mode, f_{REF} = 155.52 MHz, f_{OUT} = 174.7 MHz, f_{SYS} = 52 MHz Crystal, BW_{DPLL} = 50 Hz, Phase Buildout Mode)

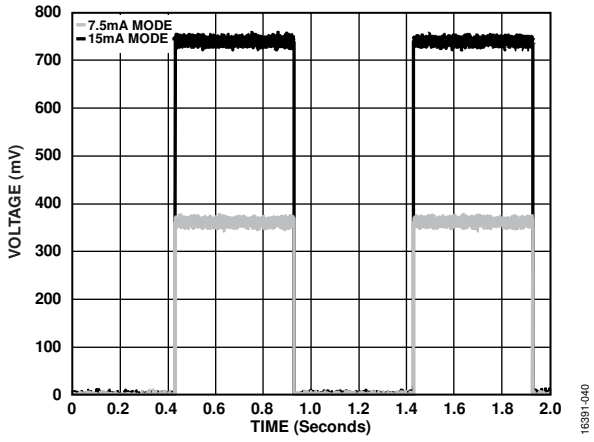

Figure 15. DC-Coupled, Single-Ended, 1 Hz Output Waveforms Using HCSL 7.5 mA and 15 mA Mode Terminated 50 Ω to GND per Figure 38; Slew Rate: ~7 V/ns for 15 mA Mode; ~3.5 V/ns for 7.5 mA Mode

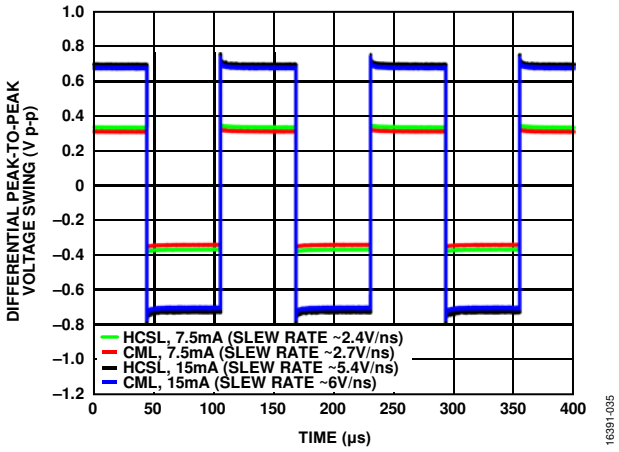

Figure 16. 8 kHz Output Waveforms for Various Driver Settings; HCSL Drivers Terminated 50 Ω to GND per Figure 32; CML Drivers Terminated 50 Ω to 1.8 V per Figure 33

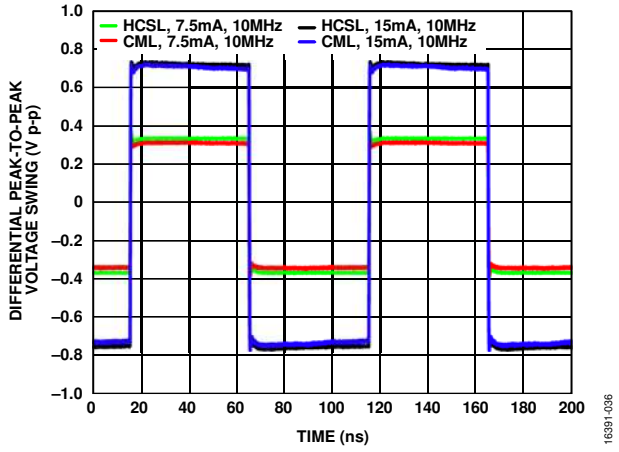

Figure 17. 10 MHz Output Waveforms for Various Driver Settings; HCSL Drivers Terminated 50 Ω to GND per Figure 32; CML Drivers Terminated 50 Ω to 1.8 V per Figure 33

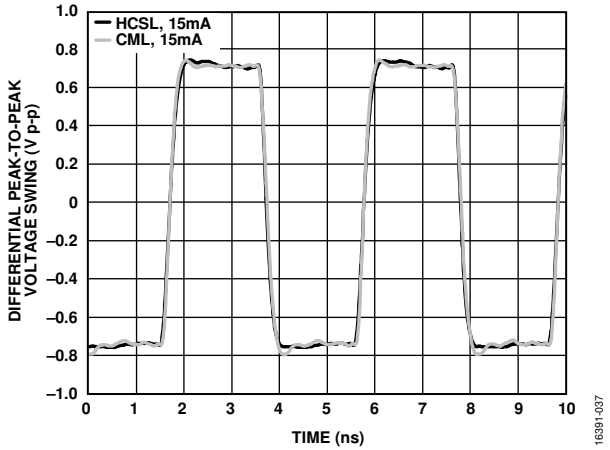

Figure 18. 245.76 MHz Output Waveform for 15 mA Driver Settings; HCSL Drivers Terminated 50 Ω to GND per Figure 32; CML Drivers Terminated 50 Ω to 1.8 V per Figure 33

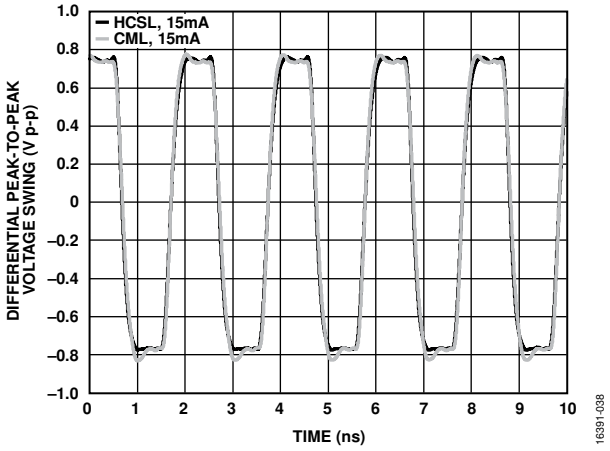

Figure 19. 491.52 MHz Output Waveform for15 mA Driver Settings; HCSL Drivers Terminated 50 Ω to GND per Figure 32; CML Drivers Terminated 50 Ω to 1.8 V per Figure 33

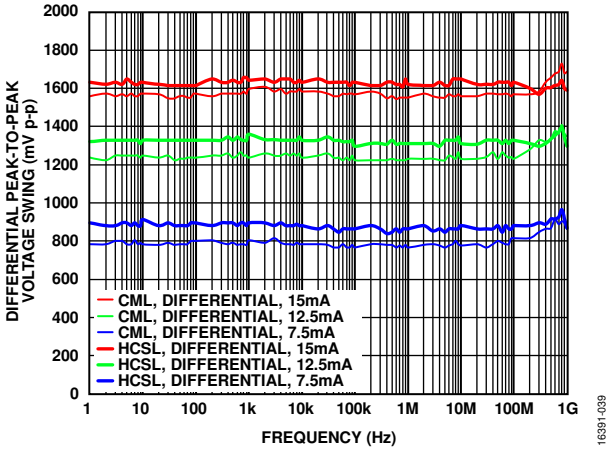

Figure 20. Differential Output Amplitude Waveforms; HCSL Drivers Terminated 50 Ω to GND per Figure 32; CML Drivers Terminated 50 Ω to 1.8 V per Figure 33

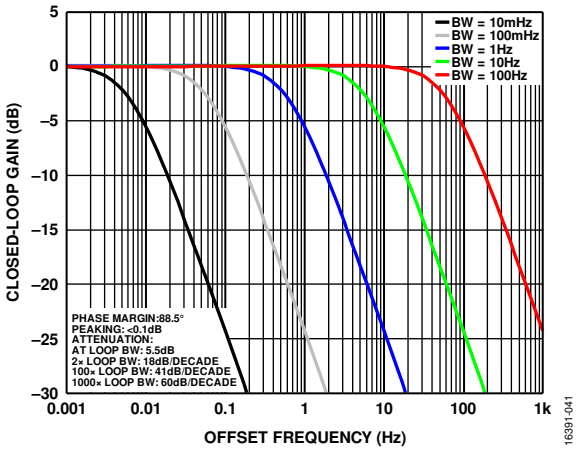

Figure 21. DPLL Closed-Loop Transfer Function Nominal Phase Margin Loop Filter Setting

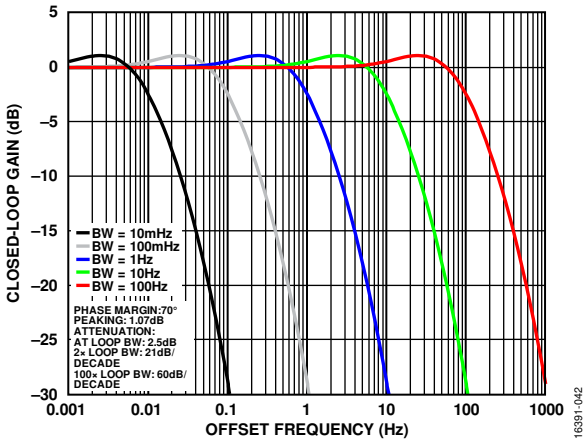

Figure 22. DPLL Closed-Loop Transfer Function High Phase Margin Loop Filter Setting