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Quad/Octal Input Network Clock Generator/Synchronizer

Data Sheet **AD9548**

FEATURES

- Supports Stratum 2 stability in holdover mode
- Supports reference switchover with phase build-out
- Supports hitless reference switchover
- Auto/manual holdover and reference switchover
- 4 pairs of reference input pins with each pair configurable as a single differential input or as 2 independent single-ended inputs
- Input reference frequencies from 1 Hz to 750 MHz
- Reference validation and frequency monitoring (1 ppm)
- Programmable input reference switchover priority
- 30-bit programmable input reference divider
- 4 pairs of clock output pins with each pair configurable as a single differential LVDS/LVPECL output or as 2 single-ended CMOS outputs
- Output frequencies up to 450 MHz
- 30-bit integer and 10-bit fractional programmable feedback divider
- Programmable digital loop filter covering loop bandwidths from 0.001 Hz to 100 kHz
- Optional low noise LC-VCO system clock multiplier
- Optional crystal resonator for system clock input
- On-chip EEPROM to store multiple power-up profiles
- Software controlled power-down
- 88-lead LFCSP package

APPLICATIONS

- Network synchronization
- Cleanup of reference clock jitter
- GPS 1 pulse per second synchronization
- SONET/SDH clocks up to OC-192, including FEC
- Stratum 2 holdover, jitter cleanup, and phase transient control
- Stratum 3E and Stratum 3 reference clocks
- Wireless base station controllers
- Cable infrastructure
- Data communications

GENERAL DESCRIPTION

The AD9548 provides synchronization for many systems, including synchronous optical networks (SONET/SDH). The AD9548 generates an output clock synchronized to one of up to four differential or eight single-ended external input references. The digital PLL allows for reduction of input time jitter or phase noise associated with the external references. The AD9548 continuously generates a clean (low jitter), valid output clock even when all references have failed by means of a digitally controlled loop and holdover circuitry.

The AD9548 operates over an industrial temperature range of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

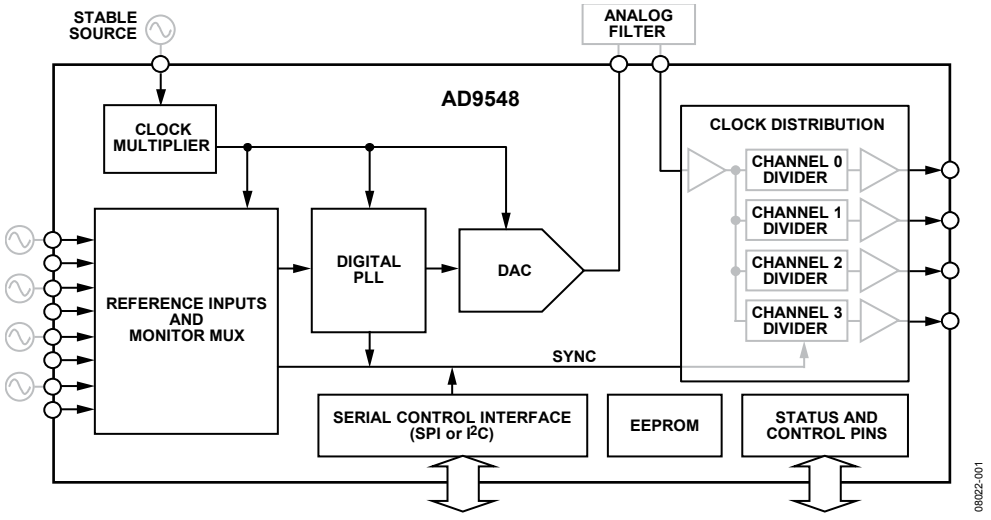

Figure 1.

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COMPARABLE PARTS

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EVALUATION KITS

- AD9548 Evaluation Board
- FPGA Mezzanine Card for Wireless Communications

DOCUMENTATION

Application Notes

- AN-1002: The AD9548 as a GPS Disciplined Stratum 2 Clock
- AN-1061: Behavior of the AD9548 Phase and Frequency Lock Detectors in the Presence of Random Jitter
- AN-1064: Understanding the Input Reference Monitors of the AD9548
- AN-1079: Determining the Maximum Tolerable Frequency Drift Rate of the AD9548 System Clock in Low Loop Bandwidth Applications

Data Sheet

- AD9548: Quad/Octal Input Network Clock Generator/ Synchronizer Data Sheet

User Guides

- UG-639: Evaluating the AD9547 and AD9548 Digital PLL Clock Synthesizers

TOOLS AND SIMULATIONS

- AD9548 IBIS Models

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

Technical Articles

- Synchronizing NxN MIMO Basestations to an External Timing Reference

DESIGN RESOURCES

- AD9548 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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SPECIFICATIONS

Minimum (min) and maximum (max) values apply for the full range of supply voltage and operating temperature variations. Typical (typ) values apply for AVDD3 = DVDD_I/O = 3.3 V; AVDD = DVDD = 1.8 V; T_A = 25°C; I_{DAC} = 20 mA (full scale), unless otherwise noted.

SUPPLY VOLTAGE

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
DVDD3	3.135	3.30	3.465	V	Pin 7, Pin 82
DVDD	1.71	1.80	1.89	V	Pin 1, Pin 6, Pin 12, Pin 14, Pin 15, Pin 77, Pin 83, Pin 88
AVDD3	3.135	3.30	3.465	V	Pin 21, Pin 22, Pin 47, Pin 60, Pin 66, Pin 67, Pin 73
3.3 V Supply (Typical)	3.135	3.30	3.465	V	Pin 31, Pin 37, Pin 38, Pin 44
1.8 V Supply (Alternative)	1.71	1.80	1.89	V	Pin 31, Pin 37, Pin 38, Pin 44
AVDD	1.71	1.80	1.89	V	Pin 23, Pin 24, Pin 29, Pin 34, Pin 41, Pin 50, Pin 55, Pin 59, Pin 63, Pin 70, Pin 74

SUPPLY CURRENT

The test conditions for the maximum (max) supply current are the same as the test conditions for the All Blocks Running parameter of Table 3. The test conditions for the typical (typ) supply current are the same as the test conditions for the Typical Configuration parameter of Table 3.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT					
I_{DVDD3}		1.5	3	mA	Pin 7, Pin 82
I_{DVDD}		190	215	mA	Pin 1, Pin 6, Pin 12, Pin 14, Pin 15, Pin 77, Pin 83, Pin 88
I_{AVDD3}		52	75	mA	Pin 21, Pin 22, Pin 47, Pin 60, Pin 66, Pin 67, Pin 73
I_{AVDD3}					
3.3 V Supply (Typical)		24	110	mA	Pin 31, Pin 37, Pin 38, Pin 44
1.8 V Supply (Alternative)		24	110	mA	Pin 31, Pin 37, Pin 38, Pin 44
I_{AVDD}		135	163	mA	Pin 23, Pin 24, Pin 29, Pin 34, Pin 41, Pin 50, Pin 55, Pin 59, Pin 63, Pin 70, Pin 74

POWER DISSIPATION

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION					
Typical Configuration		800	1100	mW	f_{SYSCLK} = 20 MHz[1]; f_S = 1 GHz[2]; f_{DDS} = 122.88 MHz[3]; one LVPECL clock distribution output running at 122.88 MHz (all others powered down); one input reference running at 100 MHz (all others powered down)
All Blocks Running		900	1400	mW	f_{SYSCLK} = 20 MHz[1]; f_S = 1 GHz[2]; f_{DDS} = 399 MHz[3]; all clock distribution outputs configured as LVPECL at 399 MHz; all input references configured as differential at 100 MHz; fractional-N active (R = 10, S = 39, U = 9, V = 10)
Full Power-Down		13		mW	Conditions = typical configuration; no external pull-up or pull-down resistors

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Incremental Power Dissipation					Conditions = typical configuration; table values show the change in power due to the indicated operation.
SYSCLK PLL Off		−105		mW	f_{SYSCLK} = 1 GHz[1]; high frequency direct input mode.
Input Reference On					
Differential		7		mW	
Single-Ended		13		mW	
Output Distribution Driver On					
LVDS		70		mW	
LVPECL		75		mW	
CMOS		65		mW	A single 3.3 V CMOS output with a 10 pF load.

[1] f_{SYSCLK} is the frequency at the SYSCLKP and SYSCLKN pins.
[2] f_S is the sample rate of the output DAC.
[3] f_{DDS} is the output frequency of the DDS.

LOGIC INPUTS (M7 TO M0, RESET, TDI, TCLK, TMS)

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS (M7 to M0, RESET, TDI, TCLK, TMS)					
Input High Voltage (V_{IH})	2.1			V	
Input Low Voltage (V_{IL})			0.8	V	
Input Current (I_{INH}, I_{INL})		±80	±200	µA	
Input Capacitance (C_{IN})		3		pF	

LOGIC OUTPUTS (M7 TO M0, IRQ, TDO)

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS (M7 to M0, IRQ, TDO)					
Output High Voltage (V_{OH})	2.7			V	I_{OH} = 1 mA
Output Low Voltage (V_{OL})			0.4	V	I_{OL} = 1 mA
IRQ Leakage Current					Open-drain mode
Active Low Output Mode			1	µA	V_{OH} = 3.3 V
Active High Output Mode			1	µA	V_{OL} =-0 V

SYSTEM CLOCK INPUTS (SYSCLKP/SYSCLKN)

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SYSTEM CLOCK PLL BYPASSED					
Input Frequency Range	500		1000	MHz	
Minimum Input Slew Rate	1000			V/µs	Minimum limit imposed for jitter performance
Duty Cycle	40		60	%	
Common-Mode Voltage		1.2		V	Internally generated
Differential Input Voltage Sensitivity	100			mV p-p	Minimum voltage across pins required to ensure switching between logic states; the instantaneous voltage on either pin must not exceed the supply rails; can accommodate single-ended input by ac grounding unused input
Input Capacitance		2		pF	Single-ended, each pin
Input Resistance		2.5		kΩ	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SYSTEM CLOCK PLL ENABLED					
PLL Output Frequency Range	900		1000	MHz	
Phase-Frequency Detector (PFD) Rate			150	MHz	
Frequency Multiplication Range	6		255		Assumes valid system clock and PFD rates
VCO Gain		70		MHz/V	
High Frequency Path					
Input Frequency Range	100.1		500	MHz	
Minimum Input Slew Rate	200			V/µs	Minimum limit imposed for jitter performance
Frequency Divider Range	1		8		Binary steps (M = 1, 2, 4, 8)
Common-Mode Voltage		1		V	Internally generated
Differential Input Voltage Sensitivity	100			mV p-p	Minimum voltage across pins required to ensure switching between logic states; the instantaneous voltage on either pin must not exceed the supply rails; can accommodate single-ended input by ac grounding unused input
Input Capacitance		3		pF	Single-ended, each pin
Input Resistance		2.5		kΩ	
Low Frequency Path					
Input Frequency Range	3.5		100	MHz	
Minimum Input Slew Rate	50			V/µs	Minimum limit imposed for jitter performance
Common-Mode Voltage		1.2		V	Internally generated
Differential Input Voltage Sensitivity	100			mV p-p	Minimum voltage across pins required to ensure switching between logic states; the instantaneous voltage on either pin must not exceed the supply rails; can accommodate single-ended input by ac grounding unused input
Input Capacitance		3		pF	Single-ended, each pin
Input Resistance		4		kΩ	
Crystal Resonator Path					
Crystal Resonator Frequency Range	10		50	MHz	Fundamental mode, AT cut
Maximum Crystal Motional Resistance			100	Ω	See the System Clock Inputs section for recommendations

DISTRIBUTION CLOCK INPUTS (CLKINP/CLKINN)

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DISTRIBUTION CLOCK INPUTS (CLKINP/CLKINN)					
Input Frequency Range	62.5		500	MHz	
Minimum Slew Rate	75			V/µs	Minimum limit imposed for jitter performance.
Common-Mode Voltage		700		mV	Internally generated.
Differential Input Voltage Sensitivity	100			mV p-p	Capacitive coupling required; can accommodate single-ended input by ac grounding unused input; the instantaneous voltage on either pin must not exceed the supply rails.
Differential Input Power Sensitivity	−15			dBm	The same as voltage sensitivity but specified as power into a 50 Ω load.
Input Capacitance		3		pF	
Input Resistance		5		kΩ	Each pin has a 2.5 kΩ internal dc-bias resistance.

REFERENCE INPUTS (REFA/REFAA TO REFD/REFDD)

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL OPERATION					
Frequency Range					
Sinusoidal Input	10		750	MHz	
LVPECL Input	1		750×10^6	Hz	
LVDS Input	1		750×10^6	Hz	
Minimum Input Slew Rate	40			V/µs	Minimum limit imposed for jitter performance
Common-Mode Input Voltage		2		V	Internally generated
Differential Input Voltage Sensitivity		±65		mV	Minimum differential voltage across pins required to ensure switching between logic levels; the instantaneous voltage on either pin must not exceed the supply rails
Input Resistance		25		kΩ	
Input Capacitance		3		pF	
Minimum Pulse Width High	620			ps	
Minimum Pulse Width Low	620			ps	
SINGLE-ENDED OPERATION					
Frequency Range (CMOS)	1		250×10^6	Hz	
Minimum Input Slew Rate	40			V/µs	Minimum limit imposed for jitter performance
Input Voltage High (V_{IH})					
1.2 V to 1.5 V Threshold Setting	0.9			V	
1.8 V to 2.5 V Threshold Setting	1.2			V	
3.0 V to 3.3 V Threshold Setting	1.9			V	
Input Voltage Low (V_{IL})					
1.2 V to 1.5 V Threshold Setting			0.27	V	
1.8 V to 2.5 V Threshold Setting			0.5	V	
3.0 V to 3.3 V Threshold Setting			1.0	V	
Input Resistance		45		kΩ	
Input Capacitance		3		pF	
Minimum Pulse Width High	1.5			ns	
Minimum Pulse Width Low	1.5			ns	

REFERENCE MONITORS

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE MONITORS					
Reference Monitor					
Loss of Reference Detection Time			1.2	sec	Calculated using the nominal phase detector period (NPDP = R/f_{REF})[1]
Frequency Out-of Range Limits	9.54×10^{-7}		0.1	$\Delta f/f_{REF}$	Programmable (lower bound subject to quality of SYSCLK)
Validation Timer	0.001		65.535	sec	Programmable in 1 ms increments
Redetect Timer	0.001		65.535	sec	Programmable in 1 ms increments

[1] f_{REF} is the frequency of the active reference; R is the frequency division factor determined by the R-divider.

REFERENCE SWITCHOVER SPECIFICATIONS

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE SWITCHOVER SPECIFICATIONS					
Maximum Output Phase Perturbation (Phase Build-Out Switchover)		40	200	ps	Assumes a jitter-free reference; satisfies Telcordia GR-1244-CORE requirements
Maximum Time/Time Slope (Hitless Switchover)	315		65,535	ns/sec	Minimum/maximum values are programmable upper bounds; a minimum value ensures <10% error; satisfies Telcordia GR-1244-CORE requirements
Time Required to Switch to a New Reference					
Hitless Switchover		5		sec	Calculated using the nominal phase detector period (NPDP = R/f_{REF})[1]
Phase Build-Out Switchover		3		sec	Calculated using the nominal phase detector period (NPDP = R/f_{REF})[1]

[1] f_{REF} is the frequency of the active reference; R is the frequency division factor determined by the R-divider.

DISTRIBUTION CLOCK OUTPUTS (OUT0 TO OUT3)

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL MODE					Using internal current setting resistor
Maximum Output Frequency		725		MHz	
Rise/Fall Time (20% to 80%)		180	315	ps	100 Ω termination across output pins
Duty Cycle	45		55	%	
Differential Output Voltage Swing	630	770	910	mV	Magnitude of voltage across pins; output driver static
Common-Mode Output Voltage	AVDD3 – 1.5	AVDD3 – 1.3	AVDD3 – 1.05	V	Output driver static
LVDS MODE					Using internal current setting resistor (nominal 3.12 kΩ)
Maximum Output Frequency		725		MHz	
Rise/Fall Time[1] (20% to 80%)		200	350	ps	100 Ω termination across the output pair
Duty Cycle	40		60	%	
Differential Output Voltage Swing					
Balanced, V_{OD}	247		454	mV	Voltage swing between output pins; output driver static
Unbalanced, ΔV_{OD}			50	mV	Absolute difference between voltage swing of normal pin and inverted pin; output driver static
Offset Voltage					
Common-Mode, V_{OS}	1.125		1.375	V	Output driver static
Common-Mode Difference, ΔV_{OS}			50	mV	Voltage difference between pins; output driver static
Short-Circuit Output Current		13	24	mA	Output driver static
CMOS MODE					Weak drive option not supported for operating the CMOS drivers using a 1.8 V supply
Maximum Output Frequency					
3.3 V Supply					10 pF load
Strong Drive Strength Setting		250		MHz	
Weak Drive Strength Setting		25		MHz	
1.8 V Supply		150		MHz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Rise/Fall Time[1] (20% to 80%)					10 pF load
3.3 V Supply					
Strong Drive Strength Setting		0.5	2	ns	
Weak Drive Strength Setting		8	14.5	ns	
1.8 V Supply		1.5	2.5	ns	
Duty Cycle	40		60	%	10 pF load
Output Voltage High (V_{OH})					Output driver static; strong drive strength setting
AVDD3 = 3.3 V, I_{OH} = 10 mA	2.6			V	
AVDD3 = 3.3 V, I_{OH} = 1 mA	2.9			V	
AVDD3 = 1.8 V, I_{OH} = 1 mA	1.5			V	
Output Voltage Low (V_{OL})					Output driver static; strong drive strength setting
AVDD3 = 3.3 V, I_{OL} = 10 mA			0.3	V	
AVDD3 = 3.3 V, I_{OL} = 1 mA			0.1	V	
AVDD3 = 1.8 V, I_{OL} = 1 mA			0.1	V	
OUTPUT TIMING SKEW					10 pF load
Between LVPECL Outputs		14	125	ps	Rising edge only; any divide value
Between LVDS Outputs		13	138	ps	Rising edge only; any divide value
Between CMOS 3.3 V Outputs					
Strong Drive Strength Setting		23	240	ps	
Weak Drive Strength Setting		24		ps	
Between CMOS 1.8 V Outputs		40		ps	Weak drive not supported at 1.8 V
Between LVPECL Outputs and LVDS Outputs		14	140	ps	
Between LVPECL Outputs and CMOS Outputs		19		ps	
ZERO-DELAY TIMING SKEW		±5		ns	Output relative to active input reference; output distribution synchronization to active reference feature enabled; assumes manual phase offset compensation of deterministic latency

[1] The listed values are for the slower edge (rise or fall).

DAC OUTPUT CHARACTERISTICS (DACOUTP/DACOUTN)

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DAC OUTPUT CHARACTERISTICS (DACOUTP/DACOUTN)					
Frequency Range	62.5		450	MHz	
Output Offset Voltage			15	mV	This is the single-ended voltage at either DAC output pin (no external load) when the internal DAC code implies that no current is delivered to that pin.
Voltage Compliance Range	VSS − 0.5	0.5	VSS + 0.5	V	
Output Resistance		50		Ω	Single-ended, each pin has an internal 50 Ω termination to VSS.
Output Capacitance		5		pF	
Full-Scale Output Current		20		mA	Programmable (8 mA to 31 mA; see the DAC Output section).
Gain Error	−12		+12	% FS	

TIME DURATION OF DIGITAL FUNCTIONS

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TIME DURATION OF DIGITAL FUNCTIONS					
EEPROM-to-Register Download Time		25		ms	Using default EEPROM storage sequence (see Register 0x0E10 to Register 0x0E3F)
Register-to-EEPROM Upload Time		200		ms	Using default EEPROM storage sequence (see Register 0x0E10 to Register 0x0E3F
Minimum Power-Down Exit Time		10.5		µs	Dependent on loop-filter bandwidth
Maximum Time from Assertion of the RESET pin to the M0 to M7 Pins Entering High Impedance State		45		ns	

DIGITAL PLL

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL PLL					
Phase-Frequency Detector (PFD) Input Frequency Range	1		10^7	Hz	Maximum f_{PFD}[1]: $f_S/100$[2]
Loop Bandwidth	0.001		10^5	Hz	Programmable design parameter; maximum $f_{LOOP} = f_{REF}/(20R)$[3]
Phase Margin	30		89	Degrees	Programmable design parameter
Reference Input (R) Division Factor	1		2^{30}		1, 2, …, 1,073,741,824
Integer Feedback (S) Division Factor	8		2^{30}		8, 9, …, 1,073,741,824
Fractional Feedback Divide Ratio	0		0.999		Maximum value: 1022/1023

[1] f_{PFD} is the frequency at the input to the phase-frequency detector.
[2] f_S is the sample rate of the output DAC.
[3] f_{REF} is the frequency of the active reference; R is the frequency division factor determined by the R-divider.

DIGITAL PLL LOCK DETECTION

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PHASE LOCK DETECTOR					
Threshold Programming Range	0.001		65.5	ns	
Threshold Resolution		1		ps	
FREQUENCY LOCK DETECTOR					
Threshold Programming Range	0.001		16,700	ns	Reference-to-feedback period difference
Threshold Resolution		1		ps	

HOLDOVER SPECIFICATIONS

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HOLDOVER SPECIFICATIONS					
Frequency Accuracy		<0.01		ppb	Excludes frequency drift of SYSCLK source; excludes frequency drift of input reference prior to entering holdover

SERIAL PORT SPECIFICATIONS—SPI MODE

Table 17.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{CS}$					Internal 30 kΩ pull-up resistor
Input Logic 1 Voltage		2.0		V	
Input Logic 0 Voltage		0.8		V	
Input Logic 1 Current		30		μA	
Input Logic 0 Current		110		μA	
Input Capacitance		2		pF	
SCLK					Internal 30 kΩ pull-down resistor
Input Logic 1 Voltage		2.0		V	
Input Logic 0 Voltage		0.8		V	
Input Logic 1 Current		1		μA	
Input Logic 0 Current		1		μA	
Input Capacitance		2		pF	
SDIO					
As an Input					
Input Logic 1 Voltage		2.0		V	
Input Logic 0 Voltage		0.8		V	
Input Logic 1 Current		1		μA	
Input Logic 0 Current		1		μA	
Input Capacitance		2		pF	
As an Output					
Output Logic 1 Voltage	2.7			V	1 mA load current
Output Logic 0 Voltage			0.4	V	1 mA load current
SDO					
Output Logic 1 Voltage	2.7			V	1 mA load current
Output Logic 0 Voltage			0.4	V	1 mA load current
TIMING					
SCLK					
Clock Rate, $1/t_{CLK}$			40	MHz	
Pulse Width High, t_{HI}	10			ns	
Pulse Width Low, t_{LO}	12			ns	
SDIO to SCLK Setup, t_{DS}	3			ns	
SCLK to SDIO Hold, t_{DH}	0			ns	
SCLK to Valid SDIO and SDO, t_{DV}			15	ns	
$\overline{CS}$ to SCLK Setup (t_S)	10			ns	
$\overline{CS}$ to SCLK Hold (t_C)	0			ns	
$\overline{CS}$ Minimum Pulse Width High	6			ns	

SERIAL PORT SPECIFICATIONS—I²C MODE

Table 18.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDA, SCL (AS INPUT)					No internal pull-up/down resistor.
Input Logic 1 Voltage	0.7 × DVDD3			V	
Input Logic 0 Voltage			0.3 × DVDD3	V	
Input Current	−10		+10	μA	For V_{IN} = 10% to 90% DVDD3.
Hysteresis of Schmitt Trigger Inputs	0.015 × DVDD3				
Pulse Width of Spikes That Must Be Suppressed by the Input Filter, t_{SP}			50	ns	
SDA (AS OUTPUT)					
Output Logic 0 Voltage			0.4	V	I_O = 3 mA.
Output Fall Time from V_{IHmin} to V_{ILmax}	20 + 0.1 C_b[1]		250	ns	10 pF ≤ C_b ≤ 400 pF.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TIMING					
SCL Clock Rate			400	kHz	
Bus-Free Time Between a Stop and Start Condition, t_{BUF}	1.3			µs	
Repeated Start Condition Setup Time, $t_{SU;STA}$	0.6			µs	
Repeated Hold Time Start Condition, $t_{HD;STA}$	0.6			µs	After this period, the first clock pulse is generated.
Stop Condition Setup Time, $t_{SU;STO}$	0.6			µs	
Low Period of the SCL Clock, t_{LO}	1.3			µs	
High Period of the SCL Clock, t_{HI}	0.6			µs	
SCL/SDA Rise Time, t_R	20 + 0.1 C_b[1]		300	ns	
SCL/SDA Fall Time, t_F	20 + 0.1 C_b[1]		300	ns	
Data Setup Time, $t_{SU;DAT}$	100			ns	
Data Hold Time, $t_{HD;DAT}$	100			ns	
Capacitive Load for Each Bus Line, C_b[1]			400	pF	

[1] C_b is the capacitance (pF) of a single bus line.

JITTER GENERATION

Table 19.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
JITTER GENERATION					
f_{REF} = 1 Hz[1]; f_{DDS} = 122.88 MHz[2]; f_{LOOP} = 0.01 Hz[3]					f_{SYSCLK} = 20 MHz[4] OCXO; f_S = 1 GHz[5]; Q-divider = 1; default SysClk PLL charge pump current; results valid for LVPECL, LVDS, and CMOS output logic types
Bandwidth: 100 Hz to 61 MHz		0.81		ps rms	Random jitter
Bandwidth: 5 kHz to 20 MHz		0.73		ps rms	Random jitter
Bandwidth: 20 kHz to 80 MHz		0.79		ps rms	Random jitter
Bandwidth: 50 kHz to 80 MHz		0.78		ps rms	Random jitter
Bandwidth: 4 MHz to 80 MHz		0.37		ps rms	Random jitter
f_{REF} = 8 kHz[1]; f_{DDS} = 155.52 MHz[2]; f_{LOOP} = 100 Hz[3]					f_{SYSCLK} = 50 MHz[4] crystal; f_S = 1 GHz[5]; Q-divider = 1; default SYSCLK PLL charge pump current; results valid for LVPECL, LVDS, and CMOS output logic types
Bandwidth: 100 Hz to 77 MHz		0.71		ps rms	Random jitter
Bandwidth: 5 kHz to 20 MHz		0.34		ps rms	Random jitter
Bandwidth: 20 kHz to 80 MHz		0.43		ps rms	Random jitter
Bandwidth: 50 kHz to 80 MHz		0.43		ps rms	Random jitter
Bandwidth: 4 MHz to 80 MHz		0.31		ps rms	Random jitter
f_{REF} = 19.44 MHz[1]; f_{DDS} = 155.52 MHz[2]; f_{LOOP} = 1 kHz[3]					f_{SYSCLK} = 50 MHz[4] crystal; f_S = 1 GHz[5]; Q-divider = 1; default SYSCLK PLL charge pump current; results valid for LVPECL, LVDS, and CMOS output logic types
Bandwidth: 100 Hz to 77 MHz		1.05		ps rms	Random jitter
Bandwidth: 5 kHz to 20 MHz		0.34		ps rms	Random jitter
Bandwidth: 20 kHz to 80 MHz		0.43		ps rms	Random jitter
Bandwidth: 50 kHz to 80 MHz		0.43		ps rms	Random jitter
Bandwidth: 4 MHz to 80 MHz		0.32		ps rms	Random jitter

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
f_{REF} = 19.44 Hz[1]; f_{DDS} = 311.04 MHz[2]; f_{LOOP} = 1 kHz[3]					f_{SYSCLK} = 50 MHz[4] crystal; f_S = 1 GHz[5]; Q-divider = 1; default SYSCLK PLL charge pump current; results valid for LVPECL, LVDS, and CMOS output logic types
Bandwidth: 100 Hz to 100 MHz		0.67		ps rms	Random jitter
Bandwidth: 5 kHz to 20 MHz		0.31		ps rms	Random jitter
Bandwidth: 20 kHz to 80 MHz		0.33		ps rms	Random jitter
Bandwidth: 50 kHz to 80 MHz		0.33		ps rms	Random jitter
Bandwidth: 4 MHz to 80 MHz		0.16		ps rms	Random jitter

[1] f_{REF} is the frequency of the active reference.
[2] f_{DDS} is the output frequency of the DDS.
[3] f_{LOOP} is the DPLL digital loop filter bandwidth.
[4] f_{SYSCLK} is the frequency at the SYSCLKP and SYSCLKN pins.
[5] f_S is the sample rate of the output DAC.

ABSOLUTE MAXIMUM RATINGS

Table 20.

Parameter	Rating
Analog Supply Voltage (AVDD)	2 V
Digital Supply Voltage (DVDD)	2 V
Digital I/O Supply Voltage (DVDD3)	3.6 V
DAC Supply Voltage (AVDD3)	3.6 V
Maximum Digital Input Voltage	−0.5 V to DVDD3 + 0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

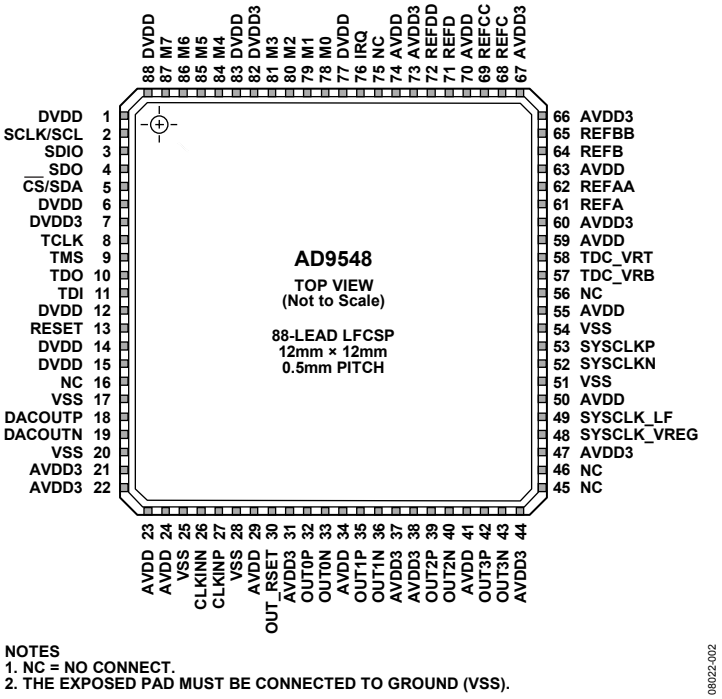


Figure 2. 88-Lead LFCSP Pin Configuration

Table 21. Pin Function Descriptions

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
1, 6, 12, 77, 83, 88	DVDD	I	Power	1.8 V Digital Supply.
2	SCLK/SCL	I	3.3 V CMOS	Serial Programming Clock. Data clock for serial programming.
3	SDIO	I/O	3.3 V CMOS	Serial Data Input/Output. When the device is in 4-wire mode, data is written via this pin. In 3-wire mode, both data reads and writes occur on this pin. There is no internal pull-up/pull-down resistor on this pin.
4	SDO	O	3.3 V CMOS	Serial Data Output. Use this pin to read data in 4-wire mode (high impedance in 3-wire mode). There is no internal pull-up/pull-down resistor on this pin.
5	$\overline{CS}$/SDA	I	3.3 V CMOS	Chip Select (SPI). Active low. When programming a device, this pin must be held low. In systems where more than one AD9548 is present, this pin enables individual programming of each AD9548 (in I^2C® mode, this is a serial data pin). This pin has an internal 10 kΩ pull-up resistor but only in SPI mode.
7, 82	DVDD3	I	Power	3.3 V I/O Digital Supply.
8	TCLK	I		JTAG Clock. Internal pull-down resistor; no connection if JTAG is not used.
9	TMS	I		JTAG Mode. Internal pull-up resistor; no connection if JTAG is not used.
10	TDO	O		JTAG Output. No connection if JTAG is not used.
11	TDI	I		JTAG Input. Internal pull-up resistor; no connection if JTAG is not used.
13	RESET	I	3.3 V CMOS	Chip Reset. When this active high pin is asserted, the chip goes into reset. This pin has an internal 50 kΩ pull-down resistor.
14, 15	DVDD	I	Power	1.8 V DAC Decode Digital Supply. Group these pins with the other DVDD pins.
16, 45, 46	NC			No Connect.
17, 20, 25, 28, 51, 54	VSS	O	Ground	Analog Ground. Connect to ground.
18	DACOUTP	O	Differential output	DAC Output. DACOUTP contains an internal 50 Ω pull-down resistor.
19	DACOUTN	O	Differential output	Complementary DAC Output. DACOUTN contains an internal 50 Ω pull-down resistor.

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
21, 22	AVDD3	I	Power	3.3 V Analog (DAC) Power Supply.
23, 24	AVDD	I	Power	1.8 V Analog (DAC) Power Supply.
26	CLKINN	I	Differential input	Clock Distribution Input. In standard operating mode, this pin is connected to the filtered DACOUTN output. This internally biased input is typically ac-coupled and, when configured as such, can accept any differential signal whose single-ended swing is at least 400 mV.
27	CLKINP	I	Differential input	Clock Distribution Input. In standard operating mode, this pin is connected to the filtered DACOUTP output.
29	AVDD	I	Power	1.8 V Analog (Input Receiver) Power Supply.
30	OUT_RSET	O	Current set resistor	Connect an optional 3.12 kΩ resistor from this pin to ground (see the Output Current Control with an External Resistor section).
31, 37, 38, 44	AVDD3	I	Power	Analog Supply for Output Driver. These pins are normally 3.3 V but can be 1.8 V. Pin 31 powers Out0x. Pin 37 powers OUT1x. Pin 38 powers OUT2x. Pin 44 powers OUT3x. Apply power to these pins even if the corresponding outputs (OUT0P/ OUT0N, OUT1P/ OUT1N, OUT2P/ OUT2N, and OUT3P/ OUT3N) are not used. See the Power Supply Partitions section.
32	OUT0P	O	LVPECL, LVDS, or CMOS	Output 0. This output can be configured as LVPECL, LVDS, or single-ended CMOS. LVPECL and LVDS operation require a 3.3 V output driver power supply. CMOS operation can be either 1.8 V or 3.3 V, depending on the output driver power supply.
33	OUT0N	O	LVPECL, LVDS, or CMOS	Complementary Output 0. This output can be configured as LVPECL, LVDS, or single-ended CMOS.
34, 41	AVDD	I	Power	1.8 V Analog (Output Divider) Power Supply.
35	OUT1P	O	LVPECL, LVDS, or CMOS	Output 1. This output can be configured as LVPECL, LVDS, or single-ended CMOS. LVPECL and LVDS operation require a 3.3 V output driver power supply. CMOS operation can be either 1.8 V or 3.3 V, depending on the output driver power supply.
36	OUT1N	O	LVPECL, LVDS, or CMOS	Complementary Output 1. This output can be configured as LVPECL, LVDS, or single-ended CMOS.
39	OUT2P	O	LVPECL, LVDS, or CMOS	Output 2. This output can be configured as LVPECL, LVDS, or single-ended CMOS. LVPECL and LVDS operation require a 3.3 V output driver power supply. CMOS operation can be either 1.8 V or 3.3 V, depending on the output driver power supply.
40	OUT2N	O	LVPECL, LVDS, or CMOS	Complementary Output 2. This output can be configured as LVPECL, LVDS, or single-ended CMOS.
42	OUT3P	O	LVPECL, LVDS, or CMOS	Output 3. This output can be configured as LVPECL, LVDS, or single-ended CMOS. LVPECL and LVDS operation require a 3.3 V output driver power supply. CMOS operation can be either 1.8 V or 3.3 V, depending on the output driver power supply.
43	OUT3N	O	LVPECL, LVDS, or CMOS	Complementary Output 3. This output can be configured as LVPECL, LVDS, or single-ended CMOS.
47	AVDD3	I	Power	3.3 V Analog (System Clock) Power Supply.
48	SYSCLK_VREG	I		System Clock Loop Filter Voltage Regulator. Connect a 0.1 µF capacitor from this pin to ground. This pin is also the ac ground reference for the integrated SYSCLK PLL multiplier's external loop filter (see the SYSCLK PLL Multiplier section).
49	SYSCLK_LF	O		System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter can be attached to this pin.
50, 55	AVDD	I	Power	1.8 V Analog (System Clock) Power Supply.

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
52	SYSCLKN	I	Differential input	Complementary System Clock Input. Complementary signal to SYSCLKP. SYSCLKN contains internal dc biasing and should be ac-coupled with a 0.01 µF capacitor, except when using a crystal. When using a crystal, connect the crystal across SYSCLKP and SYSCLKN. When using a crystal, the user should consider placing a 0 Ω series resistor on the SYSCLKN pin. In the event that the power dissipated in the crystal must be reduced, the user can replace the 0 Ω resistor with a larger resistor (for example, 500 Ω. However, this series resistor is rarely needed. (See Figure 34).
53	SYSCLKP	I	Differential input	System Clock Input. SYSCLKP contains internal dc biasing and should be ac-coupled with a 0.01 µF capacitor, except when using a crystal, in which case connect the crystal across SYSCLKP and SYSCLKN. Single-ended 1.8 V CMOS is also an option but can introduce a spur if the doubler is enabled and the duty cycle is not 50%. When using SYSCLKP as a single-ended input, connect a 0.01 µF capacitor from SYSCLKN to ground.
56, 75	NC	I		No Connection. These pins should be left floating.
59	AVDD	I	Power	1.8 V Analog Power Supply.
57, 58	TDC_VRB, TDC_VRT	I		Use capacitive decoupling on these pins (see Figure 40).
60, 66, 67, 73	AVDD3	I	Power	3.3 V Analog (Reference Input) Power Supply.
61	REFA	I	Differential input	Reference A Input. This internally biased input is typically ac-coupled and, when configured as such, can accept any differential signal with single-ended swing up to 3.3 V. If dc-coupled, input can be LVPECL, CMOS, or LVDS.
62	REFAA	I	Differential input	Complementary Reference A Input. Complementary signal to the input provided on Pin 61. The user can configure this pin as a separate single-ended input.
63, 70, 74	AVDD	I	Power	1.8 V Analog (Reference Input) Power Supply.
64	REFB	I	Differential input	Reference B Input. This internally biased input is typically ac-coupled and, when configured as such, can accept any differential signal with single-ended swing up to 3.3 V. If dc-coupled, input can be LVPECL, CMOS, or LVDS.
65	REFBB	I	Differential input	Complementary Reference B Input. Complementary signal to the input provided on Pin 64. The user can configure this pin as a separate single-ended input.
68	REFC	I	Differential input	Reference C Input. This internally biased input is typically ac-coupled and, when configured as such, can accept any differential signal with single-ended swing up to 3.3 V. If dc-coupled, input can be LVPECL, CMOS, or LVDS.
69	REFCC	I	Differential input	Complementary Reference C Input. Complementary signal to the input provided on Pin 68. The user can configure this pin as a separate single-ended input.
71	REFD	I	Differential input	Reference D Input. This internally biased input is typically ac-coupled and, when configured as such, can accept any differential signal with single-ended swing up to 3.3 V. If dc-coupled, input can be LVPECL, CMOS, or LVDS.
72	REFDD	I	Differential input	Complementary Reference D Input. Complementary signal to the input provided on Pin 71. The user can configure this pin as a separate single-ended input.
76	IRQ	O	Logic	Interrupt Request Line.
78, 79, 80, 81, 84, 85, 86, 87	M0, M1, M2, M3, M4, M5, M6, M7	I/O	3.3 V CMOS	Configurable I/O Pins. These pins are configured under program control. M0 to M2 control the serial port mode selection (see Table 29), and M3 to M7 control the EEPROM loading at startup or reset (see the Initial M0 to M7 Pin Programming section). Note that there are no internal pull-up or pull-down resistors on these pins, and the user should place pull-up or pull-down resistors on each of these pins to avoid unpredictable start-up behavior.
EP	VSS	O	Exposed pad	The exposed pad must be connected to ground (VSS).

TYPICAL PERFORMANCE CHARACTERISTICS

f_R = input reference clock frequency; f_O = clock frequency; f_{SYS} = SYSCLK input frequency; f_S = internal system clock frequency; LBW = DPLL loop bandwidth; PLL off = SYSCLK PLL bypassed; PLL on = SYSCLK PLL enabled; I_{CP} = SYSCLK PLL charge pump current; LF = SYSCLK PLL loop filter. AVDD, AVDD3, and DVDD at nominal supply voltage, f_S = 1 GHz, I_{CP} = automatic mode, LF = internal, unless otherwise noted.

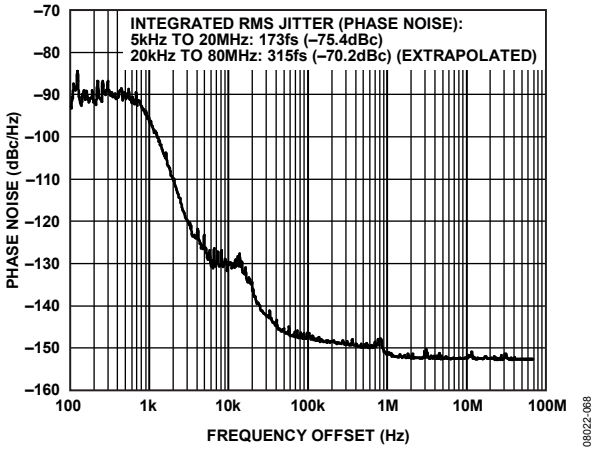


Figure 3. Additive Phase Noise (Output Driver = LVPECL), f_R = 19.44 MHz, f_O = 155.52 MHz, LBW = 1 kHz, f_{SYS} = 1 GHz, PLL Off

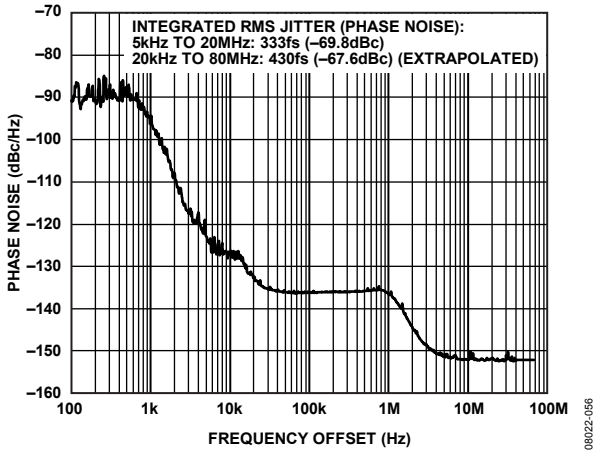


Figure 4. Additive Phase Noise (Output Driver = LVPECL), f_R = 19.44 MHz, f_O = 155.52 MHz, LBW = 1 kHz, f_{SYS} = 50 MHz (Crystal), PLL On

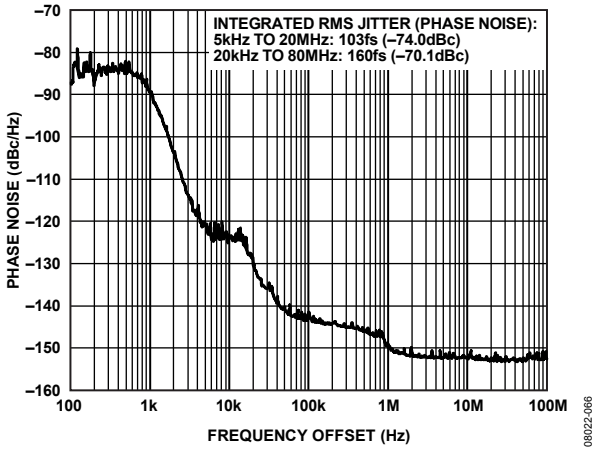


Figure 5. Additive Phase Noise (Output Driver = LVPECL), f_R = 19.44 MHz, f_O = 311.04 MHz, LBW = 1 kHz, f_{SYS} = 1 GHz, PLL Off

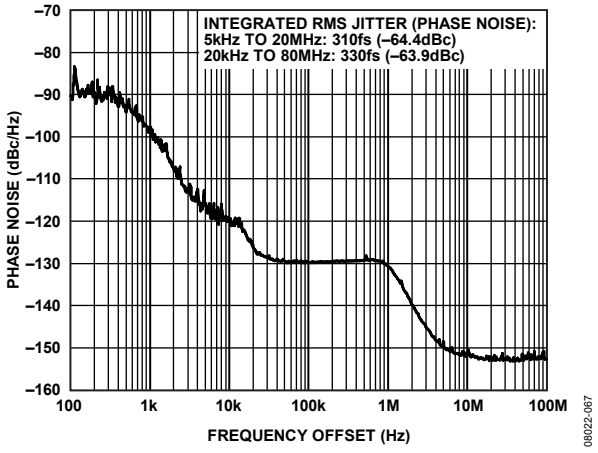


Figure 6. Additive Phase Noise (Output Driver = LVPECL), f_R = 19.44 MHz, f_O = 311.04 MHz, LBW = 1 kHz, f_{SYS} = 50 MHz (Crystal), PLL On

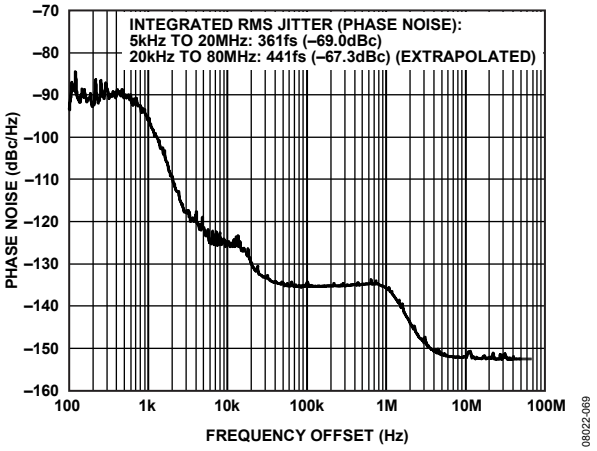


Figure 7. Absolute Phase Noise (Output Driver = LVPECL), f_R = 19.44 MHz, f_O = 155.52 MHz, LBW = 1 kHz, f_{SYS} = 50 MHz, PLL On

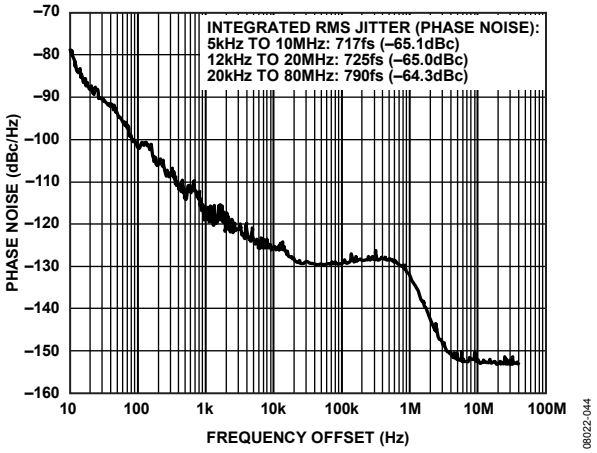


Figure 8. Absolute Phase Noise (Output Driver = LVPECL), f_R = 1 Hz, f_O = 122.88 MHz, LBW = 0.05 Hz, f_{SYS} = 20 MHz (OCXO), PLL On

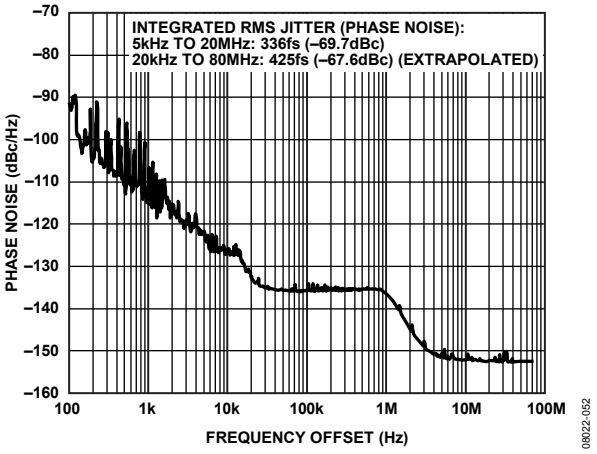


Figure 9. Absolute Phase Noise (Output Driver = LVPECL), f_R = 8 kHz, f_O = 155.52 MHz, LBW = 100 Hz, f_{SYS} = 50 MHz (Crystal), PLL On

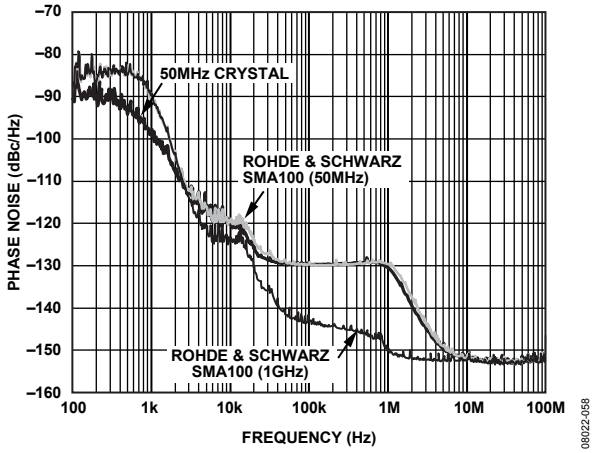


Figure 10. Absolute Phase Noise Comparison of SYSCLK Input Options (Output Driver = LVPECL), f_R = 19.44 MHz, f_O = 311.04 MHz, LBW = 1 kHz

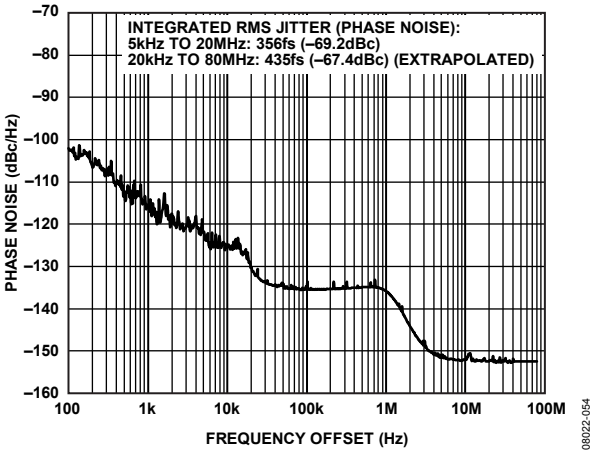


Figure 11. Absolute Phase Noise (Output Driver = LVPECL), f_R = 1 Hz, f_O = 155.52 MHz, LBW = 0.05 Hz, f_{SYS} = 50 MHz, PLL On

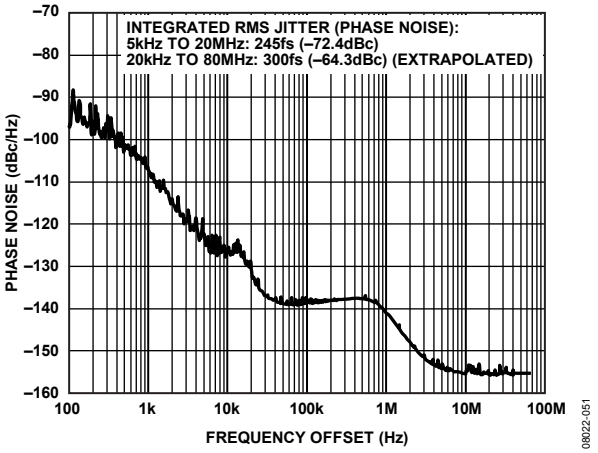


Figure 12. Absolute Phase Noise (Output Driver = LVPECL), f_R = 19.44 MHz, f_O = 155.52 MHz, LBW = 1 kHz, f_{SYS} = 50 MHz (Crystal), PLL On with 2x Frequency Multiplier, I_{CP} = 375 µA, LF = External (350 kHz)

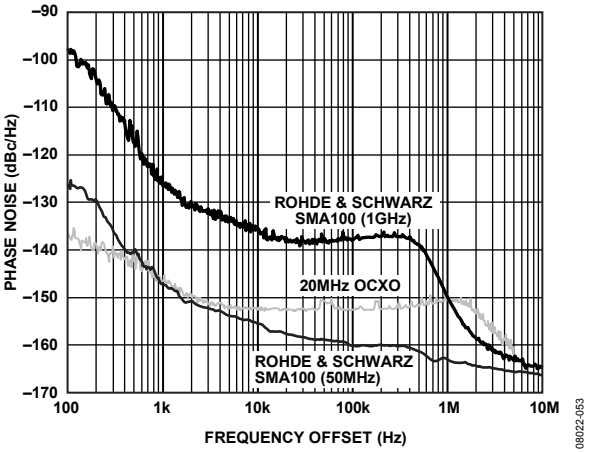


Figure 13. Phase Noise of SYSCLK Input Sources

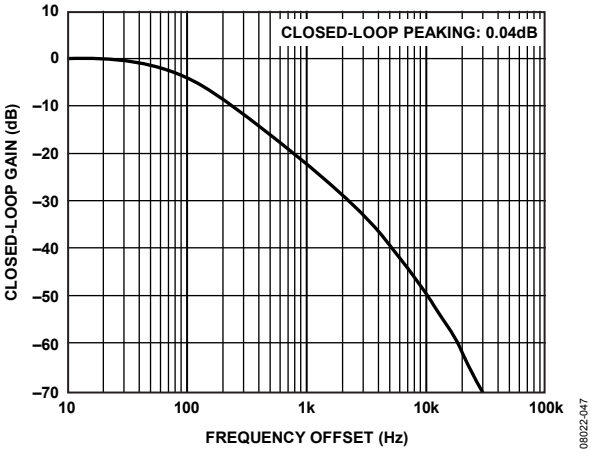


Figure 16. Jitter Transfer Bandwidth, Output Driver = LVPECL, f_R = 19.44 MHz, f_O = 155.52 MHz, LBW = 100 Hz (Phase Margin = 88°), f_{SYS} = 1 GHz, PLL Off

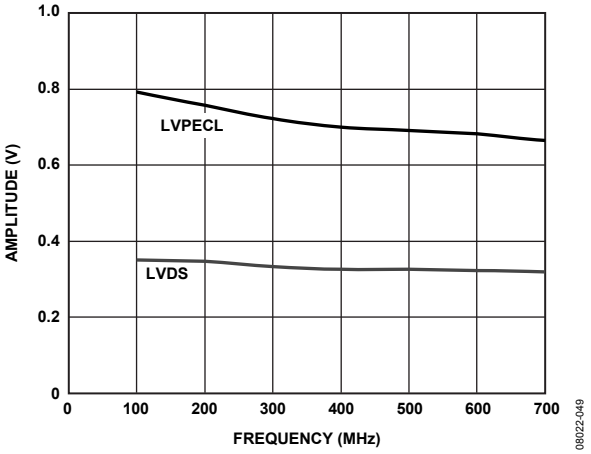


Figure 14. Amplitude vs. Toggle Rate, LVPECL and LVDS

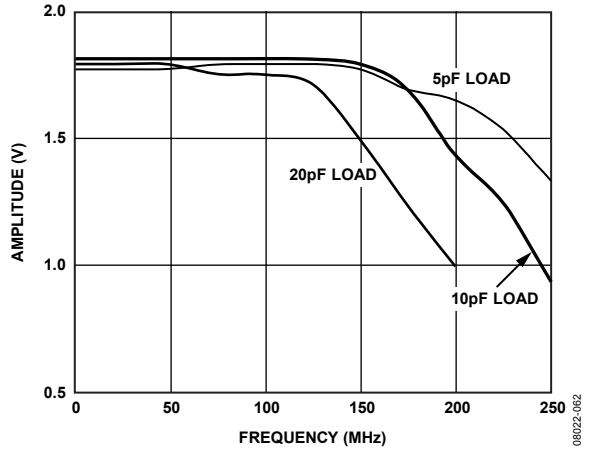


Figure 17. Amplitude vs. Toggle Rate, 1.8 V CMOS

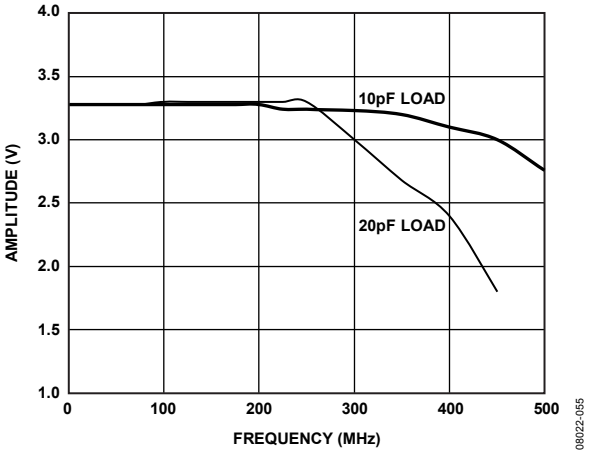


Figure 15. Amplitude vs. Toggle Rate, 3.3 V CMOS (Strong Mode)

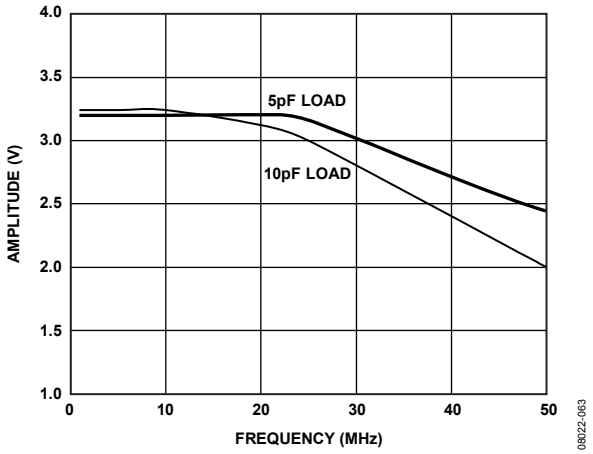


Figure 18. Amplitude vs. Toggle Rate, 3.3 V CMOS (Weak Mode)

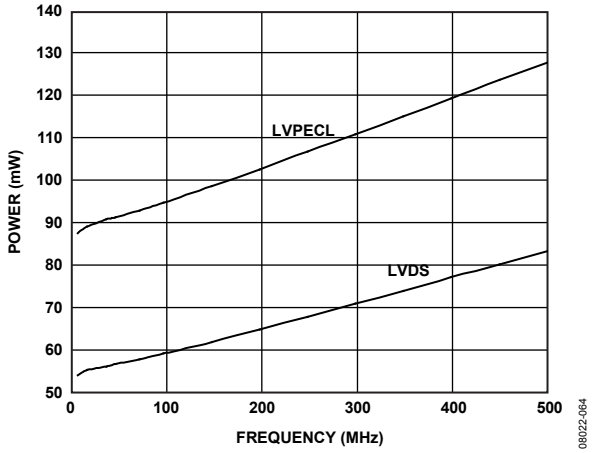


Figure 19. Power Consumption vs. Frequency, LVPECL and LVDS (Single Channel)

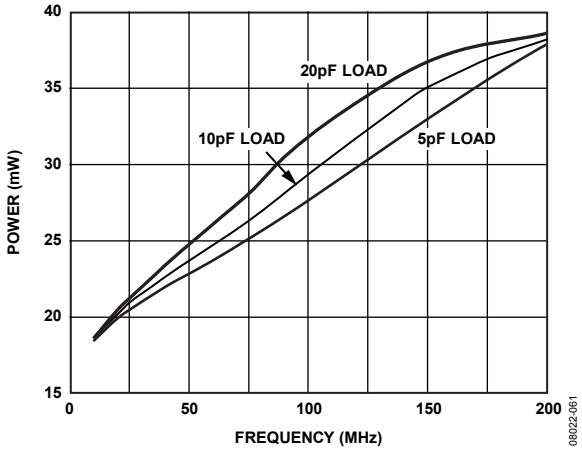


Figure 22. Power Consumption vs. Frequency, 1.8 V CMOS

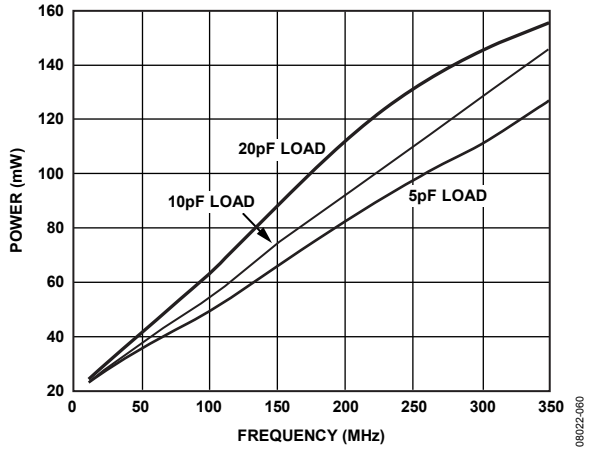


Figure 20. Power Consumption vs. Frequency, 3.3 V CMOS (Strong Mode)

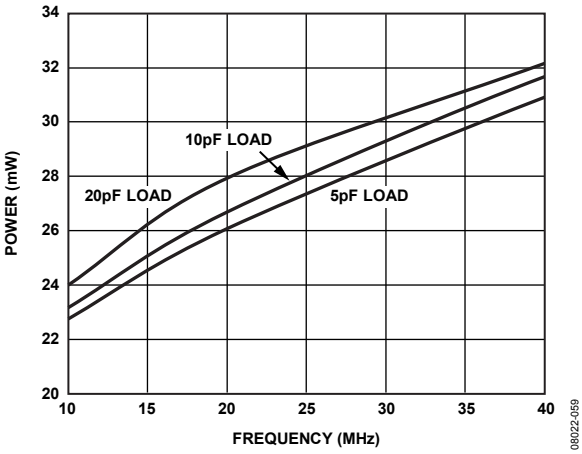


Figure 23. Power Consumption vs. Frequency, 3.3 V CMOS (Weak Mode)

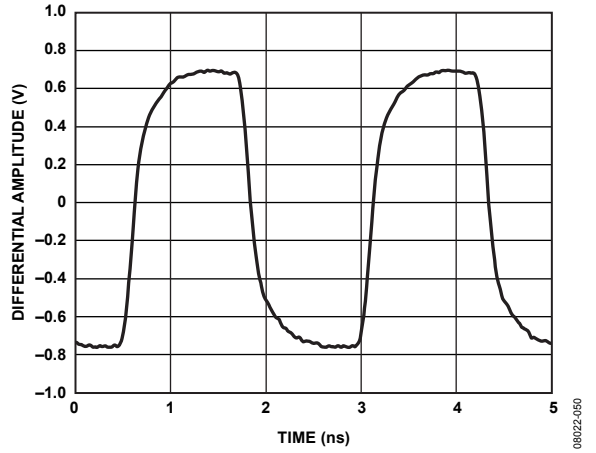


Figure 21. Output Waveform, LVPECL (400 MHz)

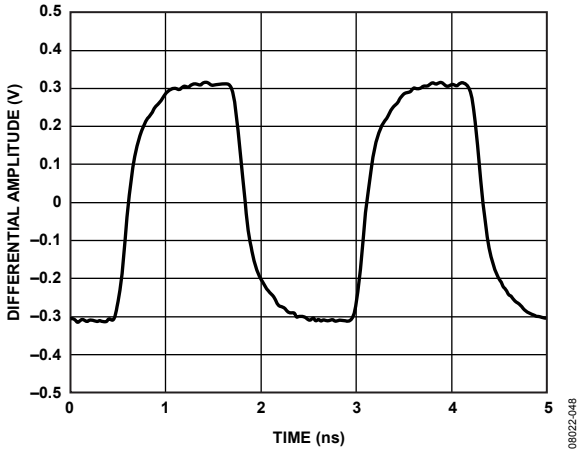


Figure 24. Output Waveform, LVDS (400 MHz)

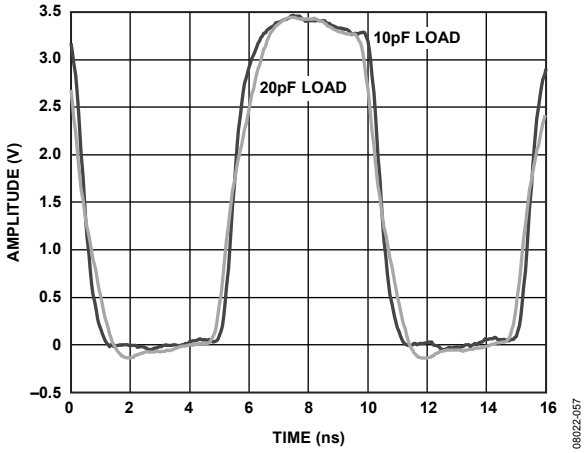


Figure 25. Output Waveform, 3.3 V CMOS (100 MHz, Strong Mode)

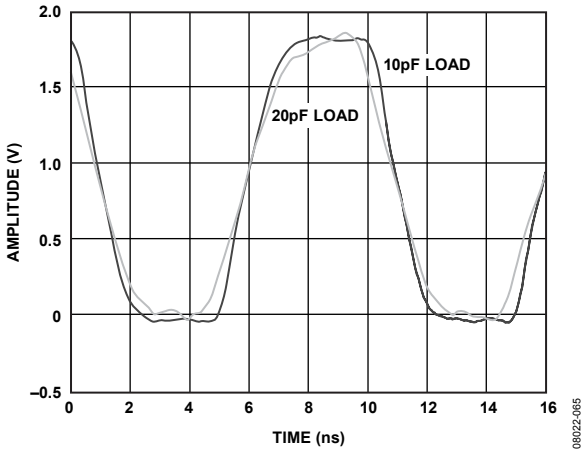


Figure 26. Output Waveform, 1.8 V CMOS (100 MHz)

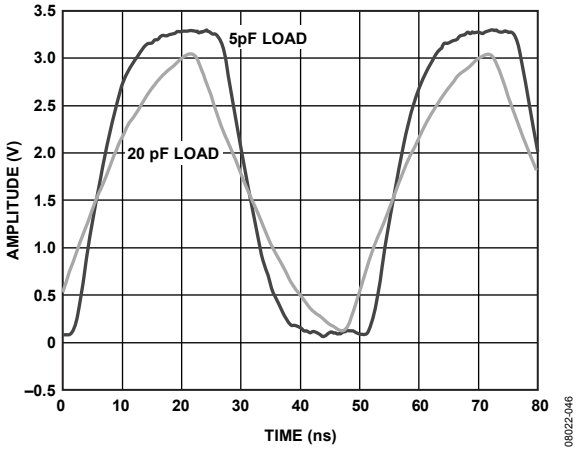


Figure 27. Output Waveform, 3.3 V CMOS (20 MHz, Weak Mode)

INPUT/OUTPUT TERMINATION RECOMMENDATIONS

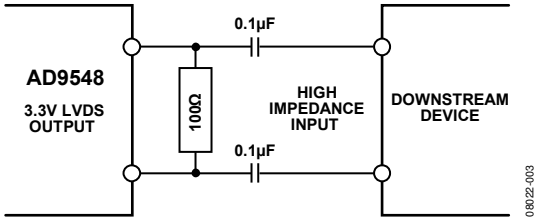


Figure 28. AC-Coupled LVDS or LVPECL Output Driver

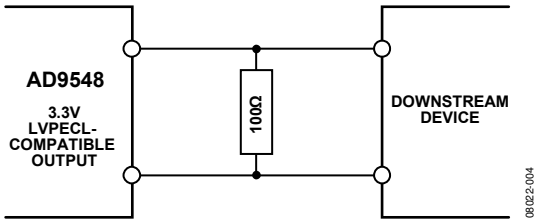


Figure 29. DC-Coupled LVDS or LVPECL Output Driver

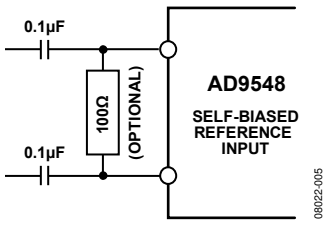


Figure 30. Reference Input

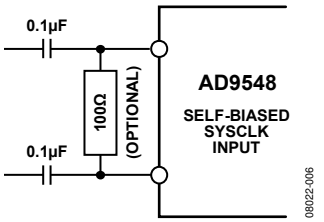


Figure 31. SYSCLKx Input

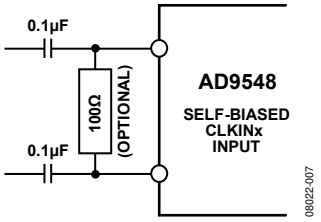


Figure 32. CLKINx Input

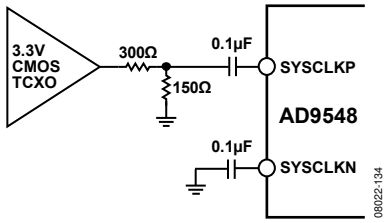
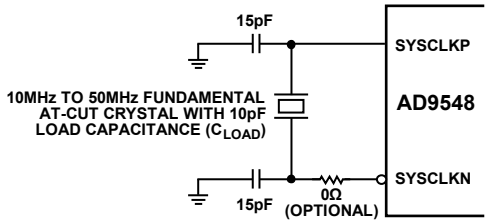


Figure 33. System Clock Input (SYSCLKP/SYSCLKN) When Using a TCXO/OCXO with 3.3 V CMOS Output



NOTES
1. THE RECOMMENDED C_{LOAD} = 10pF IS SHOWN. THE VALUES OF THE 15pF SHUNT CAPACITORS SHOWN HERE MUST EQUAL 2 × (C_{LOAD} − C_{STRAY}), WHERE C_{STRAY} IS TYPICALLY 2pF TO 5pF). THE SERIES RESISTOR CONNECTED TO SYSCLKN IS NORMALLY NOT REQUIRED, BUT CAN BE USEFUL TO LIMIT THE POWER DISSIPATED IN THE CRYSTAL.

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Figure 34. System Clock Input (XOA/XOB) in Crystal Mode

GETTING STARTED

POWER-ON RESET

The AD9548 monitors the voltage on the power supplies at power-up. When DVDD3 is greater than 2.35 V ± 0.1 V and DVDD (Pin 1, Pin 6, Pin 12, Pin 77, Pin 83, and Pin 88) is greater than 1.4 V ± 0.05 V, the device generates a 75 ns reset pulse. The power-up reset pulse is internal and independent of the RESET pin. This internal power-up reset sequence eliminates the need for the user to provide external power supply sequencing. Within 45 ns after the leading edge of the internal reset pulse, the M0 to M7 multifunction pins behave as high impedance digital inputs and remain so until programmed otherwise.

INITIAL M0 TO M7 PIN PROGRAMMING

During a device reset (either via the power-up reset pulse or the RESET pin), the multifunction pins (M0 to M7) behave as high impedance inputs, but upon removal of the reset condition, level-sensitive latches capture the logic pattern present on the multifunction pins. The AD9548 requires that the user supply the desired logic state to the M0 to M7 pins by means of pull-up and/or pull-down resistors (nominally 10 kΩ to 30 kΩ).

The initial state of the M0 to M7 pins following a reset is referred to as FncInit, Bits[7:0]. Bits[7:0] of FncInit map directly to the logic states of M7:0, respectively. The three LSBs of FncInit (FncInit, Bits[2:0]) determine whether the serial port interface behaves according to the SPI or I²C protocol. Specifically, FncInit, Bits[2:0] = 000 selects the SPI interface, while any other value selects the I²C port with the three LSBs of the I²C bus address set to the value of FncInit, Bits[2:0].

The five MSBs of FncInit (FncInit, Bits[7:3]) determine the operation of the EEPROM loader. On the falling edge of RESET, if FncInit, Bits[7:3] = 00000, then the EEPROM contents are not transferred to the control registers and the device registers assume their default values. However, if FncInit, Bits[7:3] ≠ 00000, then the EEPROM controller transfers the contents of the EEPROM to the control registers with condition = FncInit, Bits[7:3] (see the EEPROM section).

DEVICE REGISTER PROGRAMMING

The initial state of the M0 to M7 pins establishes the serial input/output port protocol (SPI or I²C). Using the appropriate serial port protocol, and assuming that an EEPROM download is not used, program the device according to the recommended sequence described in the Program the System Clock Functionality section through the Generate the Output Clock section.

Program the System Clock Functionality

The system clock parameters reside in the 0100 register address space. They include the following:

- System clock PLL controls
- System clock period
- System clock stability timer

It is essential to program the system clock period because many of the AD9548 subsystems rely on this value. It is highly recommended to program the system clock stability timer, as well. This is especially important when using the system clock PLL but also applies if using an external system clock source, especially if the external source is not expected to be completely stable when power is applied to the AD9548.

Initialize the System Clock

After the system clock functionality is programmed, issue an input/output update using Register 0x0005, Bit 0 to invoke the system clock settings.

Calibrate the System Clock (Only if Using SYSCLK PLL)

Set the calibrate system clock bit in the sync/cal register (Address 0x0A02, Bit 0) and issue an input/output update. Then clear the calibrate system clock bit and issue another input/output update. This action allows time for the calibration to proceed while programming the remaining device registers.

Program the Multifunction Pins (Optional)

This step is required only if the user intends to use any of the multifunction pins for status or control. The multifunction pin parameters reside in the 0x0200 to 0x0207 register address space. The default configuration of the multifunction pins is as an undesignated high impedance input pin.

Program the IRQ Functionality (Optional)

This step is required only if the user intends to use the IRQ feature. IRQ control resides in the 0x0200 to 0x0207 register address space. It includes the following:

- IRQ pin mode control
- IRQ mask

The IRQ mask default values prevent interrupts from being generated. The IRQ pin mode default is open-drain NMOS.

Program the Watchdog Timer (Optional)

This step is required only if the user intends to use it. Watchdog timer control resides in the 0x0200 register address space. The watchdog timer is disabled by default.

Program the DAC Full-Scale Current (Optional)

This step is required only if the user intends to use a full-scale current setting other than the default value. DAC full-scale current control resides in the 0x0200 register address space.