Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Dual Input Network Clock Generator/Synchronizer

AD9549

FEATURES

- Flexible reference inputs
- Input frequencies: 8 kHz to 750 MHz
- Two reference inputs
- Loss of reference indicators
- Auto and manual holdover modes
- Auto and manual switchover modes
- Smooth A-to-B phase transition on outputs
- Excellent stability in holdover mode
- Programmable 16 + 1-bit input divider, R
- Differential HSTL clock output
- Output frequencies to 750 MHz
- Low jitter clock doubler for frequencies of >400 MHz
- Single-ended CMOS output for frequencies of <150 MHz
- Programmable digital loop filter (<1 Hz to ~100 kHz)
- High speed digitally controlled oscillator (DCO) core
  - Direct digital synthesizer (DDS) with integrated 14-bit DAC
- Excellent dynamic performance
- Programmable 16 + 1-bit feedback divider, S
- Software controlled power-down
- Available 64-lead LFCSP package

APPLICATIONS

- Network synchronization
- Reference clock jitter cleanup
- SONET/SDH clocks up to OC-192, including FEC
- Stratum 3/3E reference clocks
- Wireless base station, controllers
- Cable infrastructure
- Data communications

GENERAL DESCRIPTION

The AD9549 provides synchronization for many systems, including synchronous optical networks (SONET/SDH). The AD9549 generates an output clock, synchronized to one of two external input references. The external references may contain significant time jitter, also specified as phase noise. Using a digitally controlled loop and holdover circuitry, the AD9549 continues to generate a clean (low jitter), valid output clock during a loss of reference condition, even when both references have failed.

The AD9549 operates over an industrial temperature range of −40°C to +85°C.

BASIC BLOCK DIAGRAM

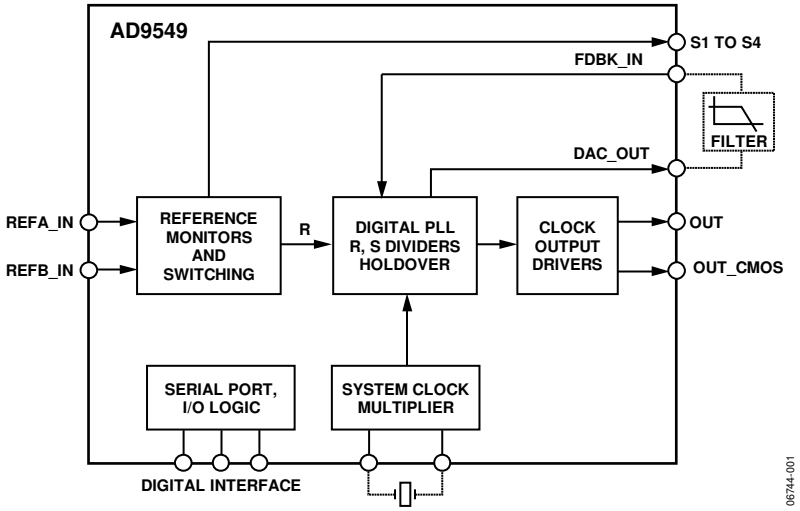


Figure 1.

Rev. D

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

AD9549* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9549 Evaluation Board

DOCUMENTATION

Application Notes

- AN-0983: Introduction to Zero-Delay Clock Timing Techniques
- AN-741: Little Known Characteristics of Phase Noise
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-769: Generating Multiple Clock Outputs from the AD9540
- AN-823: Direct Digital Synthesizers in Clocking Applications Time
- AN-837: DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance
- AN-873: Lock Detect on the ADF4xxx Family of PLL Synthesizers
- AN-927: Determining if a Spur is Related to the DDS/DAC or to Some Other Source (For Example, Switching Supplies)
- AN-939: Super-Nyquist Operation of the AD9912 Yields a High RF Output Signal

Data Sheet

- AD9549: Dual Input Network Clock Generator/ Synchronizer Data Sheet

TOOLS AND SIMULATIONS

- AD9549 IBIS Models

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

Technical Articles

- ADI Buys Korean Mobile TV Chip Maker
- Design A Clock-Distribution Strategy With Confidence
- Improved DDS Devices Enable Advanced Comm Systems
- Low-power direct digital synthesizer cores enable high level of integration
- Speedy A/Ds Demand Stable Clocks
- Understand the Effects of Clock Jitter and Phase Noise on Sampled Systems

DESIGN RESOURCES

- AD9549 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9549 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

12/10—Rev. C to Rev. D

Changes to I_{AVDD} (Pin 19, Pin 23 to Pin 26, Pin 29, Pin 30, Pin44, Pin 45) Parameter 4
Changes to Total Power Dissipation Parameter and Added Endnote 4 5
Changes to Pin 59 Description 11
Changes to Direct Digital Synthesizer (DDS) Section 20
Changes to Power-Up Section 42
Changes to Address 0x0002 Default Value (in Table 13) 48
Changes to Address 0x0400 and Address 0x40E Default Values (in Table 13) 52

5/10—Rev. B to Rev. C

Deleted 64-Lead LFCSP (CP-64-1) ..... Universal
Changes to SYSCLK PLL Enabled/Minimum Differential Input Level Parameter, Table 2 6
Updated Outline Dimensions 74
Changes to Ordering Guide 74

1/10—Rev. A to Rev. B

Changes to I/O Register Map Section, Introduction and Table 13 48
Changes to Register 0x0405 to Register 0x0408—Reserved Section 70
Added Register 0x0406—Part Version Section 71

12/09—Rev. 0 to Rev. A

Added 64-Lead LFCSP (CP-64-7) ..... Universal
Changes to Total Power Dissipation Parameter 5
Changes to Serial Port Timing Specifications and Propagation Delay Parameters 8
Added Exposed Paddle Notation to Figure 2; Changes to Table 4 10
Corrected DDS Phase Offset Resolution from 16 Bits to 14 Bits Throughout; Change to Figure 25 20
Changes to Phase Lock Detection Section 24
Change to Figure 30 25
Changes to Loss of Reference and Reference Frequency Monitor Sections 26
Change to Output Frequency Range Control Section 32
Change to Figure 46 36
Changes to Frequency Estimator Section 37
Changes to Programming Sequence Section 42
Changes to Power Supply Partitioning Section 43
Change to Serial Control Port Section 44
Changes to Figure 54 46
Added Exposed Paddle Notation to Outline Dimensions and Changes to Ordering Guide 74

8/07—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V ± 5%, AVDD3 = 3.3 V ± 5%, DVDD = 1.8 V ± 5%, DVDD_I/O = 3.3 V ± 5%. AVSS = 0 V, DVSS = 0 V, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
DVDD_I/O (Pin 1)	3.135	3.30	3.465	V	
DVDD (Pin 3, Pin 5, Pin 7)	1.71	1.80	1.89	V	
AVDD3 (Pin 14, Pin 46, Pin 47, Pin 49)	3.135	3.30	3.465	V	
AVDD3 (Pin 37)	1.71	3.30	3.465	V	Pin 37 is typically 3.3 V, but can be set to 1.8 V
AVDD (Pin 11, Pin 19, Pin 23 to Pin 26, Pin 29, Pin 30, Pin 36, Pin 42, Pin 44, Pin 45, Pin 53)	1.71	1.80	1.89	V	
SUPPLY CURRENT					
I_{AVDD3} (Pin 14)		4.7	5.6	mA	REFA, REFB buffers
I_{AVDD3} (Pin 37)		3.8	4.5	mA	CMOS output clock driver at 3.3 V
I_{AVDD3} (Pin 46, Pin 47, Pin 49)		26	29	mA	DAC output current source, f_S = 1 GSPS
I_{AVDD} (Pin 36, Pin 42)		21	26	mA	FDBK_IN input, HSTL output clock driver (output doubler turned on)
I_{AVDD} (Pin 11)		12	15	mA	REFA and REFB input buffer 1.8 V supply
I_{AVDD} (Pin 19, Pin 23 to Pin 26, Pin 29, Pin 30, Pin 44, Pin 45)		215	281	mA	Aggregate analog supply, including system clock PLL
I_{AVDD} (Pin 53)		41	49	mA	DAC power supply
I_{DVDD} (Pin 3, Pin 5, Pin 7)		254	265	mA	Digital core
$I_{DVDD\_I/O}$ (Pin 1)		4	6	mA	Digital I/O (varies dynamically)
LOGIC INPUTS (Except Pin 32)					Pin 9, Pin 10, Pin 54 to Pin 61, Pin 63, Pin 64
Input High Voltage (V_{IH})	2.0		DVDD_I/O	V	
Input Low Voltage (V_{IL})	DVSS		0.8	V	
Input Current (I_{INH}, I_{INL})		±60	±200	µA	At V_{IN} = 0 V and V_{IN} = DVDD_I/O
Maximum Input Capacitance (C_{IN})		3		pF	
CLKMODESEL (Pin 32) LOGIC INPUT					Pin 32 only
Input High Voltage (V_{IH})	1.4		AVDD	V	
Input Low Voltage (V_{IL})	AVSS		0.4	V	
Input Current (I_{INH}, I_{INL})		−18	−50	µA	At V_{IN} = 0 V and V_{IN} = AVDD
Maximum Input Capacitance (C_{IN})		3		pF	
LOGIC OUTPUTS					Pin 62 and the following bidirectional pins: Pin 9, Pin 10, Pin 54, Pin 55, Pin 63
Output High Voltage (V_{OH})	2.7		DVDD_I/O	V	I_{OH} = 1 mA
Output Low Voltage (V_{OL})	DVSS		0.4	V	I_{OL} = 1 mA
REFERENCE INPUTS					Pin 12, Pin 13, Pin 15, Pin 16
Input Capacitance		3		pF	
Input Resistance	8.5	11.5	14.5	kΩ	Differential at Register 0x040F[1:0] = 00
Differential Operation					
Common Mode Input Voltage[1] (Applicable When DC-Coupled)	1.5		AVDD3 – 0.2	V	Differential operation; note that LVDS signals must be ac-coupled
Differential Input Voltage Swing[1]	500			mV p-p	Differential operation
Single-Ended Operation					Register 0x040F[1:0] = 10
Input Voltage High (V_{IH})	2.0		AVDD3	V	
Input Voltage Low (V_{IL})	AVSS		0.8	V	
Threshold Voltage	AVDD3 – 0.66	AVDD3 – 0.82	AVDD3 – 0.98	V	Register 0x040F[1:0] = 10 (other settings possible)
Input Current			1	mA	Single-ended operation
FDBK_IN INPUT					Pin 40, Pin 41
Input Capacitance		3		pF	
Input Resistance	18	22	26	kΩ	Differential
Differential Input Voltage Swing[2]	225			mV p-p	−12 dBm into 50 Ω; must be ac-coupled

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SYSTEM CLOCK INPUT					System clock inputs should always be ac-coupled (both single-ended and differential)
SYSCLK PLL Bypassed					
Input Capacitance		1.5		pF	Single-ended, each pin
Input Resistance	2.4	2.6	2.8	kΩ	Differential
Internally Generated DC Bias Voltage[2]	0.93	1.17	1.38	V	
Differential Input Voltage Swing[3]	632			mV p-p	0 dBm into 50 Ω
SYSCLK PLL Enabled					
Input Capacitance		3		pF	Single-ended, each pin
Input Resistance	2.4	2.6	2.8	kΩ	Differential
Internally Generated DC Bias Voltage[2]	0.93	1.17	1.38	V	
Differential Input Voltage Swing[3]	632			mV p-p	0 dBm into 50 Ω
Crystal Resonator with SYSCLK PLL Enabled					
Motional Resistance		9	100	Ω	25 MHz, 3.2 mm × 2.5 mm AT cut
CLOCK OUTPUT DRIVERS					
HSTL Output Driver					
Differential Output Voltage Swing	1080	1280	1480	mV	Output driver static; see Figure 12 for output swing vs. frequency
Common-Mode Output Voltage[2]	0.7	0.88	1.06	V	
CMOS Output Driver					Output driver static; see Figure 13 and Figure 14 for output swing vs. frequency
Output Voltage High (V_{OH})	2.7			V	I_{OH} = 1 mA, (Pin 37) = 3.3 V
Output Voltage Low (V_{OL})			0.4	V	I_{OL} = 1 mA, (Pin 37) = 3.3 V
Output Voltage High (V_{OH})	1.4			V	I_{OH} = 1 mA, (Pin 37) = 1.8 V
Output Voltage Low (V_{OL})			0.4	V	I_{OL} = 1 mA, (Pin 37) = 1.8 V
TOTAL POWER DISSIPATION					
All Blocks Running[4]		1060	1310	mW	Worst case over supply, temperature, process
Power-Down Mode		24	70	mW	Using either the power-down and enable register (Register 0x0010) or the PWRDOWN pin
Digital Power-Down Mode		565	713	mW	
Default with SYSCLK PLL Enabled		955		mW	After reset or power-up with f_S = 1 GHz, S4 = 0, S1 to S3 = 1, f_{SYSCLK} = 25 MHz
Default with SYSCLK PLL Disabled		945	1115	mW	After reset or power-up with f_S = 1 GHz, S1 to S4 = 1
With REFA or REFB Power-Down			1105	mW	One reference still powered up
With HSTL Clock Driver Power-Down			1095	mW	
With CMOS Clock Driver Power-Down			1107	mW	

[1] Must be ≤0 V relative to AVDD3 (Pin 14) and ≥0 V relative to AVSS (Pin 33, Pin 43).
[2] Relative to AVSS (Pin 33, Pin 43).
[3] Must be ≤0 V relative to AVDD (Pin 36) and ≥0 V relative to AVSS (Pin 33, Pin 43).
[4] Typical measurement done with only REFA and HSTL output doubler turned off.

AC SPECIFICATIONS

f_S = 1 GHz, DAC R_{SET} = 10 kΩ, power supply pins within the range specified in the DC Specifications section, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE INPUTS					Pin 12, Pin 13, Pin 15, and Pin 16
Frequency Range (Sine Wave)	10		750	MHz	Minimum recommended slew rate: 40 V/µs
Frequency Range (CMOS)	0.008		50	MHz	
Frequency Range (LVPECL)	0.008		725	MHz	
Frequency Range (LVDS)	0.008		725	MHz	LVDS must be ac-coupled; lower frequency bound may be higher, depending on the size of the decoupling capacitor
Minimum Slew Rate	0.04			V/ns	
Minimum Pulse Width High	620			ps	
Minimum Pulse Width Low	620			ps	
FDBK_IN INPUT					Pin 40, Pin 41
Input Frequency Range	10		400	MHz	
Minimum Differential Input Level	225			mV p-p	−12 dBm into 50 Ω; must be ac-coupled
Minimum Slew Rate	40			V/µs	
SYSTEM CLOCK INPUT					Pin 27, Pin 28
SYSCLK PLL Bypassed					
Input Frequency Range	250		1000	MHz	Maximum f_{OUT} is 0.4 × f_{SYSCLK}
Duty Cycle	45		55	%	
Minimum Differential Input Level	632			mV p-p	0 dBm into 50 Ω
SYSCLK PLL Enabled					
VCO Frequency Range, Low Band	700		810	MHz	When in the range, use the low VCO band exclusively
VCO Frequency Range, Auto Band	810		900	MHz	When in the range, use the VCO Auto band select
VCO Frequency Range, High Band	900		1000	MHz	When in the range, use the high VCO band exclusively
Maximum Input Rate of System Clock PFD			200	MHz	
Without SYSCLK PLL Doubler					
Input Frequency Range	11		200	MHz	
Multiplication Range	4		66		Integer multiples of 2, maximum PFD rate and system clock frequency must be met
Minimum Differential Input Level	632			mV p-p	0 dBm into 50 Ω
With SYSCLK PLL Doubler					
Input Frequency Range	6		100	MHz	
Multiplication Range	8		132		Integer multiples of 8
Input Duty Cycle		50		%	Deviating from 50% duty cycle may adversely affect spurious performance.
Minimum Differential Input Level	632			mV p-p	0 dBm into 50 Ω
Crystal Resonator with SYSCLK PLL Enabled					
Crystal Resonator Frequency Range	10		50	MHz	AT cut, fundamental mode resonator
Maximum Crystal Motional Resistance			100	Ω	See the SYSCLK Inputs section for recommendations
CLOCK DRIVERS					
HSTL Output Driver					
Frequency Range	20		725	MHz	See Figure 12 for maximum toggle rate
Duty Cycle	48		52	%	
Rise Time/Fall Time (20-80%)		115	165	ps	100 Ω termination across OUT/OUTB, 2 pF load
Jitter (12 kHz to 20 MHz)		1.0		ps	f_{IN} = 19.44 MHz, f_{OUT} = 155.52 MHz. 50 MHz system clock input (see Figure 3 to Figure 11 for test conditions)
HSTL Output Driver with 2× Multiplier					
Frequency Range	400		725	MHz	
Duty Cycle	45		55	%	
Rise Time/Fall Time (20% to 80%)		115	165	ps	100 Ω termination across OUT/OUTB, 2 pF load
Subharmonic Spur Level		−35		dBc	Without correction
Jitter (12 kHz to 20 MHz)		1.1		ps	f_{IN} = 19.44 MHz, f_{OUT} = 622.08 MHz, 50 MHz system clock input (see Figure 3 to Figure 11 for test conditions)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CMOS Output Driver (AVDD3/Pin 37) @ 3.3 V					
Frequency Range	0.008		150	MHz	See Figure 14 for maximum toggle rate
Duty Cycle	45	55	65	%	With 20 pF load and up to 150 MHz
Rise Time/Fall Time (20-80%)		3	4.6	ns	With 20 pF load
CMOS Output Driver (AVDD3/Pin 37) @ 1.8 V					
Frequency Range	0.008		40	MHz	See Figure 13 for maximum toggle rate
Duty Cycle	45	55	65	%	With 20 pF load and up to 40 MHz
Rise Time/Fall Time (20% to 80%)		5	6.8	ns	With 20 pF load
HOLDOVER					
Frequency Accuracy					See the Holdover section
OUTPUT FREQUENCY SLEW LIMITER					
Slew Rate Resolution	0.54		111	Hz/sec	$P = 2^{16}$ for minimum; $P = 2^5$ for maximum
Slew Rate Range	0		3×10^{16}	Hz/sec	$P = 2^{16}$ for minimum; $P = 2^5$ for maximum
REFERENCE MONITORS					
Loss of Reference Monitor					
Operating Frequency Range	7.63×10^3		167×10^6	Hz	
Minimum Frequency Error for Continuous REF Present Indication			−16	ppm	f_{REF} = 8 kHz
Minimum Frequency Error for Continuous REF Present Indication			−19	%	f_{REF} = 155 MHz
Maximum Frequency Error for Continuous REF Lost Indication	−32			ppm	f_{REF} = 8 kHz
Maximum Frequency Error for Continuous REF Lost Indication	−35			%	f_{REF} = 155 MHz
Reference Quality Monitor					
Operating Frequency Range	0.008		150	MHz	
Frequency Resolution (Normalized)	0.2			ppm	f_{REF} = 8 kHz; OOL divider = 65,535 for minimum; OOL divider = 1 for max (see the Reference Frequency Monitor section)
Frequency Resolution (Normalized)	408			ppm	f_{REF} = 155 MHz; OOL divider = 65,535 for minimum; OOL divider = 1 for maximum
Validation Timer					See the Reference Validation Timers section
Timing Range	32×10^{-9}		137	sec	P_{IO} = 5
Timing Range	65×10^{-6}		2.8×10^5	sec	P_{IO} = 16
DAC OUTPUT CHARACTERISTICS					
DCO Frequency Range (1st Nyquist Zone)	10		450	MHz	DPLL loop bandwidth sets lower limit
Output Resistance		50		Ω	Single-ended (each pin internally terminated to AVSS)
Output Capacitance		5		pF	
Full-Scale Output Current		20	31.7	mA	Range depends on DAC R_{SET} resistor
Gain Error	−10		+10	% FS	
Output Offset			0.6	µA	
Voltage Compliance Range	AVSS − 0.50	+0.5	AVSS + 0.50		Outputs not dc-shorted to V_{SS}
DIGITAL PLL					
Minimum Open-Loop Bandwidth		0.1		Hz	Dependent on the frequency of REFA/REFB, the DAC sample rate, and the P-, R-, and S-divider values
Maximum Open-Loop Bandwidth		100		kHz	Dependent on the frequency of REFA/REFB, the DAC sample rate, and the P-, R-, and S-divider values
Minimum Phase Margin	0	10		Degrees	Dependent on the frequency of REFA/REFB, the DAC sample rate, and the P-, R-, and S-divider values
Maximum Phase Margin		85	90	Degrees	Dependent on the frequency of REFA/REFB, the DAC sample rate, and the P-, R-, and S-divider values
PFD Input Frequency Range	~0.008		~24.5	MHz	
Feedforward Divider Ratio	1		131,070		1, 2, …, 65,535 or 2, 4, …, 131,070
Feedback Divider Ratio	1		131,070		1, 2, …, 65,535 or 2, 4, …, 131,070

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOCK DETECTION					
Phase Lock Detector					
Time Threshold Programming Range	0		2097	µs	FPFD_gain = 200
Time Threshold Resolution		0.488		ps	FPFD_gain = 200
Lock Time Programming Range	32×10^{-9}		275	sec	In power-of-2 steps
Unlock Time Programming Range	192×10^{-9}		67×10^{-3}	sec	In power-of-2 steps
Frequency Lock Detector					
Normalized Frequency Threshold Programming Range	0		0.0021		FPFD_gain = 200; normalized to $(f_{REF}/R)^2$; see the Frequency Lock Detection section for details
Normalized Frequency Threshold Programming Resolution		5×10^{-13}			FPFD_gain = 200; normalized to $(f_{REF}/R)^2$; see the Frequency Lock Detection section for details
Lock Time Programming Range	32×10^{-9}		275	sec	In power-of-2 steps
Unlock Time Programming Range	192×10^{-9}		67×10^{-3}	sec	In power-of-2 steps
DIGITAL TIMING SPECIFICATIONS					
Time Required to Enter Power-Down		15		µs	
Time Required to Leave Power-Down		18		µs	
Reset Assert to High-Z Time for S1 to S4 Configuration Pins		60		ns	Time from rising edge of RESET to high-Z on the S1, S2, S3, and S4 configuration pins
Reset Deassert to Low-Z Time for S1 to S4 Configuration Pins		30		ns	Time from falling edge of RESET to low-Z on the S1, S2, S3, and S4 configuration pins
SERIAL PORT TIMING SPECIFICATIONS					
SCLK Clock Rate ($1/t_{CLK}$)		25	50	MHz	Refer to Figure 58 for all write-related serial port parameters, maximum SCLK rate for readback is governed by t_{DV}
SCLK Pulse Width High, t_{HIGH}	8			ns	
SCLK Pulse Width Low, t_{LOW}	8			ns	
SDO/SDIO to SCLK Setup Time, t_{DS}	1.93			ns	
SDO/SDIO to SCLK Hold Time, t_{DH}	1.9			ns	
SCLK Falling Edge to Valid Data on SDIO/SDO, t_{DV}			11	ns	Refer to Figure 56
CSB to SCLK Setup Time, t_S	1.34			ns	
CSB to SCLK Hold Time, t_H	−0.4			ns	
CSB Minimum Pulse Width High, t_{PWH}	3			ns	
IO_UPDATE Pin Setup Time from SCLK Rising Edge of the Final Bit	t_{CLK}			sec	t_{CLK} = period of SCLK in Hz
IO_UPDATE Pin Hold Time	t_{CLK}			sec	t_{CLK} = period of SCLK in Hz
PROPAGATION DELAY					
FDBK_IN to HSTL Output Driver		2.8		ns	
FDBK_IN to HSTL Output Driver with 2× Frequency Multiplier Enabled		7.3		ns	
FDBK_IN to CMOS Output Driver		8.0		ns	
FDBK_IN Through S-Divider to CMOS Output Driver		8.6		ns	
Frequency Tuning Word Update, IO_UPDATE Pin Rising Edge to DAC Output		60/fs		ns	fs = system clock frequency in GHz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Analog Supply Voltage (AVDD)	2 V
Digital Supply Voltage (DVDD)	2 V
Digital I/O Supply Voltage (DVDD_I/O)	3.6 V
DAC Supply Voltage (AVDD3 Pins)	3.6 V
Maximum Digital Input Voltage	−0.5 V to DVDD_I/O + 0.5 V
Storage Temperature	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

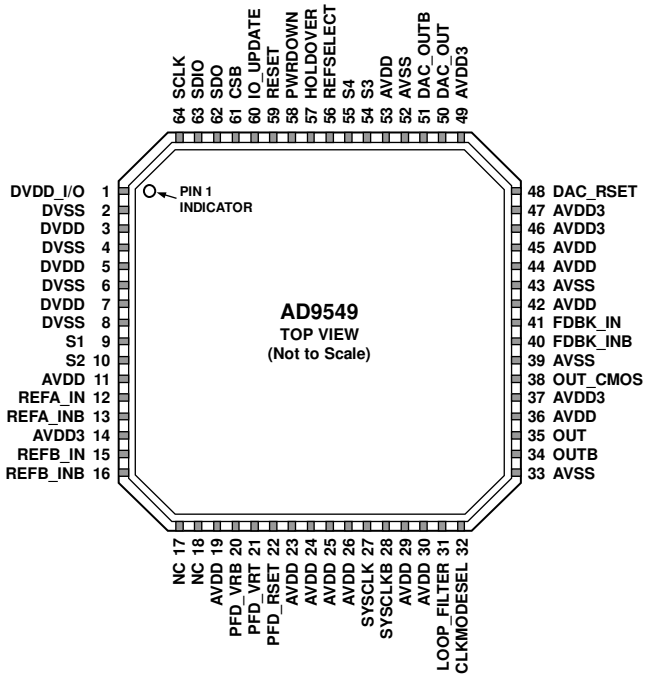
Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
64-Lead LFCSP	25.2	13.9	1.7	°C/W typical

Note that the exposed pad on the bottom of the package must be soldered to ground to achieve the specified thermal performance. See the Thermal Performance section for more information.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT.
2. THE EXPOSED THERMAL DIE ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE PART. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

06744-002

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
1	I	Power	DVDD_I/O	I/O Digital Supply.
2, 4, 6, 8	I	Power	DVSS	Digital Ground. Connect to ground.
3, 5, 7	I	Power	DVDD	Digital Supply.
9, 10, 54, 55	I/O	3.3 V CMOS	S1, S2, S3, S4	Configurable I/O Pins. These pins are configured under program control (see the Status and Warnings section) and do not have internal pull-up/pull-down resistors.
11, 19, 23 to 26, 29, 30, 36, 42, 44, 45, 53	I	Power	AVDD	Analog Supply. Connect to a nominal 1.8 V supply.
12	I	Differential input	REFA_IN	Frequency/Phase Reference A Input. This internally biased input is typically ac-coupled and, when configured as such, can accept any differential signal with single-ended swing between 0.4 V and 3.3 V. If dc-coupled, LVPECL or CMOS input is preferred.
13	I	Differential input	REFA_INB	Complementary Frequency/Phase Reference A Input. Complementary signal to the input provided on Pin 12. If using a single-ended, dc-coupled CMOS signal into REFA_IN, bypass this pin to ground with a 0.01 µF capacitor.
14, 46, 47, 49	I	Power	AVDD3	Analog Supply. Connect to a nominal 3.3 V supply.
15	I	Differential input	REFB_IN	Frequency/Phase Reference B Input. This internally biased input is typically ac-coupled and, when configured as such, can accept any differential signal with single-ended swing between 0.4 V and 3.3 V. If dc-coupled, LVPECL or CMOS input is preferred.
16	I	Differential input	REFB_INB	Complementary Frequency/Phase Reference B Input. Complementary signal to the input provided on Pin 15. If using a single-ended, dc-coupled CMOS signal into REFB_IN, bypass this pin to ground with a 0.01 µF capacitor.
17, 18			NC	No Connect. These are excess, unused pins that can be left floating.

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
20, 21	O		PFD_VRB, PFD_VRT	These pins must be capacitively decoupled. See the Phase Detector Pin Connections section for details.
22	O	Current set resistor	PFD_RSET	Connect a 5 kΩ resistor from this pin to ground (see the Phase Detector Pin Connections section).
27	I	Differential input	SYSCLK	System Clock Input. The system clock input has internal dc biasing and should always be ac-coupled, except when using a crystal. Single-ended 1.8 V CMOS can also be used, but it may introduce a spur caused by an input duty cycle that is not 50%. When using a crystal, tie the CLKMODESEL pin to AVSS, and connect crystal directly to this pin and Pin 28.
28	I	Differential input	SYSCLKB	Complementary System Clock. Complementary signal to the input provided on Pin 27. Use a 0.01 µF capacitor to ground on this pin if the signal provided on Pin 27 is single-ended.
31	O		LOOP_FILTER	System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with a 1 kΩ resistor when the system clock PLL is bypassed. See Figure 44 for a diagram of the system clock PLL loop filter.
32	I	1.8 V CMOS	CLKMODESEL	Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source. This pin can be left floating when the system clock PLL is bypassed. (See the SYSCLK Inputs section for details on the use of this pin.)
33, 39, 43, 52	O	GND	AVSS	Analog Ground. Connect to ground.
34	O	1.8 V HSTL	OUTB	Complementary HSTL Output. See the Specifications and Primary 1.8 V Differential HSTL Driver sections for details.
35	O	1.8 V HSTL	OUT	HSTL Output. See the Specifications and Primary 1.8 V Differential HSTL Driver sections for details.
37	I	Power	AVDD3	Analog Supply for CMOS Output Driver. This pin is normally 3.3 V but can be 1.8 V. This pin should be powered even if the CMOS driver is not used. See the Power Supply Partitioning section for power supply partitioning.
38	O	3.3 V CMOS	OUT_CMOS	CMOS Output. See the Specifications and the Output Clock Drivers and 2× Frequency Multiplier sections. This pin is 1.8 V CMOS if Pin 37 is set to 1.8 V.
40	I	Differential input	FDBK_INB	Complementary Feedback Input. In standard operating mode, this pin is connected to the filtered DAC_OUTB output. This internally biased input is typically ac-coupled, and when configured as such, can accept any differential signal whose single-ended swing is at least 400 mV.
41	I	Differential input	FDBK_IN	Feedback Input. In standard operating mode, this pin is connected to the filtered DAC_OUT output.
48	O	Current set resistor	DAC_RSET	DAC Output Current Setting Resistor. Connect a resistor (usually 10 kΩ) from this pin to GND. See the DAC Output section.
50	O	Differential output	DAC_OUT	DAC Output. This signal should be filtered and sent back on chip through FDBK_IN input. This pin has an internal 50 Ω pull-down resistor.
51	O	Differential output	DAC_OUTB	Complementary DAC Output. This signal should be filtered and sent back on chip through FDBK_INB input. This pin has an internal 50 Ω pull-down resistor.
56	I/O	3.3 V CMOS	REFSELECT	Reference Select Input. In manual mode, the REFSELECT pin operates as a high impedance input pin; and in automatic mode, it operates as a low impedance output pin. Logic 0 (low) indicates/selects REFA. Logic 1 (high) indicates/selects REFB. There is no internal pull-up/pull-down resistor on this pin.
57	I/O	3.3 V CMOS	HOLDOVER	Holdover (Active High). In manual holdover mode, this pin is used to force the AD9549 into holdover mode. In automatic holdover mode, it indicates holdover status. There is no internal pull-up/pull-down resistor on this pin.
58	I	3.3 V CMOS	PWRDOWN	Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power-down state. This pin has an internal 50 kΩ pull-down resistor.
59	I	3.3 V CMOS	RESET	Chip Reset. When this active high pin is asserted, the chip goes into reset. Note that on power-up, it is recommended that the user assert a high to low edge after the power supplies reach a threshold and stabilize. This pin has an internal 50 kΩ pull-down resistor.

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
60	I	3.3 V CMOS	IO_UPDATE	I/O Update. A logic transition from 0 to 1 on this pin transfers data from the I/O port registers to the control registers (see the Write section). This pin has an internal 50 kΩ pull-down resistor.
61	I	3.3 V CMOS	CSB	Chip Select. Active low. When programming a device, this pin must be held low. In systems where more than one AD9549 is present, this pin enables individual programming of each AD9549. This pin has an internal 100 kΩ pull-up resistor.
62	O	3.3 V CMOS	SDO	Serial Data Output. When the device is in 3-wire mode, data is read on this pin. There is no internal pull-up/pull-down resistor on this pin.
63	I/O	3.3 V CMOS	SDIO	Serial Data Input/Output. When the device is in 3-wire mode, data is written via this pin. In 2-wire mode, data reads and writes both occur on this pin. There is no internal pull-up/pull-down resistor on this pin.
64	I	3.3 V CMOS	SCLK	Serial Programming Clock. Data clock for serial programming. This pin has an internal 50 kΩ pull-down resistor.
Exposed Die Pad	O	GND	EPAD	Analog Ground. The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, AVDD, AVDD3, and DVDD are at nominal supply voltage; f_S = 1 GHz, DAC R_{SET} = 10 kΩ.

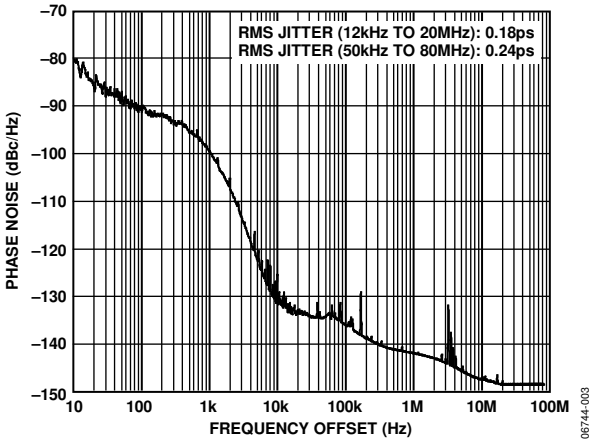


Figure 3. Additive Phase Noise at HSTL Output Driver, SYSCLK = 1 GHz (SYSCLK PLL Bypassed), f_{REF} = 19.44 MHz, f_{OUT} = 311.04 MHz, DPLL Loop BW = 1 kHz

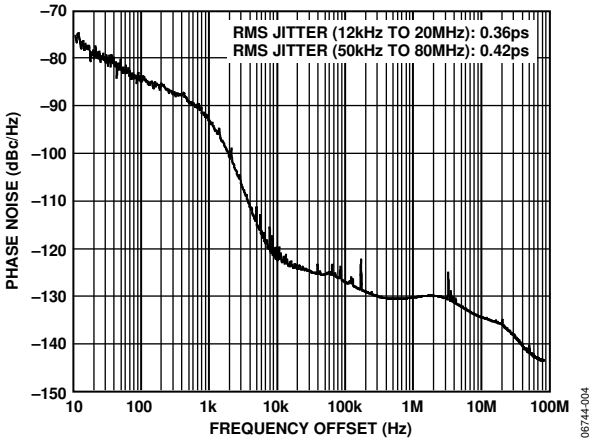


Figure 4. Additive Phase Noise at HSTL Output Driver, SYSCLK = 1 GHz (SYSCLK PLL Bypassed), f_{REF} = 19.44 MHz, f_{OUT} = 622.08 MHz, DPLL Loop BW = 1 kHz, HSTL Output Doubler Enabled

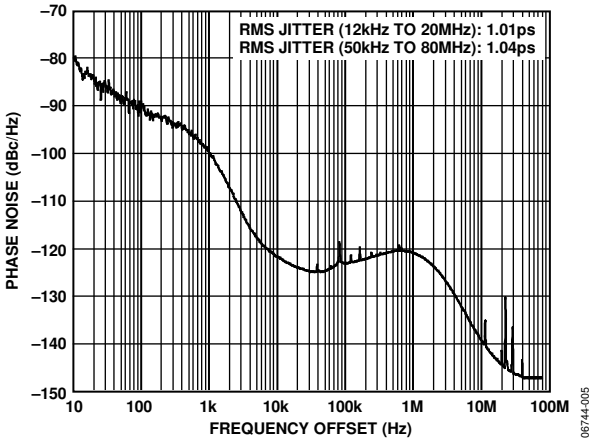


Figure 5. Additive Phase Noise at HSTL Output Driver, SYSCLK = 1 GHz (SYSCLK PLL Enabled Driven by R&S SMA100 Signal Generator at 50 MHz), f_{REF} = 19.44 MHz, f_{OUT} = 311.04 MHz, DPLL Loop BW = 1 kHz

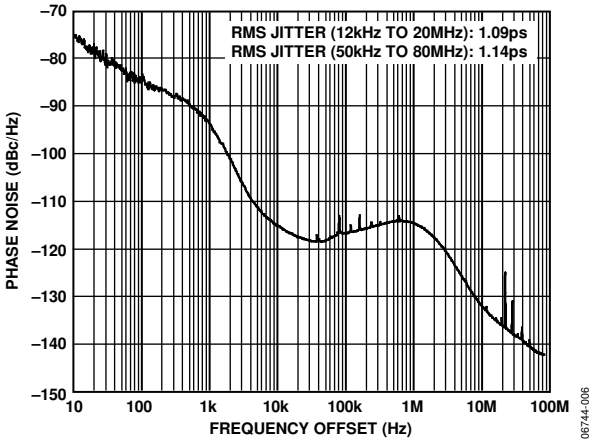


Figure 6. Additive Phase Noise at HSTL Output Driver, SYSCLK = 1 GHz (SYSCLK PLL Enabled and Driven by R&S SMA100 Signal Generator at 50 MHz), f_{REF} = 19.44 MHz, f_{OUT} = 622.08 MHz, DPLL Loop BW = 1 kHz, System Clock Doubler Enabled, HSTL Doubler Enabled

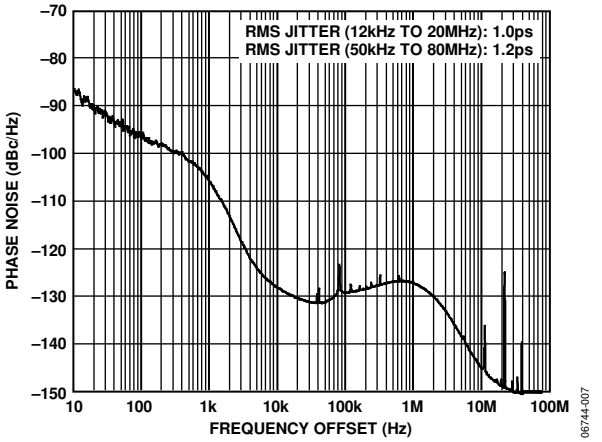


Figure 7. Additive Phase Noise at HSTL Output Driver, SYSCLK = 1 GHz (SYSCLK PLL Enabled and Driven by R&S SMA100 at 50 MHz), f_{REF} = 19.44 MHz, f_{OUT} = 155.52 MHz, SYSCLK Doubler Enabled, DPLL Loop BW = 1 kHz

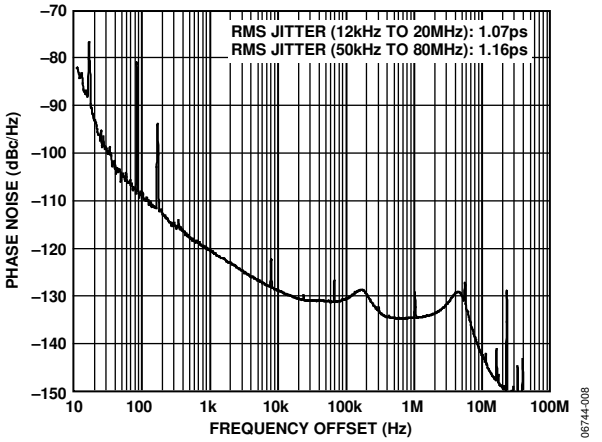


Figure 8. Additive Phase Noise at HSTL Output Driver, SYSCLK = 1 GHz (SYSCLK PLL Enabled and Driven by R&S SMA100 Signal Generator at 50 MHz), f_{REF} = 8 kHz, f_{OUT} = 155.52 MHz, DPLL Loop BW = 10 Hz

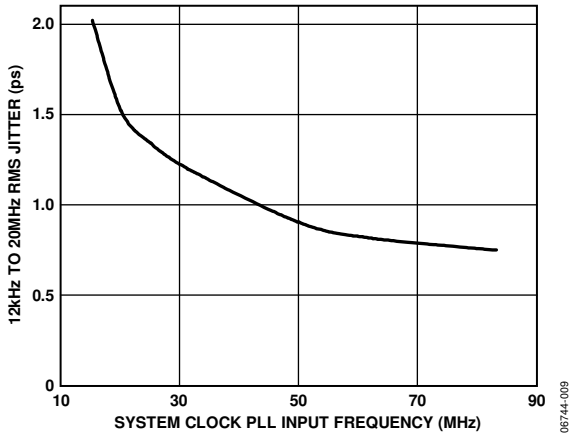


Figure 9. 12 kHz to 20 MHz RMS Jitter vs. System Clock PLL Input Frequency, SYSCLK = 1 GHz, f_{REF} = 19.44 MHz, f_{OUT} = 155.52 MHz

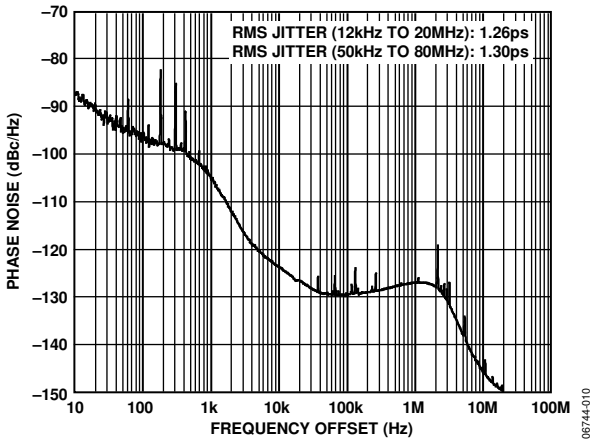


Figure 10. Additive Phase Noise at HSTL Output Driver, SYSCLK = 1 GHz (SYSCLK PLL Enabled and Driven by a 25 MHz Fox Crystal Oscillator), f_{REF} = 19.44 MHz, f_{OUT} = 155.52 MHz, DPLL Loop BW = 1 kHz

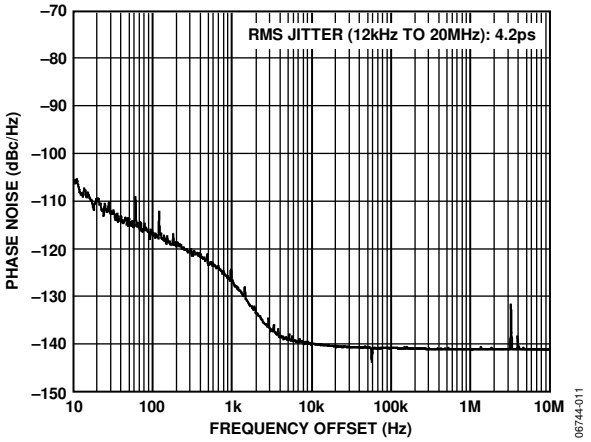


Figure 11. Additive Phase Noise at HSTL Output Driver, SYSCLK = 500 MHz (SYSCLK PLL Disabled), f_{REF} = 10.24 MHz, f_{OUT} = 20.48 MHz, DPLL Loop BW = 1 kHz

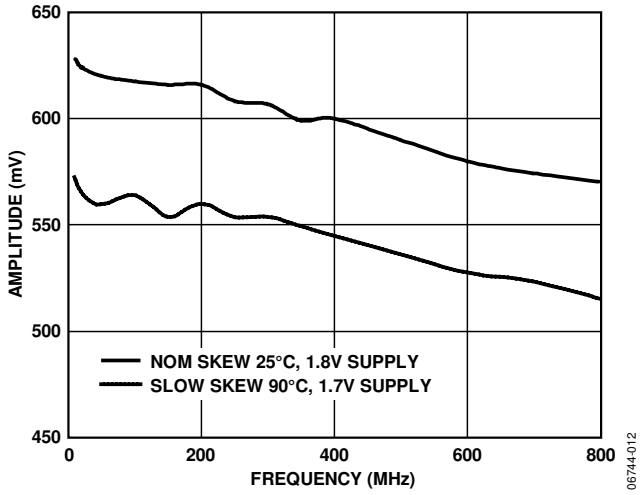


Figure 12. HSTL Output Driver Single-Ended Peak-to-Peak Amplitude vs. Toggle Rate (100 Ω Across Differential Pair)

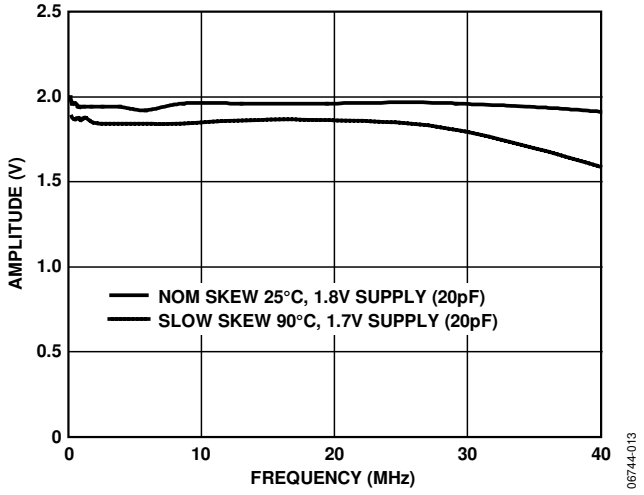


Figure 13. CMOS Output Driver Peak-to-Peak Amplitude vs. Toggle Rate (AVDD3 = 1.8 V) with 20 pF Load

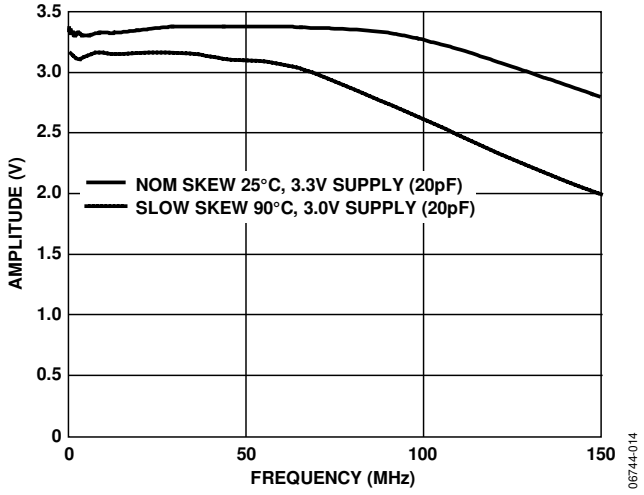


Figure 14. CMOS Output Driver Peak-to-Peak Amplitude vs. Toggle Rate (AVDD3 = 3.3 V) with 20 pF Load

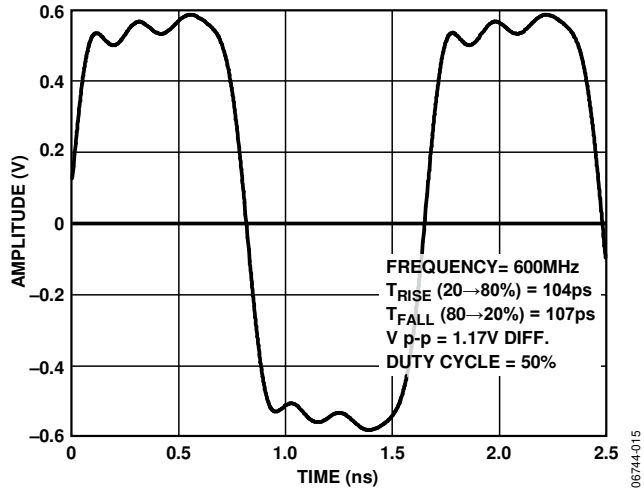


Figure 15. Typical HSTL Output Waveform, Nominal Conditions, DC-Coupled, Differential Probe Across 100 Ω load

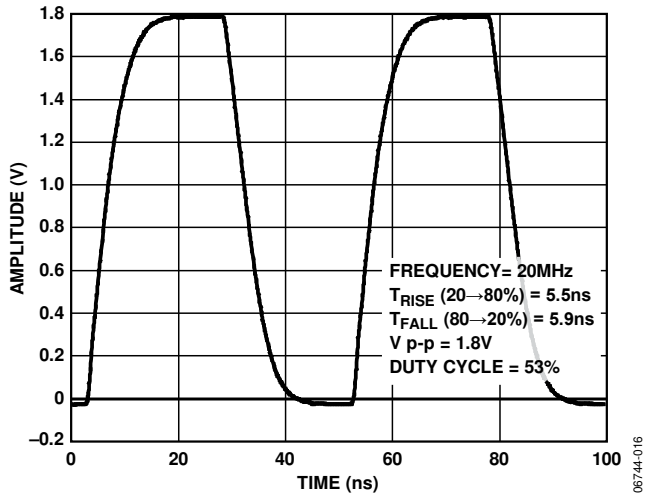


Figure 16. Typical CMOS Output Driver Waveform (@ 1.8 V), Nominal Conditions, Estimated Capacitance: 5 pF

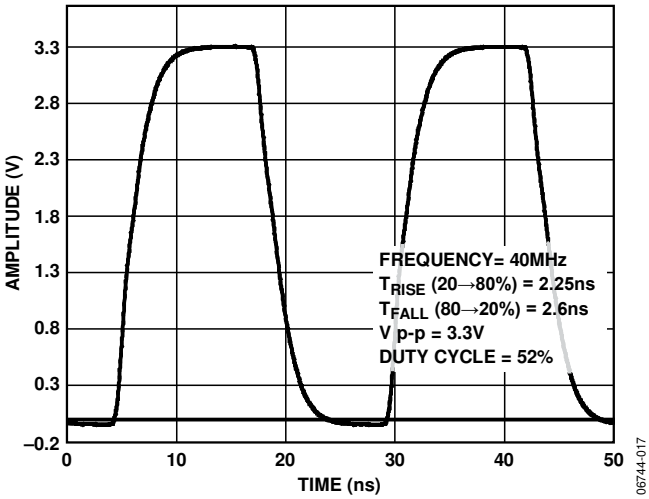


Figure 17. CMOS Output Driver Waveform (@ 3.3 V), Nominal Conditions, Estimated Capacitance: 5 pF, f_{OUT} = 20 MHz

INPUT/OUTPUT TERMINATION RECOMMENDATIONS

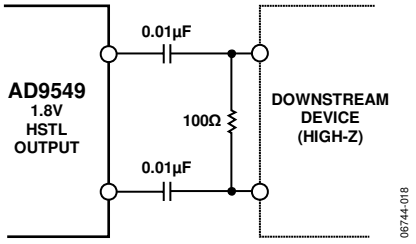


Figure 18. AC-Coupled HSTL Output Driver

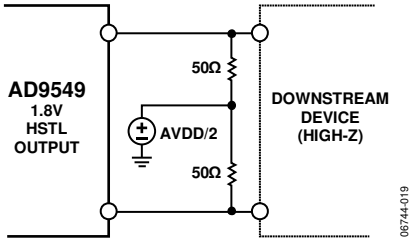


Figure 19. DC-Coupled HSTL Output Driver

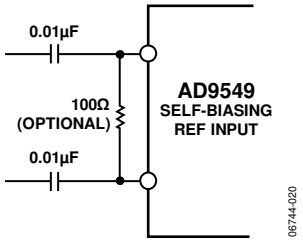


Figure 20. Reference Input

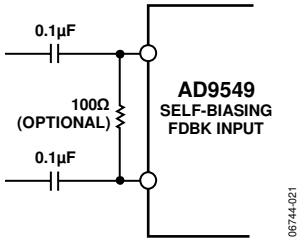


Figure 21. FDBK_IN Input

THEORY OF OPERATION

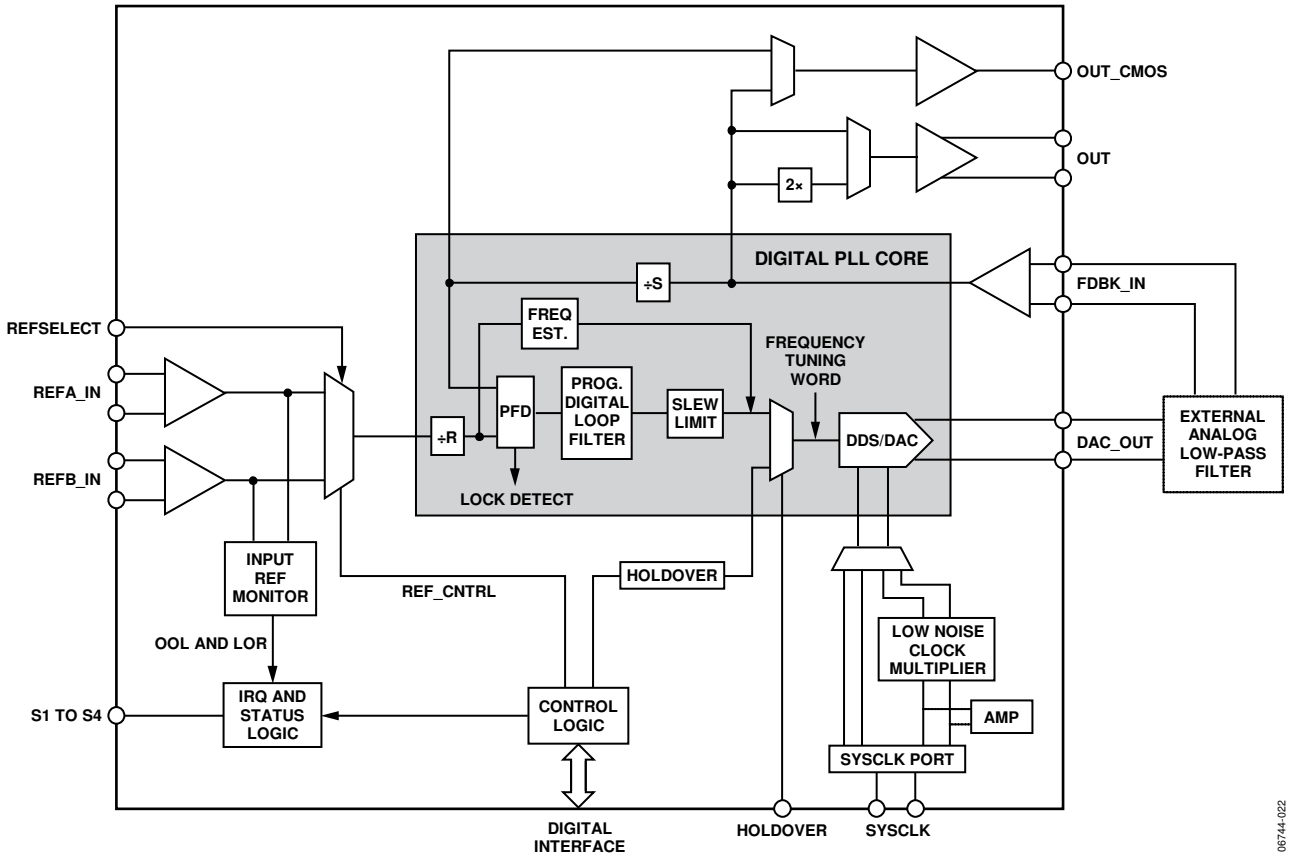


Figure 22. Detailed Block Diagram

OVERVIEW

The AD9549 provides a clocking output that is directly related in phase and frequency to the selected (active) reference (REFA or REFB) but has a phase noise spectrum primarily governed by the system clock. A wide band of reference frequencies is supported. Jitter existing on the active reference is greatly reduced by a programmable digital filter in the digital phase-locked loop (PLL), which is the core of this product. The AD9549 supports both manual and automatic holdover. While in holdover, the AD9549 continues to provide an output as long as the system clock is maintained. The frequency of the output during holdover is an average of the steady state output frequency prior to holdover.

Also offered are manual and automatic switchover modes for changing between the two references, should one become suspect or lost. A digitally controlled oscillator (DCO) is implemented using a direct digital synthesizer (DDS) with an integrated output digital-to-analog converter (DAC), clocked by the system clock. A bypassable PLL-based frequency multiplier is present, enabling use of an inexpensive, low frequency source for the system clock. For best jitter performance, the system clock PLL should be bypassed; and a low noise, high frequency system clock should be provided directly. Sampling theory sets an upper bound for the DDS output frequency at 50% of f_S (where f_S is the DAC sample rate), but a practical limitation of 40% of f_S is generally recommended to allow for the selectivity of the required off-chip reconstruction filter. The output signal from the reconstruction filter is fed back to the AD9549, both to complete the PLL and to be processed through the output circuitry. The output circuitry includes HSTL and CMOS output buffers, as well as a frequency doubler for designs that must provide frequencies above the Nyquist level of the DDS.

The individual functional blocks are described in the following sections.

DIGITAL PLL CORE (DPLLC)

The digital phase-locked loop core (DPLLC) includes the frequency estimation block and the digital phase lock control block driving the DDS.

The start of the DPLLC signal chain is the reference signal, f_R, which appears on REFA or REFB inputs. The frequency of this signal can be divided by an integer factor of R via the feedforward divider. The output of the feedforward divider is routed to the phase/frequency detector (PFD). Therefore, the frequency at the input to the PFD is given by

$$f_{PFD} = \frac{f_R}{R}$$

The PFD outputs a time series of digital words that are routed to the digital loop filter. The digital filter implementation offers many advantages: The filter response is determined by numeric coefficients rather than by discrete component values; there is no aging of components and, therefore, no drift of component value over time; there is no thermal noise in the loop filter; and there is no control node leakage current (which causes reference feedthrough in a traditional analog PLL).

The output of the loop filter is a time series of digital words. These words are applied to the frequency tuning input of a DDS to steer the DCO frequency. The DDS provides an analog output signal via an integrated DAC, effectively mimicking the operation of an analog voltage-controlled oscillator (VCO).

The DPLLC can be programmed to operate in conjunction with an internal frequency estimator to help decrease the time required to achieve lock. When the frequency estimator is employed, frequency acquisition is accomplished in the following two-step process:

1. An estimate is made of the frequency of f_{PFD}. The phase lock control loop is essentially inoperative during the frequency estimation process. When a frequency estimate is made, it is delivered to the DDS so that its output frequency is approximately equal to f_{PFD} multiplied by S (the modulus of the feedback divider).
2. The phase lock control loop becomes active and acts as a servo to acquire and hold phase lock with the reference signal.

As mentioned in Step 1, the DPLLC includes a feedback divider that allows the DCO to operate at an integer multiple (S) of f_{PFD}. This establishes a nominal DCO frequency (f_{DDS}), given by

$$f_{DDS} = \left(\frac{S}{R}\right) f_R$$

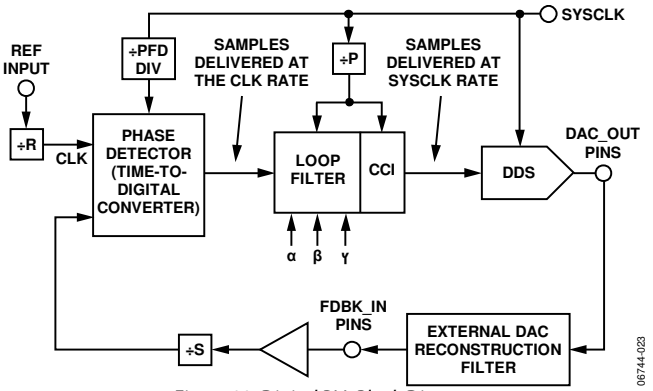


Figure 23. Digital PLL Block Diagram

Feedforward Divider (Divide-by-R)

The feedforward divider is an integer divider that allows frequency prescaling of the REF source input signal while maintaining the desired low jitter performance of the AD9549.

The feedforward divider is a programmable modulus divider with very low jitter injection. The divider is capable of handling input frequencies as high as 750 MHz. The divider depth is 16 bits, cascaded with an additional divide-by-2. Therefore, the divider is capable of integer division from 1 to 65,535 (index of 1) or from 2 to 131,070 (index of 2). The divider is programmed via the I/O register map to trigger on either the rising (default) or falling edge of the REF source input signal. Note that the value stored in the R-divider register is one less than the actual R-divider, so setting the R-divider register to 0 results in an R-divider that is equal to 1.

There is a lower bound on the value of R that is imposed by the phase frequency detector within the DPLLC, which has a maximum operating frequency of $f_{PFD[MAX]}$, as explained in the Fine Phase Detector section. The R-divider/2 bit must be set when REFA or REFB is greater than 400 MHz. The user must also ensure that R is chosen so that it satisfies the inequality.

$$R \geq \text{ceil}\left(\frac{f_R}{f_{PFD[MAX]}}\right)$$

The upper bound is

$$R \leq \text{floor}\left(\frac{f_R}{8\text{ kHz}}\right)$$

where the ceil(x) function yields the nearest integer ≥ x.

For example, if f_R = 155 MHz and $f_{PFD[MAX]}$ = 24.5 MHz, then ceil (155/24.5) = 7, so R must be ≥7.

Feedback Divider (Divide-by-S)

The feedback divider is an integer divider allowing frequency multiplication of the REF signal that appears at the input of the phase detector. It is capable of handling frequencies well above the Nyquist limit of the DDS. The divider depth is 16 bits, cascaded with an additional divide-by-2. Therefore, the divider is capable of integer division from 1 to 65,535 (index of 1) or from 2 to 131,070 (index of 2). The divider is programmed via the I/O register map to trigger on either the rising (default) or falling edge of the feedback signal. Note that the value stored in the S-divider register is one less than the actual R-divider, so setting the S-divider register to 0 results in an S-divider equal to 1.

The feedback divider must be programmed within certain boundaries. The S-divider/2 bit must be set when FDBK_IN is greater than 400 MHz. The upper boundary on the feedback divider is the lesser of the maximum programmable value of S and the maximum practical output frequency of the DDS (~40% f_S). Two equations are given: S_{MAX1} for a feedback divider index of 1 and S_{MAX2} for an index of 2.

$$S_{MAX1} = \min\left(\frac{40\% f_S R}{f_R}, 65{,}535\right)$$

or

$$S_{MAX2} = \min\left(\frac{40\% f_S R}{f_R}, 131{,}070\right)$$

where R is the modulus of the feedforward divider, f_S is the DAC sample rate, and f_R is the input reference frequency.

The DCO has a minimum frequency, $f_{DCO[MIN]}$ (see the DAC Output Characteristics section of the AC Specifications table). This minimum frequency imposes a lower bound, S_{MIN}, on the feedback divider value, as well.

$$S_{MIN} = \max\left(R\left(\frac{f_{DCO[MIN]}}{f_R}\right), 1\right)$$

Note that reduced DCO frequencies result in worse jitter performance (a consequence of the reduced slew rate of the sinusoid generated by the DDS).

Forward and Reverse FEC Clock Scaling

The feedforward divider (divide-by-R) and feedback divider (divide-by-S) enable FEC clock scaling. For instance, to multiply the incoming signal by 255/237, set the S-divider to 255 and the R-divider to 237. Be careful to abide by the limitations on the R- and S-dividers, and make sure the phase detector input frequency is within specified limits.

Phase Detector

The phase detector is composed of two detectors: a coarse phase detector and a fine phase detector. The two detectors operate in parallel. Both detectors measure the duration (Δt) of the pulses generated by a conventional three-state phase/frequency detector.

Together, the fine and coarse phase detectors produce a digital word that is a time-to-digital conversion of the separation between the edge transitions of the prescaled reference signal and the feedback signal.

If the fine phase detector is able to produce a valid result, this result alone serves as the phase error measurement. If the fine phase detector is in either an overflow or underflow condition, the phase error measurement uses the coarse phase detector instead.

Digital Loop Filter

The digital loop filter integrates and low-pass filters the digital phase error values delivered by the phase detector. The loop filter response mimics that of a second-order RC network used to filter the output of a typical phase detector and charge pump combination, as shown in Figure 24.

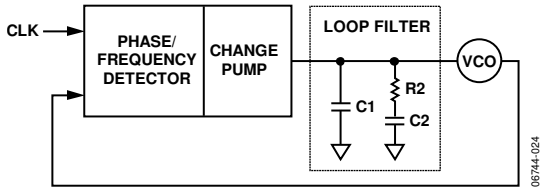


Figure 24. Typical Analog PLL Block Diagram

The building blocks implemented on the AD9549, however, are digital. A time-to-digital converter that produces digital values proportional to the edge timing error between the CLK and feedback signals replaces the phase-frequency detector and charge pump. A digital filter that processes the edge timing error samples from the time-to-digital converter replaces the loop filter. A DDS replaces the VCO, which produces a frequency that is linearly related to the digital value provided by the loop filter. This is shown in Figure 25 with some additional detail.

The samples provided by the time-to-digital converter are delivered to the loop filter at a sample rate equal to the CLK frequency (that is, f_R/R). The loop filter is intended to oversample the time-to-digital converter output at a rate determined by the P-divider. The value of P is programmable via the I/O register map. It is stored as a 5-bit number, P_{IO}. The value of P_{IO} is related to P by the equation

$$P = 2^{PIO}$$

where $5 \le P_{IO} \le 16$.

Hence, the P-divider can provide divide ratios between 32 and 65,536 in power-of-2 steps. With a DAC sample rate of 1 GHz, the loop filter sample rate can range from as low as 15.26 kHz to a maximum of 31.25 MHz. Coupled to the loop filter is a cascaded comb integrator (CCI) filter that provides a sample rate translation between the loop filter sample rate (f_S/P) and the DDS sample rate, f_S.

The choice of P is important because it controls both the response of the CCI filter and the sample rate of the loop filter. To understand the method for determining a useful value for P, it is first necessary to examine the transfer function of the CCI filter.

$$H(\omega)_{CCI} = \left[\frac{1 - e^{j\omega P}}{P(1 - e^{-j\omega}}\right]^2$$

or

$$\left|H_{CCI}(\omega)\right| = \left|\begin{array}{ll} 1, & \omega = 0 \\ \dfrac{1}{p_2}\left(\dfrac{1-\cos(\omega P)}{1-\cos(\omega)}\right), & \omega > 0 \end{array}\right.$$

To evaluate the response in terms of absolute frequency, make the substitution

$$\omega = \frac{2\pi f}{f_S}$$

where f_S is the DAC sample rate, and f is the frequency at which H_{CCI} is to be evaluated.

Analysis of this function reveals that the CCI magnitude response follows a low-pass characteristic that consists of a series of P lobes. The lobes are bounded by null points occurring at frequency multiples of f_S/P. The peak of each successive lobe is lower than its predecessor over the frequency range between dc and one-half f_S. For frequencies greater than one-half f_S, the response is a reflection about the vertical at one-half f_S. Furthermore, the first lobe (which appears between dc and f_S/P) exhibits a monotonically decreasing response. That is, the magnitude is unity at dc, and it steadily decreases with frequency until it vanishes at the first null point (f_S/P).

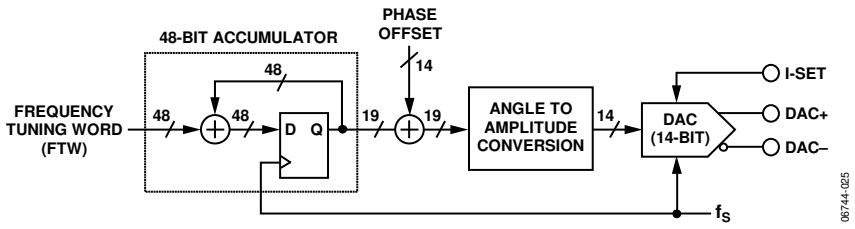


Figure 25. DDS Block Diagram

The null points imply the existence of transmission zeros placed at finite frequencies. While transmission zeros placed at infinity yield minimal phase delay, zeros placed closer to dc result in increased phase delay. Hence, the position of the first null point has a significant impact on the phase delay introduced by the CCI filter. This is an important consideration because excessive phase delay negatively impacts the overall closed-loop response. As a rule of thumb, choose a value for P so that the frequency of the first null point (f_S/P) is the greater of 80× the desired loop bandwidth or 1.5× the frequency of CLK (f_R/R).

The value of P thus calculated (P_{MAX}) is the largest usable value in practice. Because P is programmed as P_{IO}, it is necessary to define P_{MAX} in terms of P_{IO} so that P_{IOMAX} can be determined. The condition $P_{IO} \le P_{IOMAX}$ ensures that the impact of the phase delay of the CCI filter on the phase margin of the loop does not exceed 5°. P_{IOMAX} can be expressed as

$$P_{IOMAX} = \max\left\langle 5, \min\left\{ 16, \text{floor}\left[\log_2\left(\frac{f_S}{80 f_{LOOP}} \right) \right], \text{floor}\left[\log_2\left(\frac{2 f_S}{3 f_{REF}} \right) \right] \right\} \right\rangle$$

With a properly chosen value for P, the closed-loop response of the digital PLL is primarily determined by the response of the digital loop filter. Flexibility in controlling the loop filter response translates directly into flexibility in the range of applications satisfied by the architecture of the AD9549.

The AD9549 evaluation software automatically sets the value of the P-divider based on the user's input criteria. Therefore, the formulas are provided here mainly to assist in understanding how the part works.

Direct Digital Synthesizer (DDS)

One of the primary building blocks of the digital PLL is a direct digital synthesizer (DDS). The DDS behaves like a sinusoidal signal generator. The frequency of the sinusoid generated by the DDS is determined by a frequency tuning word (FTW), which is a digital (that is, numeric) value. Unlike an analog sinusoidal generator, a DDS uses digital building blocks and operates as a sampled system. Thus, it requires a sampling clock (f_S) that serves as the fundamental timing source of the DDS. The accumulator behaves as a modulo-2^{48} counter with a programmable step size that is determined by the FTW. A block diagram of the DDS is shown in Figure 25.

The input to the DDS is a 48-bit FTW that provides the accumulator with a seed value. On each cycle of f_S, the accumulator adds the value of the FTW to the running total of its output.

For example, given FTW = 5, the accumulator counts in increments of 5 sec, incrementing on each f_S cycle. Over time, the accumulator reaches the upper end of its capacity (2^{48} in this case), at which point, it rolls over, retaining the excess. The average rate at which the accumulator rolls over establishes the frequency of the output sinusoid. The average rollover rate of the accumulator is given by the following equation and establishes the output frequency (f_{DDS}) of the DDS:

$$f_{DDS} = \left(\frac{FTW}{2^{48}} \right) f_S$$

Solving this equation for FTW yields

$$FTW = \text{round}\left[2^{48} \left(\frac{f_{DDS}}{f_S} \right) \right]$$

For example, given that f_S = 1 GHz and f_{DDS} = 19.44 MHz, then FTW = 5,471,873,547,255 (0x04FA05143BF7).

The relative phase of the sinusoid can be controlled numerically, as well. This is accomplished using the phase offset input to the DDS (a programmable 14-bit value (Δphase); see the I/O Register Map section). The resulting phase offset, ΔΦ (radians), is given by

$$\Delta\Phi = 2\pi\left(\frac{\Delta phase}{2^{14}} \right)$$

The DDS can be operated in either open-loop or closed-loop mode, via the close loop bit in the PLL control register (Register 0x0100, Bit 0).

There are two open-loop modes: single tone and holdover. In single-tone mode, the DDS behaves like a frequency synthesizer and uses the value stored in the FTW0 register to determine its output frequency. Alternatively, the FTW and Δphase values can be determined by the device itself using the frequency estimator. Because single-tone mode ignores the reference inputs, it is very useful for generating test signals to aid in debugging. Single tone mode must be activated manually via register programming.

Note that due to the internal architecture of the AD9549, the LSB of the 48-bit tuning word becomes a don't care when operating the DDS in single-tone mode. This results in an effective frequency resolution of 7 μHz with the DAC system clock equal to 1 GHz.

In holdover mode, the AD9549 uses past tuning words when the loop is closed to determine its output frequency. Therefore, the loop must be successfully closed for holdover mode to work. Switching in and out of holdover mode can be either automatic or manual, depending on register settings.

Typically, the AD9549 operates in closed-loop mode. In closed-loop mode, the FTW values come from the output of the digital loop filter and vary with time. The DDS frequency is steered in a manner similar to a conventional VCO-based PLL.

Note that in closed-loop mode, the DDS phase offset capability is inoperative.

DAC Output

The output of the digital core of the DDS is a time series of numbers representing a sinusoidal waveform. This series is translated to an analog signal by means of a digital-to-analog converter (DAC).

The DAC outputs its signal to two pins driven by a balanced current source architecture (see the DAC output diagram in Figure 26). The peak output current derives from the combination of two factors. The first is a reference current (I_{DAC_REF}) established at the DAC_RSET pin, and the second is a scale factor programmed into the I/O register map.

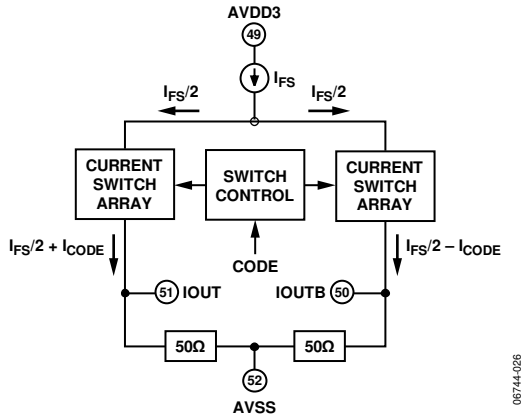


Figure 26. DAC Output Pins

The value of I_{DAC_REF} is set by connecting a resistor (R_{DAC_REF}) between the DAC_RSET pin and ground. The DAC_RSET pin is internally connected to a virtual voltage reference of 1.2 V nominal, so the reference current can be calculated by

$$I_{DAC\_REF} = \frac{1.2}{R_{DAC\_REF}}$$

Note that the recommended value of I_{DAC_REF} is 120 μA, which leads to a recommended value for R_{DAC_REF} of 10 kΩ.

The scale factor consists of a 10-bit binary number (FSC) programmed into the DAC full-scale current register (Address 0x040B and Address 0x040C) in the I/O register map. The full-scale DAC output current (I_{DAC_FS}) is given by

$$I_{DAC\_FS} = I_{DAC\_REF}\left(72 + \frac{192FSC}{1024}\right)$$

Using the recommended value of R_{DAC_REF}, the full-scale DAC output current can be set with 10-bit granularity over a range of approximately 8.6 mA to 31.7 mA. The default value is 20 mA.

PHASE DETECTOR

Coarse Phase Detector

The coarse phase detector uses the DAC sample rate (f_S) to determine the edge timing deviation between the REF signal and the feedback signal generated by the DDS. Hence, f_S sets the timing resolution of the coarse phase detector. At the recommended rate of f_S = 1 GHz, the coarse phase detector spans a range of over 131 μs (sufficient to accommodate REF signal frequencies as low as 8 kHz).

The phase gain of the coarse phase detector is controlled via the I/O registers by means of two numeric entries. The first is a 3-bit, power-of-2 scale factor, PDS. The second is a 6-bit linear scale factor, PDG.

$$PhaseGain_{CPD} = R\left(\frac{f_S}{f_R}\right)\left(2^{PDS+6}\,PDG\right)$$

Fine Phase Detector

The fine phase detector operates on a divided down version of f_S as its sampling time base. The sample rate of the fine phase detector is set using a 4-bit word (PFD_Div) in the I/O register map (Register 0x0023) and is given by

$$Fine\ Phase\ Detector\ Sample\ Rate = \frac{f_S}{4(PFD\_Div)}$$

The default value of PFD_Div is 5, so for f_S = 1 GHz, the default sample rate of the fine phase detector is 50 MHz. The upper bound on the maximum allowable input frequency to the phase detector ($f_{PFD[MAX]}$) is 49% of the sample rate, or

$$f_{PFD[MAX]} = \frac{f_S}{8(PFD\_Div)}$$

Therefore, $f_{PFD[MAX]}$ is 25 MHz in the preceding example.

The fine phase detector uses a proprietary technique to determine the phase deviation between the REF signal and feedback signal.

The phase gain of the fine phase detector is controlled by an 8-bit scale factor (FPFD_Gain) in the I/O register map (Register 0x0404). The nominal (default) value of FPFD_Gain is 200 and establishes the phase gain as

$$PhaseGain_{FP}D = \frac{R(2^{10} \times 10^7)(FPFD\_Gain)}{f_R}$$

Phase Detector Gain Matching

Although the fine and coarse phase detectors use different means to make a timing measurement, it is essential that both have equivalent phase gain. Without proper gain matching, the closed-loop dynamics of the system cannot be properly controlled. Hence, the goal is to make $PhaseGain_{CPD}$ = $PhaseGain_{FPD}$.

This leads to

$$(f_S 2^{PDS+6})PDG = (2^{10} \times 10^7)FPFD\_Gain$$

which simplifies to

$$2^{PDS} PDG = \frac{(16 \times 10^7)FPFD\_Gain}{f_S}$$

Typically, FPFD_Gain is established first, and then PDG and PDS are calculated. The proper choice for PDS is given by

$$PDS = \text{round}\left[\log_2\left(\frac{10^7 \times FPFD\_Gain}{2f_S}\right)\right]$$

The final value of PDS must satisfy 0 ≤ PDS ≤ 7. The proper choice for PDG is calculated using the following equation:

$$PDG = \text{round}\left(\frac{10^7 FPFD\_Gain}{2^{PDS-4} f_S}\right)$$

The final value of PDG must satisfy 0 ≤ PDG ≤ 63. For example, let f_S = 700 MHz and FPFD_Gain = 200; then PDS = 1 and PDG = 23.

Note that the AD9549 evaluation software calculates register values that have the phase detector gains already matched.

Phase Detector Pin Connections

There are three pins associated with the phase detector that must be connected to external components. Figure 27 shows the recommended component values and their connections.

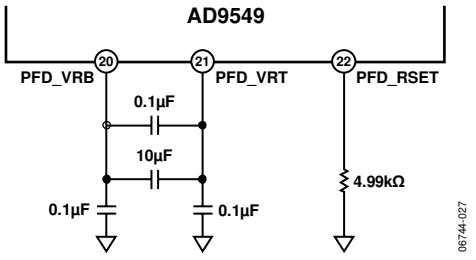


Figure 27. Phase Detector Pin Connections

DIGITAL LOOP FILTER COEFFICIENTS

To provide the desired flexibility, the loop filter has been designed with three programmable coefficients (α, β, and γ). The coefficients, along with P (where $P = 2^{PIO}$), completely define the response of the filter, which is given by

$$H(\omega)_{LoopFilter} = \alpha\left(\frac{e^{j\omega} + (\beta - \gamma - 1)}{e^{j2\omega} + (-\gamma - 2)e^{j\omega} + (\gamma + 1)}\right)$$

To evaluate the response in terms of absolute frequency, substitute

$$\omega = \frac{2\pi Pf}{f_S}$$

where P is the divide ratio of the P-divider, f_S is the DAC sample rate, and f is the frequency at which the function is to be evaluated.

The loop filter coefficients are determined by the AD9549 evaluation software according to three parameters:

- Φ is the desired closed-loop phase margin (0 < Φ< π/2 rad).
- f_{LOOP} is the desired open-loop bandwidth (Hz).
- f_{DDS} is the desired output frequency of the DDS (Hz). Note that f_{DDS} can also be expressed as $f_{DDS} = f_R(S/R)$.

The three coefficients are calculated according to parameters via the following equations:

$$\beta = -4\pi P f_C \tan(\Phi)$$

$$\gamma = \tfrac{1}{2} F(\Phi)\beta$$

$$\alpha = -\left(\frac{2^{38}\pi}{10^7 FPFD\_Gain}\right) f_{DDS} f_C F(\Phi)\beta$$

where:

$$F(\Phi) = 1 + \frac{1}{\sin(\Phi)}$$

$$f_C = \frac{f_{LOOP}}{f_S}$$

FPFD_Gain is the value of the gain scale factor for the fine phase detector as programmed into the I/O register map.

Note that the range of loop filter coefficients is limited as follows:

$0 < \alpha < 2^{23}$ (~8.39×10^6)
$-0.125 < \beta < 0$
$-0.125 < \gamma < 0$

The preceding constraints on β and γ constrain the closed-loop phase margin such that both β and γ assume negative values. Even though β and γ are limited to negative quantities, the values as programmed are positive. The negative sign is assumed internally.

Note that the closed-loop phase margin is limited to the range of 0° < Φ < 90° because β and γ are negative.

The three coefficients are implemented as digital elements, necessitating quantized values. Determination of the programmed coefficient values in this context follows.

The quantized α coefficient is composed of three factors, where α_0, α_1, and α_2 are the programmed values for the α coefficient.

$$\alpha_{QUANTIZED} = \left(\frac{\alpha_0}{2048}\right)\left(2^{\alpha_1}\right)\left(2^{-\alpha_2}\right)$$

The boundary values for each are $0 \le \alpha_0 \le 4095$, $0 \le \alpha_1 \le 22$, and $0 \le \alpha_2 \le 7$. The optimal values of α_0, α_1, and α_2 are

$$\alpha_1 = \max\left[0, \min\left\{22, \text{ceil}\left(\log_2 \frac{2048\alpha}{4095}\right)\right\}\right]$$

$$\alpha_2 = \max\left[0, \min\left\{7, \text{floor}\left(\log_2\left(\frac{4095}{\alpha}\right) + \alpha_1 - 11\right)\right\}\right]$$

$$\alpha_0 = \max\left[0, \min\left\{4095, \text{round}\left(\alpha \times 2^{\alpha_2 - \alpha_1 + 11}\right)\right\}\right]$$

The magnitude of the quantized β coefficient is composed of two factors

$$\beta_{QUANTIZED} = \left(\beta_0\right)\left(2^{-(\beta_1 + 15)}\right)$$

where β_0 and β_1 are the programmed values for the β coefficient.

The boundary values for each are $0 \le \beta_0 \le 4095$ and $0 \le \beta_1 \le 7$. The optimal values of β_0 and β_1 are

$$\beta_1 = \max\left[0, \min\left\{7, \text{floor}\left(\log_2\left(\frac{4095}{|\beta|}\right) - 15\right)\right\}\right]$$

$$\beta_0 = \max\left[0, \min\left\{4095, \text{round}\left(|\beta| \times 2^{\beta_1 + 15}\right)\right\}\right]$$

The magnitude of the quantized γ coefficient is composed of two factors.

$$\gamma_{QUANTIZED} = \left(\gamma_0\right)\left(2^{-(\gamma_1 + 15)}\right)$$

where γ_0 and γ_1 are the programmed values for the γ coefficient. The boundary values for each are $0 \le \gamma_0 \le 4095$ and $0 \le \gamma_1 \le 7$. The optimal values of γ_0 and γ_1 are

$$\gamma_1 = \max\left[0, \min\left\{7, \text{floor}\left(\log_2\left(\frac{4095}{|\gamma|}\right) - 15\right)\right\}\right]$$

$$\gamma_0 = \max\left[0, \min\left\{4095, \text{round}\left(|\gamma| \times 2^{\gamma_1 + 15}\right)\right\}\right]$$

The min(), max(), floor(), ceil() and round() functions are defined as follows:

- The function min(x_1, x_2, … x_n) chooses the smallest value in the list of arguments.
- The function max(x_1, x_2, … x_n) chooses the largest value in the list of arguments.
- The function ceil(x) increases x to the next higher integer if x is not an integer; otherwise, x is unchanged.
- The function floor(x) reduces x to the next lower integer if x is not an integer; otherwise, x is unchanged.
- The function round(x) rounds x to the nearest integer.

To demonstrate the wide programmable range of the loop filter bandwidth, consider the following design example. The system clock frequency (f_S) is 1 GHz, the input reference frequency (f_R) is 19.44 MHz, the DDS output frequency (f_{DDS}) is 155.52 MHz, and the required phase margin (Φ) is 45°. f_R is within the nominal bandwidth of the phase detector (25 MHz), and f_{DDS}/f_R is an integer (8), so the prescaler is not required. Therefore, R = 1 and S = 8 can be used for the feedforward and feedback dividers, respectively.

Note that if f_{DDS}/f_R is a noninteger, then R and S must be chosen such that $S/R = f_{DDS}/f_R$ with S and R both constrained to integer values. For example, if f_R = 10 MHz and f_{DDS} = 155.52 MHz, then the optimal choice for S and R is 1944 and 125, respectively.

The open-loop bandwidth range under the defined conditions spans 9.5 Hz to 257.5 kHz. The wide dynamic range of the loop filter coefficients allows for programming of any open-loop bandwidth within this range under these conditions. The resulting closed-loop bandwidth range under the same conditions is approximately 12 Hz to 359 kHz.

The resulting loop filter coefficients for the upper loop bandwidth, along with the necessary programming values, are shown as follows:

α = 4322509.4784981
α_0 = 2111 (0x83F)
α_1 = 22 (0x16)
α_2 = 0 (0x00)
β = −0.10354689386232
β_0 = 3393 (0xD41)
β_1 = 0 (0x00)
γ_0 = 4095 (0xFFF)
γ = −0.12499215775201
γ_1 = 0 (0x00)

The resulting loop filter coefficients for the lower loop bandwidth, along with the necessary programming values, are shown as follows:

$\alpha = 0.005883404361345$
$\alpha_0 = 1542$ (0x606)
$\alpha_1 = 0$ (0x00)
$\alpha_2 = 7$ (0x07)
$\beta = -0.000003820176667$
$\beta_0 = 16$ (0x10)
$\beta_1 = 7$ (0x07)
$\gamma = -0.00000461136116$
$\gamma_0 = 19$ (0x13)
$\gamma_1 = 7$ (0x07)

The AD9549 evaluation software generates these coefficients automatically based on the user's desired loop characteristics.

CLOSED-LOOP PHASE OFFSET

The AD9549 provides for limited control over the phase offset between the reference input signal and the output signal by adding a constant phase offset value to the output of the phase detector. An adder is included at the output of the phase detector to support this, as shown in Figure 28. The value of the constant (PLL_{OFFSET}) is set via the DPLL phase offset bits.

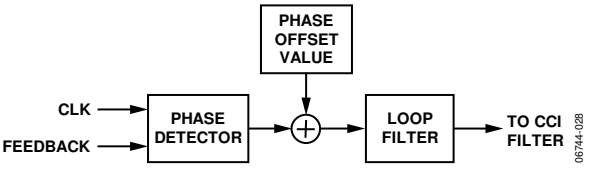


Figure 28. Input Phase Offset Adder

PLL_{OFFSET} is a function of the phase detector gain and the desired amount of timing offset (Δt_{OFFSET}). It is given by

$$PLL_{OFFSET} = \Delta t_{OFFSET}(2^{10} \times 10^7 \times FPFD\_Gain$$

FPFD_Gain is described in the Fine Phase Detector section.

For example, suppose that FPFD_Gain = 200, f_{CLK} = 3 MHz, and 1° of phase offset is desired. First, the value of Δt_{OFFSET} must be determined, as follows:

$$\Delta t_{OFFSET} = \frac{\deg}{360} t_{CLK} = \frac{1}{360}\left(\frac{1}{3\text{ MHz}}\right) = 925.9\text{ ps}$$

Having determined Δt_{OFFSET},

$$PLL_{OFFSET} = 925.9\text{ ps}(2^{10} \times 10^7 \times 200) = 1896$$

The result has been rounded because PLL_{OFFSET} is restricted to integer values.

Note that the PLL_{OFFSET} value is programmed as a 14-bit, twos complement number. However, the user must ensure that the magnitude is constrained to 12 bits, such that:

$$-2^{11} \le PLL_{OFFSET} < +2^{11}$$

The preceding constraint yields a timing adjustment range of ±1 ns. This ensures that the phase offset remains within the bounds of the fine phase detector.

LOCK DETECTION

Phase Lock Detection

During the phase locking process, the output of the phase detector tends toward a value of 0, which indicates perfect alignment of the phase detector input signals. As the control loop works to maintain the alignment of the phase detector input signals, the output of the phase detector wanders around 0.

The phase lock detector tracks the absolute value of the digital samples generated by the phase detector. These samples are compared to the phase lock detect threshold value (PLDT) programmed in the I/O register map. A false state at the output of the comparator indicates that the absolute value of a sample exceeds the value in the threshold bits. A true state at the output of the comparator indicates alignment of the phase detector input signals to the degree specified by the lock detection threshold.

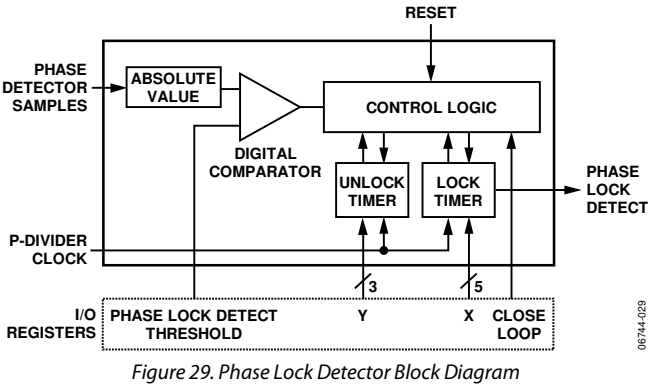


Figure 29. Phase Lock Detector Block Diagram

The phase lock detect threshold value is a 32-bit number stored in the I/O register map.

$$PLDT = \text{round}\left(\Delta t \times 2^{10} \times 10^7 \times FPFD\_Gain\right)$$

where Δt is the maximum allowable timing error between the signals at the input to the phase detector and the value of *FPFD_Gain* is as described in the Fine Phase Detector section.

For example, suppose that f_R/R = 3 MHz, FPFD_Gain = 200, and the maximum timing deviation is given as 1°. This yields a Δt value of

$$\Delta t = \frac{1°}{360°}\left(R \times T_R\right) = \frac{R}{360 f_R} = \frac{1}{360(3 \times 10^6)}$$

The resulting phase lock detect threshold is

$$PLDT = \text{round}\left(\frac{2^{10} \times 10^7 \times 200}{360(3 \times 10^6)}\right) = 1896$$

Hence, 1896 (0x00000768) is the value that must be stored in the phase lock detect threshold bits.