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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



FEATURES

- Input frequencies from 8 kHz to 710 MHz**
- Output frequencies up to 810 MHz LVPECL and LVDS (up to 200 MHz for CMOS output)**
- Preset pin-programmable frequency translation ratios cover popular wireline and wireless frequency applications, including xDSL, T1/E1, BITS, SONET, and Ethernet**
- Arbitrary frequency translation ratios via SPI port**
- On-chip VCO**
- Accepts a crystal resonator for holdover applications**
- Two single-ended (or one differential) reference input(s)**
- Two output clocks (independently programmable as LVDS, LVPECL, or CMOS)**
- SPI-compatible, 3-wire programming interface**
- Single supply (3.3 V)**
- Very low power: <450 mW (under most conditions)**
- Small package size (5 mm × 5 mm)**
- Exceeds Telcordia GR-253-CORE jitter generation, transfer, and tolerance specifications**

APPLICATIONS

- Cost effective replacement of high frequency VCXO, OCXO, and SAW resonators**
- Extremely flexible frequency translation for SONET/SDH, Ethernet, Fibre Channel, DRFI/DOCSIS, and PON/EPON/GPON**
- Wireless infrastructure**
- Test and measurement (including handheld devices)**

GENERAL DESCRIPTION

The AD9553 is a phase-locked loop (PLL) based clock translator designed to address the needs of passive optical networks (PON) and base stations. The device employs an integer-N PLL to accommodate the applicable frequency translation requirements. The user supplies up to two single-ended input reference signals or one differential input reference signal via the REFA and REFB inputs. The device supports holdover applications by allowing the user to connect a 25 MHz crystal resonator to the XTAL input.

The AD9553 is pin programmable, providing a matrix of standard input/output frequency translations from a list of 15 possible input frequencies to a list of 52 possible output frequency pairs (OUT1 and OUT2). The device also has a 3-wire SPI interface, enabling the user to program custom input-to-output frequency translations.

The AD9553 output drivers are compatible with LVPECL, LVDS, or single-ended CMOS logic levels, although the AD9553 is implemented in a strictly CMOS process.

The AD9553 operates over the extended industrial temperature range of -40°C to $+85^{\circ}\text{C}$.

BASIC BLOCK DIAGRAM

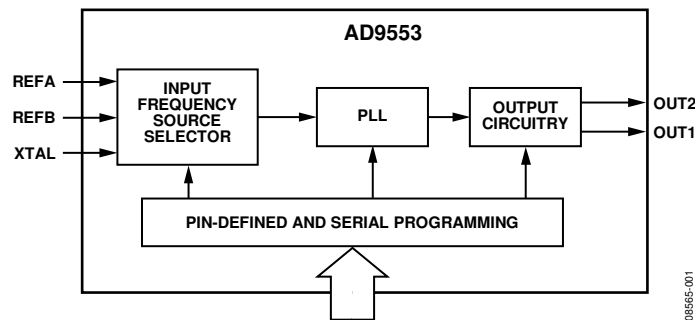


Figure 1.

08555-001

Rev. A

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AD9553* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9553 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9553: Flexible Clock Translator for GPON, Base Station, SONET/SDH, T1/E1, and Ethernet Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD9553 Evaluation Board

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

DESIGN RESOURCES

- AD9553 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9553 EngineerZone Discussions.

SAMPLE AND BUY

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REVISION HISTORY

10/10—Rev. 0 to Rev. A

Changes to Features Section, Applications Section, and General Description Section.....	1	Changes to Table 16	19
Added Table Summary to Specifications Section.....	3	Changes to PLL (PFD, Charge Pump, VCO, Feedback Divider Section.....	22
Added Supply Voltage Parameter, Table 1.....	3	Changes to Loop Filter Section, Figure 31, Table 17, PLL Locked Indicator Section, and Output Dividers Section	23
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Changes to Pin 1 and Pin 15, Table 13.....	10	Changes to Automatic Power-On Reset Section	28
Added Figure 4, Renumbered Sequentially	11	Changes to Thermal Performance Section	29
Added Figure 10, Figure 12, Figure 13, and Figure 14.....	12	Changes to Address 0x18, Address 0x32, and Address 0x34, Table 27	33
Added Input/Output Termination Recommendations Section, Figure 25, Figure 26, and Figure 27.....	15	Changes to Address 0x18, Table 31	37
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4/10—Revision 0: Initial Version

SPECIFICATIONS

Minimum (min) and maximum (max) values apply for the full range of supply voltage and operating temperature variations. Typical (typ) values apply for $V_{DD} = 3.3\text{ V}$; $T_A = 25^\circ\text{C}$, unless otherwise noted.

POWER CONSUMPTION

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE	3.135	3.30	3.465	V	Pin 18, Pin 21, and Pin 28
TOTAL CURRENT		162	185	mA	Tested with both output channels active at maximum output frequency; LVPECL and LVDS outputs use a $100\ \Omega$ termination between both pins of the output driver
VDD CURRENT BY PIN					Tested with both output channels active at maximum output frequency; LVPECL and LVDS outputs use a $100\ \Omega$ termination between both pins of the output driver
Pin 18		93	106	mA	
Pin 21					
LVDS Configured Output		35	41	mA	
LVPECL Configured Output		36	42	mA	
CMOS Configured Output		29	34	mA	
Pin 28					
LVDS Configured Output		35	41	mA	
LVPECL Configured Output		36	42	mA	
CMOS Configured Output		29	34	mA	

LOGIC INPUT PINS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT CHARACTERISTICS ¹					
Logic 1 Voltage, V_{IH}	1.02			V	For the CMOS inputs, a static Logic 1 results from either a pull-up resistor or no connection
Logic 0 Voltage, V_{IL}			0.64	V	
Logic 1 Current, I_{IH}			3	μA	
Logic 0 Current, I_{IL}			17	μA	

¹ The A3 to A0 and Y5 to Y0 pins have 100 k Ω internal pull-up resistors. The OM2 to OM0 pins have 40 k Ω pull-up resistors when the device is not in SPI mode.

LOGIC OUTPUT PINS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS					
Output Voltage High, V_{OH}	2.7			V	Tested at 1 mA load current
Output Voltage Low, V_{OL}			0.19	V	Tested at 1 mA load current

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RESET PIN

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT CHARACTERISTICS ¹					
Input Voltage High, V_{IH}	1.96			V	
Input Voltage Low, V_{IL}			0.85	V	
Input Current High, I_{INH}		0.3	12.5	μ A	
Input Current Low, I_{INL}		31	43	μ A	
MINIMUM PULSE WIDTH LOW	150			μ s	Tested with an active source driving the $\overline{\text{RESET}}$ pin

¹ The $\overline{\text{RESET}}$ pin has a 100 k Ω internal pull-up resistor.

REFERENCE CLOCK INPUT CHARACTERISTICS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments	
DIFFERENTIAL INPUT						
Input Frequency Range	0.008		250 710	MHz MHz	Assumes minimum LVDS input level and requires bypassing of the divide-by-5 divider and $\times 2$ multiplier	
Common-Mode Internally Generated Input Voltage	613	692	769	mV		Use ac coupling to preserve the internal dc bias of the differential input
Differential Input Voltage Sensitivity	250			mV p-p	Requires ac coupling; can accommodate single-ended input by ac grounding unused input; the instantaneous voltage on either pin must not exceed the 3.3 V dc supply rails	
Differential Input Resistance		5		k Ω	Pulse width high and pulse width low specifications establish the bounds for duty cycle	
Differential Input Capacitance		3		pF		
Duty Cycle						
Pulse Width Low	1.6			ns		Up to 250 MHz
Pulse Width High	1.6			ns		Up to 250 MHz
Pulse Width Low	0.64			ns		Beyond 250 MHz, up to 710 MHz
Pulse Width High	0.64			ns		Beyond 250 MHz, up to 710 MHz
CMOS SINGLE-ENDED INPUT						
Input Frequency Range	0.008		200	MHz	When ac coupling to the input receiver, the user must dc bias the input to 1 V; the single-ended CMOS input is 3.3 V compatible	
Input High Voltage	1.62			V		
Input Low Voltage			0.52	V		
Input Threshold Voltage		1.0		V		
Input High Current		0.04		μ A		
Input Low Current		0.03		μ A		
Input Capacitance		3		pF		
Duty Cycle						
Pulse Width Low	2			ns		Pulse width high and pulse width low establish the bounds for duty cycle
Pulse Width High	2			ns		
$\times 2$ FREQUENCY MULTIPLIER			125	MHz	To avoid excessive reference spurs, the $\times 2$ multiplier requires 48% to 52% duty cycle; reference clock input frequencies greater than 125 MHz require the use of the divide-by-5 divider	

VCO CHARACTERISTICS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	3350		4050	MHz	
VCO GAIN		45		MHz/V	
VCO TRACKING RANGE	±300			ppm	
VCO CALIBRATION TIME					As measured from completion of the VCO calibration command (the rising edge of \overline{CS} (Pin 12)) until the rising edge of LOCKED (Pin 20) Applies for Pin A3 to Pin A0 = 0001 to 1100, or for Pin A3 to Pin A0 = 1111
Low Bandwidth Setting (170 Hz)					
13.3 kHz PFD Frequency		214		ms	
16 kHz PFD Frequency		176		ms	
Medium Bandwidth Setting (20 kHz)					Applies for Pin A3 to Pin A0 = 1110 and Pin Y5 to Pin Y0 = 111111
1.5625 MHz PFD Frequency		1.82		ms	
High Bandwidth Setting (75 kHz)					Applies for Pin A3 to Pin A0 = 1101 to 1110
2.64 MHz PFD Frequency		1.46		ms	
4.86 MHz PFD Frequency		0.80		ms	
PLL LOCK TIME					Using the pin selected frequency settings; lock time is from the rising edge of the RESET pin to the rising edge of the LOCKED pin Applies for Pin A3 to Pin A0 = 0001 to 1100 or for Pin A3 to Pin A0 = 1111
Low Bandwidth Setting (170 Hz)					
13.3 kHz PFD Frequency		214		ms	
16 kHz PFD Frequency		176		ms	
Medium Bandwidth Setting (20 kHz)					Applies for Pin A3 to Pin A0 = 1110 and Pin Y5 to Pin Y0 = 111111
1.5625 MHz PFD Frequency		2		ms	
High Bandwidth Setting (75 kHz)					Applies for Pin A3 to Pin A0 = 1101 to 1110
2.64 MHz PFD Frequency		1.50		ms	
4.86 MHz PFD Frequency		0.89		ms	

CRYSTAL INPUT CHARACTERISTICS

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CRYSTAL FREQUENCY					
Range	10	25	52	MHz	When using the pin selected frequency settings, the device requires a 25 MHz crystal to support holdover functionality
Tolerance			20	ppm	
CRYSTAL MOTIONAL RESISTANCE			100	Ω	
CRYSTAL LOAD CAPACITANCE		10		pF	Using a crystal with a specified load capacitance other than 10 pF (8 pF to 24 pF) is possible, but necessitates using the SPI port to alter the default register values for load capacitance

OUTPUT CHARACTERISTICS

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL MODE					
Differential Output Voltage Swing	690	800	890	mV	Output driver static (for dynamic performance, see Figure 18)
Common-Mode Output Voltage	VDD – 1.66	VDD – 1.34	VDD – 1.01	V	Output driver static
Frequency Range	0		810	MHz	
Duty Cycle	40		60	%	Up to 805 MHz output frequency
Rise/Fall Time ¹ (20% to 80%)		255	305	ps	100 Ω termination between both pins of the output driver
LVDS MODE					
Differential Output Voltage Swing					Output driver static (for dynamic performance, see Figure 18)
Balanced, V _{OD}	297		398	mV	Voltage swing between the pins of a differential output pair with the output driver static
Unbalanced, ΔV _{OD}			8.3	mV	Absolute difference between voltage swing of normal pin and inverted pin with the output driver static
Offset Voltage					
Common Mode, V _{OS}	1.17		1.35	V	(V _{OH} + V _{OL})/2 across a differential pair with output driver static
Common-Mode Difference, ΔV _{OS}			7.3	mV	This is the absolute value of the difference between V _{OS} when the normal output is high vs. when the complementary output is high with output driver static
Short-Circuit Output Current		17	24	mA	Output shorted to GND
Frequency Range	0		810	MHz	
Duty Cycle	40		60	%	Up to 805 MHz output frequency
Rise/Fall Time ¹ (20% to 80%)		285	355	ps	100 Ω termination between both pins of the output driver
CMOS MODE					
Output Voltage High, V _{OH}					Output driver static; standard drive strength setting
I _{OH} = 10 mA	2.8			V	
I _{OH} = 1 mA	2.8			V	
Output Voltage Low, V _{OL}					Output driver static; standard drive strength setting
I _{OL} = 10 mA			0.5	V	
I _{OL} = 1 mA			0.3	V	
Frequency Range	0		200	MHz	3.3 V CMOS; standard drive strength setting; output toggle rates in excess of the maximum are possible, but with reduced amplitude (see Figure 17)
Duty Cycle	45		55	%	At maximum output frequency
Rise/Fall Time ¹ (20% to 80%)		500	745	ps	3.3 V CMOS; standard drive strength setting; 10 pF load

¹ The listed values are for the slower edge (rise or fall).

JITTER CHARACTERISTICS

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
JITTER GENERATION					
12 kHz to 20 MHz					
LVPECL Output		1.28		ps rms	Input = 19.44 MHz, output = 245.76 MHz
		0.89		ps rms	Input = 25 MHz, output = 125 MHz, Pin A3 to Pin A0 = 1110, Pin Y5 to Pin Y0 = 111111 (see Figure 4)
		1.31		ps rms	Input = 122.88 MHz, output = 155.52 MHz
LVDS Output		1.29		ps rms	Input = 19.44 MHz, output = 245.76 MHz
		1.32		ps rms	Input = 122.88 MHz, output = 155.52 MHz
CMOS Output		1.26		ps rms	Input = 19.44 MHz, output = 245.76 MHz, see Figure 17 regarding CMOS toggle rates above 250 MHz
		1.24		ps rms	Input = 122.88 MHz, output = 155.52 MHz
50 kHz to 80 MHz					
LVPECL Output		0.75		ps rms	Input = 19.44 MHz, output = 245.76 MHz
		0.58		ps rms	Input = 25 MHz, output = 125 MHz, Pin A3 to Pin A0 = 1110, Pin Y5 to Pin Y0 = 111111 (see Figure 4)
		0.44		ps rms	Input = 122.88 MHz, output = 155.52 MHz
LVDS Output		0.76		ps rms	Input = 19.44 MHz, output = 245.76 MHz
		0.45		ps rms	Input = 122.88 MHz, output = 155.52 MHz
CMOS Output		0.44		ps rms	Input = 19.44 MHz, output = 245.76 MHz, see Figure 17 regarding CMOS toggle rates above 250 MHz
		0.39		ps rms	Input = 122.88 MHz, output = 155.52 MHz
JITTER TRANSFER BANDWIDTH					See the Typical Performance Characteristics section
Low Bandwidth Setting		170		Hz	
Medium Bandwidth Setting		20		kHz	
High Bandwidth Setting		75		kHz	
JITTER TRANSFER PEAKING					See the Typical Performance Characteristics section
Low BW Setting		1.3		dB	
Medium BW Setting		0		dB	
High BW Setting		0.08		dB	

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SERIAL CONTROL PORT

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CS					
Input Logic 1 Voltage	1.6			V	
Input Logic 0 Voltage			0.5	V	
Input Logic 1 Current			0.03	μA	
Input Logic 0 Current		2		μA	
Input Capacitance		2		pF	
SCLK					
Input Logic 1 Voltage	1.6			V	
Input Logic 0 Voltage			0.5	V	
Input Logic 1 Current		2		μA	
Input Logic 0 Current			0.03	μA	
Input Capacitance		2		pF	
SDIO					
Input					
Input Logic 1 Voltage	1.6			V	
Input Logic 0 Voltage			0.5	V	
Input Logic 1 Current		1		μA	
Input Logic 0 Current		1		μA	
Input Capacitance		2		pF	
Output					
Output Logic 1 Voltage	2.8			V	1 mA load current
Output Logic 0 Voltage			0.3	V	1 mA load current

SERIAL CONTROL PORT TIMING

Table 11.

Parameter	Limit	Unit
SCLK		
Clock Rate, $1/t_{CLK}$	50	MHz max
Pulse Width High, t_{HIGH}	3	ns min
Pulse Width Low, t_{LOW}	3	ns min
SDIO to SCLK Setup, t_{DS}	4	ns min
SCLK to SDIO Hold, t_{DH}	0	ns min
SCLK to Valid SDIO, t_{DV}	13	ns max
\overline{CS} to SCLK Setup (t_s) and Hold (t_H)	0	ns min
\overline{CS} Minimum Pulse Width High	6.4	ns min

ABSOLUTE MAXIMUM RATINGS

Table 12.

Parameter	Rating
Supply Voltage (VDD)	3.6 V
Maximum Digital Input Voltage	-0.5 V to VDD + 0.5 V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

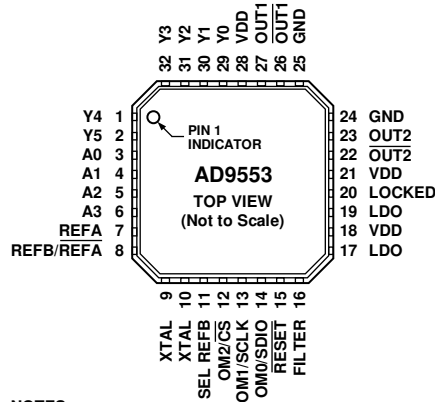
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED DIE PAD MUST BE CONNECTED TO GND.

08955-002

Figure 2. Pin Configuration

Table 13. Pin Function Descriptions

Pin No.	Mnemonic	Type ¹	Description
29, 30, 31, 32, 1, 2	Y0, Y1, Y2, Y3, Y4, Y5	I	Control Pins. These pins select one of 52 preset output frequency combinations for OUT1 and OUT2. Note that when all six control pins are Logic 0, SPI programming is active.
3, 4, 5, 6	A0, A1, A2, A3	I	Control Pins. These pins select one of 15 preset input reference frequencies. Note that when all four control pins are Logic 0, SPI programming is active.
7	REFA	I	Reference Clock Input. Connect this pin to a single-ended active clock input signal. Alternatively, this pin is the noninverted part of a differential clock input signal.
8	REFB/REFA	I	Reference Clock Input. Connect this pin to a single-ended active clock input signal. Alternatively, this pin is the inverted part of a differential clock input signal.
9, 10	XTAL	I	Crystal Resonator Input. Connect a crystal resonator across these pins. Alternatively, connect a single-ended clock source (CMOS compatible) to either input pin (let the unused pin float). When using the preset input/output frequencies via the Y5 to Y0 and A3 to A0 pins, the crystal must have a resonant frequency of 25 MHz with a specified load capacitance of 10 pF.
11	SEL REFB	I	Control Pin. This pin allows manual selection of REFA (Logic 0) or REFB (Logic 1) as the active reference assuming that the desired reference signal is present. Note that this pin is nonfunctional when Register 0x29[5] = 1.
12	OM2/CS	I	Digital Input. When the device is not in SPI mode, this pin is an output mode control pin (OM2) with an internal 40 kΩ pull-up resistor. The OM2 pin, in conjunction with the OM0 and OM1 pins, allows the user to select one of eight output configurations (see Table 21). In SPI mode, this pin is an active low chip select (CS) with no internal pull-up resistor.
13	OM1/SCLK	I	Digital Input. When the device is not in SPI mode, this pin is an output mode control pin (OM1) with an internal 40 kΩ pull-up resistor. The OM1 pin, in conjunction with the OM0 and OM2 pins, allows the user to select one of eight output configurations (see Table 21). In SPI mode, this pin is the serial data clock (SCLK) with no internal pull-up resistor.
14	OM0/SDIO	I/O	Digital Input/Output. When the device is not in SPI mode, this pin is an input only and functions as an output mode control pin (OM0) with an internal 40 kΩ pull-up resistor. The OM0 pin, in conjunction with the OM1 and OM2 pins, allows the user to select one of eight output configurations (see Table 21). In SPI mode, this pin is the serial data input/output (SDIO) with no internal pull-up resistor.
15	RESET	I	Reset Internal Logic. This is a digital input pin. This pin is active low with a 100 kΩ internal pull-up resistor and resets the internal logic to default states (see the Automatic Power-On Reset section).
16	FILTER	I/O	Loop Filter Node for the PLL. Connect external loop filter components (see Figure 30) from this pin to Pin 17 (LDO).
17, 19	LDO	P/O	LDO Decoupling Pins. Connect a 0.47 μF decoupling capacitor from each of these pins to ground.
18, 21, 28	VDD	P	Power Supply Connection: 3.3 V Analog Supply.
20	LOCKED	O	Active High Locked Status Indicator for the PLL.
26, 22	OUT1, OUT2	O	Complementary Square Wave Clocking Outputs.
27, 23	OUT1, OUT2	O	Square Wave Clocking Outputs.
24, 25	GND	P	Ground.
Not Applicable	EP		Exposed Pad. The exposed die pad must be connected to GND.

¹ I = input, I/O = input/output, O = output, P = power, and P/O = power/output.

TYPICAL PERFORMANCE CHARACTERISTICS

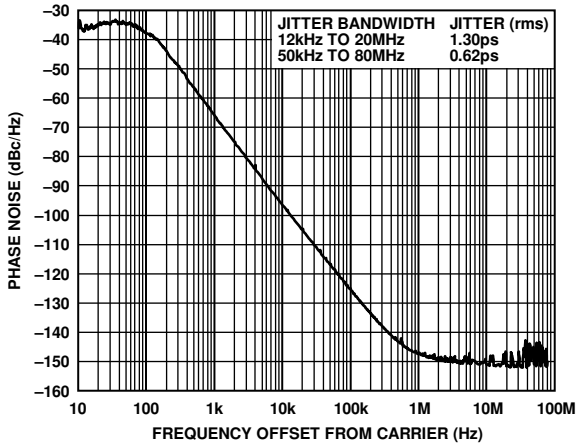


Figure 3. Phase Noise, Pin Programmed
($f_{XTAL} = 25 \text{ MHz}$, $f_{OUT1} = 156.25 \text{ MHz}$)

08955-203

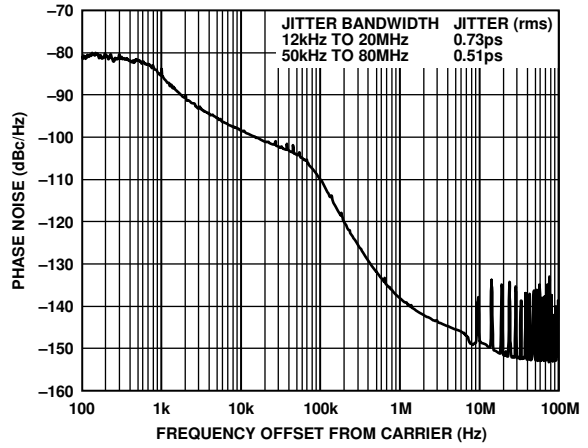


Figure 6. Phase Noise, Pin Programmed
($f_{REF} = 77.76 \text{ MHz}$, $f_{OUT1} = 622.08 \text{ MHz}$)

08955-205

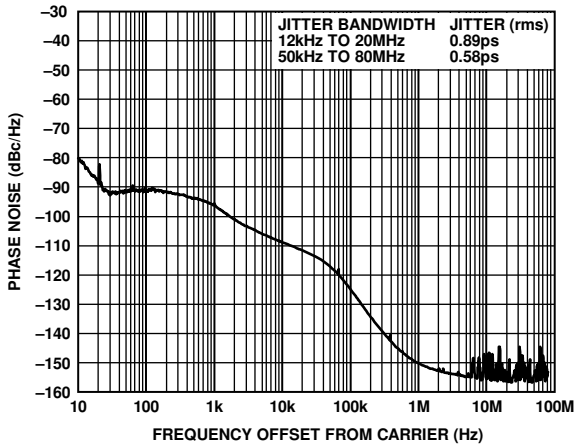


Figure 4. Phase Noise, Pin Programmed
($f_{REF} = 25 \text{ MHz}$, $f_{OUT1} = 125 \text{ MHz}$, Pin Ax = 1110)

08955-304

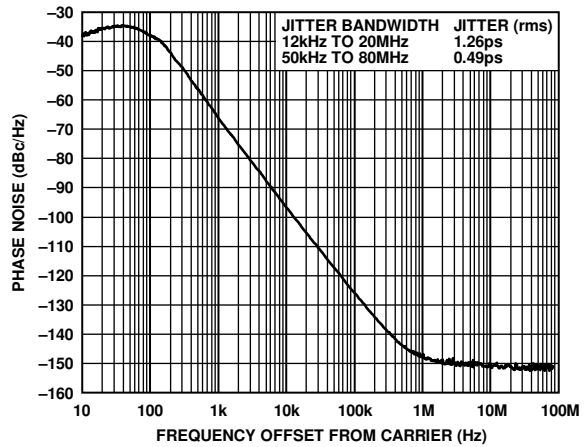


Figure 7. Phase Noise, Pin Programmed
($f_{REF} = 19.44 \text{ MHz}$, $f_{OUT1} = 155.52 \text{ MHz}$)

08955-206

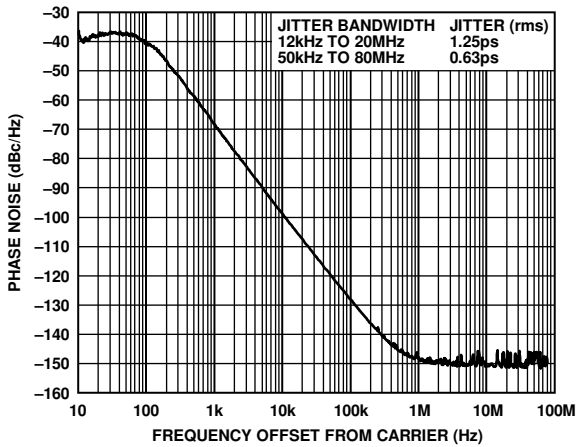


Figure 5. Phase Noise, Pin Programmed
($f_{REF} = 61.44 \text{ MHz}$, $f_{OUT1} = 122.88 \text{ MHz}$)

08955-204

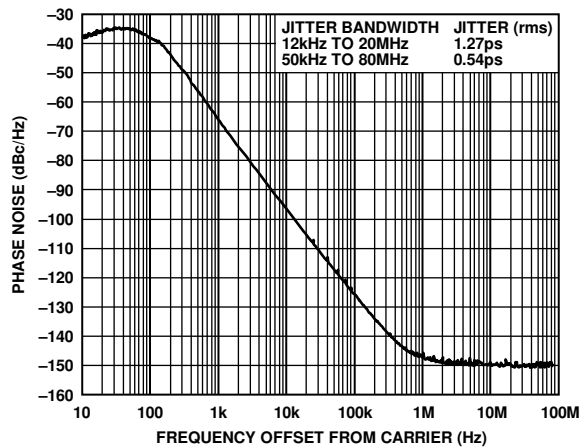


Figure 8. Phase Noise, Pin Programmed
($f_{REF} = 8 \text{ kHz}$, $f_{OUT1} = 155.52 \text{ MHz}$)

08955-207

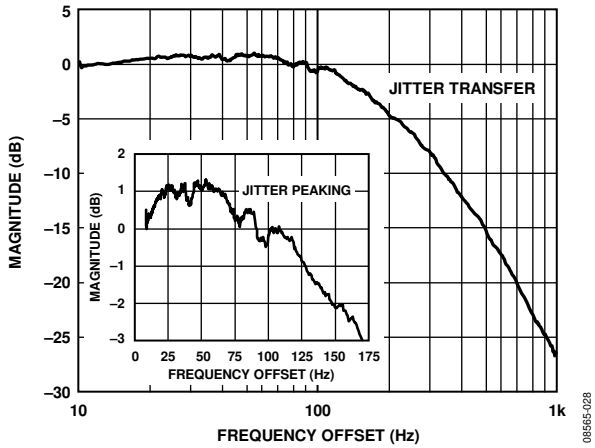


Figure 9. Jitter Transfer, Loop Bandwidth = 170 Hz

08955-028

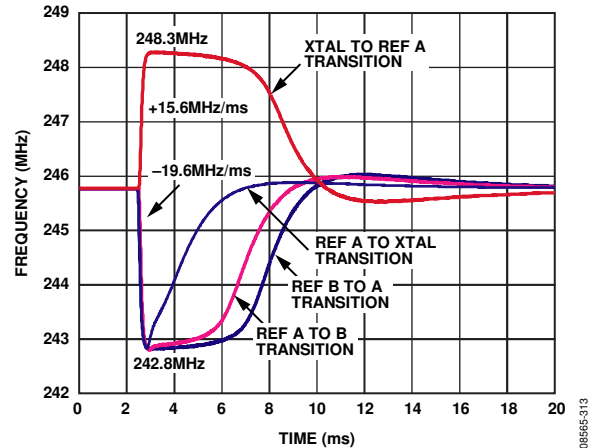


Figure 12. Output Transient Due to Input Reference Switchover, Pin Ax = 0110, Pin Yx = 000001, Loop Bandwidth = 170 Hz

08955-313

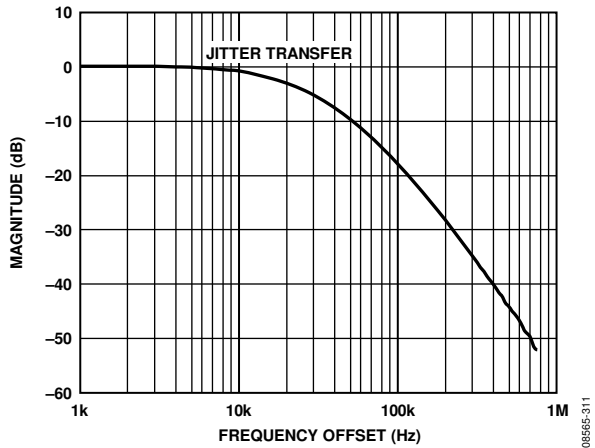


Figure 10. Jitter Transfer, Loop Bandwidth = 20 kHz

08955-311

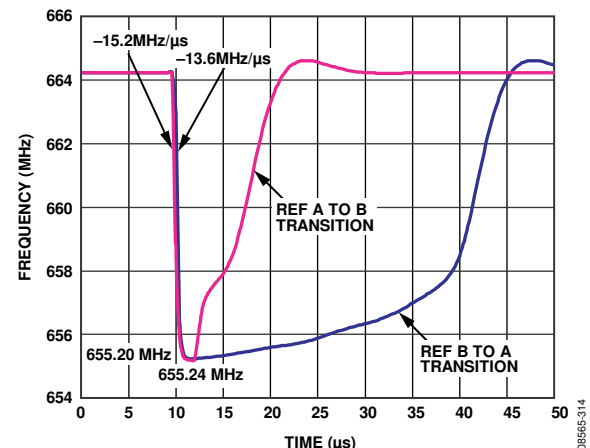


Figure 13. Output Transient Due to Input Reference Switchover, Pin Ax = 1101, Pin Yx = 101101, Loop Bandwidth = 75 kHz

08955-314

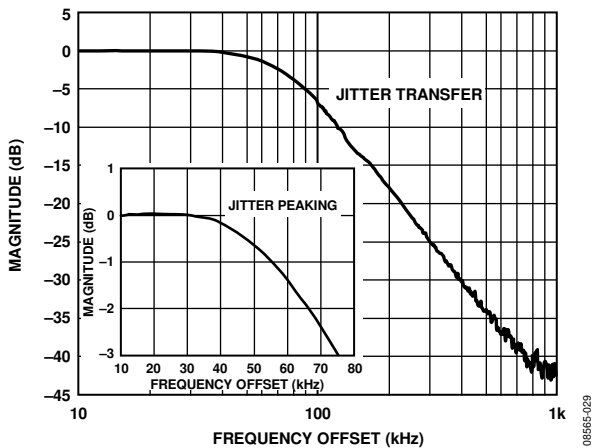


Figure 11. Jitter Transfer, Loop Bandwidth = 75 kHz

08955-029

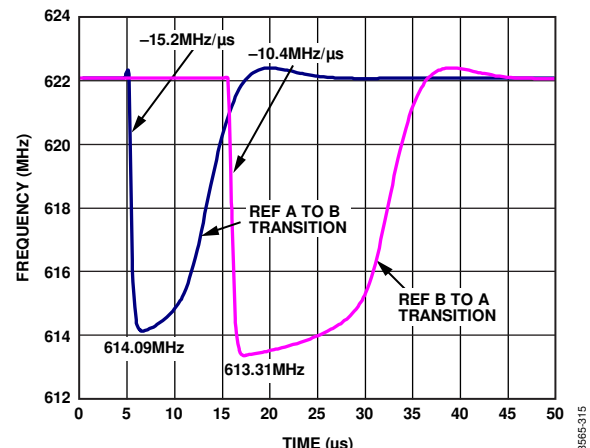


Figure 14. Output Transient Due to Input Reference Switchover, Pin Ax = 1110, Pin Yx = 110011, Loop Bandwidth = 75 kHz

08955-315

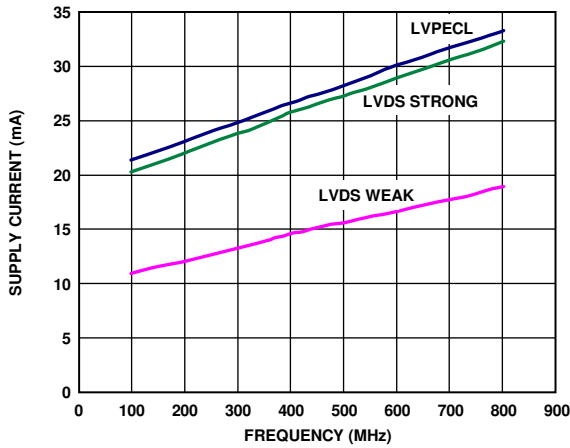


Figure 15. Supply Current vs. Output Frequency, LVPECL and LVDS (10 pF Load)

08565-209

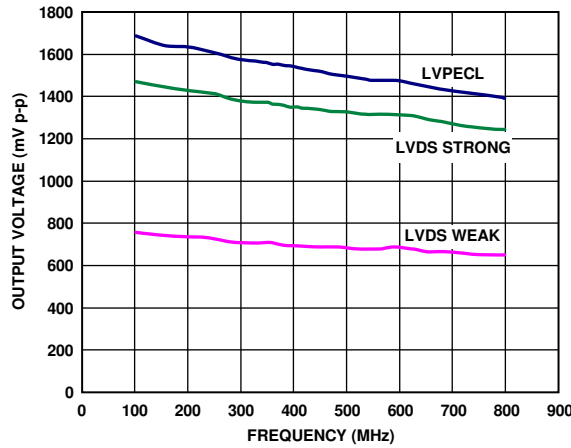


Figure 18. Peak-to-Peak Output Voltage vs. Frequency, LVPECL and LVDS (100 Ω Load)

08565-212

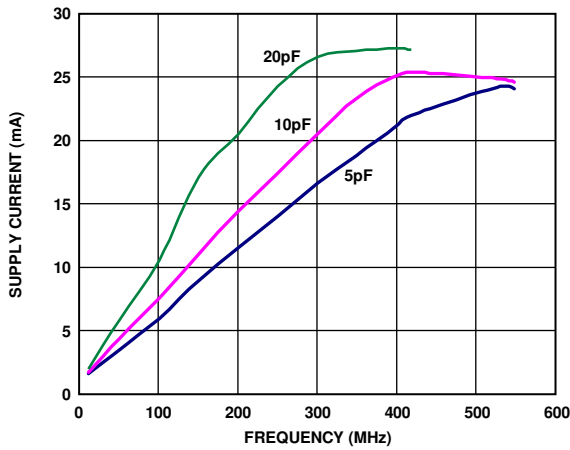


Figure 16. Supply Current vs. Output Frequency, CMOS (10 pF Load)

08565-210

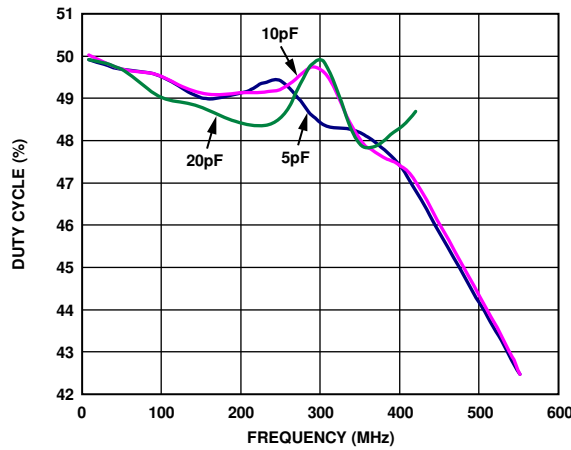


Figure 19. Duty Cycle vs. Output Frequency, CMOS

08565-213

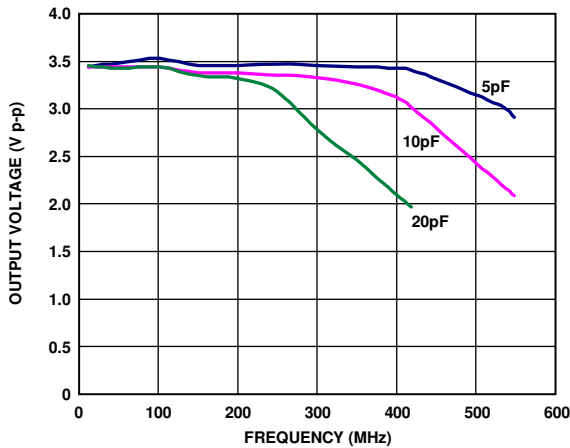


Figure 17. Peak-to-Peak Output Voltage vs. Frequency, CMOS

08565-211

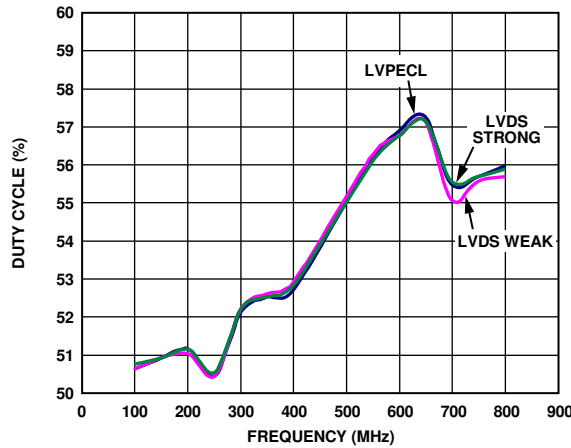


Figure 20. Duty Cycle vs. Output Frequency, LVPECL and LVDS (100 Ω Load)

08565-214

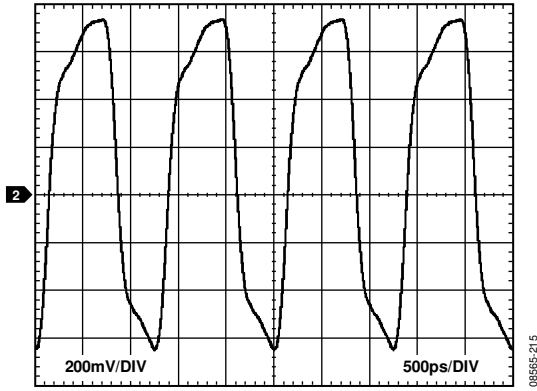


Figure 21. Typical Output Waveform, LVPECL (800 MHz)

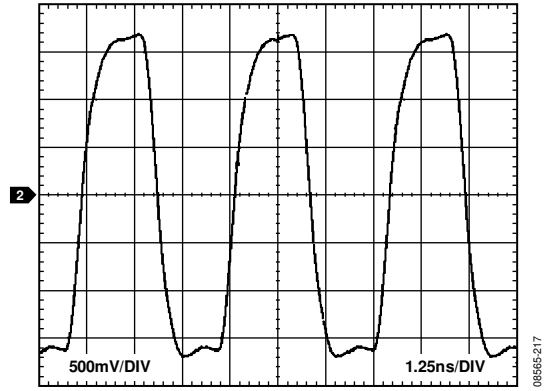


Figure 23. Typical Output Waveform, CMOS (250 MHz, 10 pF Load)

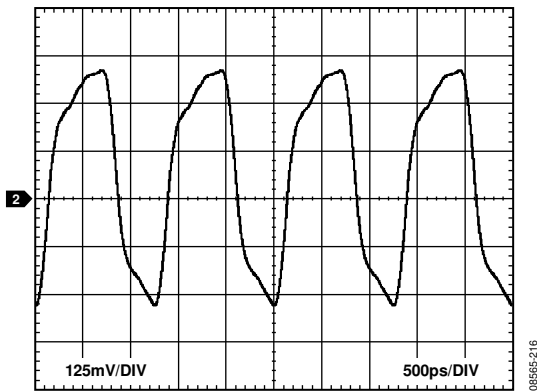


Figure 22. Typical Output Waveform, LVDS (800 MHz, 3.5 mA Drive Current)

INPUT/OUTPUT TERMINATION RECOMMENDATIONS

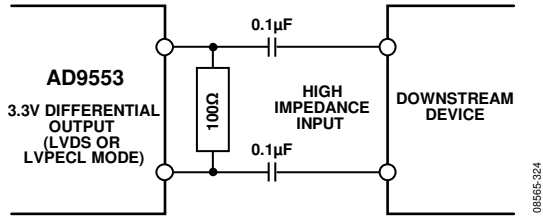


Figure 24. AC-Coupled LVDS or LVPECL Output Driver

08565-324

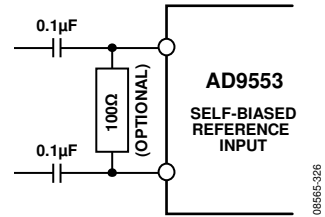


Figure 26. Reference Input

08565-326

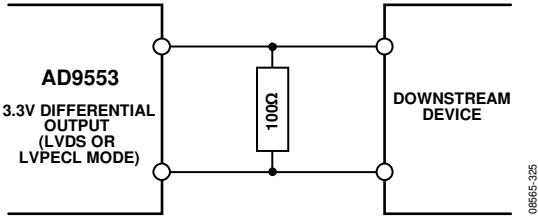


Figure 25. DC-Coupled LVDS or LVPECL Output Driver

08565-325

THEORY OF OPERATION

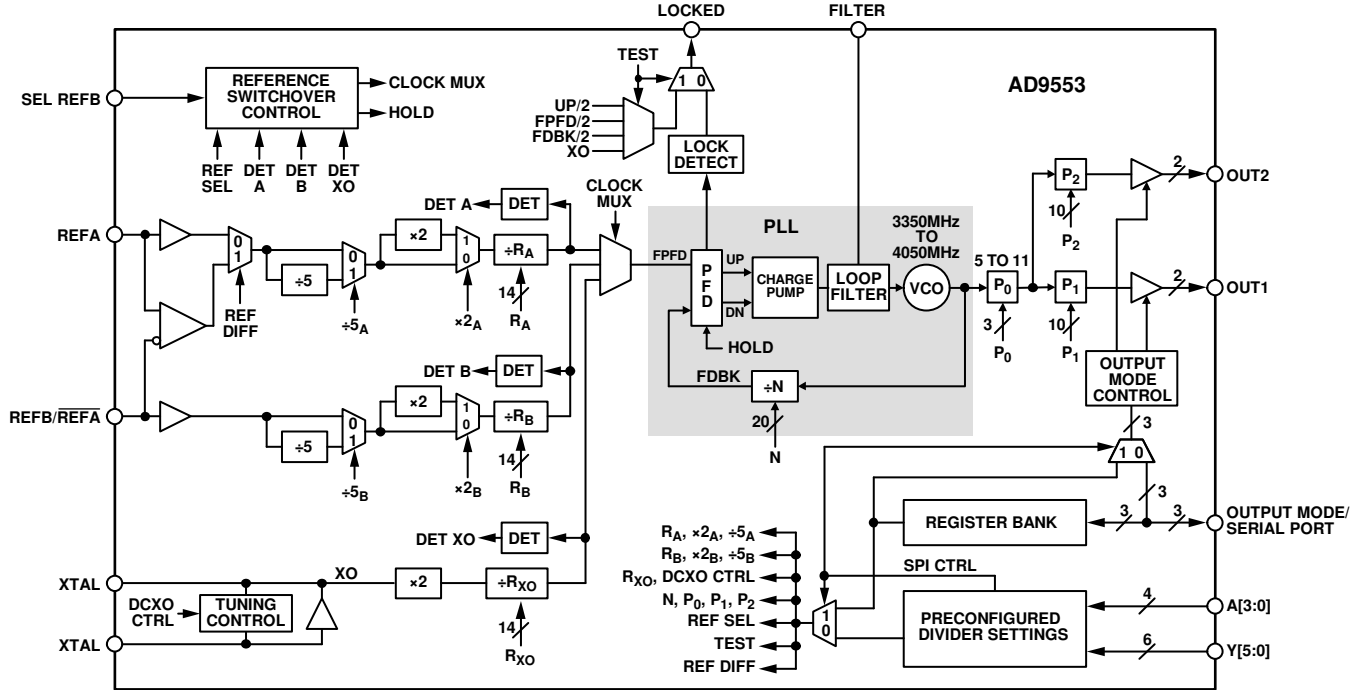


Figure 27. Detailed Block Diagram

OVERVIEW

The AD9553 can receive up to two input reference clocks, REFA and REFB. Both input clock paths include an optional divide-by-5 ($\div 5$) prescaler, an optional $\times 2$ frequency multiplier, and a 14-bit programmable divider. Alternatively, the user can program the device to operate with one differential input clock (instead of two single-ended input clocks) via the serial I/O port. In the differential operating mode, the REFB path is inactive.

The AD9553 also has a dedicated XTAL input for direct connection of an optional 25 MHz crystal resonator. This allows for a backup clock signal useful for holdover operation in case both input references fail. The XTAL clock path includes a fixed $\times 2$ frequency multiplier and a 14-bit programmable divider.

The AD9553 includes a switchover control block that automatically handles switching from REFA to REFB (or vice versa) in the event of a reference failure. If both REFA and REFB fail, however, then the switchover control block automatically enters holdover mode by selecting the XTAL clock signal (assuming the presence of a crystal resonator at the XTAL input).

Generally, the clock signals that appear at the input to the clock multiplexer (see Figure 27) all operate at the same frequency. Thus, the frequency at the input to the PLL (FFPD in Figure 27) is the same regardless of the signal selected by the clock multiplexer. The PLL converts FFPD to a frequency within the operating range of the VCO (3.35 GHz to 4.05 GHz) based on the value of the feedback divider (N). The VCO prescaler (P_0) reduces the VCO output frequency by an integer factor of 5 to 11, resulting in an intermediate frequency in the range of 305 MHz to 810 MHz.

The 10-bit P_1 and P_2 dividers can further reduce the P_0 output frequency to yield the final output clock frequencies at OUT1 and OUT2, respectively.

Thus, the frequency translation ratio from the reference input to the output depends on the selection of the $\div 5$ prescalers; the $\times 2$ frequency multipliers; the values of the three R dividers; the N divider; and the P_0 , P_1 , and P_2 dividers. These parameters are set automatically via the preconfigured divider settings per the Ax and Yx pins (see the Preset Frequencies section). Alternatively, the user can custom program these parameters via the serial I/O port (see the Serial Control Port and Register Map sections), which allows the device to accommodate custom frequency translation ratios.

PRESET FREQUENCIES

The frequency selection pins (A3 to A0 and Y5 to Y0) allow the user to hardwire the device for preset input and output frequencies based on the pin logic states (see Figure 27). The pins decode ground or open connections as Logic 0 or Logic 1, respectively.

To have access to the device control registers via the SPI port, the user must select Pin Y5 to Pin Y0 = 000000 and/or Pin A3 to Pin A0 = 0000. Doing so causes Pin 12 through Pin 14 to function as SPI port control pins instead of output mode control pins (see the Output Driver Mode Control section). Note that after selecting SPI mode, the user must write a Logic 1 to Bit 0 of Register 0x32 and Register 0x34 to enable the registers as the source of the OUT1 and OUT2 mode control bits (see Figure 31 and the Output Driver Mode Control section).

The Ax pins allow the user to select one of fifteen input reference frequencies as shown in Table 14. The device sets the appropriate divide-by-5 ($\div 5_A$, $\div 5_B$), multiply-by-2 ($\times 2_A$, $\times 2_B$), and input divider (R_A , R_B , R_{XO}) values based on the logic levels applied to the Ax pins.

The same settings apply to both the REFA and REFB input paths. Furthermore, the $\div 5$, $\times 2$, and R values cause the PLL input frequency to be either 16 kHz or 40/3 kHz. There are two exceptions. The first is for Pin A3 to Pin A0 = 1101, which yields a PLL input frequency of 155.52/59 MHz. The second is for Pin A3 to Pin A0 = 1110, which yields a PLL input frequency of either 1.5625 MHz or 4.86 MHz depending on the Yx pins.

Note that the XTAL input is not available for holdover functionality in the A3 to A0 = 1101 and 1110 pin configurations, thus the undefined R_{XO} value.

The Yx pins allow the user to select one of 52 output frequency combinations (f_{OUT1} and f_{OUT2}) per Table 15. The device sets the appropriate P_0 , P_1 , and P_2 settings based on the logic levels applied to the Yx pins. Note, however, that selections 101101 through 110010 require Pin A3 to Pin A0 = 1101, and selection 110011 requires Pin A3 to Pin A0 = 1110.

The value (N) of the PLL feedback divider and the control setting for the charge pump current (CP) depend on a combination of both the Ax and Yx pin settings as shown in Table 16.

Table 14. Pin Configured Input Frequency, Ax Pins¹

Pin A3 to Pin A0	f_{REFA} , f_{REFB} (MHz)	Divide-by-5 _A , Divide-by-5 _B	$\times 2_A$, $\times 2_B$	R_A , R_B (Decimal)	R_{XO} (Decimal)
0000	SPI mode				
0001	0.008	Bypassed	On	1	3125
0010	1.536	Bypassed	Bypassed	96	3125
0011	2.048	Bypassed	Bypassed	128	3125
0100	16.384	Bypassed	Bypassed	1024	3125
0101	19.44	Bypassed	Bypassed	1215	3125
0110 ²	25	Bypassed	On	3125	3125
0111	38.88	Bypassed	Bypassed	2430	3125
1000	61.44	Bypassed	Bypassed	3840	3125
1001	77.76	Bypassed	Bypassed	4860	3125
1010	122.88	Bypassed	Bypassed	7680	3125
1011	125	On	On	3125	3125
1100	1.544	Bypassed	On	193	3125
1101 ³	155.52	Bypassed	Bypassed	59	Undefined
1110 ⁴	25 or 77.76	Bypassed	Bypassed	16	Undefined
1111	200/3	Bypassed	Bypassed	5000	3750

¹ For divide-by-5 and $\times 2$ frequency scalars, "On" indicates active.

² Using A0 to A3 = 0110 to yield a 25 MHz to 125 MHz conversion provides a loop bandwidth of 170 Hz. An alternate 25 MHz to 125 MHz conversion uses A0 to A3 = 1110, which provides a loop bandwidth of 20 kHz.

³ Pin A3 to Pin A0 = 1101 only works with Pin Y5 to Pin Y0 = 101101 through 110010.

⁴ Pin A3 to Pin A0 = 1110 only works with Pin Y5 to Pin Y0 = 110011 or 111111.

AD9553

Table 15. Pin Configured Output Frequency, Yx Pins

Pin Y5 to Pin Y0	f _{VCO} (MHz)	f _{OUT1} (MHz)	f _{OUT2} (MHz)	P ₀	P ₁	P ₂
000000	SPI mode					
000001	3686.4	245.76	245.76	5	3	3
000010	3686.4	245.76	122.88	5	3	6
000011	3686.4	245.76	61.44	5	3	12
000100	3686.4	245.76	16.384	5	3	45
000101	3686.4	245.76	2.048	5	3	360
000110	3686.4	245.76	1.536	5	3	480
000111	3686.4	122.88	122.88	5	6	6
001000	3686.4	122.88	61.44	5	6	12
001001	3686.4	122.88	16.384	5	6	45
001010	3686.4	122.88	2.048	5	6	360
001011	3686.4	122.88	1.536	5	6	480
001100	3686.4	61.44	61.44	5	12	12
001101	3686.4	61.44	16.384	5	12	45
001110	3686.4	61.44	2.048	5	12	360
001111	3686.4	61.44	1.536	5	12	480
010000	3686.4	16.384	16.384	5	45	45
010001	3686.4	16.384	2.048	5	45	360
010010	3686.4	16.384	1.536	5	45	480
010011	3686.4	2.048	2.048	5	360	360
010100	3686.4	2.048	1.536	5	360	480
010101	3686.4	1.536	1.536	5	480	480
010110	3750	156.25	156.25	6	4	4
010111	3750	156.25	125	6	4	5
011000	3750	156.25	25	6	4	25
011001	3750	125	125	6	5	5
011010	3750	125	25	6	5	25
011011	3750	25	25	6	25	25
011100	3732.48	155.52	155.52	6	4	4
011101	3732.48	155.52	77.76	6	4	8
011110	3732.48	155.52	19.44	6	4	32
011111	3732.48	77.76	77.76	6	8	8
100000	3732.48	77.76	19.44	6	8	32
100001	3732.48	19.44	19.44	6	32	32
100010	3686.4	153.6	153.6	6	4	4
100011	3686.4	153.6	122.88	6	4	5
100100	3686.4	153.6	61.44	6	4	10
100101	3686.4	153.6	2.048	6	4	300
100110	3686.4	153.6	1.536	6	4	400
100111	3600	100	100	6	6	6
101000	3600	100	50	6	6	12
101001	3600	100	25	6	6	24
101010	3600	50	50	6	12	12
101011	3600	50	25	6	12	24
101100	3705.6	1.544	1.544	6	400	400
101101	~3985.53	f ₀ ¹	f ₀ ¹	6	1	1
101110	~3985.53	f ₀ ¹	f ₀ /2 ¹	6	1	2
101111	~3985.53	f ₀ ¹	f ₀ /4 ¹	6	1	4
110000	~3985.53	f ₀ /2 ¹	f ₀ /2 ¹	6	2	2
110001	~3985.53	f ₀ /2 ¹	f ₀ /4 ¹	6	2	4
110010	~3985.53	f ₀ /4 ¹	f ₀ /4 ¹	6	4	4
110011	3732.48	622.08	622.08	6	1	1
110100 to 111110	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
111111	3750	125	25	5	6	30

¹f₀ = 39,191.04/59 MHz.

Table 16. Pin Configuration vs. PLL Feedback Divider (N) and Charge Pump Value (CP)

A3 to A0	Y5 to Y0	N ¹	CP ²
0001 to 1100	000001 to 010101	230,400	121
	010110 to 011011	234,375	121
	011100 to 100001	233,280	121
	100010 to 100110	230,400	121
	100111 to 101011	225,000	121
	101100	231,600	121
	101101 to 111111	Undefined	Undefined
1101	000001 to 101100	Undefined	Undefined
	101101 to 110010	1512	255
	110010 to 111111	Undefined	Undefined
1110	000001 to 110010	Undefined	Undefined
	110011	768	121
	110100 to 111110	Undefined	Undefined
	111111	2400	121
1111	000001 to 010101	276,480	145
	010110 to 011011	281,250	145
	011100 to 100001	279,936	145
	100010 to 100110	276,480	145
	100111 to 101011	270,000	145
	101100	277,920	145
	101101 to 111111	Undefined	Undefined

¹ PLL feedback divider value (decimal).

² Charge pump register value (decimal). Multiply by 3.5 μ A to yield I_{CP} .

DEVICE CONTROL MODES

The AD9553 provides two modes of control: pin control and register control. Pin control, via the frequency selection pins (Ax and Yx) as described in the Preset Frequencies section, is the simplest. Typically, pin control is for applications requiring only a single set of operating parameters (assuming that one of the options available via the frequency selection pins provides the parameters that satisfy the application requirements). Register control is typically for applications that require the flexibility to program different operating parameters from time to time, or for applications that require parameters not available with any of the pin control options. The block diagram (see Figure 28) shows how the SPI and pin control modes interact.

The SPI/OM[2:0] label in Figure 28 refers to Pin 12, Pin 13, and Pin 14 of the AD9553. Furthermore, the SPI mode signal is Logic 1 when Pin A3 to Pin A0 = 0000 and/or Pin Y5 to Pin Y0 = 000000; otherwise, it is Logic 0. The SPI/OM[2:0] pins serve double duty (as either SPI pins or output mode control pins). A mux (controlled by the SPI mode signal) selects whether the three signals associated with the SPI/OM[2:0] pins connect to the output mode control decoder or to the SPI controller. Note that the SPI mode signal originates from the frequency selection pins decoder.

To enable communication with the SPI controller (SPI mode), the user must apply the appropriate logic pattern to the frequency selection pins (A3 to A0 = 0000 and/or Y5 to Y0 = 000000).

Note that as long as the frequency selection pins are set to invoke SPI mode, the user cannot establish output mode control via the output mode control decoder. Conversely, when the frequency selection pins are set to anything other than SPI mode, the user cannot communicate with the device via the SPI controller.

In Figure 28, note that some of the functions internal to the AD9553 are controlled by function bits that originate either from the two pin decoders or from within the register map. Specifically, each function receives its function bits from a function mux; and each function mux, in turn, receives its control signal from a single enable SPI control bit in the register map.

Be aware that the default values within the register map are such that all enable SPI control bits are Logic 0. Thus, the default state of the device is such that each function mux selects the pin decoders (not the register map) as the source for all control functions.

In order to switch a function mux so that it selects function bits from the register map, the user must first set the frequency selection pins to SPI mode. Then, write a Logic 1 to the appropriate enable SPI control bit in the register map. Be aware that the function mux routes the function bits in the register map to the selected function the instant that the enable SPI control bit becomes Logic 1. Thus, it is a good idea to program the function bits to the desired state prior to writing Logic 1 to the corresponding enable SPI control bit.

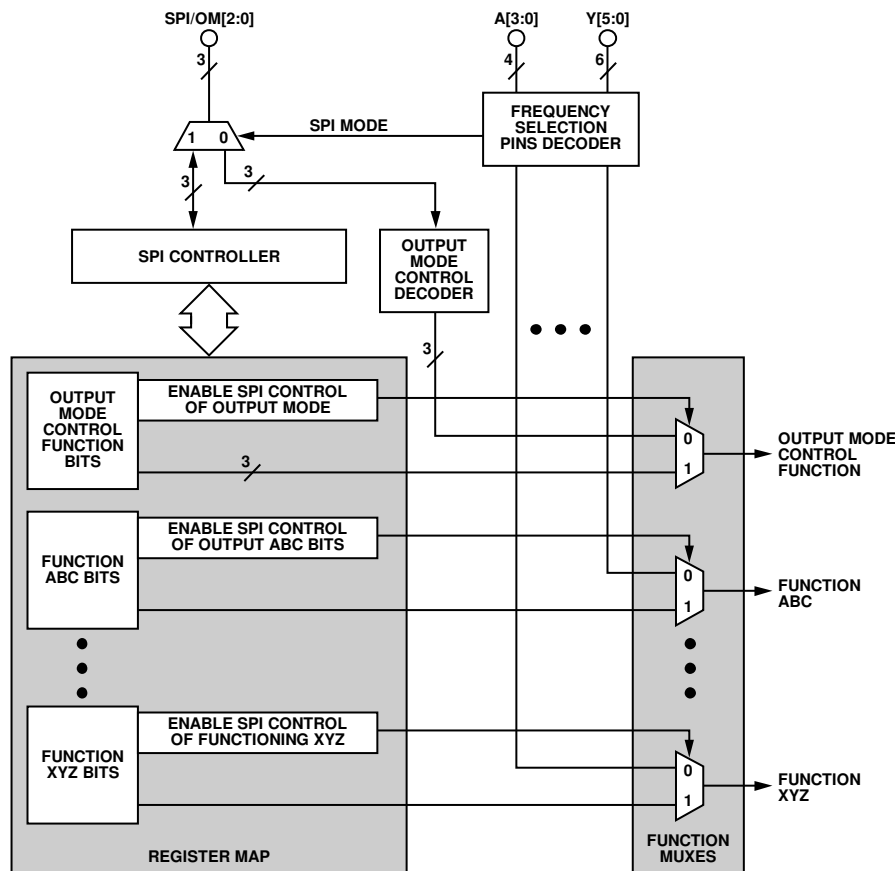


Figure 28. Control Mode Diagram

Although the SPI and pin control modes are functionally independent, it is possible to mix the control modes. For example, suppose that pin control satisfies all of the requirements for an application except for the value of the P_2 divider (which is associated with OUT2). The user could do the following:

- Activate SPI mode via the frequency selection pins.
- Program the desired P_0 , P_1 , and P_2 values in the register map (Register 0x15 to Register 0x18).
- Set the enable SPI control bit for the output dividers (Register 0x14[2] = 1).
- Calibrate the VCO by enabling SPI control of VCO calibration (Register 0x0E[2] = 1), then issue a calibrate command (Register 0x0E[7] = 1). Be sure to program the N divider, R dividers, $\div 5$ dividers, and $\times 2$ multipliers to the values defined by the A_x and Y_x pin settings prior to calibrating the VCO.
- Restore the original settings to the frequency selection pins to invoke the desired frequency selection.

In this way, the function muxes that control P_0 , P_1 , and P_2 select the appropriate register bits as the source for controlling the dividers, while all the other function muxes select the pin decoders as the source for controlling the other functions. Note that the dividers remain under register control until the user activates

SPI mode and writes Register 0x14[2] = 0, thereby causing the function mux to use the frequency selection pins decoder as the source for controlling the dividers, instead of the register map.

DESCRIPTION OF FUNCTIONAL BLOCKS

Reference Inputs

The default configuration of the AD9553 provides up to two single-ended input clock receivers, REFA and REFB, which are high impedance CMOS inputs. In applications that require redundant reference clocks with switchover capability, REFA is the primary reference and REFB the secondary reference. Alternatively, the user can configure the input (via the serial I/O port) as a single differential receiver. In this case, the REFB input functions as REFA (the complementary input of REFA). Note that in this configuration the device operates with only one reference input clock, eliminating the need for switchover functionality.

XTAL Input

The AD9553 accepts an optional 25 MHz crystal resonator connected across the XTAL pins. Alternatively, it accepts a single-ended clock source (CMOS compatible) connected to either one of the XTAL input pins (in this case, the unused input remains floating). Unless otherwise programmed, the device expects the crystal to have a specified load capacitance of 10 pF (default). The AD9553 provides the necessary load capacitance internally. The internal load capacitance consists

of a fixed component of 8 pF and a variable (programmable) component of 0 pF to 15.75 pF.

After applying power to the AD9553 (or after a device reset), the programmable component defaults to 2 pF. This establishes the default load capacitance of 10 pF (8 pF fixed plus 2 pF programmable).

To accommodate crystals with a specified load capacitance other than 10 pF (8 pF to 23.75 pF), the user can adjust the programmable capacitance in 0.25 pF increments via Register 0x1B[5:0]. Note that when the user sets Register 0x1B[7] to 0 (enabling SPI control of the XTAL tuning capacitors), the variable capacitance changes from 2 pF (its default power-up value) to 15.75 pF due to the default value of Register 0x1B[5:0]. This causes the crystal load capacitance to be 23.75 pF until the user overwrites the default contents of Register 0x1B[5:0].

A noncomprehensive, alphabetical list of crystal manufacturers includes the following:

- AVX/Kyocera
- ECS
- Epson Toyocom
- Fox Electronics
- NDK
- Siward

Although these crystals meet the load capacitance and motional resistance requirements of the AD9553 according to their data sheets, Analog Devices, Inc., does not guarantee their operation with the AD9553, nor does Analog Devices endorse one supplier of crystals over another.

Input Frequency Prescalers (Divide-by-5_A, Divide-by-5_B)

The divide-by-5 prescalers provide the option to reduce the input reference frequency by a factor of five. Note that the prescalers physically precede the $\times 2$ frequency multipliers. This allows the prescalers to bring a high frequency reference clock down to a frequency that is within the range of the $\times 2$ frequency multipliers.

Input $\times 2$ Frequency Multipliers ($\times 2_A$, $\times 2_B$)

The $\times 2$ frequency multipliers provide the option to double the frequency at their input; thereby taking advantage of a higher frequency at the input to the PLL (FPFD). This provides greater separation between the frequency generated by the PLL and the modulation spur associated with the frequency at the PLL input. However, increased reference spur separation comes at the expense of the harmonic spurs introduced by the frequency multiplier. As such, beneficial use of the frequency multiplier is application specific. Note that the maximum input frequency to the $\times 2$ frequency multipliers must not exceed 125 MHz.

Input Clock Detectors

The three clock input sections (REFA, REFB, and XTAL) include a dedicated monitor circuit that detects signal presence at the input. The detectors provide input to the switchover control block to support automatic reference switching and holdover operation.

Switchover/Holdover

The AD9553 supports automatic reference switching and holdover functions. It also supports manual reference switching via an external pin (SEL REFB) or via program control using the serial I/O port. A block diagram of the switchover/holdover capability appears in Figure 29. Note that the mux selects one of the three input signals (REFA, REFB, or XTAL) routing it to the input of the PLL. The selection of an input signal depends on which signals are present along with the contents of Register 0x29[7:6] and the logic level at the SEL REFB pin.

Note that each input signal has a dedicated signal presence detector. Each detector uses the feedback signal from the PLL as a sampling clock (which is always present due to the free-running VCO). This allows the detectors to determine the presence or absence of the input signals reliably. Note that the mux control logic uses the detector signals directly in order to determine the need for a switch to holdover operation.

Holdover occurs whenever the mux control logic determines that both the REFA and REFB signals are not present, in which case the device selects the XTAL signal if it is present. The exception is when Register 0x29[7:6] = 10 or 11, which disables the holdover function. If none of the three input signals is present, the device waits until at least one signal becomes present and selects according to the device settings (Register 0x29[7:6] and the logic level at the SEL REFB pin).

When the device is reset (or following a power-up), the internal logic defaults to revertive switchover mode (Register 0x29[7:6] = 00). In revertive switchover mode, the device selects the REFA signal whenever it is present. If REFA is not present, then the device selects the REFB signal, if present, but returns to REFA whenever it becomes available. That is, in revertive switchover mode, the device favors REFA. If both REFA and REFB are not present, the device switches to holdover mode.

When programmed for nonrevertive switchover mode (Register 0x29[7:6] = 01), the device selects the REFA signal if it is present. If REFA is not present, then the device selects the REFB signal (if present). Even if REFA becomes available, the device continues to use REFB until REFB fails. That is, in nonrevertive switchover mode, the switch to REFB is permanent unless REFB fails (or unless both REFA and REFB fail, in which case the device switches to holdover mode).

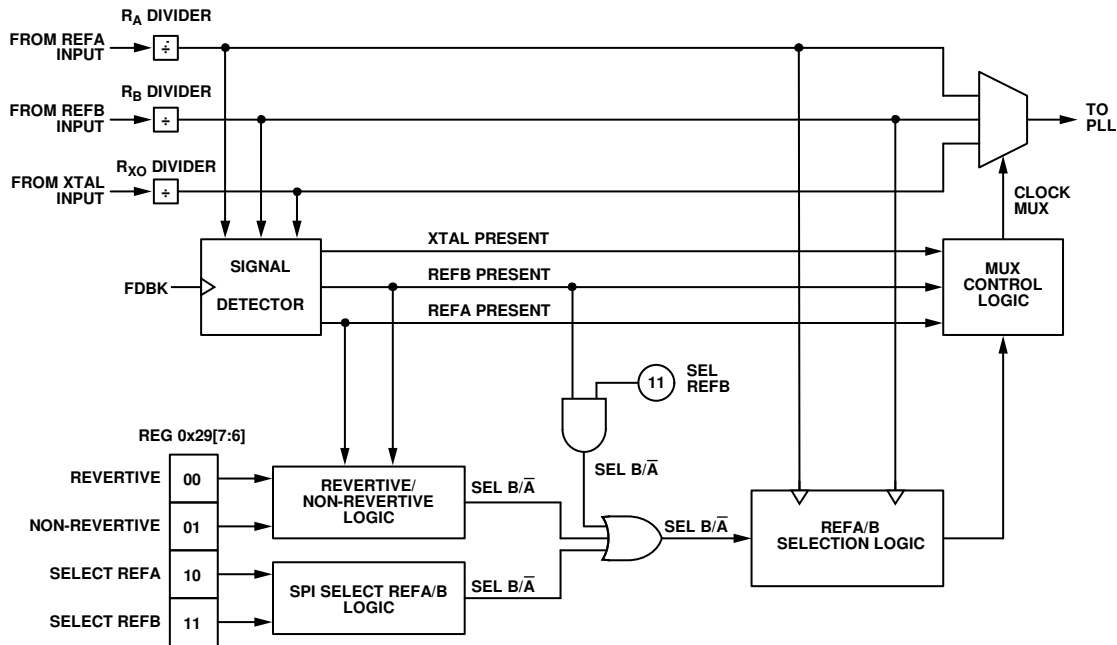


Figure 29. Switchover/Holdover Block Diagram

The user can override the automatic switchover functions (revertive and nonrevertive) and manually select the REFA or REFB signal by programming Register 0x29[7:6] = 10 or 11, respectively. Note, however, that the desired signal (REFA or REFB) must be present for the device to select it.

The user can also force the device to switch to REFB by applying a Logic 1 to the external SEL REFB pin. This overrides a REFA selection invoked by either the revertive/nonrevertive logic or when Register 0x29[7:6] = 10. Note, however, that REFB must be present to be selected by the device.

PLL (PFD, Charge Pump, VCO, Feedback Divider)

The PLL (see Figure 27) consists of a phase/frequency detector (PFD), a partially integrated analog loop filter (see Figure 30), an integrated voltage controlled oscillator (VCO), and a 20-bit programmable feedback divider. The PLL generates a 3.35 GHz to 4.05 GHz clock signal that is phase locked to the active input reference signal, and its frequency is the phase detector frequency (FPFD) multiplied by the feedback divider value (N).

The PFD of the PLL drives a charge pump that increases, decreases, or holds constant the charge stored on the loop filter capacitors (both internal and external). The stored charge results in a voltage that sets the output frequency of the VCO. The feedback loop of the PLL causes the VCO control voltage to vary in such a way as to phase lock the PFD input signals. Note that the PFD supports input frequencies spanning 13.3 kHz to 100 MHz (implying that input frequencies between 8 kHz and 13.3 kHz must use the $\times 2$ frequency multiplier in the input path).

The PLL has a VCO with 128 frequency bands spanning a range of 3350 MHz to 4050 MHz (3700 MHz nominal). However, the actual operating frequency within a particular band depends on the control voltage that appears on the loop filter capacitor. The control voltage causes the VCO output frequency to vary linearly within the selected band. This frequency variability allows the control loop of the PLL to synchronize the VCO output signal with the reference signal applied to the PFD.

Typically, selection of the VCO frequency band (as well as gain adjustment) occurs automatically as part of the automatic VCO calibration process of the device, which initiates at power up (or reset). Alternatively, the user can force VCO calibration by first enabling SPI control of VCO calibration (Register 0x0E[2] = 1) and then writing a 1 to the calibrate VCO bit (Register 0x0E[7]). Note that VCO calibration centers the dc operating point of the VCO control signal. Furthermore, during VCO calibration, the output drivers provide a static dc signal.

To facilitate system debugging, the user can override the VCO band setting by first enabling SPI control of VCO band (Register 0x0E[0] = 1) and then writing the desired value to Register 0x10[7:1].

The feedback divider (N-divider) sets the frequency multiplication factor of the PLL in integer steps over a 20-bit range. Note that the N-divider has a lower limit of 32.

Loop Filter

The charge pump in the PFD delivers current to the loop filter (see Figure 30). The components primarily responsible for the bandwidth of the loop filter are external and connect between Pin 16 and Pin 17.

The internal portion of the loop filter has two configurations: one is for low loop bandwidth applications (~170 Hz) and the other is for medium (~20 kHz)/high (~75 kHz) bandwidth applications. The low loop bandwidth condition applies when the feedback divider value (N) is 214 (16,384) or greater. Otherwise, the medium/high loop bandwidth configuration is in effect. The feedback divider value depends on the configuration of the Ax and Yx pins per Table 16.

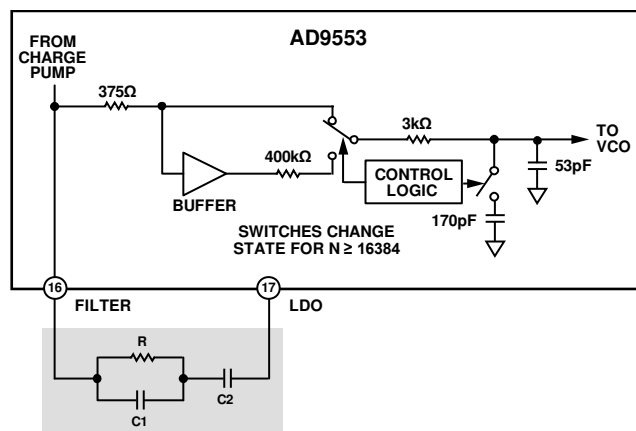


Figure 30. External Loop Filter

The bandwidth of the loop filter primarily depends on three external components (R, C1, and C2). There are two sets of recommended values for these components corresponding to the low and medium/high loop bandwidth configurations (see Table 17).

Table 17. External Loop Filter Components

A3 to A0 Pins	R	C1	C2	Loop Bandwidth
0001 to 1100, and 1111	6.8 kΩ	47 nF	1 μF	0.17 kHz
1110 ¹	12 kΩ	51 pF	220 nF	20 kHz
1101 and 1110 ²	12 kΩ	51 pF	220 nF	75 kHz

¹ The 20 kHz loop bandwidth case only applies when the A3 pin to A0 pin = 1110 and the Y5 pin to Y0 pin = 111111.

² The 75 kHz loop bandwidth case only applies when the A3 pin to A0 pin = 1101 and the Y5 pin to Y0 pin = 101101 through 110010, or when the A3 pin to A0 pin = 1110 and the Y5 pin to Y0 pin = 110011.

To achieve the best jitter performance in applications requiring a loop bandwidth of less than 1 kHz, C1 and C2 must have an insulation resistance of at least 500 ΩF.

PLL Locked Indicator

The PLL provides a status indicator that appears at Pin 20 (LOCKED). When the PLL acquires phase lock, the LOCKED pin switches to a Logic 1 state. When the PLL loses lock, however, the LOCKED pin returns to a Logic 0 state.

Alternatively, the LOCKED pin serves as a test port allowing the user to monitor one-of-four internal clocks. Register 0x17[3:1] controls the test port as shown in Table 18.

Table 18. LOCKED Pin Output Control

Register 0x17[3:1]	LOCKED Pin Output
0XX	PLL locked indication (default)
100	Crystal oscillator clock signal
101	PFD pump-up clock divided-by-2
110	PFD reference input clock divided-by-2
111	PLL feedback to PFD clock divided-by-2

Output Dividers

The output divider section consists of three dividers: P₀, P₁, and P₂. The P₀ divider (or VCO frequency prescaler) accepts the VCO frequency and reduces it by a factor of 5 to 11 (selectable). This brings the frequency down to a range between 305 MHz and 810 MHz.

The output of the P₀ divider independently drives the P₁ divider and the P₂ divider. The P₁ divider establishes the frequency at OUT1 and the P₂ divider establishes the frequency at OUT2. The P₁ and P₂ dividers are each programmable over a range of 1 to 1023, which results in a frequency at OUT1 or OUT2 that is an integer submultiple of the frequency at the output of the P₀ divider.

Output Driver Configuration

The user has complete control over all configurable parameters of the OUT1 and OUT2 drivers via the OUT1 and OUT2 driver control registers (Register 0x32 and Register 0x34, respectively, as shown in Figure 31). To alter the parameters from their default values, the user must use the SPI port to program the driver control registers as desired.

The OUT1 and OUT2 drivers are configurable in terms of the following parameters:

- Logic family (via mode control)
- Pin function (via mode control but only applies to the CMOS family)
- Polarity (only applies to the CMOS family)
- Drive current
- Power-down

Output Driver Mode Control

Three mode control bits establish the logic family and pin function of the output drivers. The three bits originate either from Bits[5:3] of Register 0x32 and Register 0x34 or from the decode logic associated with the OM2 to OM0 pins as shown in Figure 31. Note that Bit 0 of Register 0x32 and Register 0x34 determines the source of the three mode control bits for the associated output driver. Specifically, when Bit 0 of the register is Logic 0 (default), the source of the mode control bits for the associated driver is the OM2 to OM0 pin decoder. When Bit 0 is Logic 1, the source of the mode control bits is from Bits[5:3] of Register 0x32 and Register 0x34.

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The mode control bits establish the logic family and output pin function of the associated output driver per Table 19. The logic families include LVDS, LVPECL, and CMOS. Because both output drivers support the LVDS and LVPECL logic families, each driver has two pins to handle the differential signals associated with these two logic families. The OUT1 driver uses the OUT1 and OUT1 pins and the OUT2 driver uses the OUT2 and OUT2 pins. However, the CMOS logic family handles only single-ended signals, thereby requiring only one pin. Even though CMOS only requires one pin, both pins of OUT1 and both pins of OUT2 have a dedicated CMOS driver.

Note that the LVPECL mode of the AD9553 is not implemented using an emitter-follower topology, and therefore, a pull-down resistor is not needed (and should be avoided) on the output pins. Rather, it uses a CMOS output driver whose output amplitude and common-mode voltage are compatible with LVPECL specifications. 100 Ω termination across the output pair is still recommended.

The user has the option to disable (that is, tristate) either or both of the pins for OUT1 and/or OUT2 via the mode control bits (see Table 19 for the 001, 010, and 011 bit patterns). Alternatively, the user can make both pins active (see Table 19, Bit Pattern 000) to produce two single-ended CMOS output clocks at OUT1 and/or OUT2.

Table 19. Output Mode Control Bits

Mode Control Bits	Logic Family	Pin Function of the Output Driver
000	CMOS	Both pins active
001	CMOS	Positive pin active, negative pin tristate
010	CMOS	Positive pin tristate, negative pin active
011	CMOS	Both pins tristate
100	LVDS	Both pins active
101	LVPECL	Both pins active
110	Unused	Unused
111	Unused	Unused

Note that the pin decoder for the OM2 to OM0 pins generates two sets of mode control bits: one set for the OUT1 driver and another set for the OUT2 driver. The relationship between the logic levels applied to the OM2 to OM0 pins and the resulting mode control bits appears in Table 20.

Table 20. OM2 to OM0 Pin Decoder

Pin OM2 to Pin OM0	Mode Control Bits	
	OUT1	OUT2
000	101	101
001	101	100
010	100	101
011	101	001
100	100	100
101	100	001
110	001	100
111	001	001

This decoding scheme allows the OM2 to OM0 pins to establish a matrix of logic family selections for the OUT1 and OUT2 drivers as shown in Table 21. Note that when the OM2 to OM0 pins select the CMOS logic family, the signal at the OUT1 pin is a phase aligned replica of the signal at the OUT1 pin and the signal at the OUT2 pin is a phase aligned replica of the signal at the OUT2 pin.

Table 21. Logic Family Assignment via the OM2 to OM0 Pins

Pin OM2 to Pin OM0	Logic Family	
	OUT1	OUT2
000	LVPECL	LVPECL
001	LVPECL	LVDS
010	LVDS	LVPECL
011	LVPECL	CMOS
100	LVDS	LVDS
101	LVDS	CMOS
110	CMOS	LVDS
111	CMOS	CMOS