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Quad PLL, Quad Input, Multiservice Line Card Adaptive Clock Translator

Data Sheet **AD9554**

FEATURES

- Supports GR-1244 Stratum 3 stability in holdover mode
- Supports smooth reference switchover with virtually no disturbance on output phase
- Supports Telcordia GR-253 jitter generation, transfer, and tolerance for SONET/SDH up to OC-192 systems
- Supports ITU-T G.8262 synchronous Ethernet slave clocks
- Supports ITU-T G.823, ITU-T G.824, ITU-T G.825, and ITU-T G.8261
- Auto/manual holdover and reference switchover
- Adaptive clocking allows dynamic adjustment of feedback dividers for use in OTN mapping/demapping applications
- Quad digital phase-locked loop (DPLL) architecture with four reference inputs (single-ended or differential)
- 4 × 4 crosspoint allows any reference input to drive any PLL
- Input reference frequencies from 2 kHz to 1000 MHz
- Reference validation and frequency monitoring: 2 ppm
- Programmable input reference switchover priority
- 20-bit programmable input reference divider
- 8 differential clock outputs with each differential pair configurable as HCSL, LVDS-compatible, or LVPECL-compatible
- Output frequency range: 430 kHz to 941 MHz
- Programmable 18-bit integer and 24-bit fractional feedback divider in digital PLL
- Programmable loop bandwidths from 0.1 Hz to 4 kHz
- Optional off-chip EEPROM to store power-up profile
- 72-lead (10 mm × 10 mm) LFCSP package

APPLICATIONS

- Network synchronization, including synchronous Ethernet and synchronous digital hierarchy (SDH) to optical transport network (OTN) mapping/demapping
- Cleanup of reference clock jitter
- SONET/SDH clocks up to OC-192, including FEC
- Stratum 3 holdover, jitter cleanup, and phase transient control
- Cable infrastructure
- Data communications
- Professional video

GENERAL DESCRIPTION

The AD9554 is a low loop bandwidth clock translator that provides jitter cleanup and synchronization for many systems, including synchronous optical networks (SONET/SDH). The AD9554 generates an output clock synchronized to up to four external input references. The digital PLL (DPLL) allows for reduction of input time jitter or phase noise associated with the external references. The digitally controlled loop and holdover circuitry of the AD9554 continuously generates a low jitter output clock even when all reference inputs have failed.

The AD9554 operates over an industrial temperature range of −40°C to +85°C. If a smaller device is needed, the AD9554-1 is a version of this device with one output per PLL. If a single or dual DPLL version of this device is needed, refer to the AD9557 or AD9559, respectively.

FUNCTIONAL BLOCK DIAGRAM

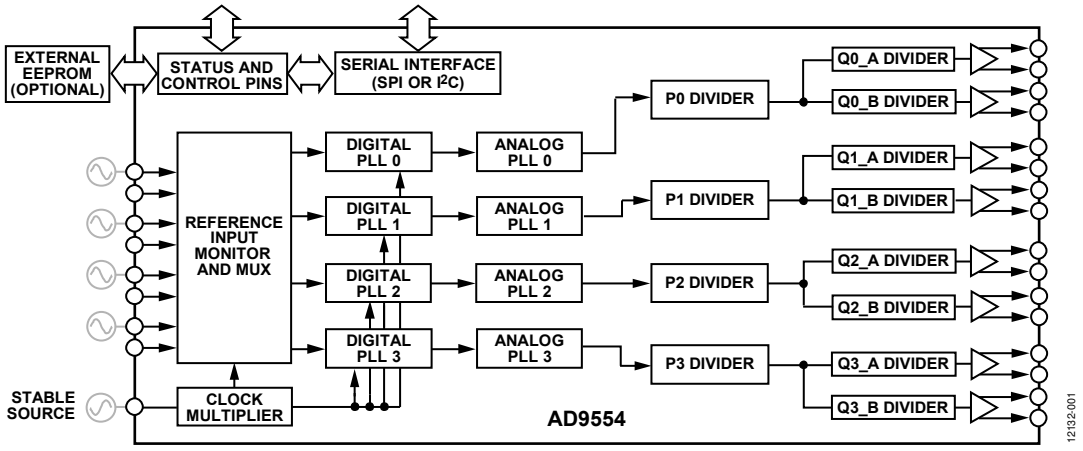

Figure 1.

Rev. D
Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

AD9554* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9554 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9554: Quad PLL, Quad Input, Multiservice Line Card Adaptive Clock Translator Data Sheet

REFERENCE MATERIALS

Press

- Analog Devices Introduces Industry's Lowest Power Quad-Channel, Jitter Attenuating, Clock Translator

DESIGN RESOURCES

- AD9554 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9554 EngineerZone Discussions.

SAMPLE AND BUY

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10/2016—Rev. B to Rev. C

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6/2016—Rev. A to Rev. B

Changes to Device Register Programming Using a Register Setup File Section 25
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8/2014—Rev. 0 to Rev. A

Changes to Applications and General Description Sections 1
Added Output Frequency of 0.430 MHz (Min) and 941 MHz (Max); Table 8 10
Added Bandwidth (f_{REF} = 19.44 MHz; f_{OUT} = 156.25 MHz; f_{LOOP} = 50 Hz) Parameters; Table 18 15
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4/2014—Revision 0: Initial Version

SPECIFICATIONS

Minimum (min) and maximum (max) values apply for the full range of supply voltage and operating temperature variations. Typical (typ) values apply for VDD = 1.8 V, T_A = 25°C, unless otherwise noted.

SUPPLY VOLTAGE

Table 1.

Parameter	Min	Typ	Max	Unit
SUPPLY VOLTAGE for 1.8 V OPERATION				
VDD_SP	1.47	1.8	2.625	V
VDD	1.71	1.8	1.89	V
SUPPLY VOLTAGE for 1.5 V OPERATION				
VDD_SP	1.47	1.5	2.625	V
VDD	1.47	1.5	1.53	V

SUPPLY CURRENT

The test conditions for the maximum (max) supply current are at the maximum supply voltage found in Table 1. The test conditions for the typical (typ) supply current are at the typical supply voltage found in Table 1. The test conditions for the minimum (min) supply current are at the minimum supply voltage found in Table 1.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT FOR TYPICAL CONFIGURATION					Typical values are for the Typical Configuration parameter listed in Table 3; valid for both 1.5 V and 1.8 V operation
I_{VDD_SP}	0.01	0.04	0.1	mA	
I_{VDD}	430	520	575	mA	
SUPPLY CURRENT FOR ALL BLOCKS RUNNING CONFIGURATION					Maximum values are for the All Blocks Running parameter listed in Table 3; valid for both 1.5 V and 1.8 V operation
I_{VDD_SP}	0.01	0.04	0.1	mA	
I_{VDD}	615	745	780	mA	

POWER DISSIPATION

Typical (typ) values apply for VDD = 1.8 V and maximum (max) values for VDD = 1.89 V.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION					
Typical Configuration		0.94	1.1	W	System clock: 49.152 MHz crystal; four DPLLs active; two 19.44 MHz input references in differential mode; four ac-coupled output drivers in 21 mA mode at 644.53125 MHz
All Blocks Running		1.3	1.47	W	System clock: 49.152 MHz crystal; four DPLLs active, four 19.44 MHz input references in differential mode; eight ac-coupled output drivers in 28 mA mode at 750 MHz
Full Power-Down		174		mW	Measured using the Typical Configuration parameter (see Table 3) and then setting the full power down bit
Incremental Power Dissipation					Typical configuration; table values show the change in power due to the indicated operation
Complete DPLL/APLL On/Off		190		mW	Power delta computed relative to the typical configuration; the blocks powered down include one reference input, one DPLL, one APLL, one P divider, two channel dividers, and one output driver in 21 mA mode
Input Reference On/Off					
Differential (Normal Mode)		22.5		mW	f_{REF} = 19.44 MHz
Differential (DC-Coupled LVDS)		24.6		mW	f_{REF} = 19.44 MHz
Single-Ended		14.3		mW	f_{REF} = 19.44 MHz
Output Distribution Driver On/Off					
28 mA Mode (at 644.53 MHz)		70		mW	
21 mA Mode (at 644.53 MHz)		48		mW	
14 mA mode (at 644.53 MHz)		23.6		mW	

SYSTEM CLOCK INPUTS (XOA, XOB)

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SYSTEM CLOCK MULTIPLIER					
PLL Output Frequency Range	2250		2415	MHz	Voltage controlled oscillator (VCO) range can place limitations on nonstandard system clock input frequencies
Phase Frequency Detector (PFD) Rate	10		300	MHz	
Frequency Multiplication Range	8		241		Assumes valid system clock and PFD rates
SYSTEM CLOCK REFERENCE INPUT PATH					System clock input must be ac-coupled
Input Frequency Range					
System Clock Input Doubler Disabled	10		268	MHz	
System Clock Input Doubler Enabled	16		150	MHz	
Minimum Input Slew Rate	250			V/µs	Minimum limit imposed for jitter performance
Self-Biased Common-Mode Voltage		0.72		V	Internally generated
Input High Voltage	0.9			V	For ac-coupled single-ended operation
Input Low Voltage			0.5	V	For ac-coupled single-ended operation
Differential Input Voltage Sensitivity	250			mV p-p	Minimum voltage across pins required to ensure switching between logic states; the instantaneous voltage on either pin must not exceed 1.14 V; single-ended input can be accommodated by ac grounding complementary input; 800 mV p-p recommended for optimal jitter performance
System Clock Input Doubler Duty Cycle					Amount of duty-cycle variation that can be tolerated on the system clock input to use the doubler
System Clock Input = 20 MHz to 150 MHz	43	50	57	%	
System Clock Input = 16 MHz to 20 MHz	47	50	53	%	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Input Capacitance		3		pF	Single-ended to ground, each pin
Input Resistance		5		kΩ	
CRYSTAL RESONATOR PATH					
Crystal Resonator Frequency Range	12		50	MHz	Fundamental mode, AT cut crystal
Input Capacitance		3		pF	Single-ended to ground, each pin
Maximum Crystal Motional Resistance			100	Ω	

REFERENCE INPUTS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL MODE					AC couple inputs in differential mode
Frequency Range					
Sinusoidal Input	10		475	MHz	
LVPECL Input	0.002		1000	MHz	
LVDS Input	0.002		700	MHz	Assumes an LVDS minimum of 494 mV p-p differential amplitude
Minimum Input Slew Rate					Minimum limit imposed for jitter performance
DPLL Loop Bandwidth = 50 Hz	40			V/µs	
DPLL Loop Bandwidth = 4 kHz	50			V/µs	Maximum loop bandwidth is $f_{PFD}/50$
Common-Mode Input Voltage		0.64		V	Internally generated self-bias voltage
Differential Input Voltage Sensitivity					Peak-to-peak differential voltage swing across pins required to ensure switching between logic levels as measured with a differential probe; instantaneous voltage on either pin must not exceed 1.3 V
f_{IN} < 400 MHz	400		2100	mV p-p	
f_{IN} = 400 MHz to 750 MHz	500		2100	mV p-p	
f_{IN} = 750 MHz to 1000 MHz	1000		2100	mV p-p	
Differential Input Voltage Hysteresis		55	100	mV	
Input Resistance		16		kΩ	Equivalent differential input resistance
Input Capacitance		9		pF	Single-ended to ground, each pin
Minimum Pulse Width High					
LVPECL	460			ps	
LVDS	560			ps	
Minimum Pulse Width Low					
LVPECL	460			ps	
LVDS	560			ps	
DC-COUPLED LVDS MODE					Intended for dc-coupled LVDS ≤10.24 MHz
Frequency Range	0.002		10.24	MHz	
Minimum Input Slew Rate					Minimum limit imposed for jitter performance
DPLL Loop Bandwidth = 50 Hz	40			V/µs	
DPLL Loop Bandwidth = 4 kHz	150			V/µs	Maximum loop bandwidth is $f_{PFD}/50$
Common-Mode Input Voltage	1.125		1.375	V	
Differential Input Voltage Sensitivity	400		1200	mV	Differential voltage across pins required to ensure switching between logic levels; instantaneous voltage on either pin must not exceed the supply rails
Differential Input Voltage Hysteresis		55	100	mV	
Input Resistance		21		kΩ	
Input Capacitance		7		pF	
Minimum Pulse Width High	25			ns	
Minimum Pulse Width Low	25			ns	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SINGLE-ENDED MODE					DC-coupled
Frequency Range (CMOS)	0.002		300	MHz	
Minimum Input Slew Rate					Minimum limit imposed for jitter performance
DPLL Loop Bandwidth = 50 Hz	40			V/µs	
DPLL Loop Bandwidth = 4 kHz	175			V/µs	Maximum loop bandwidth is $f_{PFD}/50$
Input Voltage High, V_{IH}	V_{DD} − 0.5			V	
Input Voltage Low, V_{IL}			0.5	V	
Input Resistance		30		kΩ	
Input Capacitance		5		pF	
Minimum Pulse Width High	1.5			ns	
Minimum Pulse Width Low	1.5			ns	

REFERENCE MONITORS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE MONITORS					
Reference Monitor					
Loss of Reference Detection Time			1.15	DPLL PFD period	Nominal phase detector period = R/f_{REF}, where R is the frequency division factor determined by the R divider, and f_{REF} is the frequency of the active reference
Frequency Out-of Range Limits	2		10^5	$\Delta f/f_{REF}$ (ppm)	Programmable (lower bound subject to quality of the system clock [SYSCLK]); SYSCLK accuracy must be less than the lower bound
Validation Timer	0.001		65.535	sec	Programmable in 1 ms increments

REFERENCE SWITCHOVER SPECIFICATIONS

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MAXIMUM OUTPUT PHASE PERTURBATION (PHASE BUILD-OUT SWITCHOVER)					Assumes a jitter-free reference; satisfies Telcordia GR-1244-CORE requirements; base loop filter selection bit set to 1b or all active references
50 Hz DPLL Loop Bandwidth					High phase margin mode; 19.44 MHz to 174.70308 MHz; DPLL bandwidth = 50 Hz; 49.152 MHz signal generator used for system clock source
Peak		±20	±130	ps	
Steady State		±20	±130	ps	
Time Required to Switch to a New Reference					
Phase Build-Out Switchover			10	DPLL PFD period	Calculated using the nominal phase detector period (NPDP = R/f_{REF}); the total time required is the time plus the reference validation time, plus the time required to lock to the new reference

DISTRIBUTION CLOCK OUTPUTS

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
14 mA (HCSL-, LVDS-COMPATIBLE) MODE					Unless otherwise stated, specifications dc-coupled with no output termination resistor; when ac-coupled, LVDS-compatible amplitudes are achieved with a 100 Ω resistor across the output pair; HCSL-compatible amplitudes achieved with no termination resistor across the output pair; output current setting: 14 mA
Output Frequency	0.430		941	MHz	Frequency range all four PLLs can generate using unique VCO frequencies; frequencies outside this range are possible on some of the PLLs, but can result in increased VCO coupling due to multiple PLLs using the same VCO frequency
Continuous Output Frequency Range	0.430		781	MHz	All four PLLs can generate this range at the same time while using unique VCO frequencies
Maximum Output Frequency					
PLL0 to PLL3 Using Unique VCO Frequencies		941		MHz	Maximum frequency all four PLLs can generate using unique VCO frequencies
PLL0, PLL1, and PLL2		1250		MHz	Limited by 1250 MHz maximum input frequency to channel divider (Q divider)
PLL3		1187		MHz	Limited by 4748 MHz maximum VCO frequency
Rise/Fall Time (20% to 80%)[1]		125	190	ps	
Duty Cycle					
Up to f_{OUT} = 750 MHz	45	50	55	%	
Up to f_{OUT} = 941 MHz	44	50	56	%	
Up to f_{OUT} = 1250 MHz		50		%	
Differential Output Voltage Swing					Differential voltage swing between output pins; measured with output driver static; peak-to-peak differential output amplitude 2× this level with driver toggling; see Figure 11 for output amplitude vs. output frequency
Without 100 Ω Termination Resistor	635	840	1000	mV	
With 100 Ω Termination Resistor Across Outputs	294	390	463	mV	
Common-Mode Output Voltage	310	420	525	mV	Output driver static; no termination resistor
Reference Input-to-Output Delay Variation over Temperature		600		fs/°C	DPLL locked to same input reference at all times; stable system clock source (noncrystal)
Static Phase Offset Variation from Active Reference to Output over Voltage Extremes		±75		fs/mV	
21 mA MODE					Unless otherwise stated, specifications dc-coupled with 50 Ω output termination resistor to ground; output current setting = 21 mA
Output Frequency	0.430		941	MHz	Frequency range all four PLLs can generate using unique VCO frequencies; frequencies outside this range are possible on some of the PLLs, but can result in increased VCO coupling due to multiple PLLs using the same VCO frequency
Continuous Output Frequency Range	0.430		781	MHz	All four PLLs can generate this range at the same time while using unique VCO frequencies
Maximum Output Frequency					
PLL0 to PLL3 Using Unique VCO Frequencies		941		MHz	Maximum frequency all four PLLs can generate using unique VCO frequencies
PLL0, PLL1, and PLL2		1250		MHz	Limited by 1250 MHz maximum input frequency to channel divider (Q divider)
PLL3		1187		MHz	Limited by 4748 MHz maximum VCO frequency
Rise/Fall Time (20% to 80%)[1]		125	190	ps	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Duty Cycle					
Up to f_{OUT} = 750 MHz	45	50	55	%	
Up to f_{OUT} = 941 MHz	44	50	56	%	
Up to f_{OUT} = 1250 MHz		50		%	
Differential Output Voltage Swing					Differential voltage swing between output pins; measured with output driver static; peak-to-peak differential output amplitude 2× this level with driver toggling; see Figure 13 for output amplitude vs. output frequency
No External Termination Resistor	779	1180	1510	mV	
With 50 Ω Termination Resistor to Ground on Each Leg	413	625	800	mV	
Common-Mode Output Voltage	206	312	400	mV	Output driver static with 50 Ω resistor to ground on each leg
Reference Input-to-Output Delay Variation over Temperature		600		fs/°C	DPLL locked to same input reference at all times; stable system clock source (noncrystal)
Static Phase Offset Variation from Active Reference to Output over Voltage Extremes		±75		fs/mV	
28 mA (LVPECL-COMPATIBLE) MODE					Specifications for dc-coupled, 50 Ω termination resistor from each leg to ground; ac coupling used in most applications; output current setting = 28 mA; in this mode, user must have either a 50 Ω resistor from each leg to ground, or a 100 Ω resistor across the differential pair
Output Frequency	0.430		941	MHz	Frequency range all four PLLs can be generated using unique VCO frequencies; frequencies outside this range are possible on some of the PLLs, but can result in increased VCO coupling due to multiple PLLs using the same VCO frequency
Continuous Output Frequency Range	0.430		781	MHz	Frequency range for each PLL such that all four PLLs are using unique VCO frequencies with no frequency gaps
Maximum Output Frequency					
PLL0 to PLL3 Using Unique VCO Frequencies		941		MHz	Maximum frequency all four PLLs can generate using unique VCO frequencies
PLL0, PLL1, and PLL2		1250		MHz	Limited by 1250 MHz maximum input frequency to channel divider (Q divider)
PLL3		1187		MHz	Limited by 4748 MHz maximum VCO frequency
Rise/Fall Time (20% to 80%)[1]		185	280	ps	
Duty Cycle					
Up to f_{OUT} = 750 MHz	45	50	55	%	
Up to f_{OUT} = 941 MHz	44	50	56	%	
Up to f_{OUT} = 1250 MHz		50		%	
Differential Output Voltage Swing	540	830	1020	mV	Differential voltage swing between output pins; measured with output driver static; peak-to-peak differential output amplitude 2× this level with driver toggling; see Figure 10 for output amplitude vs. output frequency
Common-Mode Output Voltage	275	415	510	mV	Output driver static; 50 Ω external termination resistor from each leg to ground
Reference Input-to-Output Delay Variation over Temperature		600		fs/°C	DPLL locked to same input reference at all times; stable system clock source (noncrystal)
Static Phase Offset Variation from Active Reference to Output over Voltage Extremes		±75		fs/mV	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT TIMING SKEW					Independent of output driver mode; rising edge only; any divide value; negative value means OUTxB is ahead of OUTxA
Between OUT0A, $\overline{\text{OUT0A}}$ and OUT0B, $\overline{\text{OUT0B}}$	−60	−6	+48	ps	
Between OUT1A, $\overline{\text{OUT1A}}$ and OUT1B, $\overline{\text{OUT1B}}$	−60	−6	+48	ps	
Between OUT2A, $\overline{\text{OUT2A}}$ and OUT2B, $\overline{\text{OUT2B}}$	−60	−6	+48	ps	
Between OUT3A, $\overline{\text{OUT3A}}$ and OUT3B, $\overline{\text{OUT3B}}$	−60	−6	+48	ps	

[1] The listed values are for the slower edge (rising or falling).

TIME DURATION OF DIGITAL FUNCTIONS

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TIME DURATION OF DIGITAL FUNCTIONS					
EEPROM to Register Download Time		30		ms	Uses default EEPROM storage sequence (see Register 0x0E10 to Register 0x0E6F) assuming full 400 kHz throughput from EEPROM
Register to EEPROM Upload Time		Varies		ms	Value dependent on write throughput of the external EEPROM
Power-Down Exit Time		51		ms	Time from power-down exit to system clock stable (including the system clock stability timer default of 50 ms); does not include time to validate input references or lock the DPLL
Mx Pin to $\overline{\text{RESET}}$ Rising Edge Setup Time			1	ns	Mx refers to Pin M0 though Pin M9
Mx Pin to $\overline{\text{RESET}}$ Rising Edge Hold Time			1	ns	
$\overline{\text{RESET}}$ Falling Edge to Mx Pin High-Z Time			10	ns	

DIGITAL PLL (DPLL_0, DPLL_1, DPLL_2, AND DPLL_3)

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL PLL					
Phase Frequency Detector (PFD) Input Frequency Range	2		200	kHz	
Loop Bandwidth	0.1		4000	Hz	Programmable design parameter; note that (f_{PFD}/loop bandwidth) ≥ 50
Phase Margin	45		89	Degrees	Programmable design parameter
Closed Loop Peaking	<0.1			dB	Programmable design parameter; device can be programmed for <0.1 dB peaking in accordance with Telcordia GR-253-CORE jitter transfer

ANALOG PLL (APLL_0, APLL_1, APLL_2, AND APLL_3)

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG PLL0 (APLL_0)					
VCO Frequency Range	2424		3132	MHz	
Phase Frequency Detector (PFD) Input Frequency Range		320	350	MHz	The AD9554 evaluation software finds the optimal value for this setting based on user input.
Loop Bandwidth		240		kHz	
Phase Margin		68		Degrees	
ANALOG PLL1 (APLL_1)					
VCO Frequency Range	3232		3905	MHz	
Phase Frequency Detector (PFD) Input Frequency Range		320	350	MHz	The AD9554 evaluation software finds the optimal value for this setting based on user input.
Loop Bandwidth		240		kHz	
Phase Margin		68		Degrees	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG PLL2 (APLL_2)					
VCO Frequency Range	4842		5650	MHz	
Phase Frequency Detector (PFD) Input Frequency Range		320	350	MHz	The AD9554 evaluation software finds the optimal value for this setting based on user input.
Loop Bandwidth		240		kHz	
Phase Margin		68		Degrees	
ANALOG PLL3 (APLL_3)					
VCO Frequency Range	4040		4748	MHz	
Phase Frequency Detector (PFD) Input Frequency Range		320	350	MHz	The AD9554 evaluation software finds the optimal value for this setting based on user input.
Loop Bandwidth		240		kHz	
Phase Margin		68		Degrees	

DIGITAL PLL LOCK DETECTION

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PHASE LOCK DETECTOR					
Threshold Programming Range	10		$2^{24} - 1$	ps	Reference-to-feedback phase difference
Threshold Resolution		1		ps	
FREQUENCY LOCK DETECTOR					
Threshold Programming Range	10		$2^{24} - 1$	ps	Reference-to-feedback period difference
Threshold Resolution		1		ps	

HOLDOVER SPECIFICATIONS

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HOLDOVER SPECIFICATIONS					
Initial Frequency Accuracy		<0.01		ppm	Excludes frequency drift of SYSCLK source; excludes frequency drift of input reference prior to entering holdover; compliant with GR-1244 Stratum 3

SERIAL PORT SPECIFICATIONS—SERIAL PORT INTERFACE (SPI) MODE

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{CS}$					Valid for VDD_SP = 1.5 V, VDD_SP = 1.8 V, and VDD_SP = 2.5 V
Input Logic 1 Voltage	VDD_SP – 0.4			V	
Input Logic 0 Voltage			0.4	V	
Input Logic 1 Current		1		µA	
Input Logic 0 Current		1		µA	
Input Capacitance		3		pF	
SCLK					No internal pull-up or pull-down resistor
Input Logic 1 Voltage	VDD_SP – 0.4			V	
Input Logic 0 Voltage			0.4	V	
Input Logic 1 Current		1		µA	
Input Logic 0 Current		1		µA	
Input Capacitance		2		pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDIO					
As an Input					
Input Logic 1 Voltage	VDD_SP – 0.4			V	
Input Logic 0 Voltage			0.4	V	
Input Logic 1 Current		1		µA	
Input Logic 0 Current		1		µA	
Input Capacitance		2		pF	
As an Output					
Output Logic 1 Voltage	VDD_SP – 0.2			V	1 mA load current
Output Logic 0 Voltage			0.1	V	1 mA load current
SDO					
Output Logic 1 Voltage	VDD_SP – 0.2			V	1 mA load current
Output Logic 0 Voltage			0.1	V	1 mA load current
High-Z Leakage Current		±6	±100	µA	
TIMING					Valid for VDD_SP = 1.5 V, VDD_SP = 1.8 V, and VDD_SP = 2.5 V
SCLK					
Clock Rate, $1/t_{CLK}$			50	MHz	
Pulse Width High, t_{HIGH}	5			ns	
Pulse Width Low, t_{LOW}	8			ns	
SDIO to SCLK Setup, t_{DS}	1.5			ns	
SCLK to SDIO Hold, t_{DH}	0			ns	
SCLK to Valid SDIO and SDO, t_{DV}			8	ns	
$\overline{CS}$ to SCLK Setup, t_S	0			ns	
$\overline{CS}$ to SCLK Hold, t_C	0			ns	
$\overline{CS}$ Minimum Pulse Width High	1.5			ns	

SERIAL PORT SPECIFICATIONS—I²C MODE

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDA, SCL (AS INPUTS)					Valid for VDD_SP = 1.5 V, VDD_SP = 1.8 V, and VDD_SP = 2.5 V
Input Logic 1 Voltage	0.7 × VDD_SP			V	
Input Logic 0 Voltage			0.3 × VDD_SP	V	
Input Current	−10		+10	µA	For V_{IN} = 10% to 90% of VDD
Hysteresis of Schmitt Trigger Inputs	0.015 × VDD				
SDA (AS OUTPUT)					
Output Logic 0 Voltage			0.2	V	I_{OUT} = 3 mA
Output Fall Time from V_{IH} Minimum to V_{IL} Maximum	$20 + 0.1 \times C_b$		250	ns	10 pF ≤ C_b ≤ 400 pF
TIMING					
SCL Clock Rate			400	kHz	
Bus-Free Time Between a Stop and Start Condition, t_{BUF}	1.3			µs	
Repeated Start Condition Setup Time, $t_{SU;STA}$	0.6			µs	
Repeated Hold Time Start Condition, $t_{HD;STA}$	0.6			µs	After this period, the first clock pulse is generated
Stop Condition Setup Time, $t_{SU;STO}$	0.6			µs	
Low Period of the SCL Clock, t_{LOW}	1.3			µs	
High Period of the SCL Clock, t_{HIGH}	0.6			µs	
SCL/SDA Rise Time, t_R	$20 + 0.1 \times C_b$		300	ns	
SCL/SDA Fall Time, t_F	$20 + 0.1 \times C_b$		300	ns	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Data Setup Time, $t_{SU;DAT}$	100			ns	
Data Hold Time, $t_{HD;DAT}$	100			ns	
Capacitive Load for Each Bus Line, C_b			400	pF	

LOGIC INPUTS ($\overline{\text{RESET}}$, M9 TO M0)

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{\text{RESET}}$ PIN					Valid for VDD_SP = 1.5 V, VDD_SP = 1.8 V, and VDD_SP = 2.5 V
Input High Voltage (V_{IH})	VDD_SP −0.5			V	
Input Low Voltage (V_{IL})			0.5	V	
Input Current (I_{INH}, I_{INL})		±85	±125	µA	
Input Capacitance (C_{IN})		3		pF	
LOGIC INPUTS (M9 to M0)					Valid for VDD = 1.5 V, and VDD = 1.8 V
Input High Voltage (V_{IH})	VDD − 0.5			V	
Input Low Voltage (V_{IL})			0.6	V	
Input Current (I_{INH}, I_{INL})		±15	±25	µA	
Input Capacitance (C_{IN})		5		pF	

LOGIC OUTPUTS (M9 TO M0)

Table 17.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS (M9 to M0)					VDD = 1.5 V and VDD = 1.8 V
Output High Voltage (V_{OH})	VDD − 0.2			V	I_{OH} = 1 mA using high drive strength (see Register 0x011E)
Output Low Voltage (V_{OL})			0.2	V	I_{OL} = 1 mA

JITTER GENERATION

Jitter Generation (Random Jitter)—49.152 MHz Crystal for System Clock Input

Table 18.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
JITTER GENERATION					System clock doubler enabled; high phase margin mode enabled; all PLLs are running with same output frequency; in cases where the four PLLs have different jitter, the higher jitter is listed; there is not a significant jitter difference between driver modes
f_{REF} = 19.44 MHz; f_{OUT} = 622.08 MHz; f_{LOOP} = 50 Hz					
Bandwidth					
5 kHz to 20 MHz		381		fs rms	
12 kHz to 20 MHz		375		fs rms	
20 kHz to 80 MHz		380		fs rms	
50 kHz to 80 MHz		365		fs rms	
4 MHz to 80 MHz		116		fs rms	
f_{REF} = 19.44 MHz; f_{OUT} = 644.53 MHz; f_{LOOP} = 50 Hz					
Bandwidth					
5 kHz to 20 MHz		388		fs rms	
12 kHz to 20 MHz		381		fs rms	
20 kHz to 80 MHz		385		fs rms	
50 kHz to 80 MHz		368		fs rms	
4 MHz to 80 MHz		106		fs rms	
f_{REF} = 19.44 MHz; f_{OUT} = 693.48 MHz; f_{LOOP} = 50 Hz					
Bandwidth					
5 kHz to 20 MHz		433		fs rms	
12 kHz to 20 MHz		427		fs rms	
20 kHz to 80 MHz		432		fs rms	
50 kHz to 80 MHz		419		fs rms	
4 MHz to 80 MHz		120		fs rms	
f_{REF} = 19.44 MHz; f_{OUT} = 156.25 MHz; f_{LOOP} = 50 Hz					
Bandwidth					
5 kHz to 20 MHz		420		fs rms	
12 kHz to 20 MHz		414		fs rms	
20 kHz to 80 MHz		461		fs rms	
50 kHz to 80 MHz		449		fs rms	
4 MHz to 80 MHz		260		fs rms	
f_{REF} = 19.44 MHz; f_{OUT} = 174.703 MHz; f_{LOOP} = 50 Hz					
Bandwidth					
5 kHz to 20 MHz		398		fs rms	
12 kHz to 20 MHz		393		fs rms	
20 kHz to 80 MHz		439		fs rms	
50 kHz to 80 MHz		427		fs rms	
4 MHz to 80 MHz		231		fs rms	
f_{REF} = 25 MHz; f_{OUT} = 161.1328 MHz; f_{LOOP} = 100 Hz					
Bandwidth					
5 kHz to 20 MHz		385		fs rms	
12 kHz to 20 MHz		379		fs rms	
20 kHz to 80 MHz		423		fs rms	
50 kHz to 80 MHz		412		fs rms	
4 MHz to 80 MHz		250		fs rms	

ABSOLUTE MAXIMUM RATINGS

Table 19.

Parameter	Rating
1.8 V Supply Voltage (VDD)	2 V
Serial Port Supply Voltage (VDD_SP)	2.75 V
Maximum Digital Input Voltage Range	−0.5 V to VDD + 0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	115°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

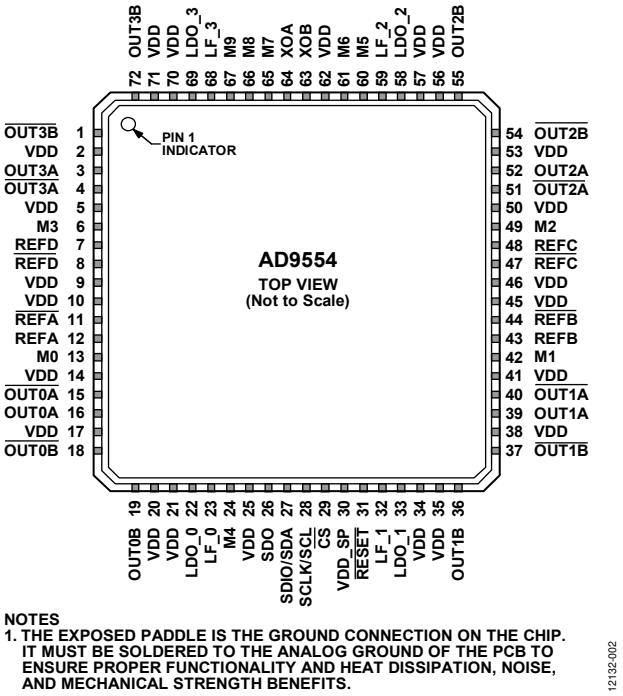

Figure 2. Pin Configuration

Table 20. Pin Function Descriptions

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
1	$\overline{\text{OUT3B}}$	O	HCSL, LVDS-compatible, LVPECL-Compatible	PLL3 Complementary Output 3B. Complementary signal to the output provided on Pin 72 (OUT3B).
2, 5, 9, 10, 14, 17, 20, 21, 25, 34, 35, 38, 41, 45, 46, 50, 53, 56, 57, 62, 70, 71	VDD	I	Power	1.5 V or 1.8 V Power Supply. See the Power Supply Partitions section for information about the recommended grouping of the power supply pins.
3	OUT3A	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL3 Output 3A. This HCSL output can be configured as a LVDS- or LVPECL-compatible output. LVPECL and LVDS levels can be achieved by ac coupling and using the Thevenin equivalent termination as described in the Input/Output Termination Recommendations section.
4	$\overline{\text{OUT3A}}$	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL3 Complementary Output 3A. Complementary signal to the output provided on Pin 3 (OUT3A).
6, 13, 42, 49	M3, M0, M1, M2	I/O	1.5 V/1.8 V CMOS	Configurable Input/Output Pins. These pins are used for status and control of the AD9554. These pins are also used at power-up and reset to control the optional external EEPROM. See the Multifunction Pins at Reset/Power-Up section for more information about the internal 100 kΩ pull-up or pull-down resistors. These pins are on the VDD power domain (Pin 9, Pin 10, Pin 45, and Pin 46), and the logic high voltage for this pin matches the voltage of the VDD pins.
7	REFD	I	Differential input	Reference D Input. This internally biased input is typically ac-coupled; when configured in this manner, it can accept any differential signal with single-ended swing up to the VDD power supply. If dc-coupled, the input can be LVDS or single-ended CMOS provided that $V_{IH} \leq$ VDD.

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
8	$\overline{\text{REFD}}$	I	Differential input	Complementary Reference D Input. Complementary signal to the input provided on Pin 7 (REFD). This pin can be left floating if REFD is a single-ended input or if REFD is not used.
11	$\overline{\text{REFA}}$	I	Differential input	Complementary Reference A Input. Complementary signal to the input provided on Pin 12 (REFA). This pin can be left floating if REFA is a single-ended input or if REFA is not used.
12	REFA	I	Differential input	Reference A Input. This internally biased input is typically ac-coupled; when configured in this manner, it can accept any differential signal with single-ended swing up to the VDD power supply. If dc-coupled, the input can be LVDS or single-ended CMOS provided that $V_{IH} \leq$ VDD.
15	$\overline{\text{OUT0A}}$	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL0 Complementary Output 0A. Complementary signal to the output provided on Pin 16 (OUT0A).
16	OUT0A	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL0 Output 0A. This HCSL output can be configured as a LVDS- or LVPECL-compatible output. LVPECL and LVDS levels can be achieved by ac-coupling and using the Thevenin equivalent termination as described in the Input/Output Termination Recommendations section.
18	$\overline{\text{OUT0B}}$	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL0 Complementary Output 0B. Complementary signal to the output provided on Pin 19 (OUT0A).
19	OUT0B	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL0 Output 0B. This HCSL output can be configured as a LVDS- or LVPECL-compatible output. LVPECL and LVDS levels can be achieved by ac-coupling and using the Thevenin equivalent termination as described in the Input/Output Termination Recommendations section.
22	LDO_0	I	LDO bypass	APLL_0 Loop Filter Voltage Regulator. Connect a 0.22 µF capacitor from this pin to ground. This pin is also the ac ground reference for the integrated APLL_0 external loop filter.
23	LF_0	I/O	Loop filter for APLL_0	Loop Filter Node for the APLL_0. Connect an external 15 nF capacitor from this pin to Pin 22 (LDO_0).
24	M4	I/O	1.5 V/1.8 V CMOS	Configurable Input/Output Pin. This pin is used for status and control of the AD9554. At power-up and reset this pin controls whether or not the M1 and M2 pins are used for the serial port connection to the optional external EEPROM. See the Multifunction Pins at Reset/Power-Up section for more information about internal 100 kΩ pull-up or pull-down resistors. This pin is on the VDD power domain, and the logic high voltage for this pin matches the voltage of the VDD pins.
26	SDO	O	CMOS	Serial Data Output (SDO). In 4-wire SPI mode, this pin is used for reading serial data. The V_{IH}/V_{OH} of this pin tracks the VDD_SP power supply, which can be 1.5 V, 1.8 V, or 2.5 V.
27	SDIO/SDA	I/O	CMOS	In SPI mode, this is the serial data input/output (SDIO) pin. In 4-wire SPI mode, data is written via this pin. In 3-wire SPI mode, data reads and writes both occur on this pin. In I^2C mode, this is the serial data pin (SDA) pin. There is no internal pull-up/pull-down resistor on this pin. The V_{IH}/V_{OH} of this pin tracks the VDD_SP power supply, which can be 1.5 V, 1.8 V, or 2.5 V.
28	SCLK/SCL	I	CMOS	In SPI mode, this is the serial programming clock (SCLK) pin. In I^2C mode, this is the serial clock pin (SCL). The V_{IH}/V_{OH} of this pin tracks the VDD_SP power supply, which can be 1.5 V, 1.8 V, or 2.5 V.
29	$\overline{\text{CS}}$	I	CMOS	Chip Select in SPI Mode ($\overline{\text{CS}}$). Active low input. When programming a device in SPI, this pin must be held low. In systems where more than one AD9554 is present, this pin enables individual programming of each AD9554. This pin has an internal 10 kΩ pull-up resistor. The V_{IH} of this pin tracks the VDD_SP power supply, which can be 1.5 V, 1.8 V, or 2.5 V.
30	VDD_SP	I	Power	Serial Port Power Supply. The power supply can be 1.5 V, 1.8 V, or 2.5 V. If this pin is at the same voltage as VDD, it can be connected to VDD pins.
31	$\overline{\text{RESET}}$	I	1.5 V/1.8 V/ 2.5 V CMOS	Chip Reset. When this active low pin is asserted, the chip goes into reset. This pin has an internal 50 kΩ pull-up resistor. The V_{IH} of this pin tracks the VDD_SP power supply, which can be 1.5 V, 1.8 V, or 2.5 V.

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
32	LF_1	I/O	Loop filter for APLL_1	Loop Filter Node for the APLL_1. Connect an external 15 nF capacitor from this pin to Pin 33 (LDO_1).
33	LDO_1	I	LDO bypass	APLL_1 Loop Filter Voltage Regulator. Connect a 0.22 µF capacitor from this pin to ground. This pin is also the ac ground reference for the integrated APLL_1 external loop filter.
36	OUT1B	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL1 Output 1B. This HCSL output can be configured as a LVDS- or LVPECL-compatible output. LVPECL and LVDS levels can be achieved by ac-coupling and using the Thevenin equivalent termination as described in the Input/Output Termination Recommendations section.
37	$\overline{\text{OUT1B}}$	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL1 Complementary Output 1B. Complementary signal to the output provided on Pin 36 (OUT1B).
39	OUT1A	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL1 Output 1A. This HCSL output can be configured as a LVDS- or LVPECL-compatible output. LVPECL and LVDS levels can be achieved by ac-coupling and using the Thevenin equivalent termination as described in the Input/Output Termination Recommendations section.
40	$\overline{\text{OUT1A}}$	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL1 Complementary Output 1A. Complementary signal to the output provided on Pin 39 (OUT1A).
43	REFB	I	Differential input	Reference B Input. This internally biased input is typically ac-coupled; when configured in this manner, it can accept any differential signal with single-ended swing up to the VDD power supply. If dc-coupled, the input can be LVDS or single-ended CMOS provided that $V_{IH} \leq$ VDD.
44	$\overline{\text{REFB}}$	I	Differential input	Complementary Reference B Input. Complementary signal to the input provided on Pin 43 (REFB). This pin can be left floating if REFB is a single-ended input, or if REFB is not used.
47	$\overline{\text{REFC}}$	I	Differential input	Complementary Reference C Input. Complementary signal to the input provided on Pin 48 (REFC). This pin can be left floating if REFC is a single-ended input, or if REFC is not used.
48	REFC	I	Differential input	Reference C Input. This internally biased input is typically ac-coupled; when configured in this manner, it can accept any differential signal with single-ended swing up to the VDD power supply. If dc-coupled, the input can be LVDS or single-ended CMOS provided that $V_{IH} \leq$ VDD.
51	$\overline{\text{OUT2A}}$	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL2 Complementary Output 2A. Complementary signal to the output provided on Pin 52 (OUT2A).
52	OUT2A	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL2 Output 2A. This HCSL output can be configured as a LVDS- or LVPECL-compatible output. LVPECL and LVDS levels can be achieved by ac-coupling and using the Thevenin equivalent termination as described in the Input/Output Termination Recommendations section.
54	$\overline{\text{OUT2B}}$	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL2 Complementary Output 2B. Complementary signal to the output provided on Pin 55 (OUT2B).
55	OUT2B	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL2 Output 2B. This HCSL output can be configured as a LVDS- or LVPECL-compatible output. LVPECL and LVDS levels can be achieved by ac-coupling and using the Thevenin equivalent termination as described in the Input/Output Termination Recommendations section.
58	LDO_2	I	LDO bypass	APLL_2 Loop Filter Voltage Regulator. Connect a 0.22 µF capacitor from this pin to ground. This pin is also the ac ground reference for the integrated APLL_2 external loop filter.
59	LF_2	I/O	Loop filter for APLL_2	Loop Filter Node for the APLL_2. Connect an external 15 nF capacitor from this pin to Pin 58 (LDO_2).

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
60, 61, 65, 66, 67	M5, M6, M7, M8, M9	I/O	1.5 V/1.8 V CMOS	Configurable Input/Output Pins. These pins are used for status and control of the AD9554. These pins are also used at power-up and reset to determine the serial port and address. See the Multifunction Pins at Reset/Power-Up section for more information about the internal 100 kΩ pull-up or pull-down resistors. These pins are on the VDD digital power domain (Pin 62), and the logic high voltage for this pin matches the voltage of the VDD pins.
63	XOB	I	Differential input	Complementary System Clock Input. Complementary signal to XOA. XOB contains internal dc biasing and must be ac-coupled with a 0.1 µF capacitor except when using a crystal. When a crystal is used, connect the crystal across XOA and XOB.
64	XOA	I	Differential input	System Clock Input. XOA contains internal dc biasing and must be ac-coupled with a 0.1 µF capacitor except when using a crystal. When a crystal is used, connect the crystal across XOA and XOB. Single-ended CMOS is also an option, but a spur may be introduced if the duty cycle is not 50%. When using XOA as a single-ended input, connect a 0.1 µF capacitor from XOB to ground.
68	LF_3	I/O	Loop filter for APLL_3	Loop Filter Node for the APLL_3. Connect an external 15 nF capacitor from this pin to Pin 69 (LDO_3).
69	LDO_3	I	LDO bypass	APLL_3 Loop Filter Voltage Regulator. Connect a 0.22 µF capacitor from this pin to ground. This pin is also the ac ground reference for the integrated APLL_3 external loop filter.
72	OUT3B	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL3 Output 3B. This HCSL output can be configured as a LVDS- or LVPECL-compatible output. LVPECL and LVDS levels can be achieved by ac-coupling and using the Thevenin equivalent termination as described in the Input/Output Termination Recommendations section.
0	EPAD	GND	Exposed pad	The exposed pad is the ground connection on the chip. It must be soldered to the analog ground of the printed circuit board (PCB) to ensure proper functionality and heat dissipation, noise, and mechanical strength benefits.

TYPICAL PERFORMANCE CHARACTERISTICS

f_R = input reference clock frequency, f_{OUT} = output clock frequency, f_{SYS} = SYSCLK input frequency, and VDD at 1.8 V.

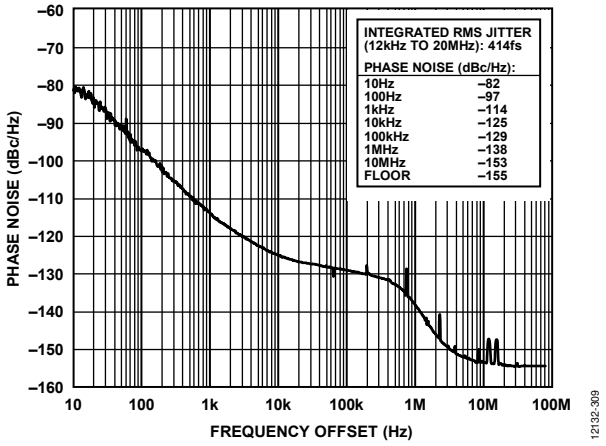

Figure 3. Absolute Phase Noise (Output Driver = 21 mA Mode), f_R = 19.44 MHz, f_{OUT} = 156.25 MHz, DPLL Loop Bandwidth = 50 Hz, f_{SYS} = 49.152 MHz Crystal

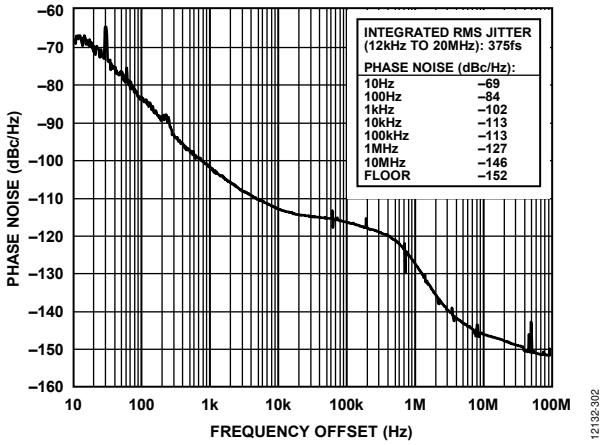

Figure 4. Absolute Phase Noise (Output Driver = 21 mA Mode), f_R = 19.44 MHz, f_{OUT} = 622.08 MHz, DPLL Loop Bandwidth = 50 Hz, f_{SYS} = 49.152 MHz Crystal

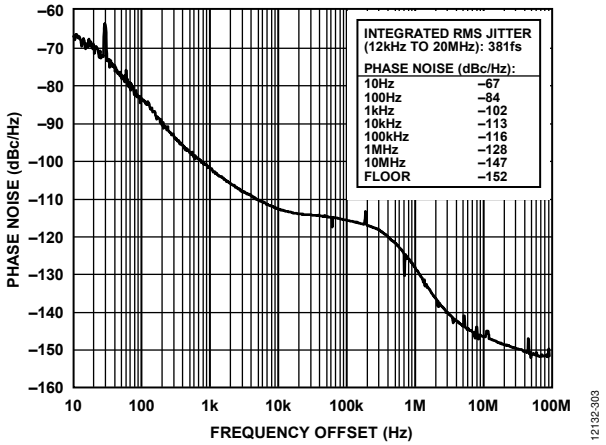

Figure 5. Absolute Phase Noise (Output Driver = 21 mA Mode), f_R = 19.44 MHz, f_{OUT} = 644.53125 MHz, DPLL Loop Bandwidth = 50 Hz, f_{SYS} = 49.152 MHz Crystal

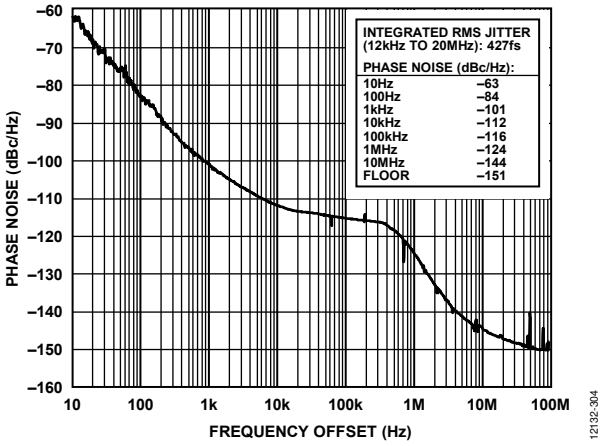

Figure 6. Absolute Phase Noise (Output Driver = 21 mA Mode), f_R = 19.44 MHz, f_{OUT} = 693.482991 MHz, DPLL Loop Bandwidth = 50 Hz, f_{SYS} = 49.152 MHz Crystal

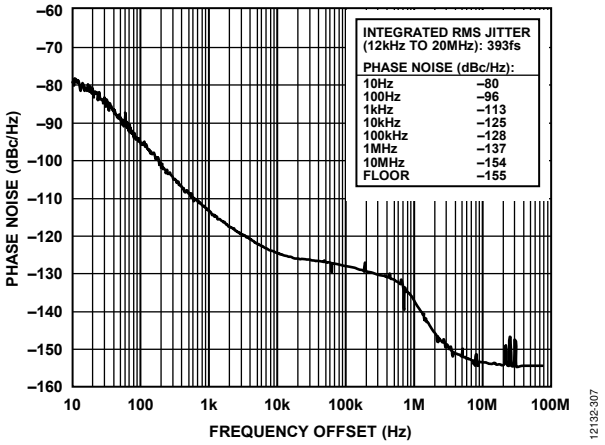

Figure 7. Absolute Phase Noise (Output Driver = 21 mA Mode), f_R = 19.44 MHz, f_{OUT} = 174.703 MHz, DPLL Loop Bandwidth = 1 kHz, f_{SYS} = 49.152 MHz Crystal

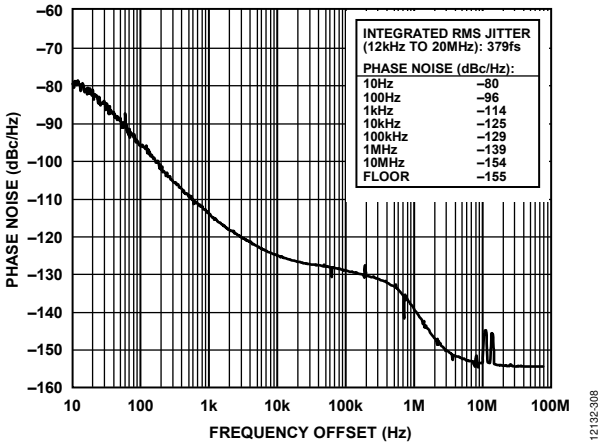

Figure 8. Absolute Phase Noise, f_R = 19.44 MHz, f_{OUT} = 161.1328125 MHz, DPLL Loop Bandwidth = 100 Hz, f_{SYS} = 49.152 MHz Crystal

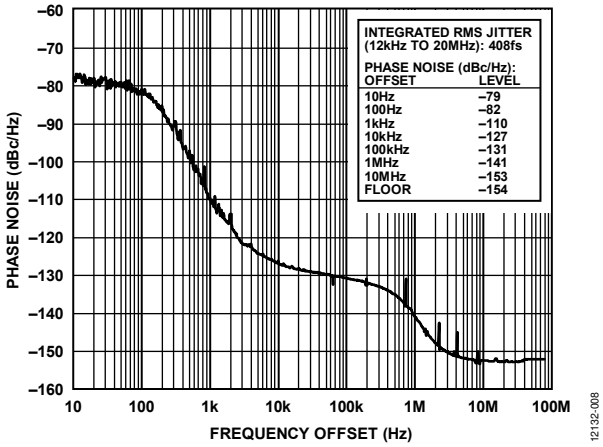

Figure 9. Absolute Phase Noise (Output Driver = 14 mA Mode), f_R = 2 kHz, f_{OUT} = 125 MHz, DPLL Loop Bandwidth = 100 Hz, f_{SYS} = 49.152 MHz Crystal

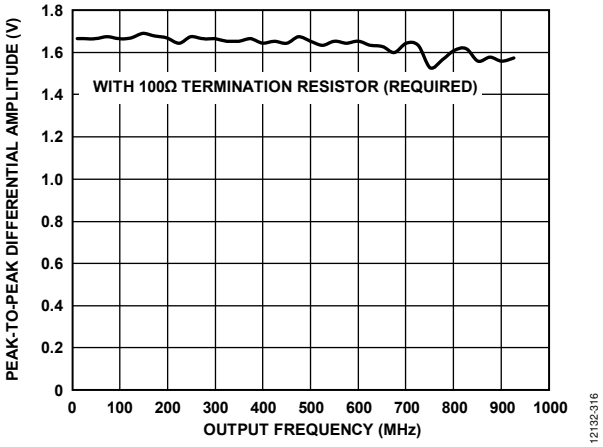

Figure 10. Peak-to-Peak Differential Amplitude vs. Output Frequency, 28 mA Mode (LVPECL-Compatible Mode) with 100 Ω Termination Resistor (Required)

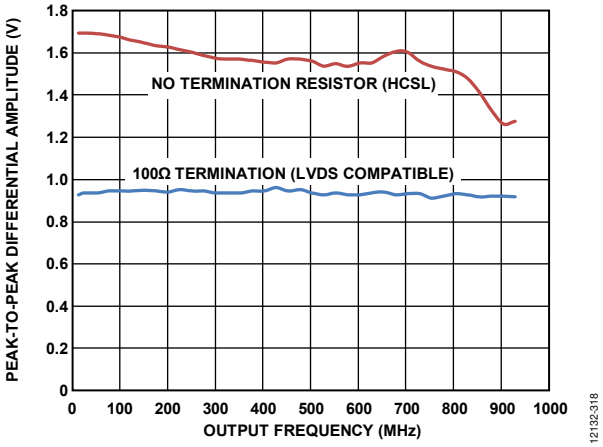

Figure 11. Peak-to-Peak Differential Amplitude vs. Output Frequency, 14 mA Mode

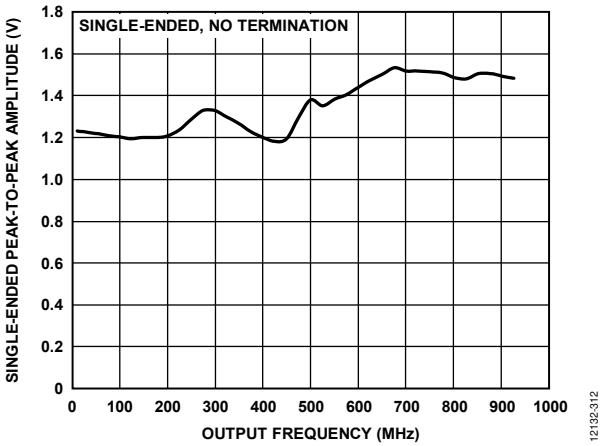

Figure 12. Single-Ended Peak-to-Peak Amplitude vs. Output Frequency, 21 mA Mode (No Termination)

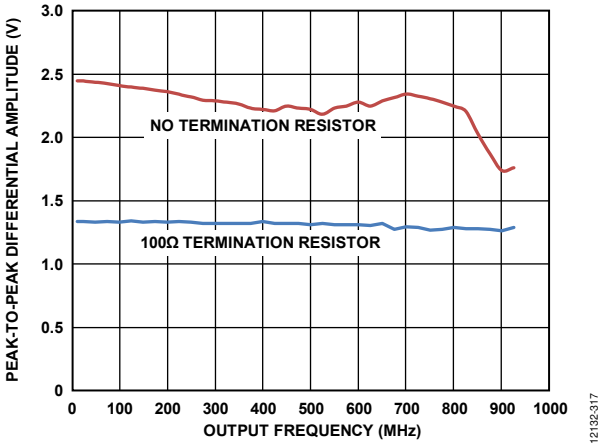

Figure 13. Peak-to-Peak Differential Amplitude vs. Output Frequency, 21 mA Mode

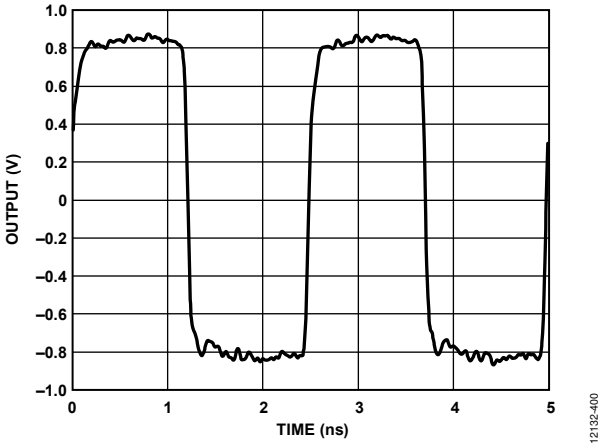

Figure 14. Output Waveform, 28 mA LVPECL-Compatible Mode (400 MHz) with 100 Ω Termination Resistor

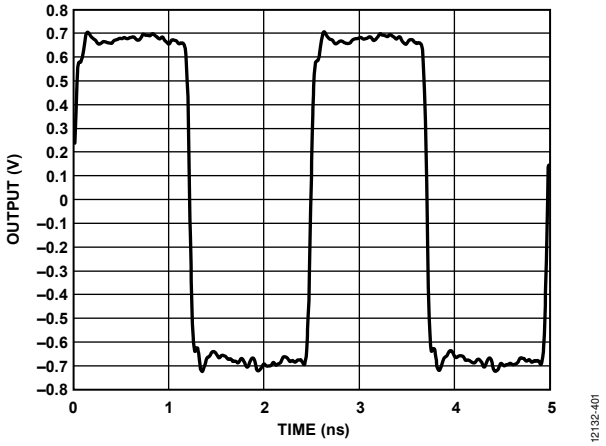

Figure 15. Output Waveform, 21 mA Mode (400 MHz) with 100 Ω Termination at Load

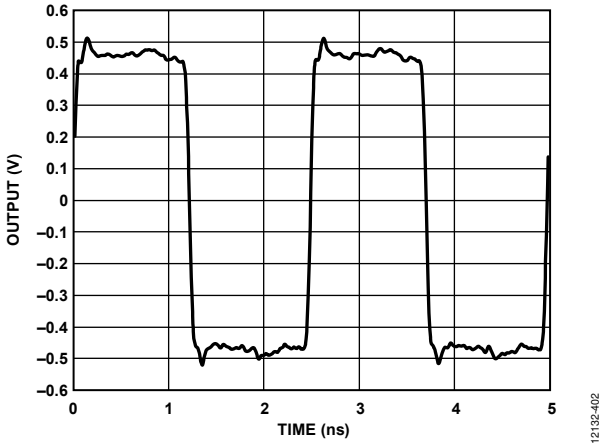

Figure 16. Output Waveform, 14 mA LVDS-Compatible Mode (400 MHz) with 100 Ω Termination at Load

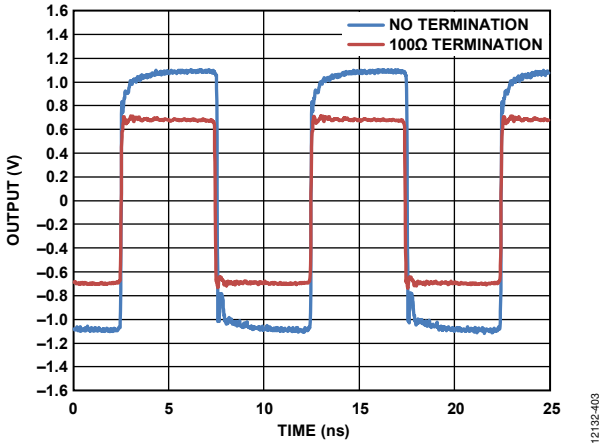

Figure 17. Output Waveform, 21 mA Mode (100 MHz)

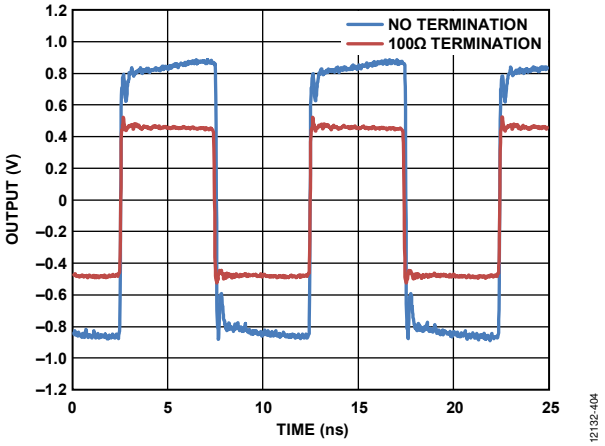

Figure 18. Output Waveform, 14 mA Mode (100 MHz)

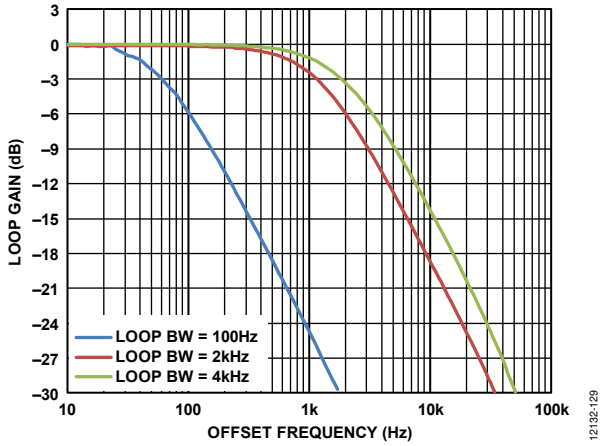

Figure 19. Closed-Loop Transfer Function for 100 Hz, 2 kHz, and 4 kHz Loop Bandwidth Settings; High Phase Margin Loop Filter Setting; Figure Compliant with Telcordia GR-253 Jitter Transfer Test for Loop Bandwidths <2 kHz (Note that the bandwidth register setting is the point where the open-loop gain = 0 dB.)

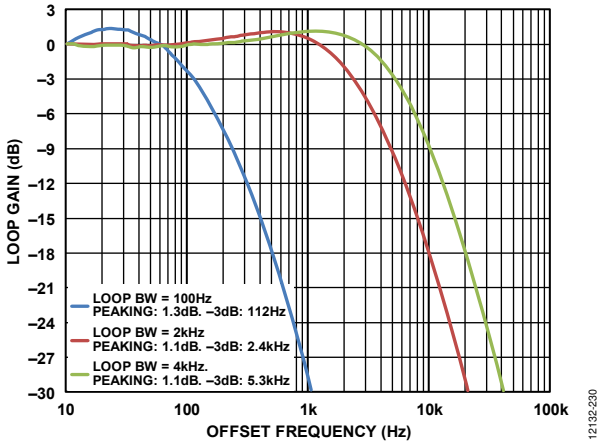

Figure 20. Closed-Loop Transfer Function for 100 Hz, 2 kHz, and 4 kHz Loop Bandwidth Settings; Normal Phase Margin Loop Filter Setting (Note that the bandwidth register setting is the point where the open-loop gain = 0 dB.)

INPUT/OUTPUT TERMINATION RECOMMENDATIONS

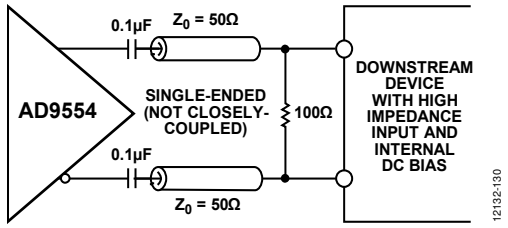

Figure 21. Destination Self-Biased Differential Receiver; Use 14 mA Mode for LVDS-Compatible Amplitude or 28 mA for LVPECL-Compatible Amplitudes (100 Ω resistor must be as close to the destination receiver as possible.)

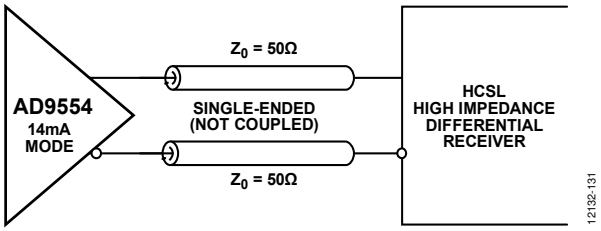

Figure 22. DC-Coupled HCSL Receiver

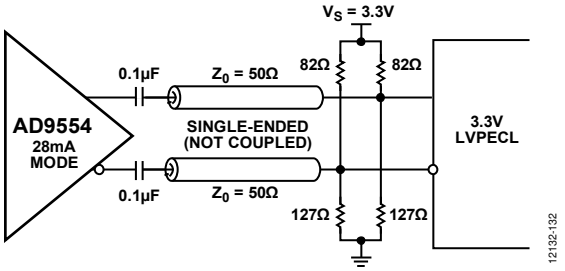

Figure 23. Interfacing the HCSL Driver to a 3.3 V LVPECL Input (This method incorporates impedance matching and dc-biasing for bipolar LVPECL receivers. If the receiver is self-biased, the termination scheme shown in Figure 21 is recommended.)

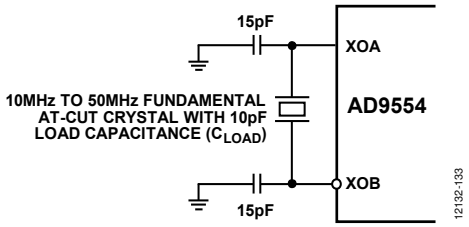

Figure 24. System Clock Input (XOA/XOB) in Crystal Mode (The recommended C_{LOAD} = 10 pF is shown. The values of 15 pF shunt capacitors shown here must equal 2 × (C_{LOAD} − C_{STRAY}), where C_{STRAY} is typically 2 pF to 5 pF.)

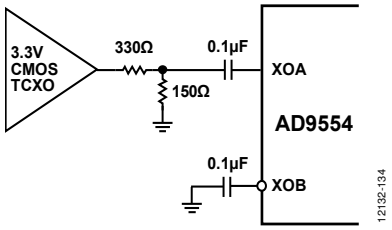

Figure 25. System Clock Input (XOA, XOB) When Using a TCXO/OCXO with 3.3 V CMOS Output