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Dual Input Multiservice Line Card Adaptive Clock Translator

Data Sheet **AD9557**

FEATURES

- Supports GR-1244 Stratum 3 stability in holdover mode
- Supports smooth reference switchover with virtually no disturbance on output phase
- Supports Telcordia GR-253 jitter generation, transfer, and tolerance for SONET/SDH up to OC-192 systems
- Supports ITU-T G.8262 synchronous Ethernet slave clocks
- Supports ITU-T G.823, G.824, G.825, and G.8261
- Auto/manual holdover and reference switchover
- 2 reference inputs (single-ended or differential)
- Input reference frequencies: 2 kHz to 1250 MHz
- Reference validation and frequency monitoring (1 ppm)
- Programmable input reference switchover priority
- 20-bit programmable input reference divider
- 2 pairs of clock output pins, with each pair configurable as a single differential LVDS/HSTL output or as 2 single-ended CMOS outputs
- Output frequencies: 360 kHz to 1250 MHz
- Programmable 17-bit integer and 23-bit fractional feedback divider in digital PLL
- Programmable digital loop filter covering loop bandwidths from 0.1 Hz to 5 kHz (2 kHz maximum for <0.1 dB of peaking)
- Low noise system clock multiplier
- Frame sync support
- Adaptive clocking
- Optional crystal resonator for system clock input
- On-chip EEPROM to store multiple power-up profiles
- Pin program function for easy frequency translation configuration
- Software controlled power-down
- 40-lead, 6 mm × 6 mm, LFCSP package

APPLICATIONS

- Network synchronization, including synchronous Ethernet and SDH to OTN mapping/demapping
- Cleanup of reference clock jitter
- SONET/SDH/OTN clocks up to 100 Gbps, including FEC
- Stratum 3 holdover, jitter cleanup, and phase transient control
- Wireless base station controllers
- Cable infrastructure
- Data communications

GENERAL DESCRIPTION

The AD9557 is a low loop bandwidth clock multiplier that provides jitter cleanup and synchronization for many systems, including synchronous optical networks (OTN/SONET/SDH). The AD9557 generates an output clock synchronized to up to four external input references. The digital PLL allows for reduction of input time jitter or phase noise associated with the external references. The digitally controlled loop and holdover circuitry of the AD9557 continuously generates a low jitter output clock even when all reference inputs have failed.

The AD9557 operates over an industrial temperature range of −40°C to +85°C. If more inputs/outputs are needed, refer to the AD9558 for the four-input/six-output version of the same device.

FUNCTIONAL BLOCK DIAGRAM

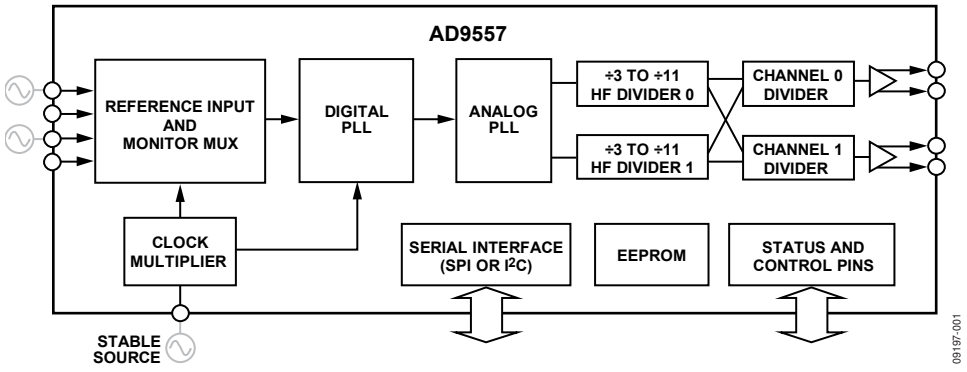

Figure 1.

Rev. C
Document Feedback

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- AD9557 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9557: Dual Input Multiservice Line Card Adaptive Clock Translator Data Sheet

TOOLS AND SIMULATIONS

- AD9557 IBIS Model

REFERENCE MATERIALS

Press

- Dual Adaptive Clock Translator Supports Wide Range of Wired Network Applications including OTN De-mapping and High-density Line Cards

Product Selection Guide

- RF Source Booklet

DESIGN RESOURCES

- AD9557 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9557 EngineerZone Discussions.

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10/2011—Revision 0: Initial Version

SPECIFICATIONS

Minimum (min) and maximum (max) values apply for the full range of supply voltage and operating temperature variations. Typical (typ) values apply for AVDD3 = DVDD_I/O = 3.3 V; AVDD = DVDD = 1.8 V; T_A = 25°C, unless otherwise noted.

SUPPLY VOLTAGE

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
DVDD3	3.135	3.30	3.465	V	
DVDD	1.71	1.80	1.89	V	
AVDD3	3.135	3.30	3.465	V	
AVDD	1.71	1.80	1.89	V	

SUPPLY CURRENT

The test conditions for the maximum (max) supply current are the same as the test conditions for the All Blocks Running parameter of Table 3. The test conditions for the typical (typ) supply current are the same as the test conditions for the Typical Configuration parameter of Table 3.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT FOR TYPICAL CONFIGURATION					Typical numbers are for the typical configuration listed in Table 3
I_{DVDD3}	12	18	26	mA	Pin 30, Pin 31, Pin 40
I_{DVDD}	13	20	28	mA	Pin 6, Pin 34, Pin 35
I_{AVDD3}	35	49	63	mA	Pin 14, Pin 19
I_{AVDD}	112	162	215	mA	Pin 7, Pin 10, Pin 11, Pin 17, Pin 18, Pin 22, Pin 23, Pin 24
SUPPLY CURRENT FOR THE ALL BLOCKS RUNNING CONFIGURATION					Maximum numbers are for all blocks running configuration in Table 3
I_{DVDD3}	12	18	33	mA	Pin 30, Pin 31, Pin 40
I_{DVDD}	10	19	30	mA	Pin 6, Pin 34, Pin 35
I_{AVDD3}	47	68	89	mA	Pin 14, Pin 19
I_{AVDD}	113	163	215	mA	Pin 7, Pin 10, Pin 11, Pin 17, Pin 18, Pin 22, Pin 23, Pin 24

POWER DISSIPATION

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION					
Typical Configuration	0.36	0.55	0.76	W	System clock: 49.152 MHz crystal; DPLL active; both 19.44 MHz input references in differential mode; one HSTL driver at 644.53125 MHz; one 3.3 V CMOS driver at 161.1328125 MHz and 80 pF capacitive load on CMOS output
All Blocks Running	0.39	0.61	0.85	W	System clock: 49.152 MHz crystal; DPLL active; both input references in differential mode; one HSTL driver at 750 MHz; two 3.3 V CMOS drivers at 250 MHz and 80 pF capacitive load on CMOS outputs
Full Power-Down		44	125	mW	Typical configuration with no external pull-up or pull-down resistors; approximately 2/3 of this power is on AVDD3
Incremental Power Dissipation					Conditions = typical configuration; table values show the change in power due to the indicated operation
Input Reference On/Off					
Differential Without Divide-by-2	20	25	32	mW	Additional current draw is in the DVDD3 domain only
Differential With Divide-by-2	26	32	40	mW	Additional current draw is in the DVDD3 domain only
Single-Ended Without Divide-by-2	5	7	9	mW	Additional current draw is in the DVDD3 domain only
Output Distribution Driver On/Off					
LVDS (at 750 MHz)	12	17	22	mW	Additional current draw is in the AVDD domain only
HSTL (at 750 MHz)	14	21	28	mW	Additional current draw is in the AVDD domain only
1.8 V CMOS (at 250 MHz)	14	21	28	mW	A single 1.8 V CMOS output with an 80 pF load
3.3 V CMOS (at 250 MHz)	18	27	36	mW	A single 3.3 V CMOS output with an 80 pF load
Other Blocks On/Off					
Second RF Divider	36	51	64	mW	Additional current draw is in the AVDD domain only
Channel Divider Bypassed	10	17	23	mW	Additional current draw is in the AVDD domain only

LOGIC INPUTS ($\overline{\text{RESET}}$, $\overline{\text{SYNC}}$, PINCONTROL, M3 TO M0)

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS ($\overline{\text{RESET}}$, $\overline{\text{SYNC}}$, PINCONTROL)					
Input High Voltage (V_{IH})	2.1			V	
Input Low Voltage (V_{IL})			0.8	V	
Input Current (I_{INH}, I_{INL})		±50	±100	µA	
Input Capacitance (C_{IN})		3		pF	
LOGIC INPUTS (M3 to M0)					
Input High Voltage (V_{IH})	2.5			V	
Input ½ Level Voltage (V_{IM})	1.0		2.2	V	
Input Low Voltage (V_{IL})			0.6	V	
Input Current (I_{INH}, I_{INL})		±60	±100	µA	
Input Capacitance (C_{IN})		3		pF	

LOGIC OUTPUTS (M3 TO M0, IRQ)

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS (M3 to M0, IRQ)					
Output High Voltage (V_{OH})	DVDD3 – 0.4			V	I_{OH} = 1 mA
Output Low Voltage (V_{OL})			0.4	V	I_{OL} = 1 mA
IRQ Leakage Current					Open-drain mode
Active Low Output Mode			−200	µA	V_{OH} = 3.3 V
Active High Output Mode			100	µA	V_{OL} = 0 V

SYSTEM CLOCK INPUTS (XOA, XOB)

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SYSTEM CLOCK MULTIPLIER					
Output Frequency Range	750		805	MHz	The VCO range may place limitations on nonstandard system clock input frequencies
Phase Frequency Detector (PFD) Rate			150	MHz	
Frequency Multiplication Range	2		255		Assumes valid system clock and PFD rates
SYSTEM CLOCK REFERENCE INPUT PATH					
Input Frequency Range	10		600	MHz	
Minimum Input Slew Rate	20			V/µs	Minimum limit imposed for jitter performance
Common-Mode Voltage	1.05	1.16	1.25	V	Internally generated
Differential Input Voltage Sensitivity	250			mV p-p	Minimum voltage across pins required to ensure switching between logic states; the instantaneous voltage on either pin must not exceed the supply rails; can accommodate single-ended input by ac grounding of complementary input; 1 V p-p recommended for optimal jitter performance
System Clock Input Doubler Duty Cycle					This is the amount of duty cycle variation that can be tolerated on the system clock input to use the doubler
System Clock Input = 50 MHz	45	50	55	%	
System Clock Input = 20 MHz	46	50	54	%	
System Clock Input = 16 MHz to 20 MHz	47	50	53	%	
Input Capacitance		3		pF	Single-ended, each pin
Input Resistance		4.2		kΩ	
CRYSTAL RESONATOR PATH					
Crystal Resonator Frequency Range	10		50	MHz	Fundamental mode, AT cut crystal
Maximum Crystal Motional Resistance			100	Ω	

REFERENCE INPUTS

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL OPERATION					
Frequency Range					
Sinusoidal Input	10		750	MHz	
LVPECL Input	0.002		1250	MHz	The reference input divide-by-2 block must be engaged for f_{IN} > 705 MHz
LVDS Input	0.002		750	MHz	The reference input divide-by-2 block must be engaged for f_{IN} > 705 MHz
Minimum Input Slew Rate	40			V/µs	Minimum limit imposed for jitter performance
Common-Mode Input Voltage					
AC-Coupled	1.9	2	2.2	V	Internally generated
DC-Coupled	1.0		2.4	V	
Differential Input Voltage Sensitivity				mV	Minimum differential voltage across pins is required to ensure switching between logic levels; instantaneous voltage on either pin must not exceed the supply rails
f_{IN} < 800 MHz	240			mV	
f_{IN} = 800 to 1050 MHz	320			mV	
f_{IN} = 1050 to 1250 MHz	400			mV	
Differential Input Voltage Hysteresis		58	100	mV	
Input Resistance		21		kΩ	
Input Capacitance		3		pF	
Minimum Pulse Width High					
LVPECL	390			ps	
LVDS	640			ps	
Minimum Pulse Width Low					
LVPECL	390			ps	
LVDS	640			ps	
SINGLE-ENDED OPERATION					
Frequency Range (CMOS)	0.002		300	MHz	
Minimum Input Slew Rate	40			V/µs	Minimum limit imposed for jitter performance
Input Voltage High (V_{IH})					
1.2 V to 1.5 V Threshold Setting	1.0			V	
1.8 V to 2.5 V Threshold Setting	1.4			V	
3.0 V to 3.3 V Threshold Setting	2.0			V	
Input Voltage Low (V_{IL})					
1.2 V to 1.5 V Threshold Setting			0.35	V	
1.8 V to 2.5 V Threshold Setting			0.5	V	
3.0 V to 3.3 V Threshold Setting			1.0	V	
Input Resistance		47		kΩ	
Input Capacitance		3		pF	
Minimum Pulse Width High	1.5			ns	
Minimum Pulse Width Low	1.5			ns	

REFERENCE MONITORS

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE MONITORS					
Reference Monitor					
Loss of Reference Detection Time			1.1	DPLL PFD period	Nominal phase detector period = R/f_{REF}[1]
Frequency Out-of Range Limits	<2		10^5	$\Delta f/f_{REF}$ (ppm)	Programmable (lower bound is subject to quality of the system clock (SYSCLK)); SYSCLK accuracy must be better than the lower bound
Validation Timer	0.001		65.535	sec	Programmable in 1 ms increments

[1] f_{REF} is the frequency of the active reference; R is the frequency division factor determined by the R divider.

REFERENCE SWITCHOVER SPECIFICATIONS

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE SWITCHOVER SPECIFICATIONS					Assumes a jitter-free reference; satisfies Telcordia GR-1244-CORE requirements; select high PM base loop filter bit (Register 0x070E, Bit 0) is set to 1 for all active references
Maximum Output Phase Perturbation (Phase Build-Out Switchover)					
50 Hz DPLL Loop Bandwidth					Valid for automatic and manual reference switching
Peak		0	±100	ps	
Steady State		0	±100	ps	
2 kHz DPLL Loop Bandwidth					Valid for automatic and manual reference switching
Peak		0	±250	ps	
Steady State		0	±100	ps	
Time Required to Switch to a New Reference					
Phase Build-Out Switchover			1.1	DPLL PFD period	Calculated using the nominal phase detector period (NPDP = R/f_{REF}); the total time required is equal to the time plus the reference validation time and the time required to lock to the new reference

DISTRIBUTION CLOCK OUTPUTS

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL MODE					
Output Frequency	0.36		1250	MHz	
Rise/Fall Time (20% to 80%)[1]		140	250	ps	100 Ω termination across output pins
Duty Cycle					
Up to f_{OUT} = 700 MHz	45	48	52	%	
Up to f_{OUT} = 750 MHz	42	48	53	%	
Up to f_{OUT} = 1250 MHz		43		%	
Differential Output Voltage Swing	700	950	1200	mV	Magnitude of voltage across pins; output driver static
Common-Mode Output Voltage	700	870	960	mV	Output driver static
LVDS MODE					
Output Frequency	0.36		1250	MHz	
Rise/Fall Time (20% to 80%)[1]		185	280	ps	100 Ω termination across the output pair
Duty Cycle					
Up to f_{OUT} = 750 MHz	44	48	53	%	
Up to f_{OUT} = 800 MHz	43	47	53	%	
Up to f_{OUT} = 1250 MHz		43		%	
Differential Output Voltage Swing					
Balanced, V_{OD}	247		454	mV	Voltage swing between output pins; output driver static
Unbalanced, ΔV_{OD}			50	mV	Absolute difference between voltage swing of normal pin and inverted pin; output driver static
Offset Voltage					
Common Mode, V_{OS}	1.125	1.26	1.375	V	Output driver static
Common-Mode Difference, ΔV_{OS}			50	mV	Voltage difference between pins; output driver static
Short-Circuit Output Current		13	24	mA	Output driver static
CMOS MODE					
Output Frequency					
1.8 V Supply	0.36		150	MHz	10 pF load
3.3 V Supply (OUT0)					
Strong Drive Strength Setting	0.36		250	MHz	10 pF load
Weak Drive Strength Setting	0.36		25	MHz	10 pF load
Rise/Fall Time(20% to 80%)[1]					
1.8 V Supply		1.5	3	ns	10 pF load
3.3 V Supply					
Strong Drive Strength Setting		0.4	0.6	ns	10 pF load
Weak Drive Strength Setting		8		ns	10 pF load
Duty Cycle					
1.8 V Mode		50		%	10 pF load
3.3 V Strong Mode		47		%	10 pF load
3.3 V Weak Mode		51		%	10 pF load
Output Voltage High (V_{OH})					Output driver static; strong drive strength
AVDD3 = 3.3 V, I_{OH} = 10 mA	AVDD3 – 0.3			V	
AVDD3 = 3.3 V, I_{OH} = 1 mA	AVDD3 – 0.1			V	
AVDD3 = 1.8 V, I_{OH} = 1 mA	AVDD – 0.2			V	
Output Voltage Low (V_{OL})					Output driver static; strong drive strength
AVDD3 = 3.3 V, I_{OL} = 10 mA			0.3	V	
AVDD3 = 3.3 V, I_{OL} = 1 mA			0.1	V	
AVDD3 = 1.8 V, I_{OL} = 1 mA			0.1	V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT TIMING SKEW					10 pF load
Between OUT0 and OUT1		10	70	ps	HSTL mode on both drivers; rising edge only; any divide value
Additional Delay on One Driver by Changing Its Logic Type					
HSTL to LVDS	−5	+1	+5	ps	Positive value indicates that the LVDS edge is delayed relative to HSTL
HSTL to 1.8 V CMOS	−5	0	+5	ps	Positive value indicates that the CMOS edge is delayed relative to HSTL
OUT1 HSTL to OUT0 3.3 V CMOS, Strong Mode		3.53	3.59	ns	The CMOS edge is delayed relative to HSTL

[1] The listed values are for the slower edge (rise or fall).

TIME DURATION OF DIGITAL FUNCTIONS

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TIME DURATION OF DIGITAL FUNCTIONS					
EEPROM-to-Register Download Time		13	20	ms	Using default EEPROM storage sequence (see Register 0x0E10 to Register 0x0E3F)
Register-to-EEPROM Upload Time		138	145	ms	Using default EEPROM storage sequence (see Register 0x0E10 to Register 0x0E3F
Minimum Power-Down Exit Time		1		ms	Time from power-down exit to system clock lock detect

DIGITAL PLL

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL PLL					
Phase-Frequency Detector (PFD) Input Frequency Range	2		100	kHz	
Loop Bandwidth	0.1		2000	Hz	Programmable design parameter
Phase Margin	30		89	Degrees	Programmable design parameter
Closed-Loop Peaking	<0.1			dB	Programmable design parameter; device can be programmed for <0.1 dB peaking in accordance with Telcordia GR-253 jitter transfer
Reference Input (R) Division Factor	1		2^{20}		1, 2, …, 1,048,576
Integer Feedback (N1) Division Factor	180		2^{17}		180, 181, …, 131,072
Fractional Feedback Divide Ratio	0		0.999		Maximum value: 16,777,215/16,777,216

DIGITAL PLL LOCK DETECTION

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PHASE LOCK DETECTOR					
Threshold Programming Range	0.001		65.5	ns	
Threshold Resolution		1		ps	
FREQUENCY LOCK DETECTOR					
Threshold Programming Range	0.001		16,700	ns	Reference to feedback period difference
Threshold Resolution		1		ps	

HOLDOVER SPECIFICATIONS

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HOLDOVER SPECIFICATIONS					
Initial Frequency Accuracy		<0.01		ppm	Excludes frequency drift of SYSCLK source; excludes frequency drift of input reference prior to entering holdover; compliant with GR-1244 Stratum 3

SERIAL PORT SPECIFICATIONS—SPI MODE

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{CS}$					
Input Logic 1 Voltage	2.2			V	
Input Logic 0 Voltage			1.2	V	
Input Logic 1 Current		44		μA	
Input Logic 0 Current		88		μA	
Input Capacitance		2		pF	
SCLK					Internal 30 kΩ pull-down resistor
Input Logic 1 Voltage	2.2			V	
Input Logic 0 Voltage		0.8	1.2	V	
Input Logic 1 Current		200		μA	
Input Logic 0 Current		1		μA	
Input Capacitance		2		pF	
SDIO					
As an Input					
Input Logic 1 Voltage	2.2			V	
Input Logic 0 Voltage			1.2	V	
Input Logic 1 Current		1		μA	
Input Logic 0 Current		1		μA	
Input Capacitance		2		pF	
As an Output					
Output Logic 1 Voltage	DVDD3 – 0.6			V	1 mA load current
Output Logic 0 Voltage			0.4	V	1 mA load current
SDO					
Output Logic 1 Voltage	DVDD3 – 0.6			V	1 mA load current
Output Logic 0 Voltage			0.4	V	1 mA load current
TIMING					
SCLK					
Clock Rate, $1/t_{CLK}$			40	MHz	
Pulse Width High (t_{HIGH})	10			ns	
Pulse Width Low (t_{LOW})	13			ns	
SDIO to SCLK Setup (t_{DS})	3			ns	
SCLK to SDIO Hold (t_{DH})	6			ns	
SCLK to Valid SDIO and SDO (t_{DV})			10	ns	
$\overline{CS}$ to SCLK Setup (t_S)	10			ns	
$\overline{CS}$ to SCLK Hold (t_C)	0			ns	
$\overline{CS}$ Minimum Pulse Width High	6			ns	

SERIAL PORT SPECIFICATIONS—I²C MODE

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDA, SCL (AS INPUT)					
Input Logic 1 Voltage	0.7 × DVDD3			V	
Input Logic 0 Voltage			0.3 × DVDD3	V	
Input Current	−10		+10	µA	For V_{IN} = 10% to 90% DVDD3
Hysteresis of Schmitt Trigger Inputs	0.015 × DVDD3				
Pulse Width of Spikes That Must Be Suppressed by the Input Filter (t_{SP})			50	ns	
SDA (AS OUTPUT)					
Output Logic 0 Voltage			0.4	V	I_O = 3 mA
Output Fall Time from V_{IHmin} to V_{ILmax}	20 + 0.1 × C_b[1]		250	ns	10 pF ≤ C_b ≤ 400 pF[1]
TIMING					
SCL Clock Rate			400	kHz	
Bus-Free Time Between a Stop and Start Condition (t_{BUF})	1.3			µs	
Repeated Start Condition Setup Time ($t_{SU;STA}$)	0.6			µs	
Repeated Hold Time Start Condition ($t_{HD;STA}$)	0.6			µs	After this period, the first clock pulse is generated
Stop Condition Setup Time ($t_{SU;STO}$)	0.6			µs	
Low Period of the SCL Clock (t_{LOW})	1.3			µs	
High Period of the SCL Clock (t_{HIGH})	0.6			µs	
SCL/SDA Rise Time (t_R)	20 + 0.1 × C_b[1]		300	ns	
SCL/SDA Fall Time (t_F)	20 + 0.1 × C_b[1]		300	ns	
Data Setup Time ($t_{SU;DAT}$)	100			ns	
Data Hold Time ($t_{HD;DAT}$)	100			ns	
Capacitive Load for Each Bus Line (C_b[1])			400	pF	

[1] C_b is the capacitance (pF) of a single bus line.

JITTER GENERATION

Jitter generation (random jitter) uses 49.152 MHz crystal for system clock input.

Table 17.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
JITTER GENERATION					System clock doubler enabled; high phase margin mode enabled; Register 0x0405 = 0x20; Register 0x0403 = 0x07; Register 0x0400 = 0x81; in cases where multiple driver types are listed, both driver types were tested at those conditions, and the one with higher jitter is quoted, although there is usually not a significant jitter difference between the driver types
f_{REF} = 19.44 MHz; f_{OUT} = 622.08 MHz; f_{LOOP} = 50 Hz; HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		304		fs rms	
Bandwidth: 12 kHz to 20 MHz		296		fs rms	
Bandwidth: 20 kHz to 80 MHz		300		fs rms	
Bandwidth: 50 kHz to 80 MHz		266		fs rms	
Bandwidth: 16 MHz to 320 MHz		185		fs rms	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
f_{REF} = 19.44 MHz; f_{OUT} = 644.53 MHz; f_{LOOP} = 50 Hz; HSTL and/or LVDS Driver					
Bandwidth: 5 kHz to 20 MHz		334		fs rms	
Bandwidth: 12 kHz to 20 MHz		321		fs rms	
Bandwidth: 20 kHz to 80 MHz		319		fs rms	
Bandwidth: 50 kHz to 80 MHz		277		fs rms	
Bandwidth: 16 MHz to 320 MHz		185		fs rms	
f_{REF} = 19.44 MHz; f_{OUT} = 693.48 MHz; f_{LOOP} = 50 Hz; HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		298		fs rms	
Bandwidth: 12 kHz to 20 MHz		285		fs rms	
Bandwidth: 20 kHz to 80 MHz		286		fs rms	
Bandwidth: 50 kHz to 80 MHz		252		fs rms	
Bandwidth: 16 MHz to 320 MHz		183		fs rms	
f_{REF} = 19.44 MHz; f_{OUT} = 174.703 MHz; f_{LOOP} = 1 kHz; HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		354		fs rms	
Bandwidth: 12 kHz to 20 MHz		301		fs rms	
Bandwidth: 20 kHz to 80 MHz		321		fs rms	
Bandwidth: 50 kHz to 80 MHz		290		fs rms	
Bandwidth: 4 MHz to 80 MHz		177		fs rms	
f_{REF} = 19.44 MHz; f_{OUT} = 174.703 MHz; f_{LOOP} = 100 Hz; LVDS and/or 3.3 V CMOS Driver					
Bandwidth: 5 kHz to 20 MHz		306		fs rms	
Bandwidth: 12 kHz to 20 MHz		293		fs rms	
Bandwidth: 20 kHz to 80 MHz		313		fs rms	
Bandwidth: 50 kHz to 80 MHz		283		fs rms	
Bandwidth: 4 MHz to 80 MHz		166		fs rms	
f_{REF} = 25 MHz; f_{OUT} = 161.1328 MHz; f_{LOOP} = 100 Hz; HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		316		fs rms	
Bandwidth: 12 kHz to 20 MHz		302		fs rms	
Bandwidth: 20 kHz to 80 MHz		324		fs rms	
Bandwidth: 50 kHz to 80 MHz		292		fs rms	
Bandwidth: 4 MHz to 80 MHz		171		fs rms	
f_{REF} = 2 kHz; f_{OUT} = 70.656 MHz; f_{LOOP} = 100 Hz; HSTL and/or 3.3 V CMOS Driver					
Bandwidth: 10 Hz to 30 MHz		3.22		ps rms	
Bandwidth: 5 kHz to 20 MHz		338		fs rms	
Bandwidth: 12 kHz to 20 MHz		324		fs rms	
Bandwidth: 10 kHz to 400 kHz		278		fs rms	
Bandwidth: 100 kHz to 10 MHz		210		fs rms	
f_{REF} = 25 MHz; f_{OUT} = 1 GHz; f_{LOOP} = 500 Hz; HSTL Driver					
Bandwidth: 100 Hz to 500 MHz (Broadband)		1.71		ps rms	
Bandwidth: 12 kHz to 20 MHz		343		fs rms	
Bandwidth: 20 kHz to 80 MHz		338		fs rms	

Jitter generation (random jitter) uses 19.2 MHz TCXO for system clock input.

Table 18.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
JITTER GENERATION					System clock doubler enabled; high phase margin mode enabled; Register 0x0405 = 0x20; Register 0x0403 = 0x07; Register 0x0400 = 0x81; in cases where multiple driver types are listed, both driver types were tested at those conditions, and the one with higher jitter is quoted, although there is usually not a significant jitter difference between the driver types
f_{REF} = 19.44 MHz; f_{OUT} = 644.53 MHz; f_{LOOP} = 0.1 Hz; HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		402		fs rms	
Bandwidth: 12 kHz to 20 MHz		393		fs rms	
Bandwidth: 20 kHz to 80 MHz		391		fs rms	
Bandwidth: 50 kHz to 80 MHz		347		fs rms	
Bandwidth: 16 MHz to 320 MHz		179		fs rms	
f_{REF} = 19.44 MHz; f_{OUT} = 693.48 MHz; f_{LOOP} = 0.1 Hz; HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		379		fs rms	
Bandwidth: 12 kHz to 20 MHz		371		fs rms	
Bandwidth: 20 kHz to 80 MHz		371		fs rms	
Bandwidth: 50 kHz to 80 MHz		335		fs rms	
Bandwidth: 16 MHz to 320 MHz		175		fs rms	
f_{REF} = 19.44 MHz; f_{OUT} = 312.5 MHz; f_{LOOP} = 0.1 Hz; HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		413		fs rms	
Bandwidth: 12 kHz to 20 MHz		404		fs rms	
Bandwidth: 20 kHz to 80 MHz		407		fs rms	
Bandwidth: 50 kHz to 80 MHz		358		fs rms	
Bandwidth: 4 MHz to 80 MHz		142		fs rms	
f_{REF} = 25 MHz; f_{OUT} = 161.1328 MHz; f_{LOOP} = 0.1 Hz; HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		399		fs rms	
Bandwidth: 12 kHz to 20 MHz		391		fs rms	
Bandwidth: 20 kHz to 80 MHz		414		fs rms	
Bandwidth: 50 kHz to 80 MHz		376		fs rms	
Bandwidth: 4 MHz to 80 MHz		190		fs rms	
f_{REF} = 2 kHz; f_{OUT} = 70.656 MHz; f_{LOOP} = 0.1 Hz; HSTL and/or 3.3 V CMOS Driver					
Bandwidth: 10 Hz to 30 MHz		970		fs rms	
Bandwidth: 12 kHz to 20 MHz		404		fs rms	
Bandwidth: 10 kHz to 400 kHz		374		fs rms	
Bandwidth: 100 kHz to 10 MHz		281		fs rms	

ABSOLUTE MAXIMUM RATINGS

Table 19.

Parameter	Rating
Analog Supply Voltage (AVDD)	2 V
Digital Supply Voltage (DVDD)	2 V
Digital I/O Supply Voltage (DVDD3)	3.6 V
Analog Supply Voltage (AVDD3)	3.6 V
Maximum Digital Input Voltage	−0.5 V to DVDD3 + 0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Maximum Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

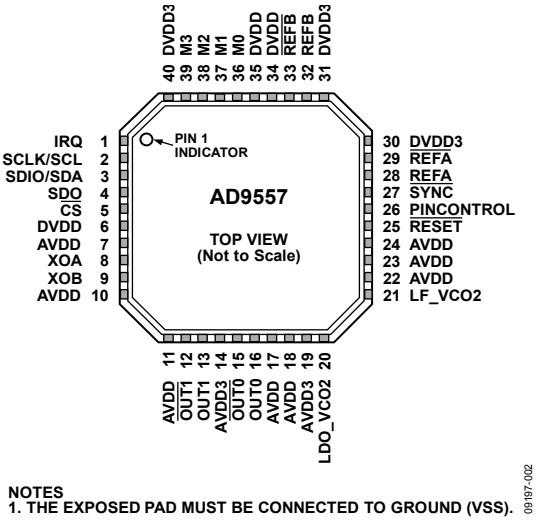

Figure 2. Pin Configuration

Table 20. Pin Function Descriptions

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
1	IRQ	O	3.3 V CMOS	Interrupt Request Line.
2	SCLK/SCL	I	3.3 V CMOS	Serial Programming Clock (SCLK) in SPI Mode. Data clock for serial programming. Open-Collector Serial Clock Pin (SCL) in I²C Mode. Requires a pull-up resistor, usually 2.2 kΩ; the resistor size depends on the number of I²C devices on the bus.
3	SDIO/SDA	I/O	3.3 V CMOS	Serial Data Input/Output (SDIO) in SPI Mode. When the device is in 4-wire SPI mode, data is written via this pin. In 3-wire SPI mode, both data reads and writes occur on this pin. There is no internal pull-up/pull-down resistor on this pin. Open-Collector Serial Data Pin (SDA) in I²C Mode. Requires a pull-up resistor, usually 2.2 kΩ; the resistor size depends on the number of I²C devices on the bus.
4	SDO	O	3.3 V CMOS	Serial Data Output. Use this pin to read data in 4-wire mode. There is no internal pull-up/pull-down resistor on this pin. This pin is high impedance in the default 3-wire mode.
5	$\overline{CS}$	I	3.3 V CMOS	Chip Select (SPI), Active Low. When programming a device, this pin must be held low. In systems where more than one AD9557 is present, this pin enables individual programming of each AD9557. This pin has an internal 10 kΩ pull-up resistor.
6, 34, 35	DVDD	I	Power	1.8 V Digital Supply.
7	AVDD	I	Power	1.8 V Analog (SYSCLK) Power Supply.
8	XOA	I	Differential input	System Clock Input. XOA contains internal dc biasing. It is recommended to ac couple XOA with a 0.01 µF capacitor, except when using a crystal. If a crystal is used, connect the crystal across XOA and XOB. Single-ended 1.8 V CMOS is also an option but can introduce a spur if the duty cycle is not 50%. When using XOA as a single-ended input, connect a 0.01 µF capacitor from XOB to ground.
9	XOB	I	Differential input	Complementary System Clock Input. Complementary signal to XOA. XOB contains internal dc biasing. It is recommended to ac couple XOB with a 0.01 µF capacitor, except when using a crystal. If a crystal is used, connect the crystal across XOA and XOB.
10, 22, 23, 24	AVDD	I	Power	1.8 V Analog Power Supply.
11, 17, 18	AVDD	I	Power	1.8 V Analog (Output Divider and Drivers) Power Supply.
12	$\overline{OUT1}$	O	HSTL, LVDS, or 1.8 V CMOS	Complementary Output 1. This output can be configured as HSTL, LVDS, or single-ended 1.8 V CMOS.

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
13	OUT1	O	HSTL, LVDS, or 1.8 V CMOS	Output 1. This output can be configured as HSTL, LVDS, or single-ended 1.8 V CMOS. LVPECL levels can be achieved by ac coupling and using the Thevenin-equivalent termination as described in the Input/Output Termination Recommendations section.
14, 19	AVDD3	I	Power	3.3 V Analog Power Supply.
15	$\overline{\text{OUT0}}$	O	HSTL, LVDS, 1.8 V CMOS, 3.3 V CMOS	Complementary Output 0. This output can be configured as HSTL, LVDS, or single-ended 1.8 V or 3.3 V CMOS.
16	OUT0	O	HSTL, LVDS, 1.8 V CMOS, 3.3 V CMOS	Output 0. This output can be configured as HSTL, LVDS, or single-ended 1.8 V or 3.3 V CMOS. LVPECL levels can be achieved by ac coupling and using the Thevenin-equivalent termination as described in the Input/Output Termination Recommendations section.
20	LDO_VCO2	I	LDO bypass	Output PLL Loop Filter Voltage Regulator. Connect a 0.47 µF capacitor from this pin to ground. This pin is also the ac ground reference for the integrated output PLL external loop filter.
21	LF_VCO2	I/O	Loop filter	Loop Filter Node for the Output PLL. Connect an external 6.8 nF capacitor from this pin to Pin 20 (LDO_VCO2).
25	$\overline{\text{RESET}}$	I	3.3 V CMOS	Chip Reset. When this active low pin is asserted, the chip goes into reset. This pin has an internal 50 kΩ pull-up resistor.
26	PINCONTROL	I	3.3 V CMOS	Pin Program Mode Enable Pin. When pulled high during startup, this pin enables pin programming of the AD9557 configuration during startup. If this pin is low during startup, the user must program the device via the serial port or use values that are stored in the EEPROM.
27	$\overline{\text{SYNC}}$	I	3.3 V CMOS	Clock Distribution Synchronization Pin. When this pin is activated, output drivers are held static and then synchronized on a low-to-high transition of this pin. This pin has an internal 60 kΩ pull-up resistor.
28	REFA	I	Differential input	Reference A Input. This internally biased input is typically ac-coupled and, when configured as such, can accept any differential signal with single-ended swing up to 3.3 V. If dc-coupled, this input can be LVPECL, LVDS, or single-ended CMOS.
29	$\overline{\text{REFA}}$	I	Differential input	Complementary Reference A Input. This pin is the complementary input to Pin 28.
30, 31, 40	DVDD3	I	Power	3.3 V Digital Power Supply.
32	REFB	I	Differential input	Reference B Input. This internally biased input is typically ac-coupled and, when configured as such, can accept any differential signal with single-ended swing up to 3.3 V. If dc-coupled, this input can be LVPECL, LVDS, or single-ended CMOS.
33	$\overline{\text{REFB}}$	I	Differential input	Complementary Reference B Input. This pin is the complementary input to Pin 32.
36, 37, 38, 39	M0, M1, M2, M3	I/O	3.3 V CMOS (3-level logic at startup)	Configurable I/O Pins. These pins are 3-level logic at startup and are used for pin strapping the input and output frequency configuration at startup. Setting Register 0x0200, Bit 0 = 1 changes these pins to 2-level logic and allows these pins to be used for status and control of the AD9557. These pins have both a 30 kΩ pull-up resistor and a 30 kΩ pull-down resistor.
	EP	O	Exposed pad	The exposed pad must be connected to ground (VSS).

TYPICAL PERFORMANCE CHARACTERISTICS

f_R = input reference clock frequency; f_{OUT} = output clock frequency; f_{SYS} = SYSCLK input frequency; f_S = internal system clock frequency; LF = SYSCLK PLL internal loop filter used. AVDD, AVDD3, and DVDD at nominal supply voltage; f_S = 786.432 MHz, unless otherwise noted.

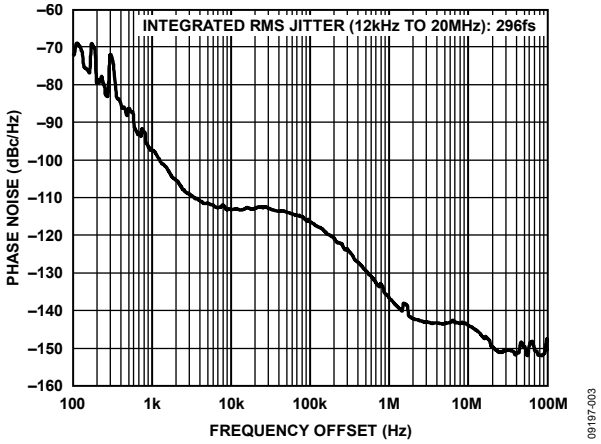

Figure 3. Absolute Phase Noise (Output Driver = HSTL), f_R = 19.44 MHz, f_{OUT} = 622.08 MHz, DPLL Loop BW = 50 Hz, f_{SYS} = 49.152 MHz Crystal

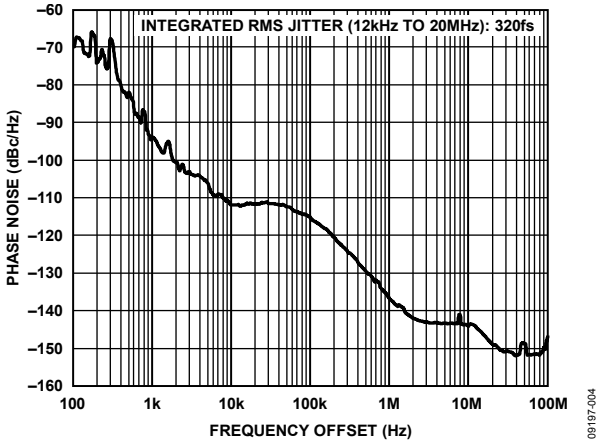

Figure 4. Absolute Phase Noise (Output Driver = HSTL), f_R = 19.44 MHz, f_{OUT} = 644.53125 MHz, DPLL Loop BW = 50 Hz, f_{SYS} = 49.152 MHz Crystal

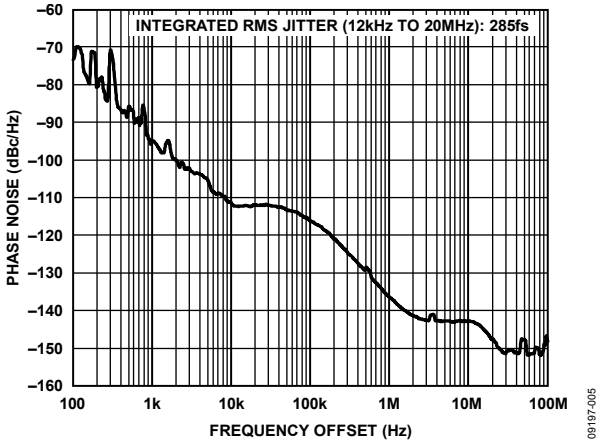

Figure 5. Absolute Phase Noise (Output Driver = HSTL), f_R = 19.44 MHz, f_{OUT} = 693.482991 MHz, DPLL Loop BW = 50 Hz, f_{SYS} = 49.152 MHz Crystal

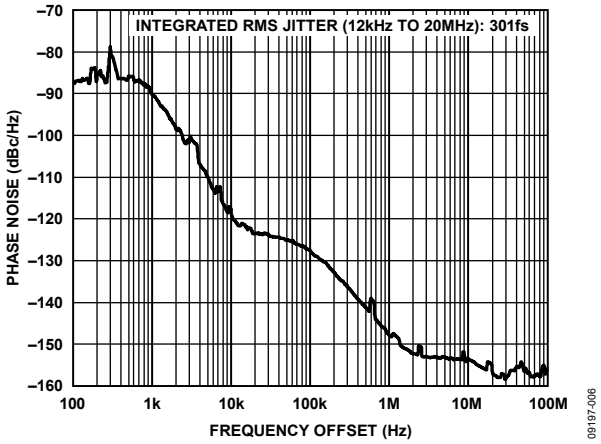

Figure 6. Absolute Phase Noise (Output Driver = HSTL), f_R = 19.44 MHz, f_{OUT} = 174.703 MHz, DPLL Loop BW = 1 kHz, f_{SYS} = 49.152 MHz Crystal

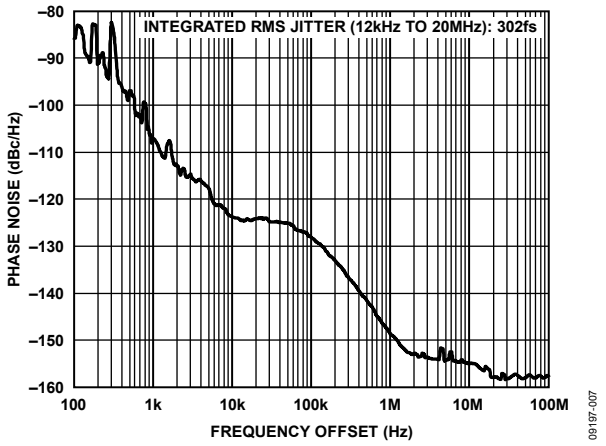

Figure 7. Absolute Phase Noise (Output Driver = 3.3.V CMOS), f_R = 19.44 MHz, f_{OUT} = 161.1328125 MHz, DPLL Loop BW = 100 Hz, f_{SYS} = 49.152 MHz Crystal

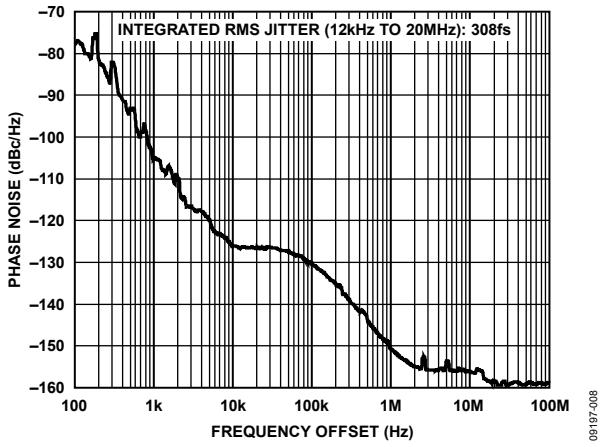

Figure 8. Absolute Phase Noise (Output Driver = HSTL), f_R = 2 kHz, f_{OUT} = 125 MHz, DPLL Loop BW = 100 Hz, f_{SYS} = 49.152 MHz Crystal

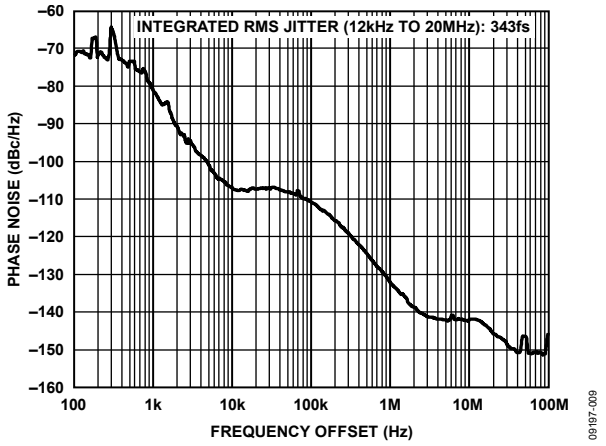

Figure 9. Absolute Phase Noise (Output Driver = HSTL), f_R = 25 MHz, f_{OUT} = 1 GHz, DPLL Loop BW = 500 Hz, f_{SYS} = 49.152 MHz Crystal

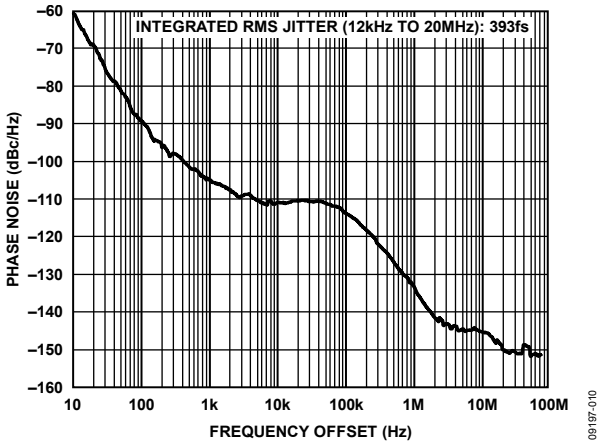

Figure 10. Absolute Phase Noise (Output Driver = HSTL), f_R = 19.44 MHz, f_{OUT} = 644.53 MHz, DPLL Loop BW = 0.1 Hz, f_{SYS} = 19.2 MHz TCXO

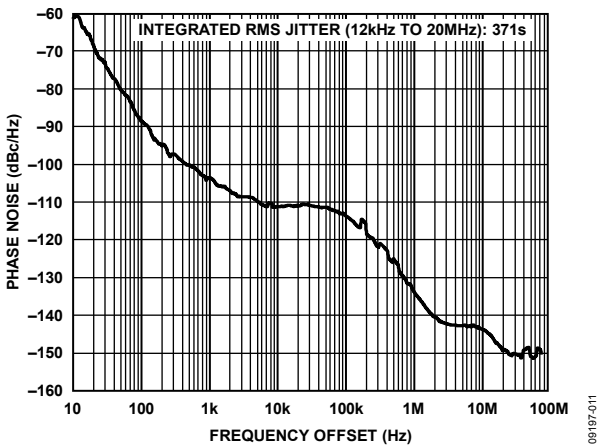

Figure 11. Absolute Phase Noise (Output Driver = HSTL), f_R = 19.44 MHz, f_{OUT} = 693.482991 MHz, DPLL Loop BW = 0.1 Hz, f_{SYS} = 19.2 MHz TCXO

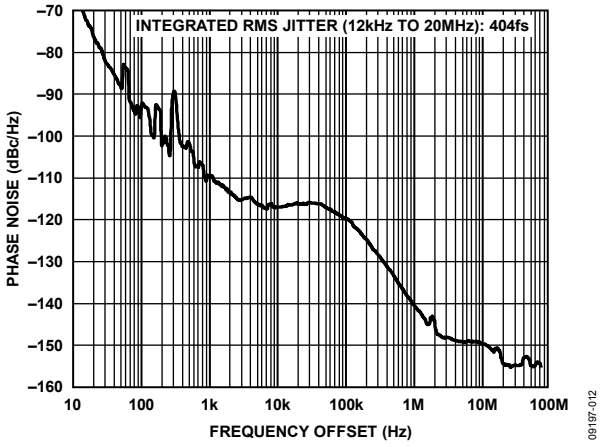

Figure 12. Absolute Phase Noise (Output Driver = HSTL), f_R = 19.44 MHz, f_{OUT} = 312.5 MHz, DPLL Loop BW = 0.1 Hz, f_{SYS} = 19.2 MHz TCXO

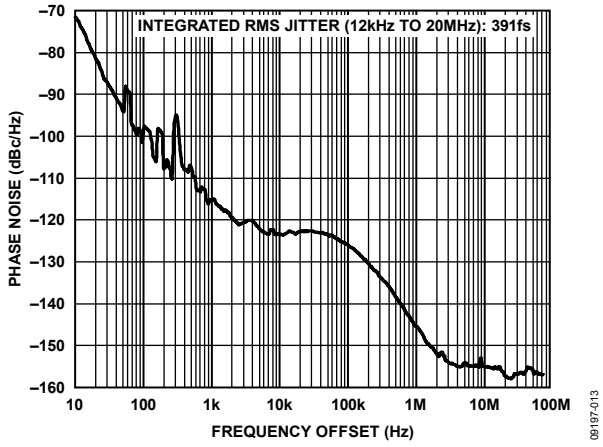

Figure 13. Absolute Phase Noise (Output Driver = 3.3 V CMOS), f_R = 19.44 MHz, f_{OUT} = 161.1328125 MHz, DPLL Loop BW = 0.1 Hz, f_{SYS} = 19.2 MHz TCXO

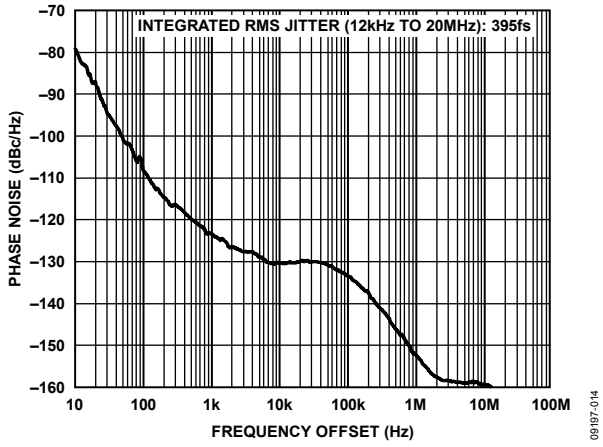

Figure 14. Absolute Phase Noise (Output Driver = 1.8 V CMOS), f_R = 2 kHz, f_{OUT} = 70.656 MHz, DPLL Loop BW = 0.1 Hz, f_{SYS} = 19.2 MHz TCXO

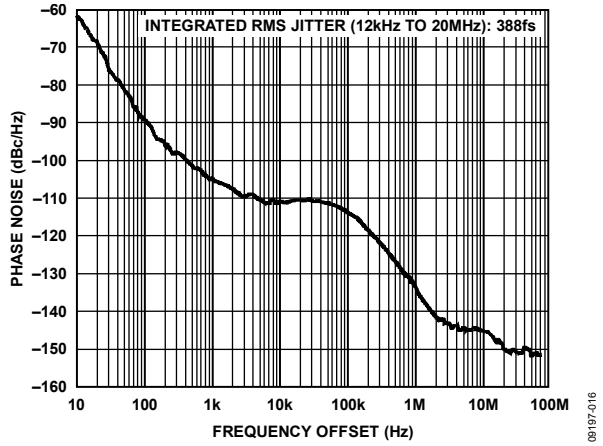

Figure 15. Absolute Phase Noise (Output Driver = HSTL), f_R = 19.44 MHz, f_{OUT} = 644.53 MHz, f_{SYS} = 19.2 MHz TCXO, Holdover Mode

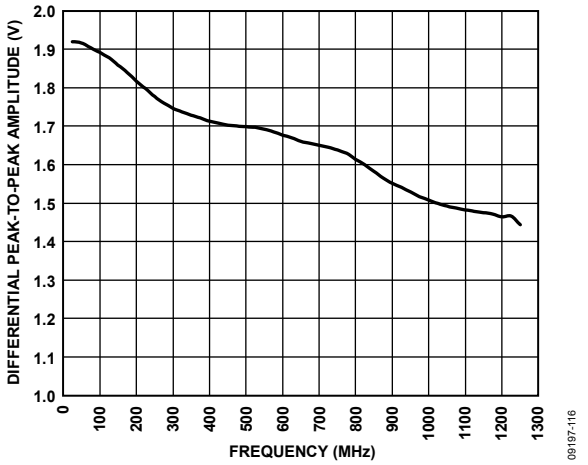

Figure 16. Amplitude vs. Toggle Rate, HSTL Mode (LVPECL-Compatible Mode)

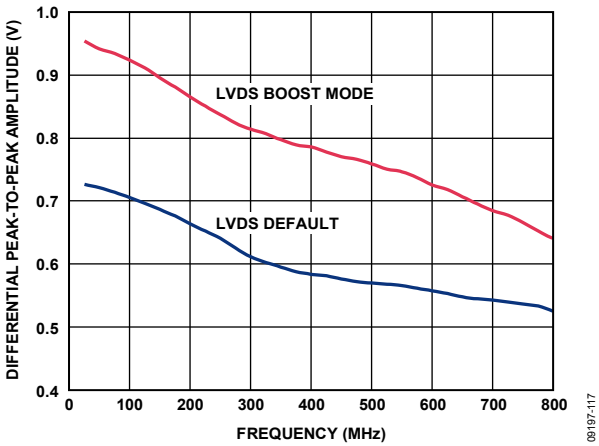

Figure 17. Amplitude vs. Toggle Rate, LVDS

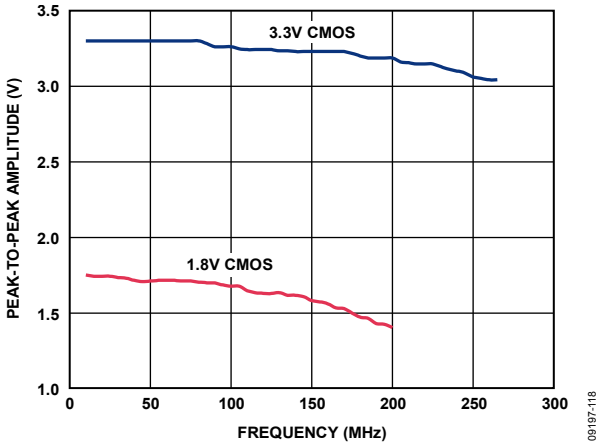

Figure 18. Amplitude vs. Toggle Rate with 10 pF Load, 3.3 V (Strong Mode) and 1.8 V CMOS

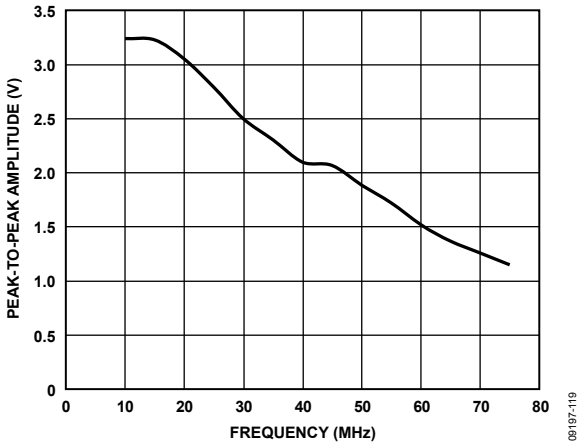

Figure 19. Amplitude vs. Toggle Rate with 10 pF Load, 3.3 V (Weak Mode) CMOS

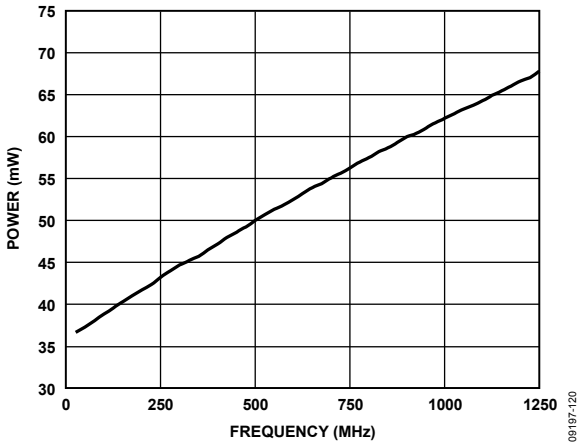

Figure 20. Power Consumption vs. Frequency, HSTL Mode on Output Driver Power Supply Only (Pin 11 and Pin 17)

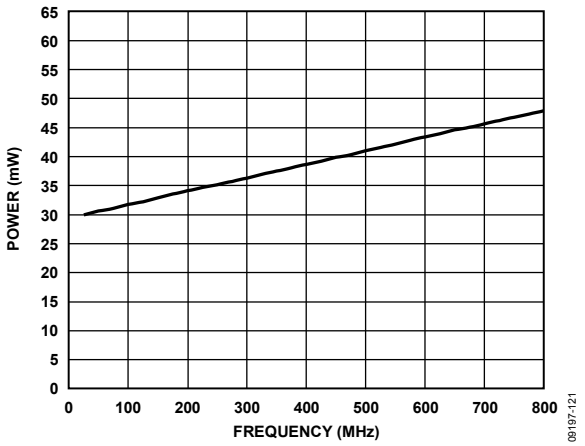

Figure 21. Power Consumption vs. Frequency, LVDS Mode on Output Driver Power Supply Only (Pin 11 and Pin 17)

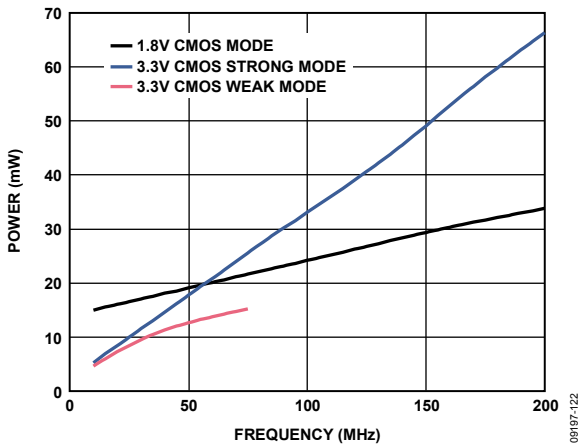

Figure 22. Power Consumption vs. Frequency, CMOS Mode on Output Driver Power Supply Only (Pin 11 and Pin 17) for 1.8 V CMOS Mode or on Pin 19 for 3.3 V CMOS Mode, One CMOS Driver

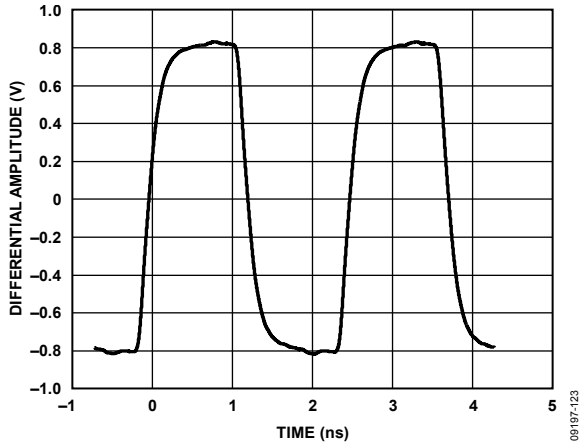

Figure 23. Output Waveform, HSTL (400 MHz)

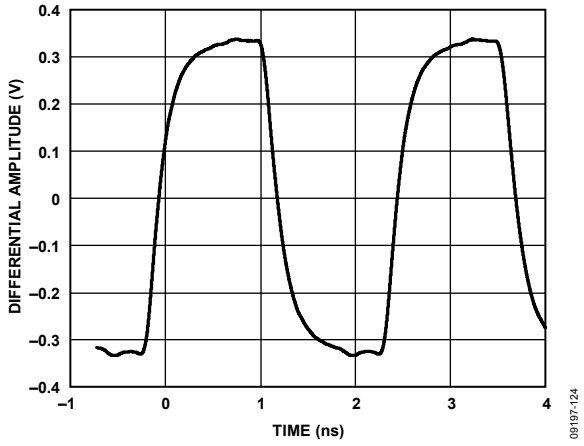

Figure 24. Output Waveform, LVDS (400 MHz)

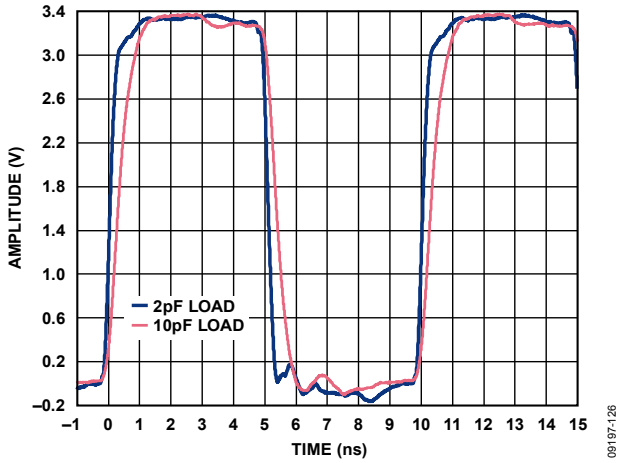

Figure 25. Output Waveform, 3.3 V CMOS (100 MHz, Strong Mode)

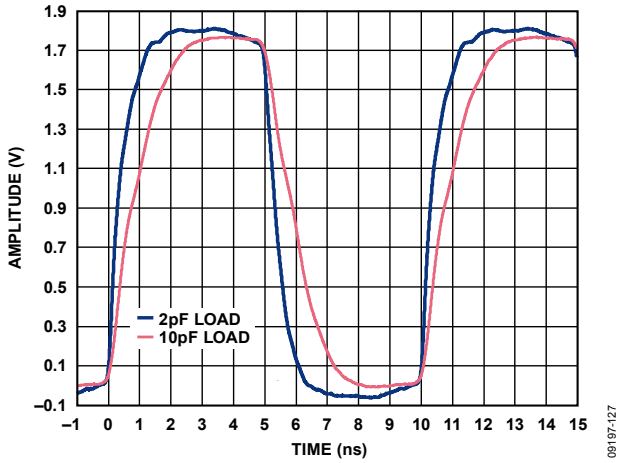

Figure 26. Output Waveform, 1.8 V CMOS (100 MHz)

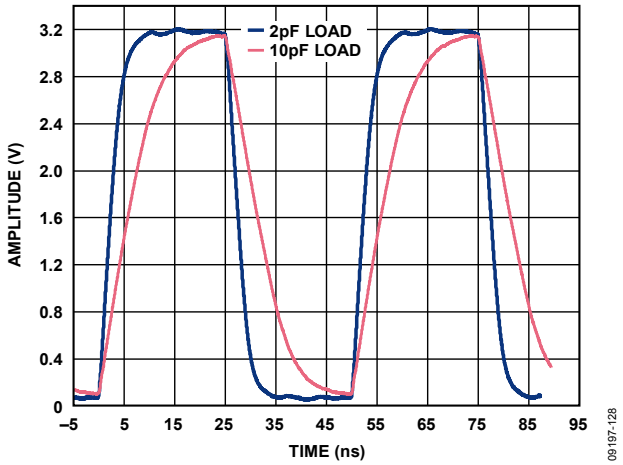

Figure 27. Output Waveform, 3.3 V CMOS (20 MHz, Weak Mode)

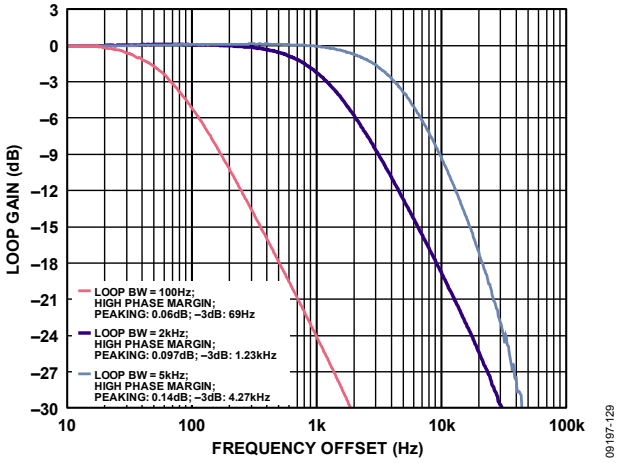

Figure 28. Closed-Loop Transfer Function for 100 Hz, 2 kHz, and 5 kHz Loop Bandwidth Settings; High Phase Margin Loop Filter Setting (Compliant with Telcordia GR-253 Jitter Transfer Test for Loop Bandwidths < 2 kHz)

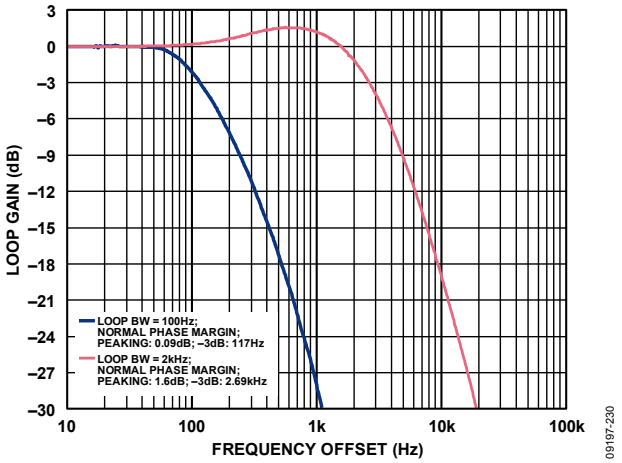

Figure 29. Closed-Loop Transfer Function for 100 Hz and 2 kHz Loop Bandwidth Settings; Normal Phase Margin Loop Filter Setting