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Dual PLL, Quad Input, Multiservice Line Card Adaptive Clock Translator

Data Sheet **AD9559**

FEATURES

- Supports GR-1244 Stratum 3 stability in holdover mode
- Supports smooth reference switchover with virtually no disturbance on output phase
- Supports Telcordia GR-253 jitter generation, transfer, and tolerance for SONET/SDH up to OC-192 systems
- Supports ITU-T G.8262 synchronous Ethernet slave clocks
- Supports ITU-T G.823, G.824, G.825, and G.8261
- Auto/manual holdover and reference switchover
- Adaptive clocking allows dynamic adjustment of feedback dividers for use in OTN mapping/demapping applications
- Dual digital PLL architecture with four reference inputs (single-ended or differential)
- 4x2 crosspoint allows any reference input to drive either PLL
- Input reference frequencies from 2 kHz to 1250 MHz
- Reference validation and frequency monitoring (2 ppm)
- Programmable input reference switchover priority
- 20-bit programmable input reference divider
- 4 pairs of clock output pins with each pair configurable as a single differential LVDS/HSTL output or as 2 single-ended CMOS outputs
- Output frequencies: 262 kHz to 1250 MHz
- Programmable 17-bit integer and 23-bit fractional feedback divider in digital PLL
- Programmable digital loop filter covering loop bandwidths from 0.1 Hz to 2 kHz
- Low noise system clock multiplier
- Optional crystal resonator for system clock input
- On-chip EEPROM to store multiple power-up profiles
- Pin program function for easy frequency translation configuration
- Software controlled power-down
- 72-lead (10 mm × 10 mm) LFCSP package

APPLICATIONS

- Network synchronization, including synchronous Ethernet and SDH to OTN mapping/demapping
- Cleanup of reference clock jitter
- SONET/SDH clocks up to OC-192, including FEC
- Stratum 3 holdover, jitter cleanup, and phase transient control
- Wireless base station controllers
- Cable infrastructure
- Data communications

GENERAL DESCRIPTION

The AD9559 is a low loop bandwidth clock multiplier that provides jitter cleanup and synchronization for many systems, including synchronous optical networks (SONET/SDH). The AD9559 generates an output clock synchronized to up to four external input references. The digital PLL allows for reduction of input time jitter or phase noise associated with the external references. The digitally controlled loop and holdover circuitry of the AD9559 continuously generates a low jitter output clock even when all reference inputs have failed.

The AD9559 operates over an industrial temperature range of −40°C to +85°C. If a single DPLL version of this part is needed, refer to the AD9557.

FUNCTIONAL BLOCK DIAGRAM

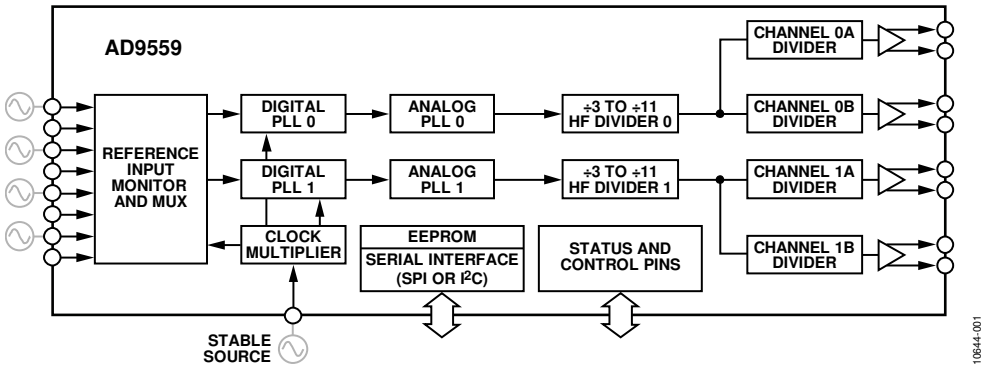

Figure 1.

Rev. C
Document Feedback

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- AD9559 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9559: Dual PLL, Quad Input, Multiservice Line Card Adaptive Clock Translator Data Sheet

TOOLS AND SIMULATIONS

- AD9559 IBIS Model

REFERENCE MATERIALS

Press

- Dual Adaptive Clock Translator Supports Wide Range of Wired Network Applications including OTN De-mapping and High-density Line Cards

Product Selection Guide

- RF Source Booklet

DESIGN RESOURCES

- AD9559 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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View all AD9559 EngineerZone Discussions.

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SPECIFICATIONS

Minimum (min) and maximum (max) values apply for the full range of supply voltage and operating temperature variations. Typical (typ) values apply for VDD3 = 3.3 V; VDD = 1.8 V; T_A= 25°C, unless otherwise noted.

SUPPLY VOLTAGE

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
VDD3	3.135	3.30	3.465	V	
VDD	1.71	1.80	1.89	V	

SUPPLY CURRENT

The test conditions for the maximum (max) supply current are at the maximum supply voltage found in Table 1.
The test conditions for the typical (typ) supply current are at the typical supply voltage found in Table 1.
The test conditions for the minimum (min) supply current are at the minimum supply voltage found in Table 1.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT FOR TYPICAL CONFIGURATION					Typical values are for the Typical Configuration parameter listed in Table 3
I_{VDD3}	34	42	50	mA	
I_{VDD}	253	316	380	mA	
SUPPLY CURRENT FOR ALL BLOCKS RUNNING CONFIGURATION					Maximum values are for the All Blocks Running parameter listed in Table 3
I_{VDD3}	75	94	113	mA	
I_{VDD}	256	320	384	mA	

POWER DISSIPATION

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION					
Typical Configuration	0.57	0.71	0.85	W	System clock: 49.152 MHz crystal; two DPLLs active; two 19.44 MHz input references in differential mode; two HSTL drivers at 644.53125 MHz; two 3.3 V CMOS drivers at 161.1328125 MHz and 80 pF capacitive load on CMOS output
All Blocks Running	0.71	0.89	1.1	W	System clock: 49.152 MHz crystal; two DPLLs active, all input references in differential mode; two HSTL drivers at 750 MHz; four 3.3 V CMOS drivers at 250 MHz and 80 pF capacitive load on CMOS outputs
Full Power-Down		75	110	mW	Typical configuration with no external pull-up or pull-down resistors; about 2/3 of this power is on VDD3
Incremental Power Dissipation					Typical configuration; table values show the change in power due to the indicated operation
Complete DPLL/APLL On/Off	171	214	257	mW	This power delta is computed relative to the typical configuration; the blocks powered down include one reference input, one DPLL, one APLL, one P divider, two channel dividers, one HSTL driver, and one CMOS driver; roughly 2/3 of the power savings is on the 1.8 V supply
Input Reference On/Off					
Differential Without Divide-by-2	19	25	31	mW	Additional current draw is in the VDD3 domain only
Differential With Divide-by-2	25	32	39	mW	Additional current draw is in the VDD3 domain only
Single-Ended (Without Divide-by-2)	5	6.6	8	mW	Additional current draw is in the VDD3 domain only
Output Distribution Driver On/Off					
LVDS (at 750 MHz)	12	17	22	mW	Additional current draw is in the VDD domain only
HSTL (at 750 MHz)	14	21	28	mW	Additional current draw is in the VDD domain only
1.8 V CMOS (at 250 MHz)	14	21	28	mW	A single 1.8 V CMOS output with an 80 pF load
3.3 V CMOS (at 250 MHz)	18	27	36	mW	A single 3.3 V CMOS output with an 80 pF load

SYSTEM CLOCK INPUTS (XOA, XOB)

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SYSTEM CLOCK MULTIPLIER					
PLL Output Frequency Range	750		805	MHz	VCO range may place limitations on nonstandard system clock input frequencies
Phase Frequency Detector (PFD) Rate			150	MHz	
Frequency Multiplication Range	4		255		Assumes valid system clock and PFD rates
SYSTEM CLOCK REFERENCE INPUT PATH					
Input Frequency Range	10		400	MHz	
Minimum Input Slew Rate	50			V/µs	Minimum limit imposed for jitter performance; jitter performance affected if sine wave input ≤ 20 MHz
Common-Mode Voltage	1.05	1.16	1.27	V	Internally generated
Differential Input Voltage Sensitivity	250			mV p-p	Minimum voltage across pins required to ensure switching between logic states; the instantaneous voltage on either pin must not exceed supply rails; single-ended input can be accommodated by ac grounding complementary input; 1 V p-p recommended for optimal jitter performance
System Clock Input Doubler Duty Cycle					Amount of duty cycle variation that can be tolerated on the system clock input to use the doubler
System Clock input = 50 MHz	45	50	55	%	
System Clock input = 20 MHz	46	50	54	%	
System Clock input = 16 MHz to 20 MHz	47	50	53	%	
Input Capacitance		3		pF	Single-ended, each pin
Input Resistance		4.1		kΩ	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CRYSTAL RESONATOR PATH					
Crystal Resonator Frequency Range	10		50	MHz	Fundamental mode, AT cut crystal
Maximum Crystal Motional Resistance			100	Ω	

REFERENCE INPUTS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL OPERATION					
Frequency Range					The reference input divide-by-2 block must be engaged for f_{IN} > 705 MHz
Sinusoidal Input	10		750	MHz	
LVPECL Input	0.002		1250	MHz	
LVDS Input	0.002		750	MHz	
Minimum Input Slew Rate	40			V/µs	Minimum limit imposed for jitter performance
Common-Mode Input Voltage					
AC-Coupled	1.9	2	2.1	V	Internally generated
DC-Coupled	1.0		2.4	V	
Differential Input Voltage Sensitivity				mV	Minimum differential voltage across pins required to ensure switching between logic levels; instantaneous voltage on either pin must not exceed the supply rails
f_{IN} < 800 MHz	240			mV	
f_{IN} = 800 MHz to 1050 MHz	320			mV	
f_{IN} = 1050 MHz to 1250 MHz	400			mV	
Differential Input Voltage Hysteresis		55	100	mV	
Input Resistance		21		kΩ	
Input Capacitance		3		pF	
Minimum Pulse Width High					
LVPECL	390			ps	
LVDS	640			ps	
Minimum Pulse Width Low					
LVPECL	390			ps	
LVDS	640			ps	
SINGLE-ENDED OPERATION					
Frequency Range (CMOS)	0.002		300	MHz	
Minimum Input Slew Rate	40			V/µs	Minimum limit imposed for jitter performance
Input Voltage High (V_{IH})					
1.2 V to 1.5 V Threshold Setting	1.0			V	
1.8 V to 2.5 V Threshold Setting	1.4			V	
3.0 V to 3.3 V Threshold Setting	2.0			V	
Input Voltage Low (V_{IL})					
1.2 V to 1.5 V Threshold Setting			0.35	V	
1.8 V to 2.5 V Threshold Setting			0.5	V	
3.0 V to 3.3 V Threshold Setting			1.0	V	
Input Resistance		47		kΩ	
Input Capacitance		3		pF	
Minimum Pulse Width High	1.5			ns	
Minimum Pulse Width Low	1.5			ns	

REFERENCE MONITORS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE MONITORS					
Reference Monitor					
Loss of Reference Detection Time			1.15	DPLL PFD period	Nominal phase detector period = R/f_{REF}[1]
Frequency Out-of Range Limits	2		10^5	$\Delta f/f_{REF}$ (ppm)	Programmable (lower bound subject to quality of the system clock (SYSCLK)); SYSCLK accuracy must be less than the lower bound
Validation Timer	0.001		65.535	sec	Programmable in 1 ms increments

[1] f_{REF} is the frequency of the active reference; R is the frequency division factor determined by the R divider.

REFERENCE SWITCHOVER SPECIFICATIONS

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE SWITCHOVER SPECIFICATIONS					Assumes a jitter-free reference; satisfies Telcordia GR-1244-CORE requirements; base loop filter selection bit set to 1b for all active references
Maximum Output Phase Perturbation (Phase Build-Out Switchover)					
50 Hz DPLL Loop Bandwidth					Test conditions: 19.44 MHz to 174.70308 MHz; DPLL BW = 50 Hz; 49.152 MHz signal generator used for system clock source
Peak		±55	±100	ps	
Steady State		±55	±100	ps	
Time Required to Switch to a New Reference					
Phase Build-Out Switchover			10	DPLL PFD period	Calculated using the nominal phase detector period (NPDP = R/f_{REF}); the total time required is the time plus the reference validation time, plus the time required to lock to the new reference

DISTRIBUTION CLOCK OUTPUTS

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL MODE					
Output Frequency					
OUT0A, $\overline{\text{OUT0A}}$ and OUT0B, $\overline{\text{OUT0B}}$	0.262		1250	MHz	
OUT1A, $\overline{\text{OUT1A}}$ and OUT1B, $\overline{\text{OUT1B}}$	0.302		1250	MHz	
Rise/Fall Time (20% to 80%)[1]		140	250	ps	100 Ω termination across the output pair
Duty Cycle					
Up to f_{OUT} = 700 MHz	44	48	53	%	
Up to f_{OUT} = 750 MHz	43	48	54	%	
Up to f_{OUT} = 1250 MHz		43		%	
Differential Output Voltage Swing	700	925	1200	mV	Magnitude of voltage across pins; output driver static
Common-Mode Output Voltage	750	850	1000	mV	Output driver static
Reference Input-to-Output Delay Variation over Temperature		3.2		ps/°C	HSTL mode; DPLL locked to same input reference at all times; stable system clock source (non-XTAL)
Static Phase Offset Variation from Active Reference to Output over Voltage Extremes		0.875		ps/mV	Valid for HSTL, LVDS, and 1.8 V CMOS output driver modes
LVDS MODE					
Output Frequency					
OUT0A, $\overline{\text{OUT0A}}$ and OUT0B, $\overline{\text{OUT0B}}$	0.262		1250	MHz	
OUT1A, $\overline{\text{OUT1A}}$ and OUT1B, $\overline{\text{OUT1B}}$	0.302		1250	MHz	
Rise/Fall Time (20% to 80%)[1]		185	280	ps	100 Ω termination across the output pair
Duty Cycle					
Up to f_{OUT} = 750 MHz	43	48	53	%	
Up to f_{OUT} = 800 MHz	42.5	48	53.5	%	
Up to f_{OUT} = 1250 MHz		43		%	
Differential Output Voltage Swing					
Balanced, V_{OD}	247		454	mV	Voltage swing between output pins; output driver static
Unbalanced, ΔV_{OD}			50	mV	Absolute difference between voltage swing of normal pin and inverted pin; output driver static
Offset Voltage					
Common Mode, V_{OS}	1.125	1.25	1.375	V	Output driver static
Common-Mode Difference, ΔV_{OS}			50	mV	Voltage difference between pins; output driver static
Short-Circuit Output Current		10	24	mA	Output driver static
CMOS MODE					
Output Frequency					
1.8 V Supply					
OUT0A, $\overline{\text{OUT0A}}$ and OUT0B, $\overline{\text{OUT0B}}$	0.262		250	MHz	10 pF load
OUT1A, $\overline{\text{OUT1A}}$ and OUT1B, $\overline{\text{OUT1B}}$	0.302		250	MHz	10 pF load
3.3 V Supply (OUT0A and OUT1A)					
Strong Drive Strength Setting					
OUT0A, $\overline{\text{OUT0A}}$	0.262		250	MHz	10 pF load
OUT1A, $\overline{\text{OUT1A}}$	0.302		250	MHz	10 pF load
Weak Drive Strength Setting					
OUT0A, $\overline{\text{OUT0A}}$	0.262		25	MHz	10 pF load
OUT1A, $\overline{\text{OUT1A}}$	0.302		25	MHz	10 pF load

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Rise/Fall Time (20% to 80%)[1]					
1.8 V Mode		1.5	3	ns	10 pF load
3.3 V Strong Mode		0.4	0.6	ns	10 pF load
3.3 V Weak Mode		8		ns	10 pF load
Duty Cycle					
1.8 V Mode		50		%	10 pF load
3.3 V Strong Mode	47	51	56	%	10 pF load
3.3 V Weak Mode		51		%	10 pF load
Output Voltage High (V_{OH})					Output driver static; strong drive strength
VDD3 = 3.3 V, I_{OH} = 10 mA	VDD3 − 0.3			V	
VDD3 = 3.3 V, I_{OH} = 1 mA	VDD3 − 0.1			V	
VDD3 = 1.8 V, I_{OH} = 1 mA	VDD − 0.2			V	
Output Voltage Low (V_{OL})					Output driver static; strong drive strength
VDD3 = 3.3 V, I_{OL} = 10 mA			0.3	V	
VDD3 = 3.3 V, I_{OL} = 1 mA			0.1	V	
VDD3 = 1.8 V, I_{OL} = 1 mA			0.1	V	
OUTPUT TIMING SKEW					10 pF load
Between OUT0A, $\overline{\text{OUT0A}}$ and OUT0B, $\overline{\text{OUT0B}}$ or OUT1A, $\overline{\text{OUT1A}}$ and OUT1B, $\overline{\text{OUT1B}}$		116	265	ps	HSTL mode on both drivers; rising edge only; any divide value
Additional Delay on One Driver by Changing Its Logic Type					
HSTL to LVDS	0	+15	+35	ps	Positive value indicates that the LVDS edge is delayed relative to HSTL
HSTL to 1.8 V CMOS	−5	0	+5	ps	Positive value indicates that the CMOS edge is delayed relative to HSTL
OUT0B, $\overline{\text{OUT0B}}$ HSTL to OUT0B, $\overline{\text{OUT0B}}$ 3.3 V CMOS, Strong Mode	−765	−280	+250	ns	The CMOS edge is delayed relative to HSTL
OUT1B, $\overline{\text{OUT1B}}$ HSTL to OUT1B, $\overline{\text{OUT1B}}$ 3.3 V CMOS, Strong Mode	−765	−280	+250	ns	The CMOS edge is delayed relative to HSTL

[1] The listed values are for the slower edge (rising or falling).

TIME DURATION OF DIGITAL FUNCTIONS

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TIME DURATION OF DIGITAL FUNCTIONS					
EEPROM-to-Register Download Time		16	25	ms	Uses default EEPROM storage sequence (see Register 0x0E10 to Register 0x0E4F)
Register-to-EEPROM Upload Time			180	ms	Uses default EEPROM storage sequence (see Register 0x0E10 to Register 0x0E4F
Power-Down Exit Time		1		ms	Time from power-down exit to system clock lock detect; system clock stability timer setting should be added to calculate the time needed for system clock stable

DIGITAL PLL (DPLL_0 AND DPLL_1)

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL PLL					
Phase Frequency Detector (PFD) Input Frequency Range	2		100	kHz	
Loop Bandwidth	0.1		2000	Hz	Programmable design parameter; note that (f_{PFD}/loop BW) ≥ 20
Phase Margin	45		89	Degrees	Programmable design parameter
Closed Loop Peaking	<0.1			dB	Programmable design parameter; part can be programmed for <0.1 dB peaking in accordance with Telcordia GR-253-CORE jitter transfer

ANALOG PLL (APLL_0 AND APLL_1)

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG PLL0					
VCO Frequency Range	2940		3543	MHz	
Phase Frequency Detector (PFD) Input Frequency Range		180	195	MHz	
Loop Bandwidth		240		kHz	Programmable design parameter
Phase Margin		68		Degrees	Programmable design parameter
ANALOG PLL1					
VCO Frequency Range	3405		4260	MHz	
Phase Frequency Detector (PFD) Input Frequency Range		180	195	MHz	
Loop Bandwidth		240		kHz	Programmable design parameter
Phase Margin		68		Degrees	Programmable design parameter

DIGITAL PLL LOCK DETECTION

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PHASE LOCK DETECTOR					
Threshold Programming Range	10		$2^{24} - 1$	ps	Reference-to-feedback phase difference
Threshold Resolution		1		ps	
FREQUENCY LOCK DETECTOR					
Threshold Programming Range	10		$2^{24} - 1$	ps	Reference-to-feedback period difference
Threshold Resolution		1		ps	

HOLDOVER SPECIFICATIONS

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HOLDOVER SPECIFICATIONS					
Initial Frequency Accuracy		<0.01		ppm	Excludes frequency drift of SYSCLK source; excludes frequency drift of input reference prior to entering holdover; compliant with GR-1244 Stratum 3

SERIAL PORT SPECIFICATIONS—SPI MODE

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
M5/$\overline{CS}$					M5/$\overline{CS}$ is a dual function pin; the values in this table apply when this pin is used as a serial port pin, that is, $\overline{CS}$; see Table 16 for the specifications when this pin is used as a multifunction pin (M5)
Input Logic 1 Voltage	2.2			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		20		µA	
Input Logic 0 Current		50		µA	
Input Capacitance		2		pF	
SCLK					Internal 10 kΩ pull-down resistor
Input Logic 1 Voltage	2.2			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		200		µA	
Input Logic 0 Current		1		µA	
Input Capacitance		2		pF	
SDIO					
As an Input					
Input Logic 1 Voltage	2.2			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		1		µA	
Input Logic 0 Current		1		µA	
Input Capacitance		2		pF	
As an Output					
Output Logic 1 Voltage	VDD3 – 0.6			V	1 mA load current
Output Logic 0 Voltage			0.4	V	1 mA load current
M4/SDO					M4/SDO is a dual function pin; the values in this table apply when this pin is used as a serial port pin, that is SDO; see Table 16 for the specifications when this pin is used as a multifunction pin (M4)
Output Logic 1 Voltage	VDD3 – 0.6			V	1 mA load current
Output Logic 0 Voltage			0.4	V	1 mA load current
TIMING					See Figure 47 and Figure 50
SCLK					
Clock Rate, $1/t_{CLK}$			40	MHz	
Pulse Width High, t_{HIGH}	10			ns	
Pulse Width Low, t_{LOW}	13			ns	
SDIO to SCLK Setup, t_{DS}	3			ns	
SCLK to SDIO Hold, t_{DH}	6			ns	
SCLK to Valid SDIO and SDO, t_{DV}			10	ns	
$\overline{CS}$ to SCLK Setup (t_S)	10			ns	
$\overline{CS}$ to SCLK Hold (t_C)	0			ns	
$\overline{CS}$ Minimum Pulse Width High	6			ns	

SERIAL PORT SPECIFICATIONS—I²C MODE

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDA, SCL (AS INPUTS)					
Input Logic 1 Voltage	0.7 × VDD3			V	
Input Logic 0 Voltage			0.3 × VDD3	V	
Input Current	−10		+10	µA	For V_{IN} = 10% to 90% of VDD3
Hysteresis of Schmitt Trigger Inputs	0.015 × VDD3				
Pulse Width of Spikes That Must Be Suppressed by the Input Filter, t_{SP}			50	ns	
SDA (AS OUTPUT)					
Output Logic 0 Voltage			0.4	V	I_O = 3 mA
Output Fall Time from V_{IHmin} to V_{ILmax}	20 + 0.1 C_b[1]		250	ns	10 pF ≤ C_b ≤ 400 pF
TIMING					
SCL Clock Rate			400	kHz	
Bus-Free Time Between a Stop and Start Condition, t_{BUF}	1.3			µs	
Repeated Start Condition Setup Time, $t_{SU;STA}$	0.6			µs	
Repeated Hold Time Start Condition, $t_{HD;STA}$	0.6			µs	After this period, the first clock pulse is generated
Stop Condition Setup Time, $t_{SU;STO}$	0.6			µs	
Low Period of the SCL Clock, t_{LOW}	1.3			µs	
High Period of the SCL Clock, t_{HIGH}	0.6			µs	
SCL/SDA Rise Time, t_R	20 + 0.1 C_b[1]		300	ns	
SCL/SDA Fall Time, t_F	20 + 0.1 C_b[1]		300	ns	
Data Setup Time, $t_{SU;DAT}$	100			ns	
Data Hold Time, $t_{HD;DAT}$	100			ns	
Capacitive Load for Each Bus Line, C_b[1]			400	pF	

[1] C_b is the capacitance (pF) of a single bus line.

LOGIC INPUTS ($\overline{\text{RESET}}$, M5 TO M0)

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{\text{RESET}}$ PIN					
Input High Voltage (V_{IH})	2.1			V	
Input Low Voltage (V_{IL})			0.8	V	
Input Current (I_{INH}, I_{INL})		±85	±125	µA	
Input Capacitance (C_{IN})		3		pF	
LOGIC INPUTS (M5 to M0)					The M4 and M5 pins are dual function pins; the values in this table apply when M4/SDO and M5/$\overline{\text{CS}}$ are used as M pins; see Table 14 in the Serial Port Specifications—SPI Mode section for the specifications when these pins are used as serial port pins (SDO, $\overline{\text{CS}}$)
Input High Voltage (V_{IH})	2.5			V	
Input Low Voltage (V_{IL})			0.6	V	
Input Current (I_{INH}, I_{INL})		±1	±5	µA	
Input Capacitance (C_{IN})		3		pF	

LOGIC OUTPUTS (M5 TO M0)

Table 17.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS (M5 to M0)					
Output High Voltage (V_{OH})	VDD3 − 0.4			V	I_{OH} = 1 mA
Output Low Voltage (V_{OL})			0.4	V	I_{OL} = 1 mA

JITTER GENERATION

Jitter Generation (Random Jitter)—49.152 MHz Crystal for System Clock Input

Table 18.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
JITTER GENERATION					System clock doubler enabled. High phase margin mode enabled. Both PLLs are running with same output frequency. In cases where the two PLLs have different jitter, the higher jitter is listed. When two driver types are listed, both were tested at those conditions; the driver type with higher jitter is quoted, although there is usually not a significant jitter difference between driver types.
f_{REF} = 19.44 MHz; f_{OUT} = 622.08 MHz; f_{LOOP} = 50 Hz; HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		307		fs rms	
Bandwidth: 12 kHz to 20 MHz		310		fs rms	
Bandwidth: 20 kHz to 80 MHz		313		fs rms	
Bandwidth: 50 kHz to 80 MHz		292		fs rms	
Bandwidth: 16 MHz to 320 MHz		149		fs rms	
f_{REF} = 19.44 MHz; f_{OUT} = 644.53 MHz; f_{LOOP} = 50 Hz; HSTL Driver, LVDS Driver					
Bandwidth: 5 kHz to 20 MHz		313		fs rms	
Bandwidth: 12 kHz to 20 MHz		306		fs rms	
Bandwidth: 20 kHz to 80 MHz		308		fs rms	
Bandwidth: 50 kHz to 80 MHz		286		fs rms	
Bandwidth: 16 MHz to 320 MHz		154		fs rms	
f_{REF} = 19.44 MHz; f_{OUT} = 693.48 MHz; f_{LOOP} = 50 Hz; HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		335		fs rms	
Bandwidth: 12 kHz to 20 MHz		328		fs rms	
Bandwidth: 20 kHz to 80 MHz		328		fs rms	
Bandwidth: 50 kHz to 80 MHz		298		fs rms	
Bandwidth: 16 MHz to 320 MHz		150		fs rms	
f_{REF} = 19.44 MHz; f_{OUT} = 174.703 MHz; f_{LOOP} = 1 kHz; HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		396		fs rms	
Bandwidth: 12 kHz to 20 MHz		335		fs rms	
Bandwidth: 20 kHz to 80 MHz		369		fs rms	
Bandwidth: 50 kHz to 80 MHz		347		fs rms	
Bandwidth: 4 MHz to 80 MHz		230		fs rms	
f_{REF} = 19.44 MHz; f_{OUT} = 174.703 MHz; f_{LOOP} = 100 Hz; LVDS Driver, 3.3 V CMOS Driver					
Bandwidth: 5 kHz to 20 MHz		337		fs rms	
Bandwidth: 12 kHz to 20 MHz		330		fs rms	
Bandwidth: 20 kHz to 80 MHz		354		fs rms	
Bandwidth: 50 kHz to 80 MHz		339		fs rms	
Bandwidth: 4 MHz to 80 MHz		220		fs rms	
f_{REF} = 25 MHz; f_{OUT} = 161.1328 MHz; f_{LOOP} = 100 Hz; HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		318		fs rms	
Bandwidth: 12 kHz to 20 MHz		310		fs rms	
Bandwidth: 20 kHz to 80 MHz		384		fs rms	
Bandwidth: 50 kHz to 80 MHz		361		fs rms	
Bandwidth: 4 MHz to 80 MHz		267		fs rms	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
f_{REF} = 2 kHz; f_{OUT} = 70.656 MHz; f_{LOOP} = 100 Hz; HSTL Driver, 3.3 V CMOS Driver					
Bandwidth: 10Hz to 30 MHz		6.5		ps rms	
Bandwidth: 5 kHz to 20 MHz		343		fs rms	
Bandwidth: 12 kHz to 20 MHz		335		fs rms	
Bandwidth: 10 kHz to 400 kHz		243		fs rms	
Bandwidth: 100 kHz to 10 MHz		256		fs rms	
f_{REF} = 25 MHz; f_{OUT} = 1 GHz; f_{LOOP} = 500 Hz; HSTL Driver					
Bandwidth: 100 Hz to 500 MHz (Broadband)		881		fs rms	
Bandwidth: 12 kHz to 20 MHz		331		fs rms	
Bandwidth: 20 kHz to 80 MHz		330		fs rms	

Jitter Generation (Random Jitter)—19.2 MHz TCXO for System Clock Input

Table 19.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
JITTER GENERATION					System clock doubler enabled. High phase margin mode enabled. Both PLLs are running with same output frequency. In cases where the two PLLs have different jitter, the higher jitter is listed. Where two driver types are listed, both were tested at those conditions; the driver type with higher jitter is quoted, although there is usually not a significant jitter difference between driver types.
f_{REF} = 19.44 MHz; f_{OUT} = 644.53 MHz; f_{LOOP} = 10 Hz; HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		380		fs rms	
Bandwidth: 12 kHz to 20 MHz		373		fs rms	
Bandwidth: 20 kHz to 80 MHz		373		fs rms	
Bandwidth: 50 kHz to 80 MHz		348		fs rms	
Bandwidth: 16 MHz to 320 MHz		148		fs rms	
f_{REF} = 19.44 MHz; f_{OUT} = 693.48 MHz; f_{LOOP} = 10 Hz; HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		390		fs rms	
Bandwidth: 12 kHz to 20 MHz		383		fs rms	
Bandwidth: 20 kHz to 80 MHz		382		fs rms	
Bandwidth: 50 kHz to 80 MHz		350		fs rms	
Bandwidth: 16 MHz to 320 MHz		144		fs rms	
f_{REF} = 19.44 MHz; f_{OUT} = 312.5 MHz; f_{LOOP} = 10 Hz; HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		398		fs rms	
Bandwidth: 12 kHz to 20 MHz		392		fs rms	
Bandwidth: 20 kHz to 80 MHz		400		fs rms	
Bandwidth: 50 kHz to 80 MHz		379		fs rms	
Bandwidth: 4 MHz to 80 MHz		172		fs rms	
f_{REF} = 25 MHz; f_{OUT} = 161.1328 MHz; f_{LOOP} = 10 Hz; HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		384		fs rms	
Bandwidth: 12 kHz to 20 MHz		378		fs rms	
Bandwidth: 20 kHz to 80 MHz		416		fs rms	
Bandwidth: 50 kHz to 80 MHz		396		fs rms	
Bandwidth: 4 MHz to 80 MHz		223		fs rms	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
f_{REF} = 2 kHz; f_{OUT} = 70.656 MHz; f_{LOOP} = 10 Hz; HSTL Driver, 3.3 V CMOS Driver					
Bandwidth: 10 Hz to 30 MHz		3.19		ps rms	
Bandwidth: 12 kHz to 20 MHz		418		fs rms	
Bandwidth: 10 kHz to 400 kHz		339		fs rms	
Bandwidth: 100 kHz to 10 MHz		348		fs rms	

ABSOLUTE MAXIMUM RATINGS

Table 20.

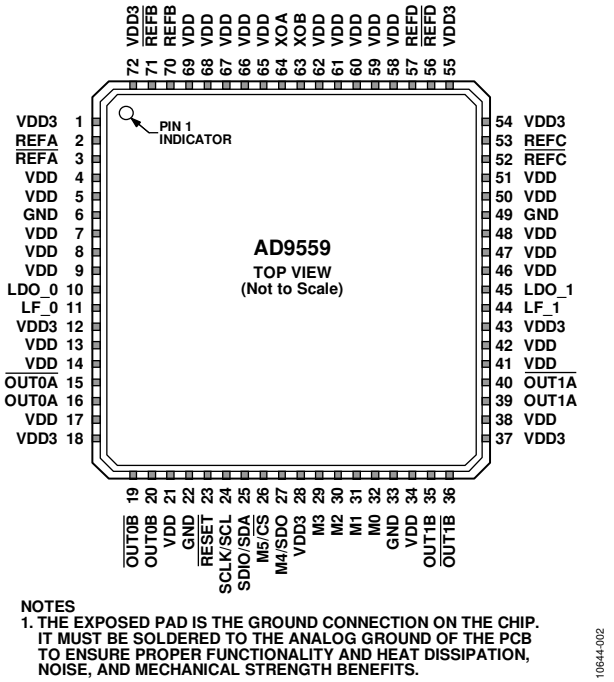
Parameter	Rating
1.8 V Supply Voltage (VDD)	2 V
3.3 V Supply Voltage (VDD3)	3.6 V
Maximum Digital Input Voltage	−0.5 V to VDD3 + 0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD IS THE GROUND CONNECTION ON THE CHIP. IT MUST BE SOLDERED TO THE ANALOG GROUND OF THE PCB TO ENSURE PROPER FUNCTIONALITY AND HEAT DISSIPATION, NOISE, AND MECHANICAL STRENGTH BENEFITS.

10644-002

Figure 2. Pin Configuration

Table 21. Pin Function Descriptions

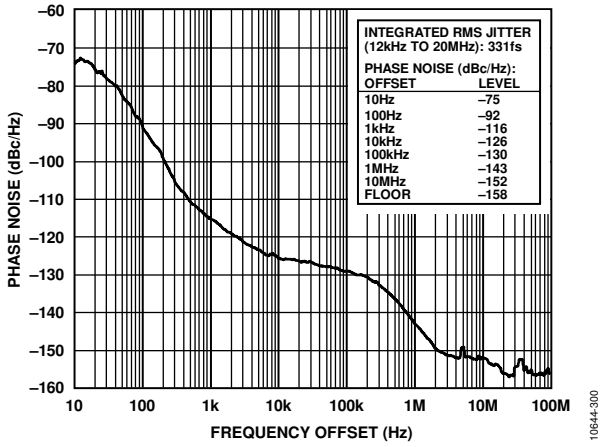
Pin No.	Mnemonic	Input/ Output	Pin Type	Description
1, 12, 18, 28, 37, 43, 54, 55, 72	VDD3	I	Power	3.3 V Power Supply. See the Power Supply Partitions section for information about the recommended grouping of the power supply pins.
2	REFA	I	Differential input	Reference A Input. This internally biased input is typically ac-coupled; when configured in this manner, it can accept any differential signal with single-ended swing up to 3.3 V. If dc-coupled, input can be LVPECL, LVDS, or single-ended CMOS.
3	$\overline{\text{REFA}}$	I	Differential input	Complementary Reference A Input. Complementary signal to the input provided on Pin 2.
4, 5, 7, 8, 9, 13, 14, 17, 21, 34, 38, 41, 42, 46, 47, 48, 50, 51, 58, 59, 60, 61, 62, 65, 66, 67, 68, 69	VDD	I	Power	1.8 V Power Supply. See the Power Supply Partitions section for information about the recommended grouping of the power supply pins. Note that, for Pin 34 and Pin 21, it is recommended that a Size 0201, 0.1 µF bypass capacitor be placed between Pin 33 and Pin 34, as well as between Pin 21 and Pin 22, as close as possible to the AD9559.
6, 22, 33, 49	GND	O	Ground	Connect these pins (along with the exposed die pad) to ground.
10	LDO_0	I	LDO bypass	Output PLL0 Loop Filter Voltage Regulator. Connect a 0.47 µF capacitor from this pin to ground. This pin is also the ac ground reference for the integrated output PLL external loop filter.
11	LF_0	I/O	Loop filter for APLL_0	Loop Filter Node for the Output PLL0. Connect an external 6.8 nF capacitor from this pin to Pin 10 (LDO_0).
15	$\overline{\text{OUT0A}}$	O	HSTL, LVDS, 1.8 V CMOS	PLL0 Complementary Output 0A. This output can be configured as HSTL, LVDS, or single-ended 1.8 V CMOS.
16	OUT0A	O	HSTL, LVDS, 1.8 V CMOS	PLL0 Output 0A. This output can be configured as HSTL, LVDS, or single-ended 1.8 V CMOS. LVPECL levels can be achieved by ac-coupling and using the Thevenin-equivalent termination as described in the Input/Output Termination Recommendations section.

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
19	$\overline{\text{OUT0B}}$	O	HSTL, LVDS, 1.8 V CMOS, 3.3 V CMOS	PLL0 Complementary Output 0B. This output can be configured as HSTL, LVDS, or single-ended 1.8 V or 3.3 V CMOS.
20	OUT0B	O	HSTL, LVDS, 1.8 V CMOS, 3.3 V CMOS	PLL0 Output 0B. This output can be configured as HSTL, LVDS, or single-ended 1.8 V or 3.3 V CMOS. LVPECL levels can be achieved by ac-coupling and using the Thevenin-equivalent termination as described in the Input/Output Termination Recommendations section.
23	$\overline{\text{RESET}}$	I	3.3 V CMOS Logic	Chip Reset. When this active low pin is asserted, the chip goes into reset. This pin has an internal 50 kΩ pull-up resistor.
24	SCLK/SCL	I	3.3 V CMOS	Serial Programming Clock in SPI Mode (SCLK). Data clock for serial programming. Serial Clock Pin in I^2C Mode (SCL).
25	SDIO/SDA	I/O	3.3 V CMOS	Serial Data Input/Output (SDIO). When the device is in 4-wire SPI mode, data is written via this pin. In 3-wire SPI mode, data reads and writes both occur on this pin. There is no internal pull-up/pull-down resistor on this pin. Serial Data Pin in I^2C Mode (SDA).
26	M5/$\overline{\text{CS}}$	I/O	3.3 V CMOS	Configurable I/O Pin (M5). Used for status and control of the AD9559. Chip Select in SPI Mode ($\overline{\text{CS}}$). Active low input. When programming a device in SPI, this pin must be held low. In systems where more than one AD9559 is present, this pin enables individual programming of each AD9559. This pin has an internal 10 kΩ pull-up resistor.
27	M4/SDO	I/O	3.3 V CMOS	Configurable I/O Pin (M4). Used for status and control of the AD9559. Serial Data Output (SDO). In 4-wire SPI mode, this pin is used for reading serial data.
29, 30, 31, 32	M3, M2, M1, M0	I/O	3.3 V CMOS	Configurable I/O Pins. These pins are used for status and control of the AD9559. These pins are also used at power-up and reset to control the serial port configuration and EEPROM loading. See Table 23 and Table 25 for more information. These pins do NOT have internal pull-down resistors.
35	OUT1B	O	HSTL, LVDS, 1.8 V CMOS, 3.3 V CMOS	PLL1 Output 1B. This output can be configured as HSTL, LVDS, or single-ended 1.8 V or 3.3 V CMOS. LVPECL levels can be achieved by ac-coupling and using the Thevenin-equivalent termination as described in the Input/Output Termination Recommendations section.
36	$\overline{\text{OUT1B}}$	O	HSTL, LVDS, 1.8 V CMOS, 3.3 V CMOS	PLL1 Complementary Output 1B. This output can be configured as HSTL, LVDS, or single-ended 1.8 V or 3.3 V CMOS.
39	OUT1A	O	HSTL, LVDS, 1.8 V CMOS	PLL1 Output 1A. This output can be configured as HSTL, LVDS, or single-ended 1.8 V CMOS. LVPECL levels can be achieved by ac-coupling and using the Thevenin-equivalent termination as described in the Input/Output Termination Recommendations section.
40	$\overline{\text{OUT1A}}$	O	HSTL, LVDS, 1.8 V CMOS	PLL1 Complementary Output 1A. This output can be configured as HSTL, LVDS, or single-ended 1.8 V CMOS.
44	LF_1	I/O	Loop filter for APLL_1	Loop Filter Node for the Output PLL1. Connect an external 6.8 nF capacitor from this pin to Pin 45 (LDO_1).
45	LDO_1	I	LDO bypass	Output PLL1 Loop Filter Voltage Regulator. Connect a 0.47 µF capacitor from this pin to ground. This pin is also the ac ground reference for the integrated output PLL external loop filter.
52	$\overline{\text{REFC}}$	I	Differential input	Complementary Reference C Input. Complementary signal to the input provided on Pin 53.
53	REFC	I	Differential input	Reference C Input. This internally biased input is typically ac-coupled; when configured in that manner, it can accept any differential signal with single-ended swing up to 3.3 V. If dc-coupled, input can be LVPECL, LVDS, or single-ended CMOS.
56	$\overline{\text{REFD}}$	I	Differential input	Complementary Reference D Input. Complementary signal to the input provided on Pin 57.
57	REFD	I	Differential input	Reference D Input. This internally biased input is typically ac-coupled; when configured in this manner, it can accept any differential signal with single-ended swing up to 3.3 V. If dc-coupled, input can be LVPECL, LVDS, or single-ended CMOS.

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
63	XOB	I	Differential input	Complementary System Clock Input. Complementary signal to XOA. XOB contains internal dc biasing and should be ac-coupled with a 0.1 µF capacitor except when using a crystal. When a crystal is used, connect the crystal across XOA and XOB.
64	XOA	I	Differential input	System Clock Input. XOA contains internal dc biasing and should be ac-coupled with a 0.01 µF capacitor except when using a crystal. When a crystal is used, connect the crystal across XOA and XOB. Single-ended 1.8 V CMOS is also an option, but a spur may be introduced if the duty cycle is not 50%. When using XOA as a single-ended input, connect a 0.1 µF capacitor from XOB to ground.
70	REFB	I	Differential input	Reference B Input. This internally biased input is typically ac-coupled; when configured in this manner, it can accept any differential signal with single-ended swing up to 3.3 V. If dc-coupled, input can be LVPECL, LVDS, or single-ended CMOS.
71	$\overline{\text{REFB}}$	I	Differential input	Complementary Reference B Input. Complementary signal to the input provided on Pin 70.
EP	GND	O	Exposed pad	The exposed pad is the ground connection on the chip. It must be soldered to the analog ground of the PCB to ensure proper functionality and heat dissipation, noise, and mechanical strength benefits.

TYPICAL PERFORMANCE CHARACTERISTICS

f_R = input reference clock frequency; f_{OUT} = output clock frequency; f_{SYS} = SYSCLK input frequency; VDD3 and VDD at nominal supply voltage.



Absolute Phase Noise (Output Driver = HSTL), f_R = 19.44 MHz, f_{OUT} = 156.25 MHz, DPLL Loop BW = 50 Hz, f_{SYS} = 49.152 MHz Crystal

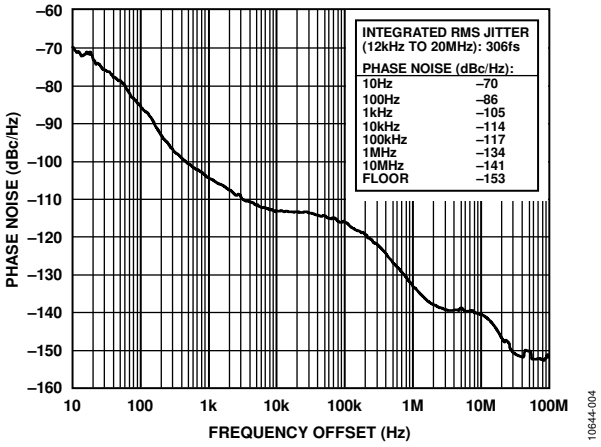


Figure 4. Absolute Phase Noise (Output Driver = HSTL), f_R = 19.44 MHz, f_{OUT} = 644.53125 MHz, DPLL Loop BW = 50 Hz, f_{SYS} = 49.152 MHz Crystal

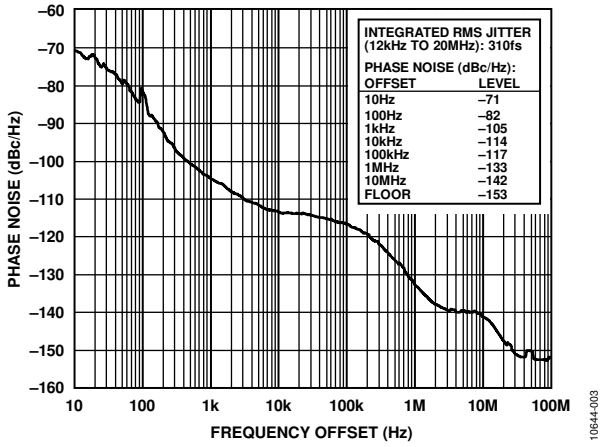


Figure 3. Absolute Phase Noise (Output Driver = HSTL), f_R = 19.44 MHz, f_{OUT} = 622.08 MHz, DPLL Loop BW = 50 Hz, f_{SYS} = 49.152 MHz Crystal

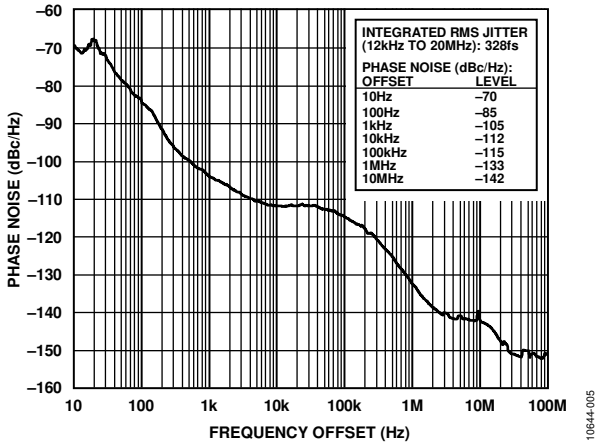


Figure 5. Absolute Phase Noise (Output Driver = HSTL), f_R = 19.44 MHz, f_{OUT} = 693.482991 MHz, DPLL Loop BW = 50 Hz, f_{SYS} = 49.152 MHz Crystal

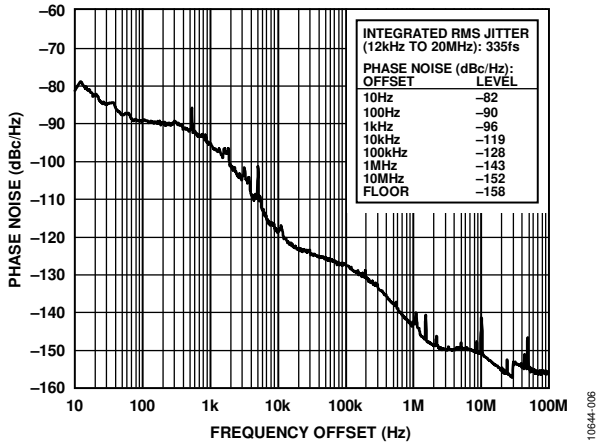


Figure 6. Absolute Phase Noise (Output Driver = HSTL), f_R = 19.44 MHz, f_{OUT} = 174.703 MHz, DPLL Loop BW = 1 kHz, f_{SYS} = 49.152 MHz Crystal

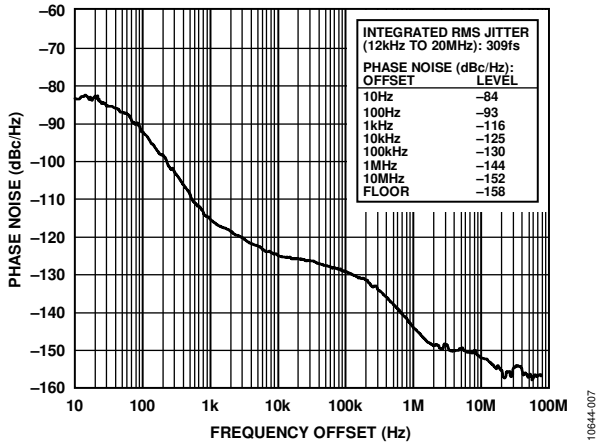


Figure 7. Absolute Phase Noise (Output Driver = 3.3.V CMOS), f_R = 19.44 MHz, f_{OUT} = 161.1328125 MHz, DPLL Loop BW = 100 Hz, f_{SYS} = 49.152 MHz Crystal

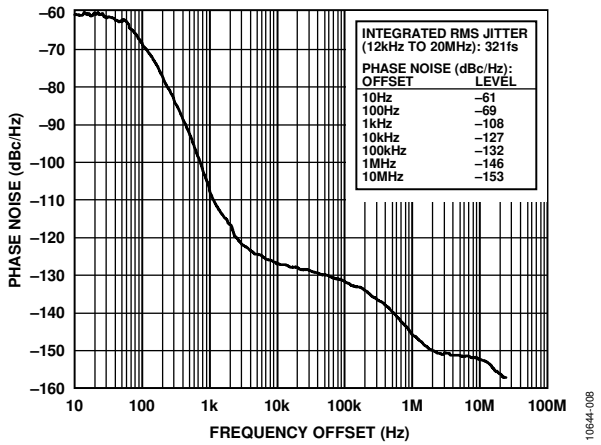


Figure 8. Absolute Phase Noise (Output Driver = HSTL), f_R = 2 kHz, f_{OUT} = 125 MHz, DPLL Loop BW = 100 Hz, f_{SYS} = 49.152 MHz Crystal

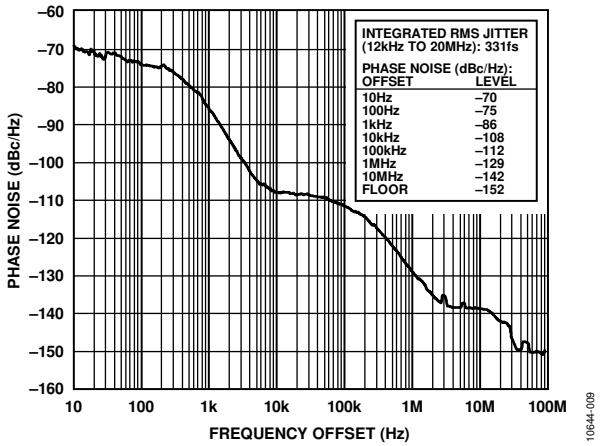


Figure 9. Absolute Phase Noise (Output Driver = HSTL), f_R = 25 MHz, f_{OUT} = 1 GHz, DPLL Loop BW = 500 Hz, f_{SYS} = 49.152 MHz Crystal

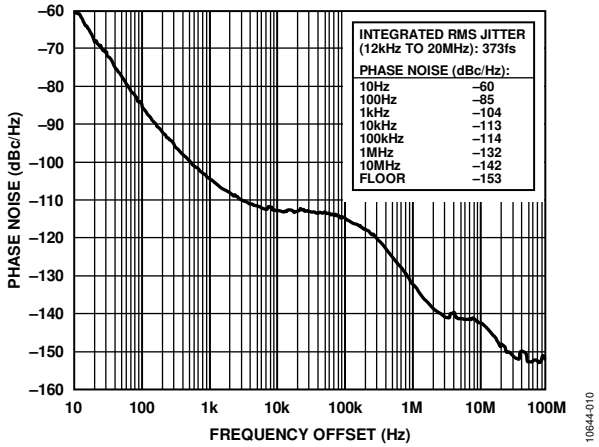


Figure 10. Absolute Phase Noise (Output Driver = HSTL), f_R = 19.44 MHz, f_{OUT} = 644.53 MHz, DPLL Loop BW = 10 Hz, f_{SYS} = 19.2 MHz TCXO

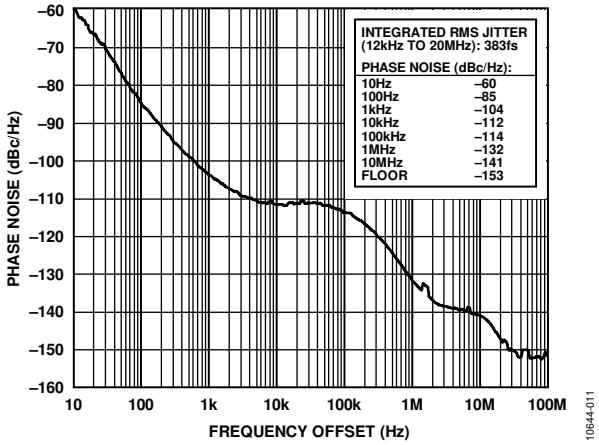


Figure 11. Absolute Phase Noise (Output Driver = HSTL), f_R = 19.44 MHz, f_{OUT} = 693.482991 MHz, DPLL Loop BW = 10 Hz, f_{SYS} = 19.2 MHz TCXO

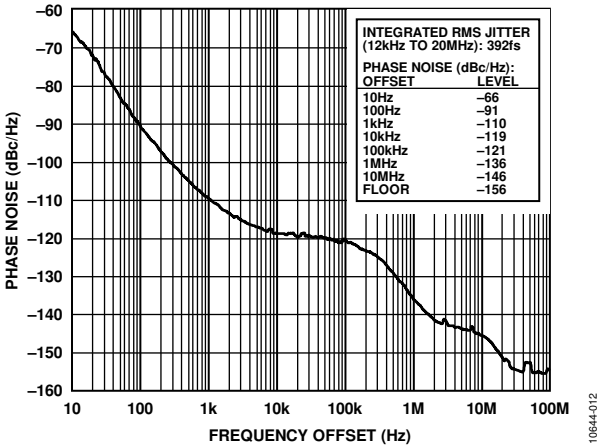


Figure 12. Absolute Phase Noise (Output Driver = HSTL), f_R = 19.44 MHz, f_{OUT} = 312.5 MHz, DPLL Loop BW = 0.1 Hz, f_{SYS} = 19.2 MHz TCXO

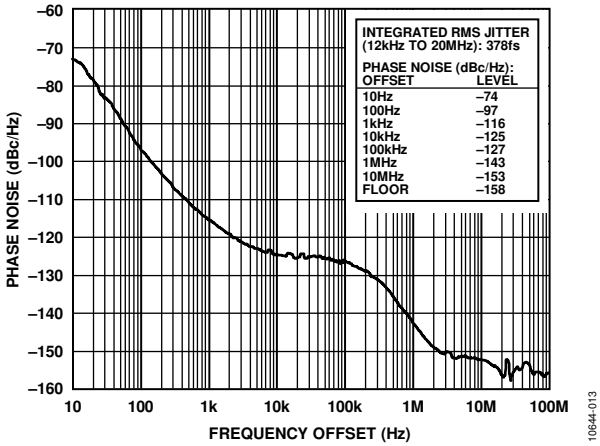


Figure 13. Absolute Phase Noise (Output Driver = 3.3 V CMOS), f_R = 19.44 MHz, f_{OUT} =161.1328125 MHz, DPLL Loop BW = 10 Hz, f_{SYS} = 19.2 MHz TCXO

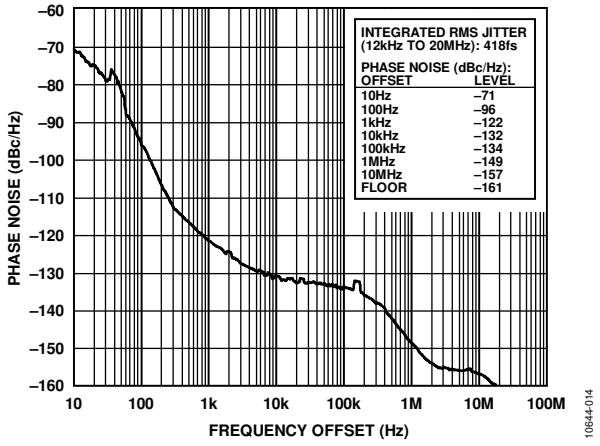


Figure 14. Absolute Phase Noise (Output Driver = 1.8V CMOS), f_R = 2 kHz, f_{OUT} = 70.656 MHz, DPLL Loop BW = 10 Hz, f_{SYS} = 19.2 MHz TCXO

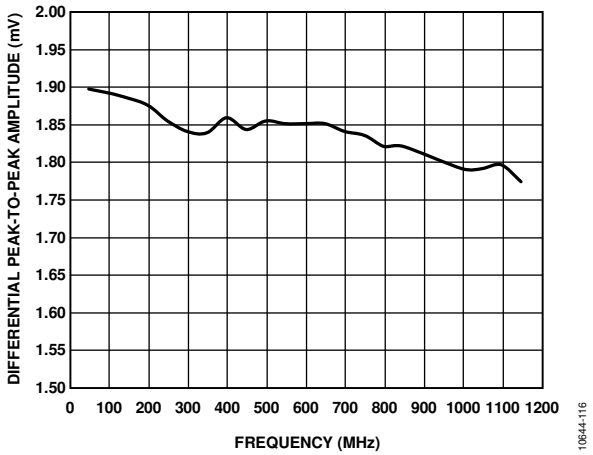


Figure 15. Amplitude vs. Toggle Rate, HSTL Mode (LVPECL-Compatible Mode)

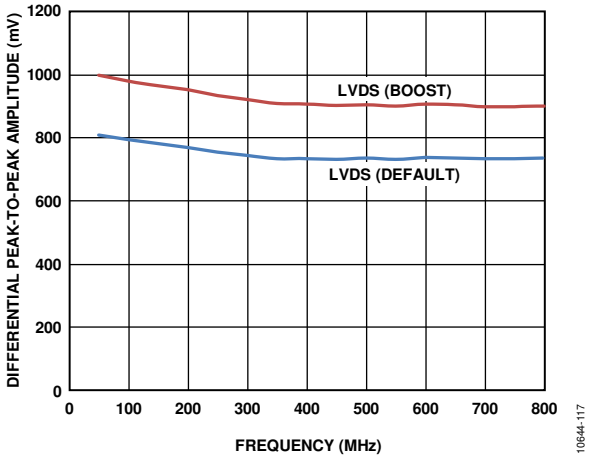


Figure 16. Amplitude vs. Toggle Rate, LVDS

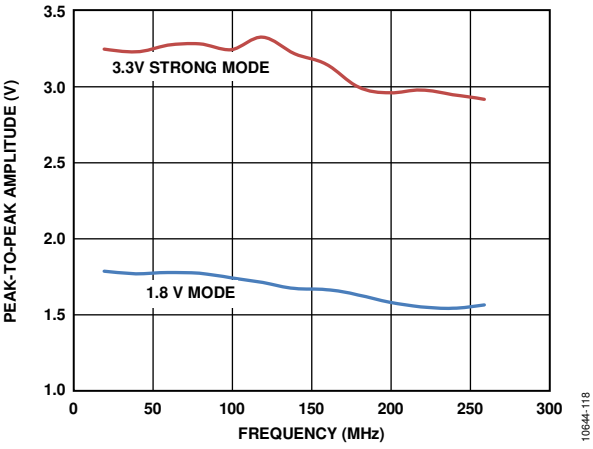


Figure 17. Amplitude vs. Toggle Rate with 10 pF Load, 3.3 V (Strong Mode) and 1.8 V CMOS

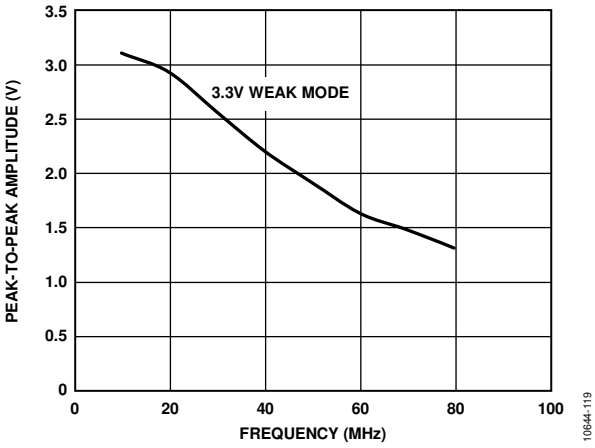


Figure 18. Amplitude vs. Toggle Rate with 10 pF Load, 3.3 V (Weak Mode) CMOS

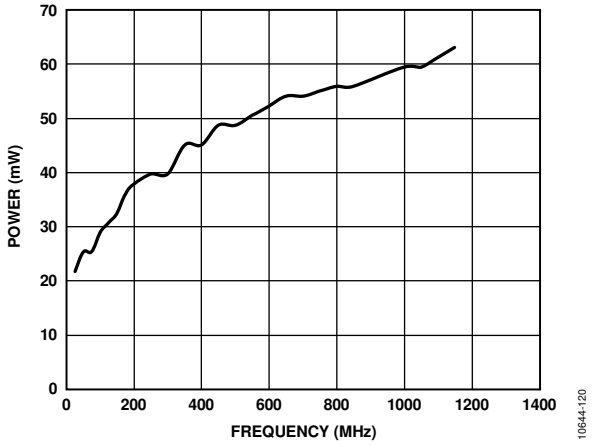


Figure 19. Power Consumption vs. Frequency, HSTL Mode on Output Driver Power Supply Only (Pin 17, Pin 21, Pin 34, and Pin 38)

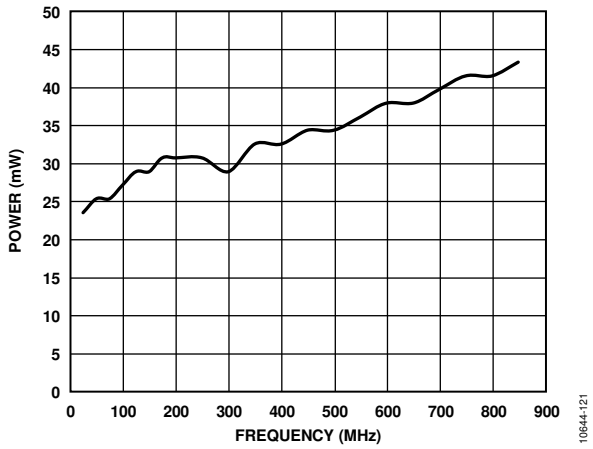


Figure 20. Power Consumption vs. Frequency, LVDS Mode on Output Driver Power Supply Only (Pin 17, Pin 21, Pin 34, and Pin 38)

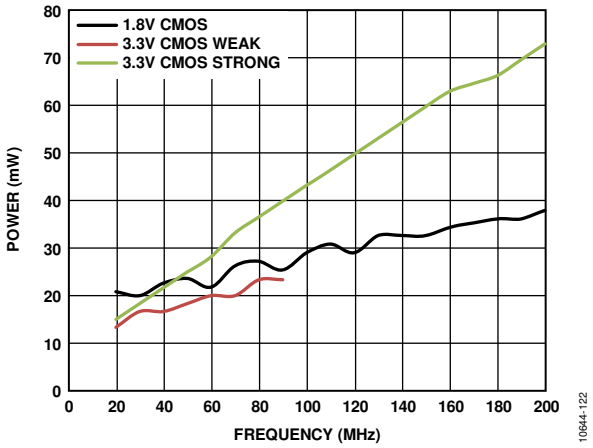


Figure 21. Power Consumption vs. Frequency for Two CMOS Drivers; Power Is Measured on Output Driver Power Supply Only (Pin 17, Pin 21, Pin 34, and Pin 38 for 1.8 V CMOS Mode or on Pin 18 and Pin 37 for 3.3 V CMOS Mode); C_{LOAD} = 80 pF

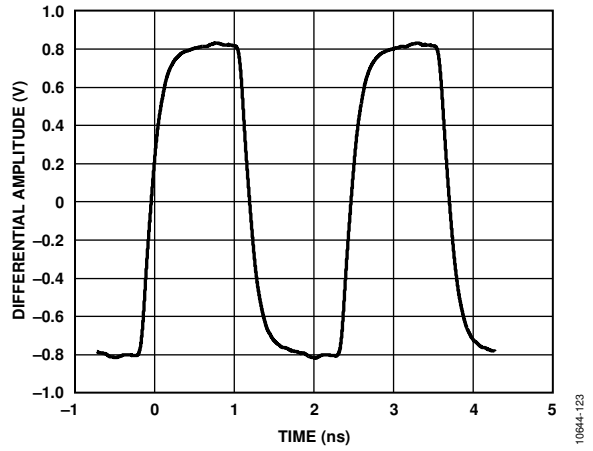


Figure 22. Output Waveform, HSTL (400 MHz)

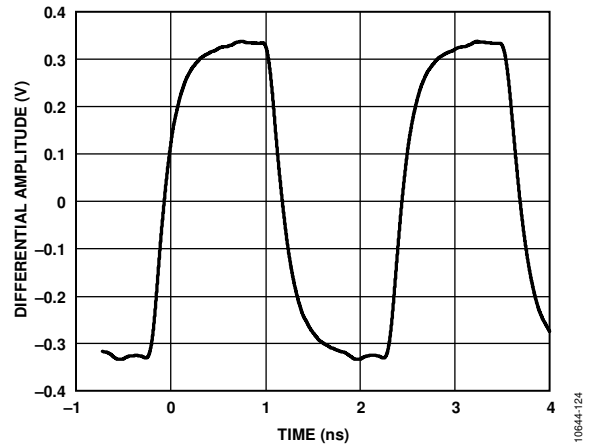


Figure 23. Output Waveform, LVDS (400 MHz)

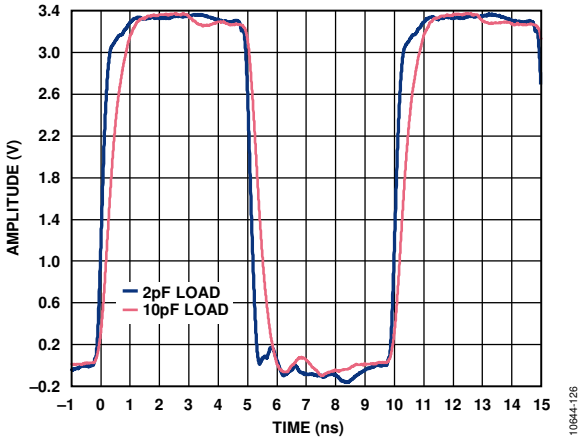


Figure 24. Output Waveform, 3.3 V CMOS (100 MHz, Strong Mode)

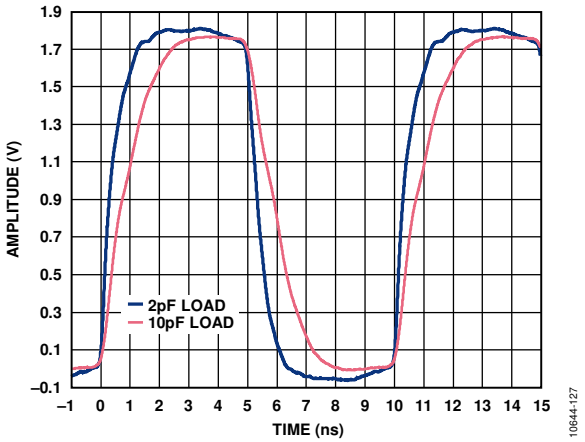


Figure 25. Output Waveform, 1.8 V CMOS (100 MHz)

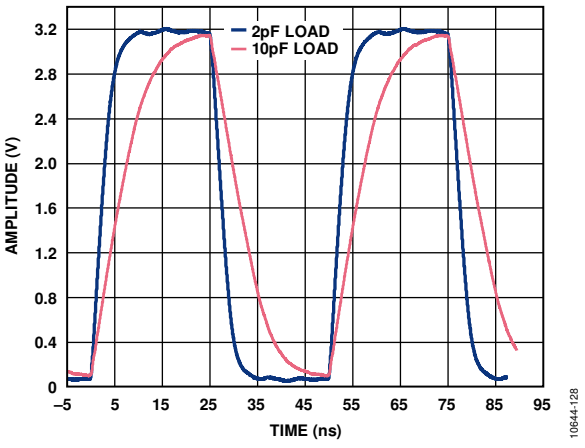


Figure 26. Output Waveform, 3.3 V CMOS (20 MHz, Weak Mode)