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Clock Generator with Dual PLLs, Spread Spectrum, and Margining

Data Sheet

AD9577

FEATURES

- Fully integrated dual PLL/VCO cores
- 1 integer-N and 1 fractional-N PLL
- Continuous frequency coverage from 11.2 MHz to 200 MHz
  - Most frequencies from 200 MHz to 637.5 MHz available
- PLL1 phase jitter (12 kHz to 20 MHz): 460 fs rms typical
- PLL2 phase jitter (12 kHz to 20 MHz)
  - Integer-N mode: 470 fs rms typical
  - Fractional-N mode: 660 fs rms typical
- Input crystal or reference clock frequency
- Optional reference frequency divide-by-2
- I²C programmable output frequencies
- Up to 4 LVDS/LVPECL or up to 8 LVCMOS output clocks
- 1 CMOS buffered reference clock output
- Spread spectrum: downspread [0, −0.5]%
- 2 pin-controlled frequency maps: margining
- Integrated loop filters
- Space saving, 6 mm × 6 mm, 40-lead LFCSP package
- 1.02 W power dissipation (LVDS operation)
- 1.235 W power dissipation (LVPECL operation)
- 3.3 V operation

APPLICATIONS

- Low jitter, low phase noise multioutput clock generator for data communications applications including Ethernet, Fibre Channel, SONET, SDH, PCI-e, SATA, PTN, OTN, ADC/DAC, and digital video
- Spread spectrum clocking

GENERAL DESCRIPTION

The AD9577 provides a multioutput clock generator function, along with two on-chip phase-locked loop cores, PLL1 and PLL2, optimized for network clocking applications. The PLL designs are based on the Analog Devices, Inc., proven portfolio of high performance, low jitter frequency synthesizers to maximize network performance. The PLLs have I²C programmable output frequencies and formats. The fractional-N PLL can support spread spectrum clocking for reduced EMI radiated peak power. Both PLLs can support frequency margining. Other applications with demanding phase noise and jitter requirements can benefit from this part.

The first integer-N PLL section (PLL1) consists of a low noise phase frequency detector (PFD), a precision charge pump (CP), a low phase noise voltage controlled oscillator (VCO), a programmable feedback divider, and two independently programmable output dividers. By connecting an external crystal or applying a reference clock to the REFCLK pin, frequencies of up to 637.5 MHz can be synchronized to the input reference. Each output divider and feedback divider ratio is I²C programmed for the required output rates.

A second fractional-N PLL (PLL2) with a programmable modulus allows VCO frequencies that are fractional multiples of the reference frequency to be synthesized. Each output divider and feedback divider ratio can be programmed for the required output rates, up to 637.5 MHz. This fractional-N PLL can also operate in integer-N mode for the lowest jitter.

Up to four differential output clock signals can be configured as either LVPECL or LVDS signaling formats. Alternatively, the outputs can be configured for up to eight CMOS outputs. Combinations of these formats are supported. No external loop filter components are required, thus conserving valuable design time and board space. The AD9577 is available in a 40-lead, 6 mm × 6 mm LFCSP package and can operate from a single 3.3 V supply. The operating temperature range is −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

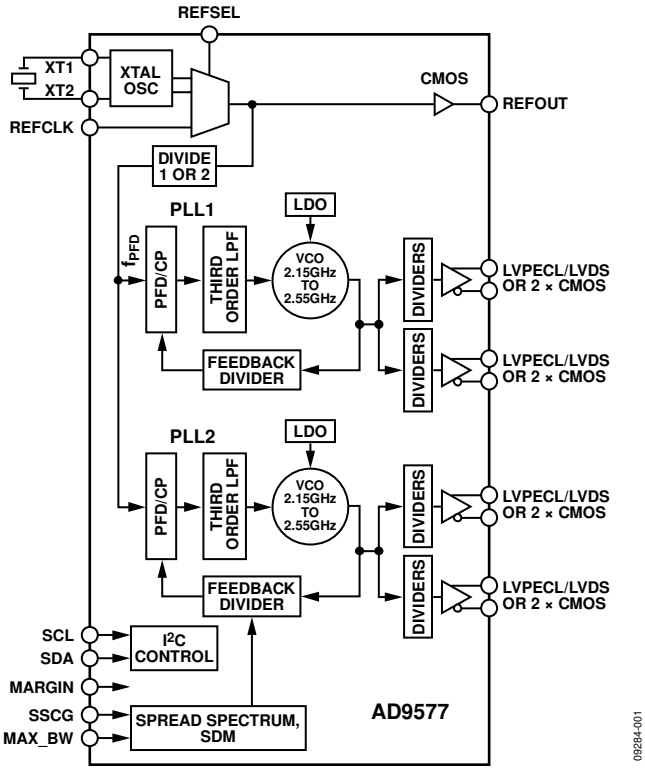

Figure 1.

Rev. A Document Feedback

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- AD9577 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9577: Clock Generator with Dual PLLs, Spread Spectrum, and Margining Data Sheet

User Guides

- UG-551: XStream™ ADI-BERT: An 11.3 Gbps Bit Error Rate Tester Solution Based on ADN2915, a Continuous-Tuning Wideband Clock and Data Recovery IC

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- AD9577 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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View all AD9577 EngineerZone Discussions.

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REVISION HISTORY

8/2016—Rev. 0 to Rev. A

Changes to Outputs Section ... 30

10/2011—Revision 0: Initial Version

SPECIFICATIONS

Typical (typ) is given for V_S = 3.3 V, T_A = 25°C, unless otherwise noted. Minimum (min) and maximum (max) values are given over full V_S (3.0 V to 3.6 V) and T_A (−40°C to +85°C) variation. AC coupling capacitors of 0.1 µF used where appropriate. A Fox Electronics FX532A 25 MHz crystal is used throughout, unless otherwise stated.

PLL1 CHARACTERISTICS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments[1]
NOISE CHARACTERISTICS					
Phase Noise (106.25 MHz LVPECL Output)					Na = 102, Vx = 4, Dx = 6, f_{PFD} = 25 MHz
At 1 kHz		−121		dBc/Hz	
At 10 kHz		−127		dBc/Hz	
At 100 kHz		−128		dBc/Hz	
At 1 MHz		−150		dBc/Hz	
At 10 MHz		−156		dBc/Hz	
At 30 MHz		−158		dBc/Hz	
Phase Noise (156.25 MHz LVPECL Output)					Na = 100, Vx = 4, Dx = 4, f_{PFD} = 25 MHz
At 1 kHz		−117		dBc/Hz	
At 10 kHz		−124		dBc/Hz	
At 100 kHz		−124		dBc/Hz	
At 1 MHz		−147		dBc/Hz	
At 10 MHz		−156		dBc/Hz	
At 30 MHz		−156		dBc/Hz	
Phase Noise (625 MHz LVPECL Output)					Na = 100, Vx = 2, Dx = 2, f_{PFD} = 25 MHz
At 1 kHz		−105		dBc/Hz	
At 10 kHz		−112		dBc/Hz	
At 100 kHz		−112		dBc/Hz	
At 1 MHz		−135		dBc/Hz	
At 10 MHz		−150		dBc/Hz	
At 30 MHz		−150		dBc/Hz	
Phase Noise (106.25 MHz LVDS Output)					Na = 102, Vx = 4, Dx = 6, f_{PFD} = 25 MHz
At 1 kHz		−119		dBc/Hz	
At 10 kHz		−127		dBc/Hz	
At 100 kHz		−128		dBc/Hz	
At 1 MHz		−148		dBc/Hz	
At 10 MHz		−156		dBc/Hz	
At 30 MHz		−156		dBc/Hz	
Phase Noise (156.25 MHz LVDS Output)					Na = 100, Vx = 4, Dx = 4, f_{PFD} = 25 MHz
At 1 kHz		−116		dBc/Hz	
At 10 kHz		−124		dBc/Hz	
At 100 kHz		−124		dBc/Hz	
At 1 MHz		−145		dBc/Hz	
At 10 MHz		−155		dBc/Hz	
At 30 MHz		−155		dBc/Hz	
Phase Noise (625 MHz LVDS Output)					Na = 100, Vx = 2, Dx = 2, f_{PFD} = 25 MHz
At 1 kHz		−104		dBc/Hz	
At 10 kHz		−111		dBc/Hz	
At 100 kHz		−112		dBc/Hz	
At 1 MHz		−134		dBc/Hz	
At 10 MHz		−149		dBc/Hz	
At 30 MHz		−149		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments[1]
Phase Noise (106.25 MHz CMOS Output)					Na = 102, Vx = 4, Dx = 6, f_{PFD} = 25 MHz
At 1 kHz		−118		dBc/Hz	
At 10 kHz		−127		dBc/Hz	
At 100 kHz		−127		dBc/Hz	
At 1 MHz		−149		dBc/Hz	
At 10 MHz		−156		dBc/Hz	
At 30 MHz		−157		dBc/Hz	
Phase Noise (156.25 MHz CMOS Output)					Na = 100, Vx = 4, Dx = 4, f_{PFD} = 25 MHz
At 1 kHz		−115		dBc/Hz	
At 10 kHz		−124		dBc/Hz	
At 100 kHz		−124		dBc/Hz	
At 1 MHz		−146		dBc/Hz	
At 10 MHz		−155		dBc/Hz	
At 30 MHz		−155		dBc/Hz	
Phase Noise (155.52 MHz LVPECL Output)					Na = 112, Vx = 2, Dx = 7, f_{PFD} = 19.44 MHz
At 1 kHz		−117		dBc/Hz	
At 10 kHz		−122		dBc/Hz	
At 100 kHz		−123		dBc/Hz	
At 1 MHz		−148		dBc/Hz	
At 10 MHz		−156		dBc/Hz	
At 30 MHz		−156		dBc/Hz	
Phase Noise (622.08 MHz LVPECL Output)					Na = 128, Vx = 2, Dx = 2, f_{PFD} = 19.44 MHz
At 1 kHz		−105		dBc/Hz	
At 10 kHz		−110		dBc/Hz	
At 100 kHz		−110		dBc/Hz	
At 1 MHz		−136		dBc/Hz	
At 10 MHz		−150		dBc/Hz	
At 30 MHz		−150		dBc/Hz	
Phase Noise (155.52 MHz LVDS Output)					Na = 112, Vx = 2, Dx = 7, f_{PFD} = 19.44 MHz
At 1 kHz		−117		dBc/Hz	
At 10 kHz		−122		dBc/Hz	
At 100 kHz		−123		dBc/Hz	
At 1 MHz		−146		dBc/Hz	
At 10 MHz		−155		dBc/Hz	
At 30 MHz		−155		dBc/Hz	
Phase Noise (622.08 MHz LVDS Output)					Na = 128, Vx = 2, Dx = 2, f_{PFD} = 19.44 MHz
At 1 kHz		−105		dBc/Hz	
At 10 kHz		−110		dBc/Hz	
At 100 kHz		−110		dBc/Hz	
At 1 MHz		−134		dBc/Hz	
At 10 MHz		−149		dBc/Hz	
At 30 MHz		−150		dBc/Hz	
Phase Noise (155.52 MHz CMOS Output)					Na = 112, Vx = 2, Dx = 7, f_{PFD} = 19.44 MHz
At 1 kHz		−117		dBc/Hz	
At 10 kHz		−122		dBc/Hz	
At 100 kHz		−123		dBc/Hz	
At 1 MHz		−147		dBc/Hz	
At 10 MHz		−155		dBc/Hz	
At 30 MHz		−155		dBc/Hz	

[1] x indicates either 0 or 1 for any given test condition.

PLL1 CLOCK OUTPUT JITTER

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments[2]
LVPECL INTEGRATED RANDOM PHASE JITTER					25 MHz crystal used
RMS Jitter (625 MHz Output)		460	750	fs rms	12 kHz to 20 MHz, Na = 100, Vx = 2, Dx = 2
		430	650	fs rms	50 kHz to 80 MHz, Na = 100, Vx = 2, Dx = 2
RMS Jitter (156.25 MHz Output)		460	750	fs rms	12 kHz to 20 MHz, Na = 100, Vx = 4, Dx = 4
RMS Jitter (106.25 MHz Output)		460	750	fs rms	12 kHz to 20 MHz, Na = 102, Vx = 4, Dx = 6
LVDS INTEGRATED RANDOM PHASE JITTER					25 MHz crystal used
RMS Jitter (625 MHz Output)		470	820	fs rms	12 kHz to 20 MHz, Na = 100, Vx = 2, Dx = 2
		450	790	fs rms	50 kHz to 80 MHz, Na = 100, Vx = 2, Dx = 2
RMS Jitter (156.25 MHz Output)		470	790	fs rms	12 kHz to 20 MHz, Na = 100, Vx = 4, Dx = 4
RMS Jitter (106.25 MHz Output)		470	790	fs rms	12 kHz to 20 MHz, Na = 102, Vx = 4, Dx = 6
CMOS INTEGRATED RANDOM PHASE JITTER					25 MHz crystal used, 50 Ω load
RMS Jitter (100 MHz Output)		470	920	f_S rms	12 kHz to 20 MHz, Na = 96, Vx = 4, Dx = 6
RMS Jitter (33.3 MHz Output)		420	700	f_S rms	12 kHz to 5 MHz, Na = 88, Vx = 6, Dx = 11
LVPECL INTEGRATED RANDOM PHASE JITTER					19.44 MHz crystal used
RMS Jitter (622.08 MHz Output)		500	680	fs rms	12 kHz to 20 MHz, Na = 128, Vx = 2, Dx = 2
		460	590	fs rms	50 kHz to 80 MHz, Na = 128, Vx = 2, Dx = 2
RMS Jitter (155.52 MHz Output)		480	680	fs rms	12 kHz to 20 MHz, Na = 112, Vx = 2, Dx = 7
LVDS INTEGRATED RANDOM PHASE JITTER					19.44 MHz crystal used
RMS Jitter (622.08 MHz Output)		520	780	fs rms	12 kHz to 20 MHz, Na = 128, Vx = 2, Dx = 2
		480	710	fs rms	50 kHz to 80 MHz, Na = 128, Vx = 2, Dx = 2
RMS Jitter (155.52 MHz Output)		480	750	fs rms	12 kHz to 20 MHz, Na = 112, Vx = 2, Dx = 7
CMOS INTEGRATED RANDOM PHASE JITTER					19.44 MHz crystal used, 50 Ω load
RMS Jitter (155.52 MHz Output)		470	700	fs rms	12 kHz to 20 MHz, Na = 112, Vx = 2, Dx = 7
RMS Jitter (38.88 MHz Output)		440	650	fs rms	12 kHz to 5 MHz, Na = 112, Vx = 2, Dx = 28
LVPECL PERIOD AND CYCLE-TO-CYCLE JITTER (100 MHz OUTPUT)					25 MHz crystal used, Na = 96, Vx = 4, Dx = 6
Output Peak-to-Peak Period Jitter		13		ps p-p	10,000 cycles, average of 25 measurements
Output RMS Period Jitter		2		ps rms	10,000 cycles, average of 25 measurements
Output Peak-to-Peak, Cycle-to-Cycle Jitter		19		ps p-p	1,000 cycles, average of 25 measurements
Output RMS Cycle-to-Cycle Jitter		3		ps rms	1,000 cycles, average of 25 measurements
LVDS PERIOD AND CYCLE-TO-CYCLE JITTER (100 MHz OUTPUT)					25 MHz crystal used, Na = 96, Vx = 4, Dx = 6
Output Peak-to-Peak Period Jitter		17		ps p-p	10,000 cycles, average of 25 measurements
Output RMS Period Jitter		2		ps rms	10,000 cycles, average of 25 measurements
Output Peak-to-Peak, Cycle-to-Cycle Jitter		25		ps p-p	1,000 cycles, average of 25 measurements
Output RMS Cycle-to-Cycle Jitter		4		ps rms	1,000 cycles, average of 25 measurements
CMOS PERIOD AND CYCLE-TO-CYCLE JITTER (100 MHz OUTPUT)					25 MHz crystal used, 50 Ω load, Na = 96, Vx = 4, Dx = 6
Output Peak-to-Peak Period Jitter		25		ps p-p	10,000 cycles, average of 25 measurements
Output RMS Period Jitter		3		ps rms	10,000 cycles, average of 25 measurements
Output Peak-to-Peak Cycle-to-Cycle Jitter		36		ps p-p	1,000 cycles, average of 25 measurements
Output RMS Cycle-to-Cycle Jitter		6		ps rms	1,000 cycles, average of 25 measurements

[1] All period and cycle-to-cycle jitter measurements are made with a Tektronix DPO70604 oscilloscope.
[2] x indicates either 0 or 1 for any given test condition.

PLL2 FRACTIONAL-N MODE CHARACTERISTICS

Table 3. Bleed = 1

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments[1]
NOISE CHARACTERISTICS					25 MHz crystal used
Phase Noise (155.52 MHz LVPECL Output)					Nb = 87, FRAC = 57, MOD = 625, Vx = 2, Dx = 7
At 1 kHz		−107		dBc/Hz	
At 10 kHz		−115		dBc/Hz	
At 100 kHz		−122		dBc/Hz	
At 1 MHz		−146		dBc/Hz	
At 10 MHz		−153		dBc/Hz	
At 30 MHz		−152		dBc/Hz	
Phase Noise (622.08 MHz LVPECL Output)					Nb = 99, FRAC = 333, MOD = 625, Vx = 2, Dx = 2
At 1 kHz		−95		dBc/Hz	
At 10 kHz		−103		dBc/Hz	
At 100 kHz		−109		dBc/Hz	
At 1 MHz		−133		dBc/Hz	
At 10 MHz		−148		dBc/Hz	
At 30 MHz		−150		dBc/Hz	
Phase Noise (155.52 MHz LVDS Output)					Nb = 87, FRAC = 57, MOD = 625, Vx = 2, Dx = 7
At 1 kHz		−107		dBc/Hz	
At 10 kHz		−114		dBc/Hz	
At 100 kHz		−122		dBc/Hz	
At 1 MHz		−145		dBc/Hz	
At 10 MHz		−154		dBc/Hz	
At 30 MHz		−154		dBc/Hz	
Phase Noise (622.08 MHz LVDS Output)					Nb = 99, FRAC = 333, MOD = 625, Vx = 2, Dx = 2
At 1 kHz		−95		dBc/Hz	
At 10 kHz		−103		dBc/Hz	
At 100 kHz		−109		dBc/Hz	
At 1 MHz		−132		dBc/Hz	
At 10 MHz		−147		dBc/Hz	
At 30 MHz		−149		dBc/Hz	
Phase Noise (155.52 MHz CMOS Output)					Nb = 87, FRAC = 57, MOD = 625, Vx = 2, Dx = 7
At 1 kHz		−107		dBc/Hz	
At 10 kHz		−114		dBc/Hz	
At 100 kHz		−122		dBc/Hz	
At 1 MHz		−146		dBc/Hz	
At 10 MHz		−154		dBc/Hz	
At 30 MHz		−154		dBc/Hz	
SPREAD SPECTRUM					
Modulation Range	+0.1		−0.5	%	Downspread, triangle modulation profile
Modulation Frequency		31.25		kHz	Programmable
Peak Power Reduction		10		dB	First harmonic of 100 MHz output, triangle modulation profile, spectrum analyzer resolution bandwidth = 20 kHz

[1] x indicates either 2 or 3 for any given test condition.

PLL2 INTEGER-N MODE CHARACTERISTICS

Table 4. Bleed = 0

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments[1]
NOISE CHARACTERISTICS					
Phase Noise (106.25 MHz LVPECL Output)					Nb = 102, Vx = 4, Dx = 6, f_{PFD} = 25 MHz
At 1 kHz		−116		dBc/Hz	
At 10 kHz		−123		dBc/Hz	
At 100 kHz		−127		dBc/Hz	
At 1 MHz		−148		dBc/Hz	
At 10 MHz		−156		dBc/Hz	
At 30 MHz		−158		dBc/Hz	
Phase Noise (156.25 MHz LVPECL Output)					Nb = 100, Vx = 4, Dx = 4, f_{PFD} = 25 MHz
At 1 kHz		−113		dBc/Hz	
At 10 kHz		−120		dBc/Hz	
At 100 kHz		−124		dBc/Hz	
At 1 MHz		−146		dBc/Hz	
At 10 MHz		−156		dBc/Hz	
At 30 MHz		−156		dBc/Hz	
Phase Noise (625 MHz LVPECL Output)					Nb = 100, Vx = 2, Dx = 2, f_{PFD} = 25 MHz
At 1 kHz		−101		dBc/Hz	
At 10 kHz		−108		dBc/Hz	
At 100 kHz		−112		dBc/Hz	
At 1 MHz		−134		dBc/Hz	
At 10 MHz		−149		dBc/Hz	
At 30 MHz		−150		dBc/Hz	
Phase Noise (106.25 MHz LVDS Output)					Nb = 102, Vx = 4, Dx = 6, f_{PFD} = 25 MHz
At 1 kHz		−117		dBc/Hz	
At 10 kHz		−123		dBc/Hz	
At 100 kHz		−127		dBc/Hz	
At 1 MHz		−147		dBc/Hz	
At 10 MHz		−156		dBc/Hz	
At 30 MHz		−156		dBc/Hz	
Phase Noise (156.25 MHz LVDS Output)					Nb = 100, Vx = 4, Dx = 4, f_{PFD} = 25 MHz
At 1 kHz		−113		dBc/Hz	
At 10 kHz		−120		dBc/Hz	
At 100 kHz		−124		dBc/Hz	
At 1 MHz		−145		dBc/Hz	
At 10 MHz		−155		dBc/Hz	
At 30 MHz		−155		dBc/Hz	
Phase Noise (625 MHz LVDS Output)					Nb = 100, Vx = 2, Dx = 2, f_{PFD} = 25 MHz
At 1 kHz		−101		dBc/Hz	
At 10 kHz		−108		dBc/Hz	
At 100 kHz		−112		dBc/Hz	
At 1 MHz		−133		dBc/Hz	
At 10 MHz		−148		dBc/Hz	
At 30 MHz		−149		dBc/Hz	
Phase Noise (106.25 MHz CMOS Output)					Nb = 102, Vx = 4, Dx = 6, f_{PFD} = 25 MHz
At 1 kHz		−117		dBc/Hz	
At 10 kHz		−123		dBc/Hz	
At 100 kHz		−127		dBc/Hz	
At 1 MHz		−147		dBc/Hz	
At 10 MHz		−156		dBc/Hz	
At 30 MHz		−157		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments[1]
Phase Noise (156.25 MHz CMOS Output)					Nb = 100, Vx = 4, Dx = 4, f_{PFD} = 25 MHz
At 1 kHz		−113		dBc/Hz	
At 10 kHz		−119		dBc/Hz	
At 100 kHz		−123		dBc/Hz	
At 1 MHz		−145		dBc/Hz	
At 10 MHz		−154		dBc/Hz	
At 30 MHz		−155		dBc/Hz	
Phase Noise (155.52 MHz LVPECL Output)					Nb = 112, Vx = 2, Dx = 7, f_{PFD} = 19.44 MHz
At 1 kHz		−112		dBc/Hz	
At 10 kHz		−118		dBc/Hz	
At 100 kHz		−126		dBc/Hz	
At 1 MHz		−147		dBc/Hz	
At 10 MHz		−155		dBc/Hz	
At 30 MHz		−156		dBc/Hz	
Phase Noise (622.08 MHz LVPECL Output)					Nb = 128, Vx = 2, Dx = 2, f_{PFD} = 19.44 MHz
At 1 kHz		−100		dBc/Hz	
At 10 kHz		−106		dBc/Hz	
At 100 kHz		−112		dBc/Hz	
At 1 MHz		−134		dBc/Hz	
At 10 MHz		−149		dBc/Hz	
At 30 MHz		−150		dBc/Hz	
Phase Noise (155.52 MHz LVDS Output)					Nb = 112, Vx = 2, Dx = 7, f_{PFD} = 19.44 MHz
At 1 kHz		−113		dBc/Hz	
At 10 kHz		−118		dBc/Hz	
At 100 kHz		−126		dBc/Hz	
At 1 MHz		−145		dBc/Hz	
At 10 MHz		−154		dBc/Hz	
At 30 MHz		−155		dBc/Hz	
Phase Noise (622.08 MHz LVDS Output)					Nb = 128, Vx = 2, Dx = 2, f_{PFD} = 19.44 MHz
At 1 kHz		−101		dBc/Hz	
At 10 kHz		−106		dBc/Hz	
At 100 kHz		−112		dBc/Hz	
At 1 MHz		−133		dBc/Hz	
At 10 MHz		−148		dBc/Hz	
At 30 MHz		−150		dBc/Hz	
Phase Noise (155.52 MHz CMOS Output)					Nb = 112, Vx = 2, Dx = 7, f_{PFD} = 19.44 MHz
At 1 kHz		−113		dBc/Hz	
At 10 kHz		−118		dBc/Hz	
At 100 kHz		−126		dBc/Hz	
At 1 MHz		−146		dBc/Hz	
At 10 MHz		−155		dBc/Hz	
At 30 MHz		−155		dBc/Hz	

[1] x indicates either 2 or 3 for any given test condition.

PLL2 CLOCK OUTPUT JITTER

Table 5. Bleed = 0 for Integer-N Mode, Bleed = 1 for Fractional-N Mode

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments[2]
LVPECL INTEGRATED RANDOM PHASE JITTER					25 MHz crystal used
RMS Jitter (622.08 MHz Output)		660	1200	fs rms	12 kHz to 20 MHz, fractional-N operation, Nb = 99, FRAC = 333, MOD = 625, Vx = 2, Dx = 2
		500	900	fs rms	50 kHz to 80 MHz, fractional-N operation, Nb = 99, FRAC = 333, MOD = 625, Vx = 2, Dx = 2
RMS Jitter (625 MHz Output)		470	800	fs rms	12 kHz to 20 MHz, integer-N operation, Nb = 100, Vx = 2, Dx = 2
		380	650	fs rms	50 kHz to 80 MHz, integer-N operation, Nb = 100, Vx = 2, Dx = 2
RMS Jitter (155.52 MHz Output)		630	1100	fs rms	12 kHz to 20 MHz, fractional-N operation, Nb = 87, FRAC = 57, MOD = 625, Vx = 2, Dx = 7
RMS Jitter (156.25 MHz Output)		470	800	fs rms	12 kHz to 20 MHz, integer-N operation, Nb = 100, Vx = 4, Dx = 4
LVDS INTEGRATED RANDOM PHASE JITTER					25 MHz crystal used
RMS Jitter (622.08 MHz Output)		660	1200	fs rms	12kHz to 20 MHz, fractional-N operation, Nb = 99, FRAC = 333, MOD = 625, Vx = 2, Dx = 2
		510	900	fs rms	50 kHz to 80 MHz, fractional-N operation, Nb = 99, FRAC = 333, MOD = 625, Vx = 2, Dx = 2
RMS Jitter (625 MHz Output)		470	820	fs rms	12 kHz to 20 MHz, integer-N operation, Nb = 100, Vx = 2, Dx = 2
		380	650	fs rms	50 kHz to 80 MHz, integer-N operation, Nb = 100, Vx = 2, Dx = 2
RMS Jitter (155.52 MHz Output)		620	1100	fs rms	12 kHz to 20 MHz, fractional-N operation, Nb = 87, FRAC = 57, MOD = 625, Vx = 2, Dx = 7
RMS Jitter (156.25 MHz Output)		480	800	fs rms	12 kHz to 20 MHz, integer-N operation, Nb = 100, Vx = 4, Dx = 4
CMOS INTEGRATED RANDOM PHASE JITTER					25 MHz crystal used, 50 Ω load
RMS Jitter (155.52 MHz Output)		630	1100	fs rms	12 kHz to 20 MHz, fractional-N operation, Nb = 87, FRAC = 57, MOD = 625, Vx = 2, Dx = 7
RMS Jitter (100 MHz Output)		490	800	fs rms	12 kHz to 20 MHz, integer-N operation, Nb = 96, Vx = 4, Dx = 6
RMS Jitter (33.33 MHz Output)		450	700	fs rms	12 kHz to 5 MHz, integer-N operation, Nb = 88, Vx = 6, Dx = 11
LVPECL INTEGRATED RANDOM PHASE JITTER					19.44 MHz crystal used
RMS Jitter (622.08 MHz Output)		510	800	fs rms	12 kHz to 20 MHz, integer-N operation, Nb = 128, Vx = 2, Dx = 2
		380	650	fs rms	50 kHz to 80 MHz, integer-N operation, Nb = 128, Vx = 2, Dx = 2
RMS Jitter (155.52 MHz Output)		470	800	fs rms	12 kHz to 20 MHz, integer-N operation, Nb = 112, Vx = 2, Dx = 7
LVDS INTEGRATED RANDOM PHASE JITTER					19.44 MHz crystal used
RMS Jitter (622.08 MHz Output)		530	900	fs rms	12 kHz to 20 MHz, integer-N operation, Nb = 128, Vx = 2, Dx = 2
		390	700	fs rms	50 kHz to 80 MHz, integer-N operation, Nb = 128, Vx = 2, Dx = 2
RMS Jitter (155.52 MHz Output)		480	750	fs rms	12 kHz to 20 MHz, integer-N operation, Nb = 112, Vx = 2, Dx = 7

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments[2]
CMOS INTEGRATED RANDOM PHASE JITTER					19.44 MHz crystal used, 50 Ω load
RMS Jitter (155.52 MHz Output)		470	700	fs rms	12 kHz to 20 MHz, integer-N operation, Nb = 112, Vx = 2, Dx = 7
RMS Jitter (38.88 MHz Output)		430	650	fs rms	12 kHz to 5 MHz, integer-N operation, Nb = 112, Vx = 2, Dx = 28
LVPECL PERIOD AND CYCLE-TO-CYCLE JITTER (100 MHz OUTPUT)					25 MHz crystal used, integer-N operation, Nb = 96, Vx = 4, Dx = 6
Output Peak-to-Peak Period Jitter		13		ps p-p	10,000 cycles, average of 25 measurements
Output RMS Period Jitter		2		ps rms	10,000 cycles, average of 25 measurements
Output Peak-to-Peak, Cycle-to-Cycle Jitter		19		ps p-p	1,000 cycles, average of 25 measurements
Output RMS Cycle-to-Cycle Jitter		3		ps rms	1,000 cycles, average of 25 measurements
LVDS PERIOD AND CYCLE-TO-CYCLE JITTER (100 MHz OUTPUT)					25 MHz crystal used, integer-N operation, Nb = 96, Vx = 4, Dx = 6
Output Peak-to-Peak Period Jitter		17		ps p-p	10,000 cycles, average of 25 measurements
Output RMS Period Jitter		2		ps rms	10,000 cycles, average of 25 measurements
Output Peak-to-Peak, Cycle-to-Cycle Jitter		26		ps p-p	1,000 cycles, average of 25 measurements
Output RMS Cycle-to-Cycle Jitter		4		ps rms	1,000 cycles, average of 25 measurements
CMOS PERIOD AND CYCLE-TO-CYCLE JITTER (100 MHz OUTPUT)					25 MHz crystal used, 50 Ω load, integer-N operation, Nb = 96, Vx = 4, Dx = 6
Output Peak-to-Peak Period Jitter		25		ps p-p	10,000 cycles, average of 25 measurements
Output RMS Period Jitter		3		ps rms	10,000 cycles, average of 25 measurements
Output Peak-to-Peak, Cycle-to-Cycle		36		ps p-p	1,000 cycles, average of 25 measurements
Output RMS Cycle-to-Cycle Jitter		6		ps rms	1,000 cycles, average of 25 measurements
LVPECL PERIOD AND CYCLE-TO-CYCLE JITTER (100 MHz OUTPUT)					25 MHz crystal used, SSCG on, Nb = 100, FRAC = 0, MOD = 1000, Vx = 5, Dx = 5, CkDiv = 7, NumSteps = 59, FracStep = −8, f_{OUT} = 100 MHz with −0.5% downspread at 30.2 kHz
Output Peak-to-Peak Period Jitter		60		ps p-p	10,000 cycles, average of 25 measurements
Output RMS Period Jitter		15		ps rms	10,000 cycles, average of 25 measurements
Output Peak-to-Peak, Cycle-to-Cycle Jitter		20		ps p-p	1,000 cycles, average of 25 measurements
Output RMS Cycle-to-Cycle Jitter		3		ps rms	1,000 cycles, average of 25 measurements
LVDS PERIOD AND CYCLE-TO-CYCLE JITTER (100 MHz OUTPUT)					25 MHz crystal used, SSCG on, Nb = 100, FRAC = 0, MOD = 1000, Vx = 5, Dx = 5, CkDiv = 7, NumSteps = 59, FracStep = −8, f_{OUT} = 100 MHz with −0.5% downspread at 30.2 kHz
Output Peak-to-Peak Period Jitter		63		ps p-p	10,000 cycles, average of 25 measurements
Output RMS Period Jitter		15		ps rms	10,000 cycles, average of 25 measurements
Output Peak-to-Peak, Cycle-to-Cycle Jitter		25		ps p-p	1,000 cycles, average of 25 measurements
Output RMS Cycle-to-Cycle Jitter		4		ps rms	1,000 cycles, average of 25 measurements
CMOS PERIOD AND CYCLE-TO-CYCLE JITTER (100 MHz OUTPUT)					25 MHz crystal used, SSCG on, 50 Ω load, Nb = 100, FRAC = 0, MOD = 1000, Vx = 5, Dx = 5, CkDiv = 7, NumSteps = 59, FracStep = −8, f_{OUT} = 100 MHz with −0.5% downspread at 30.2 kHz
Output Peak-to-Peak Period Jitter		70		ps p-p	10,000 cycles, average of 25 measurements
Output RMS Period Jitter		15		ps rms	10,000 cycles, average of 25 measurements
Output Peak-to-Peak, Cycle-to-Cycle Jitter		36		ps p-p	1,000 cycles, average of 25 measurements
Output RMS Cycle-Cycle Jitter		6		ps rms	1,000 cycles, average of 25 measurements

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments[2]
LVPECL PERIOD AND CYCLE-TO-CYCLE JITTER (100.12 MHz OUTPUT)					25 MHz crystal used, fractional-N operation, Nb = 100, FRAC = 15, MOD = 125, Vx = 5, Dx = 5
Output Peak-to-Peak Period Jitter		13		ps p-p	10,000 cycles, average of 25 measurements
Output RMS Period Jitter		2		ps rms	10,000 cycles, average of 25 measurements
Output Peak-to-Peak, Cycle-to-Cycle Jitter		20		ps p-p	1,000 cycles, average of 25 measurements
Output RMS Cycle-to-Cycle Jitter		3		ps rms	1,000 cycles, average of 25 measurements
LVDS PERIOD AND CYCLE-TO-CYCLE JITTER (100.12 MHz OUTPUT)					25 MHz crystal used, fractional-N operation, Nb = 100, FRAC = 15, MOD = 125, Vx = 5, Dx = 5
Output Peak-to-Peak Period Jitter		17		ps p-p	10,000 cycles, average of 25 measurements
Output RMS Period Jitter		2		ps rms	10,000 cycles, average of 25 measurements
Output Peak-to-Peak, Cycle-to-Cycle Jitter		26		ps p-p	1,000 cycles, average of 25 measurements
Output RMS Cycle-to-Cycle Jitter		4		ps rms	1,000 cycles, average of 25 measurements
CMOS PERIOD AND CYCLE-TO-CYCLE JITTER (100.12 MHz OUTPUT)					25 MHz crystal used, 50 Ω load, fractional-N operation, Nb = 100, FRAC = 15, MOD = 125, Vx = 5, Dx = 5
Output Peak-to-Peak Period Jitter		25		ps p-p	10,000 cycles, average of 25 measurements
Output RMS Period Jitter		3		ps rms	10,000 cycles, average of 25 measurements
Output Peak-to-Peak, Cycle-to-Cycle Jitter		36		ps p-p	1,000 cycles, average of 25 measurements
Output RMS Cycle-to-Cycle Jitter		6		ps rms	1,000 cycles, average of 25 measurements

[1] All period and cycle-to-cycle jitter measurements are made with a Tektronix DPO70604 oscilloscope.
[2] x indicates either 2 or 3 for any given test condition.

CMOS REFERENCE CLOCK OUTPUT JITTER

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
JITTER INTEGRATION BANDWIDTH					Jitter measurement at 25 MHz is equipment limited
12 kHz to 5 MHz		680	1000	fs rms	25 MHz
200 kHz to 5 MHz		670	950	fs rms	

TIMING CHARACTERISTICS

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL (see Figure 2)					Termination = 200 Ω to 0 V, ac-coupled to 50 Ω oscilloscope; C_{LOAD} = 5 pF
Output Rise Time, t_{RP}	170	225	300	ps	20% to 80%, measured differentially
Output Fall Time, t_{FP}	170	230	310	ps	80% to 20%, measured differentially
Skew		20		ps	Between the outputs of the same PLL at the same frequency. SyncCh01/SyncCh23 set to 1
LVDS (see Figure 3)					Termination = 100 Ω differential; C_{LOAD} = 5 pF
Output Rise Time, t_{RL}	180	250	340	ps	20% to 80%, measured differentially
Output Fall Time, t_{FL}	180	260	330	ps	80% to 20%, measured differentially
Skew		20		ps	Between the outputs of the same PLL at the same frequency; SyncCh01/SyncCh23 set to 1
CMOS (see Figure 4)					
Output Rise Time, t_{RC}	250	680	950	ps	Termination is high impedance active probe, total C_{LOAD} = 5 pF, R_{LOAD} = 20 kΩ, 20% to 80%
Output Fall Time, t_{FC}	350	700	1000	ps	Termination is high impedance active probe, total C_{LOAD} = 5 pF, R_{LOAD} = 20 kΩ, 80% to 20%
Skew		20		ps	Between the outputs of the same PLL at the same frequency; SyncCh01/SyncCh23 set to 1

Timing Diagrams

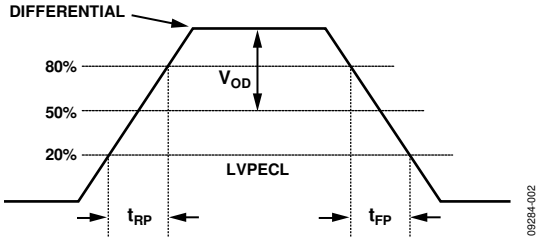

Figure 2. LVPECL Timing, Differential

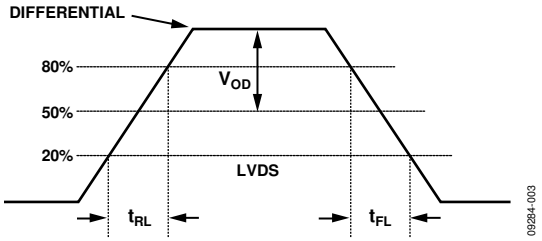

Figure 3. LVDS Timing, Differential

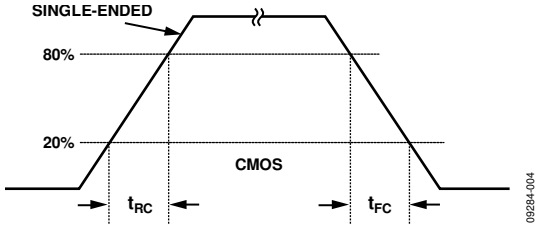

Figure 4. CMOS Timing, Single-Ended, 5 pF Load

CLOCK OUTPUTS

AC coupling capacitors of 0.1 µF used where appropriate.

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL CLOCK OUTPUTS					
Output Frequency			637.5	MHz	Load is 200 Ω to GND at output pins, then ac-coupled to 50 Ω terminated measurement equipment.
Output Voltage Swing, V_{OD}	610	740	950	mV	Load is 200 Ω to GND at output pins, then ac-coupled to 50 Ω terminated measurement equipment. For differential amplitude, see Figure 2.
Duty Cycle	45		55	%	Load is 200 Ω to GND at output pins, then ac-coupled to 50 Ω terminated measurement equipment.
Output High Voltage, V_{OH}	V_S – 1.24	V_S – 0.94	V_S – 0.83	V	Load is 127 Ω/83 Ω potential divider across supply dc-coupled into 1 MΩ terminated measurement equipment, outputs static.
Output Low Voltage, V_{OL}	V_S – 2.07	V_S – 1.75	V_S – 1.62	V	Load is 127 Ω/83 Ω potential divider across supply dc-coupled into 1 MΩ terminated measurement equipment, outputs static.
LVDS CLOCK OUTPUTS					
Output Frequency			637.5	MHz	Load is ac-coupled to measurement equipment that provides 100 Ω differential input termination.
Differential Output Voltage, V_{OD}	250	350	475	mV	Load is ac-coupled to measurement equipment that provides 100 Ω differential input termination. For differential amplitude, see Figure 3.
Delta V_{OD}			25	mV	Load is ac-coupled to measurement equipment that provides 100 Ω differential input termination.
Duty Cycle	45		55	%	Load is ac-coupled to measurement equipment that provides 100 Ω differential input termination.
Output Offset Voltage, V_{OS}	1.125	1.25	1.375	V	Load is dc-coupled to a 100 Ω differential resistor into 1 MΩ terminated measurement equipment, outputs static.
Delta V_{OS}			25	mV	Load is dc-coupled to a 100 Ω differential resistor into 1 MΩ terminated measurement equipment, outputs static.
Short-Circuit Current, I_{SA}, I_{SB}		13	24	mA	Load is dc-coupled to a 100 Ω differential resistor into 1 MΩ terminated measurement equipment, output shorted to GND.
CMOS CLOCK OUTPUTS					
Output Frequency			200	MHz	
Output High Voltage, V_{OH}	V_S – 0.15			V	Sourcing 1.0 mA current, outputs static.
Output Low Voltage, V_{OL}			0.1	V	Sinking 1.0 mA current, outputs static.
Duty Cycle	45		55	%	Termination is high impedance active probe; total C_{LOAD} = 5 pF, R_{LOAD} = 20 kΩ.

POWER

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY	3.0	3.3	3.6	V	
LVPECL POWER DISSIPATION		1235	1490	mW	Typical part configuration, both PLLs enabled for integer-N operation, f_{OUT0} = 156.25 MHz, f_{OUT1} = 125 MHz, f_{OUT2} = 100 MHz, f_{OUT3} = 33.33 MHz, Na = 100, V0 = 4, D0 = 4, V1 = 4, D1 = 5, Nb = 96, V2 = 4, D2 = 6, V3 = 4, D3 = 18, 25 MHz crystal used, load is 200 Ω to GND at output pins, then ac-coupled to 50 Ω terminated measurement equipment
		1270	1530	mW	Worst-case part configuration, PLL2 in fractional-N mode, with SSCG enabled, f_{OUT0} = 379.16 MHz, f_{OUT1} = 379.16 MHz, f_{OUT2} = 359.33 MHz, f_{OUT3} = 359.33 MHz, Na = 91, V0 = 3, D0 = 2, V1 = 3, D1 = 2, Nb = 86, V2 = 3, D2 = 2, V3 = 3, D3 = 2, FRAC = 300, MOD = 1250, CkDiv = 5, NumSteps = 77, FracStep = −7, −0.5% downspread at 32 kHz, 25 MHz crystal used, load is 200 Ω to GND at output pins, then ac-coupled to 50 Ω terminated measurement equipment
LVDS POWER DISSIPATION		1020	1200	mW	Typical part configuration, both PLLs enabled for integer-N operation, f_{OUT0} = 156.25 MHz, f_{OUT1} = 125 MHz, f_{OUT2} = 100 MHz, f_{OUT3} = 33.33 MHz, Na = 100, V0 = 4, D0 = 4, V1 = 4, D1 = 5, Nb = 96, V2 = 4, D2 = 6, V3 = 4, D3 = 18, 25 MHz crystal used, load ac-coupled to measurement equipment that provides 100 Ω differential input termination
		1085	1290	mW	Worst-case part configuration, PLL2 in fractional-N mode, with SSCG enabled, f_{OUT0} = 379.16 MHz, f_{OUT1} = 379.16 MHz, f_{OUT2} = 359.33 MHz, f_{OUT3} = 359.33 MHz, Na = 91, V0 = 3, D0 = 2, V1 = 3, D1 = 2, Nb = 86, V2 = 3, D2 = 2, V3 = 3, D3 = 2, FRAC = 300, MOD = 1250, CkDiv = 5, NumSteps = 77, FracStep = −7, −0.5% downspread at 32 kHz, 25 MHz crystal used, load ac-coupled to measurement equipment that provides 100 Ω differential input termination
CMOS POWER DISSIPATION		1065	1380	mW	Typical part configuration, both PLLs enabled for integer-N operation, f_{OUT0} = 156.25 MHz, f_{OUT1} = 125 MHz, f_{OUT2} = 100 MHz, f_{OUT3} = 33.33 MHz, Na = 100, V0 = 4, D0 = 4, V1 = 4, D1 = 5, Nb = 96, V2 = 4, D2 = 6, V3 = 4, D3 = 18, 25 MHz crystal used, eight single-ended outputs active, C_{LOAD} = 5 pF
		1190	1510	mW	Worst-case part configuration, PLL2 in fractional-N mode, with SSCG enabled, f_{OUT0} = 189.58 MHz, f_{OUT1} = 189.58 MHz, f_{OUT2} = 179.66 MHz, f_{OUT3} = 179.66 MHz, Na = 91, V0 = 3, D0 = 4, V1 = 3, D1 = 4, Nb = 86, V2 = 3, D2 = 4, V3 = 3, D3 = 4, FRAC = 300, MOD = 1250, CkDiv = 5, NumSteps = 77, FracStep = −7, −0.5% downspread at 32 kHz, 25 MHz crystal used, eight single-ended outputs active, C_{LOAD} = 5 pF
POWER CHANGES					Reduction in power due to turning off a channel of one VCO divider, one output divider, and one output buffer; data for Channel 1, with typical part configuration, both PLLs enabled for integer-N operation, f_{OUT0} = 156.25 MHz, f_{OUT1} = 125 MHz, f_{OUT2} = 100 MHz, f_{OUT3} = 33.33 MHz, Na = 100, V0 = 4, D0 = 4, V1 = 4, D1 = 5, Nb = 96, V2 = 4, D2 = 6, V3 = 4, D3 = 18, 25 MHz crystal used
Power-Down 1 LVPECL Channel	160	205		mW	Load 200 Ω to GND at output pins, and ac-coupled to 50 Ω terminated measurement equipment
Power-Down 1 LVDS Channel	105	155		mW	Load ac-coupled to measurement equipment that provides 100 Ω differential input termination
Power-Down 1 CMOS Channel	130	170		mW	Eight single-ended outputs active, C_{LOAD} = 5 pF

CRYSTAL OSCILLATOR

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CRYSTAL SPECIFICATION					Fundamental mode
Frequency	19.44	25	27	MHz	Reference divider, R = 1, only
ESR			50	Ω	
Load Capacitance		14		pF	
Phase Noise		−135		dBc/Hz	1 kHz offset
Stability	−50		+50	ppm	

REFERENCE INPUT

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK INPUT (REFCLK)					
Input Frequency	19.44	25	27	MHz	Reference divider, R = 1
	38.88	50	54	MHz	Reference divider, R = 2
Input High Voltage	2.0			V	
Input Low Voltage			0.8	V	
Input Current	−1.0		+1.0	µA	
Input Capacitance		2		pF	

CONTROL PINS

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT CHARACTERISTICS					
SSCG, MAX_BW, and MARGIN					SSCG, MAX_BW, and MARGIN have a 30 kΩ internal pull-down resistor
Logic 1 Voltage	2.0			V	
Logic 0 Voltage			0.8	V	
Logic 1 Current			240	µA	
Logic 0 Current			40	µA	
REFSEL					REFSEL has a 30 kΩ internal pull-up resistor
Logic 1 Voltage	2.0			V	
Logic 0 Voltage			0.8	V	
Logic 1 Current			70	µA	
Logic 0 Current			240	µA	
I^2C DC CHARACTERISTICS					LVCMOS; the SCL and SDA pins only, see Figure 48
Input Voltage High	0.7 Vcc			V	
Input Voltage Low			0.3 Vcc	V	
Input Current	−10		+10	µA	V_{IN} = 0.1 V_{CC} or V_{IN} = 0.9 V_{CC}
Output Low Voltage			0.4	V	V_{OL} with a load current of I_{OL} = 3.0 mA
I^2C TIMING CHARACTERISTICS					LVCMOS; the SCL and SDA pins only, see Figure 48
SCL Clock Frequency			400	kHz	
SCL Pulse Width High					
High, t_{HIGH}	600			ns	
Low, t_{LOW}	1300			ns	
Start Condition					
Hold Time, $t_{HD;STA}$	600			ns	
Setup Time, $t_{SU;STA}$	600			ns	
Data					
Setup Time, $t_{SU;DAT}$	100			ns	
Hold Time, $t_{HD;DAT}$	300			ns	
Stop Condition Setup Time, $t_{SU;STO}$	600			ns	
Bus Free Time Between a Stop and a Start, t_{BUF}	1300			ns	

ABSOLUTE MAXIMUM RATINGS

Table 13.

Parameter	Rating
V_S to GND	−0.3 V to +3.6 V
REFCLK to GND	−0.3 V to V_S + 0.3 V
LDO to GND	−0.3V to V_S + 0.3 V
XT1, XT2 to GND	−0.3 V to V_S + 0.3 V
SSCG, MAX_BW, MARGIN, SCL, SDA, REFSEL to GND	−0.3 V to V_S + 0.3 V
REFOUT, OUTxP, OUTxN to GND	−0.3 V to V_S + 0.3 V
Junction Temperature[1]	150°C
Storage Temperature	−65°C to+150°C
Lead Temperature (10 sec)	300°C

[1] See the Thermal Characteristics section for θ_{JA}.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Thermal impedance measurements were taken on a 4-layer board in still air in accordance with EIA/JESD51-7.

Table 14. Thermal Resistance

Package Type	θ_{JA}	Unit
40-Lead LFCSP	27.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

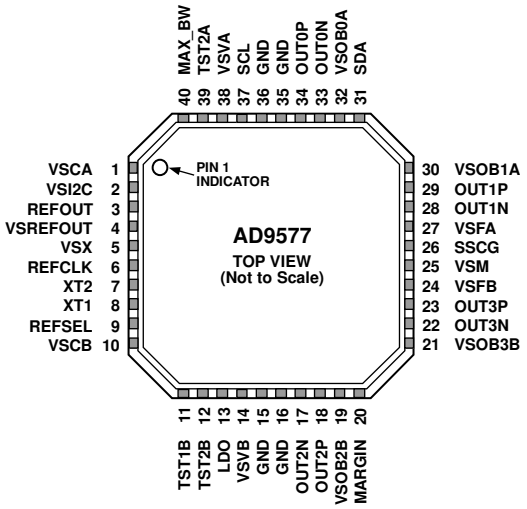

Figure 5. Pin Configuration

Table 15. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VSCA	PLL1 Power Supply.
2	VSI2C	I^2C Digital Power Supply.
3	REFOUT	CMOS Reference Output.
4	VSREFOUT	Reference Output Buffer Power Supply.
5	VSX	Crystal Oscillator and Input Reference Power Supply.
6	REFCLK	Reference Clock Input. Tie low when not in use.
7, 8	XT2, XT1	External 19.44 MHz to 27 MHz Crystal. Leave unconnected when not in use.
9	REFSEL	Logic Input. Use this pin to select the reference source. Internal 30 kΩ pull-up resistor.
10	VSCB	PLL2 Analog Power Supply.
11	TST1B	Test Pin. Connect this pin to Pin 13 (LDO).
12	TST2B	Test Pin. Connect this pin to Pin 13 (LDO).
13	LDO	This pin is for bypassing the PLL2 LDO to ground with a 220 nF capacitor.
14	VSVB	PLL2 VCO Power Supply.
15, 16, 35, 36	GND	Ground.
17	OUT2N	LVPECL/LVDS/CMOS Clock Output.
18	OUT2P	LVPECL/LVDS/CMOS Clock Output.
19	VSOB2B	Output Port OUT2 Power Supply.
20	MARGIN	Logic 1 sets the margining frequency on the clock output pins. Internal 30 kΩ pull-down resistor.
21	VSOB3B	Output Port OUT3 Power Supply.
22	OUT3N	LVPECL/LVDS/CMOS Clock Output.
23	OUT3P	LVPECL/LVDS/CMOS Clock Output.
24	VSFB	PLL2 Analog Power Supply.
25	VSM	PLL2 Digital Power Supply.
26	SSCG	Logic 1 enables spread spectrum operation of PLL2. Internal 30 kΩ pull-down resistor.
27	VSFA	PLL1 Analog Power Supply.
28	OUT1N	LVPECL/LVDS/CMOS Clock Output.
29	OUT1P	LVPECL/LVDS/CMOS Clock Output.

Pin No.	Mnemonic	Description
30	VSOB1A	Output Port OUT1 Power Supply.
31	SDA	Serial Data Line for I²C.
32	VSOB0A	Output Port OUT0 Power Supply.
33	OUT0N	LVPECL/LVDS/CMOS Clock Output.
34	OUT0P	LVPECL/LVDS/CMOS Clock Output.
37	SCL	Serial Clock for I²C.
38	VSVA	PLL1 VCO Power Supply.
39	TST2A	Test Pin. Connect this pin to the printed circuit board (PCB) ground plane.
40	MAX_BW	Logic 1 widens the loop bandwidth of the fractional-N PLL during spread spectrum. Internal 30 kΩ pull-down resistor.
	EPAD	The exposed paddle on this package is an electrical connection as well as a thermal enhancement. For the device to function properly, the paddle must be attached to ground (GND). It is recommended that a minimum of nine vias be used to connect the paddle to the printed circuit board (PCB) ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

REFOUT AND PLL1 PHASE NOISE PERFORMANCE

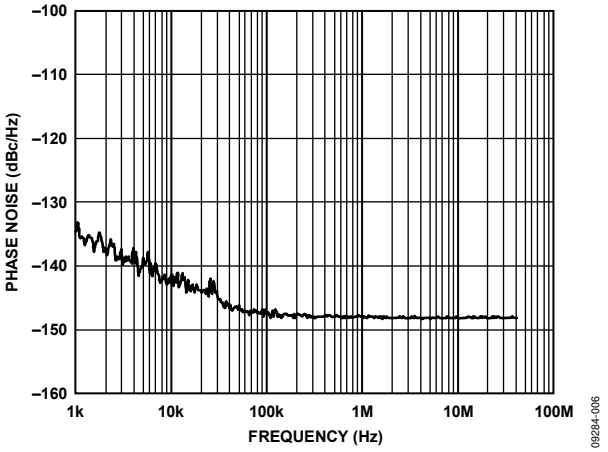

Figure 6. Phase Noise, REFOUT Output, 25 MHz (f_{XTAL} = 25 MHz)

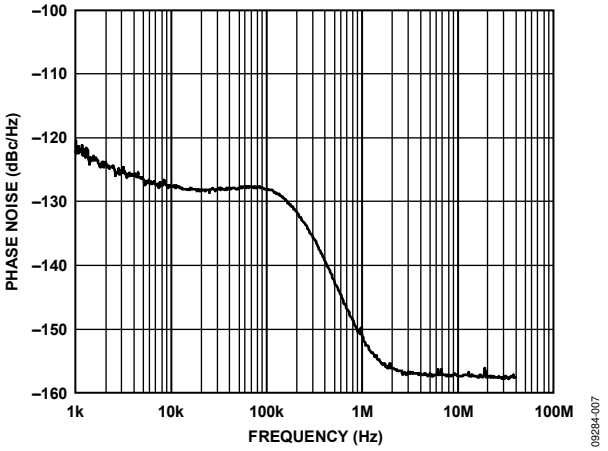

Figure 7. Phase Noise, PLL1, OUT0 LVPECL, 106.25 MHz, Integer-N Mode (f_{XTAL} = 25 MHz, Na = 102, V0 = 4, D0 = 6)

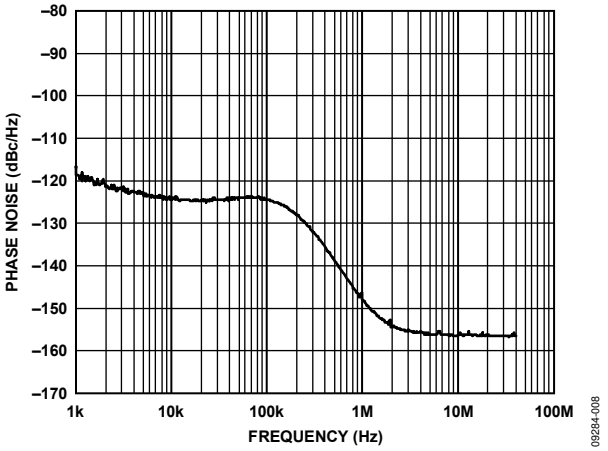

Figure 8. Phase Noise, PLL1, OUT0 LVPECL, 156.25 MHz Integer-N Mode (f_{XTAL} = 25 MHz, Na = 100, V0 = 4, D0 = 4)

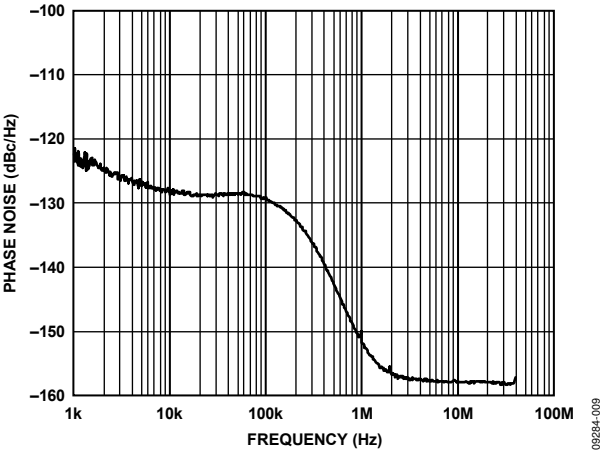

Figure 9. Phase Noise, PLL1, OUT0 LVPECL, 100 MHz, Integer-N Mode (f_{XTAL} = 25 MHz, Na = 100, V0 = 5, D0 = 5)

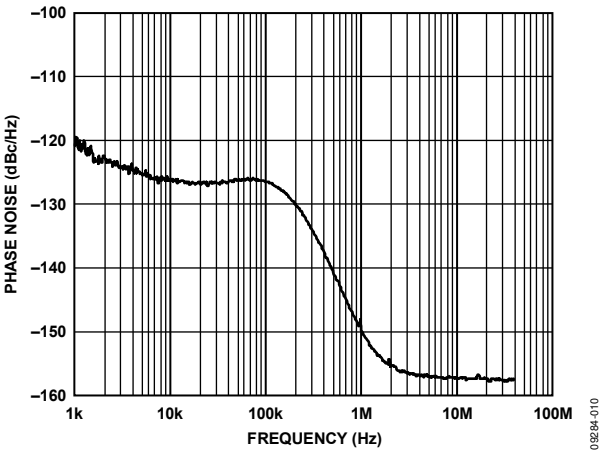

Figure 10. Phase Noise, PLL1, OUT0 LVPECL, 125 MHz, Integer-N Mode (f_{XTAL} = 25 MHz, Na = 100, V0 = 4, D0 = 5)

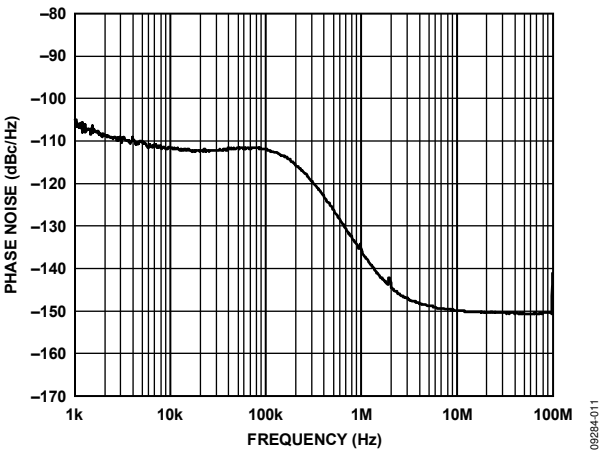

Figure 11. Phase Noise, PLL1, OUT0 LVPECL, 625 MHz, Integer-N Mode (f_{XTAL} = 25 MHz, Na = 100, V0 = 2, D0 = 2)

PLL2 PHASE NOISE PERFORMANCE

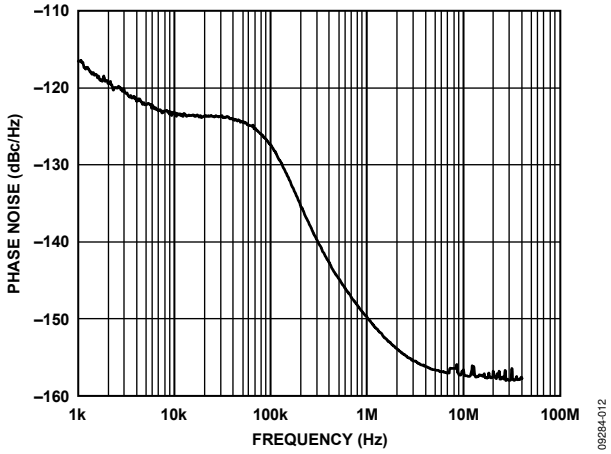

Figure 12. Phase Noise, PLL2, OUT2 LVPECL, 100 MHz, Integer-N Mode (f_{XTAL} = 25 MHz, Nb = 100, V2 = 5, D2 = 5)

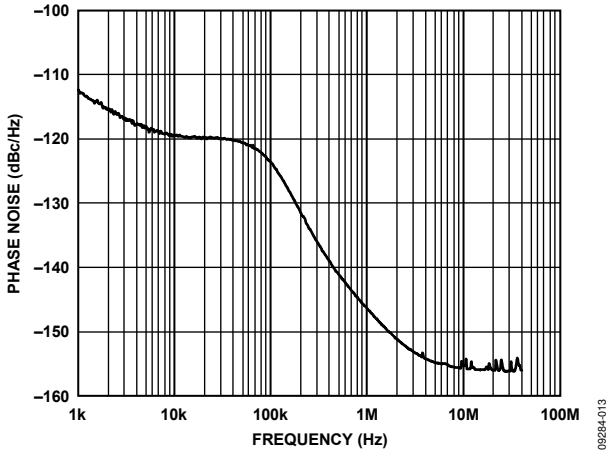

Figure 13. Phase Noise, PLL2, OUT2 LVPECL, 156.25 MHz, Integer-N Mode (f_{XTAL} = 25 MHz, Nb = 100, V2 = 4, D2 = 4)

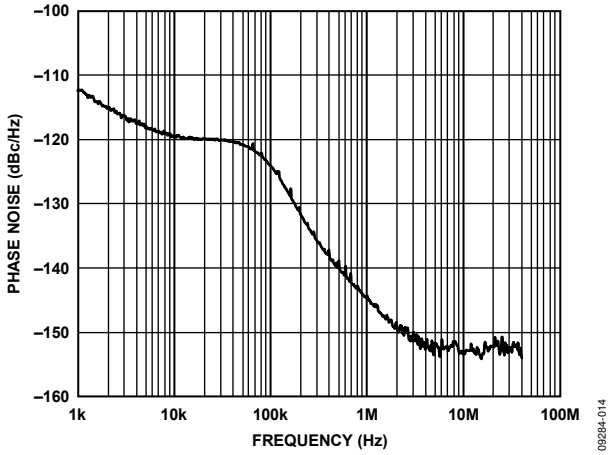

Figure 14. Phase Noise, PLL2, OUT2 LVPECL, 155.52 MHz, Fractional-N Mode (f_{XTAL} = 25 MHz, Nb = 99, FRAC = 333, MOD = 625, V2 = 2, D2 = 8), Spurs Disabled

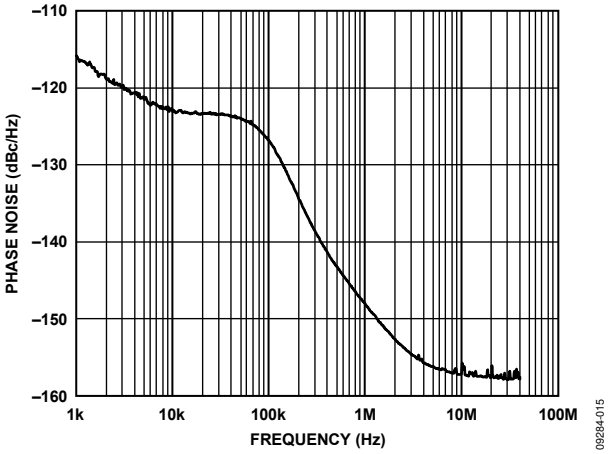

Figure 15. Phase Noise, PLL2, OUT2 LVPECL, 106.25 MHz, Integer-N Mode (f_{XTAL} = 25 MHz, Nb = 102, V2 = 4, D2 = 6)

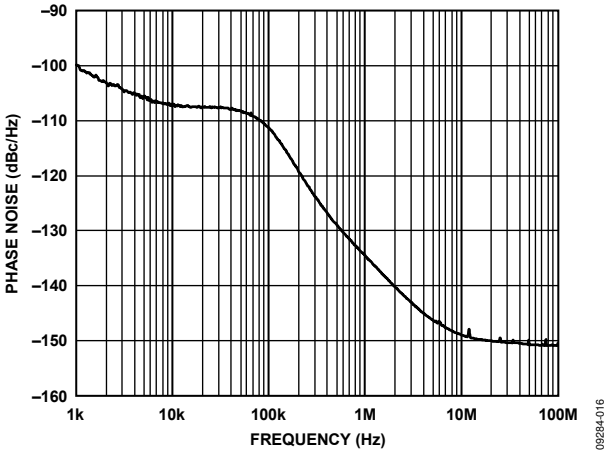

Figure 16. Phase Noise, PLL2, OUT2 LVPECL, 625 MHz, Integer-N Mode (f_{XTAL} = 25 MHz, Nb = 100, V2 = 2, D2 = 2)

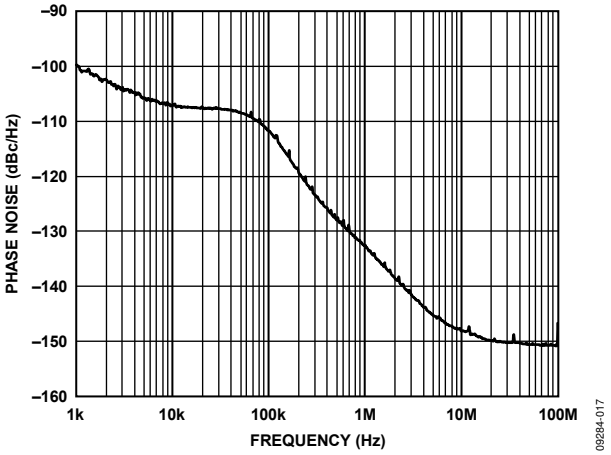

Figure 17. Phase Noise, PLL2, OUT2 LVPECL, 622.08 MHz, Fractional-N Mode (f_{XTAL} = 25 MHz, Nb = 99, FRAC = 333, MOD = 625, V2 = 2, D2 = 2), Spurs Disabled

OUTPUT JITTER

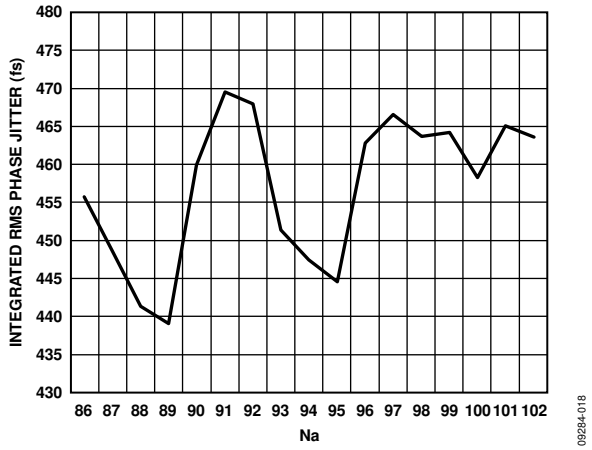

Figure 18. Typical Integrated Random Phase Jitter in fs rms for PLL1 and OUT0P LVPECL as Feedback Divider Value Na Swept (f_{XTAL} = 25 MHz, V0 = 5, D0 = 5)

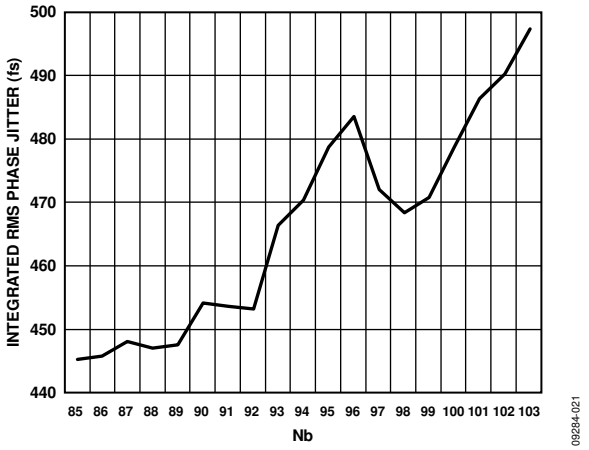

Figure 19. Typical Integrated Random Phase Jitter in fs rms for PLL2 and OUT2P LVPECL as Feedback Divider Value Nb Swept (f_{XTAL} = 25 MHz, V2 = 5, D2 = 5, Integer-N Mode)

TYPICAL OUTPUT SIGNAL

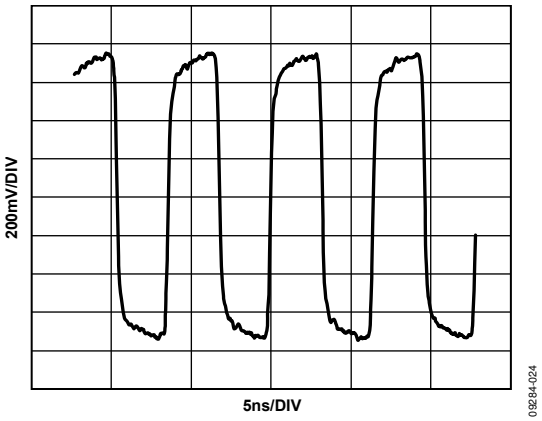

Figure 20 Typical LVPECL Differential Output Trace, 156.25 MHz

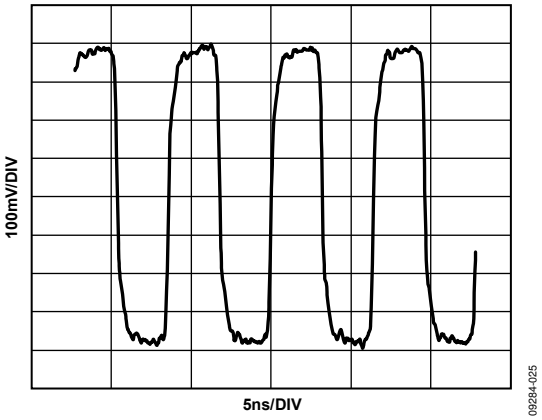

Figure 21. Typical LVDS Differential Output Trace, 156.25 MHz

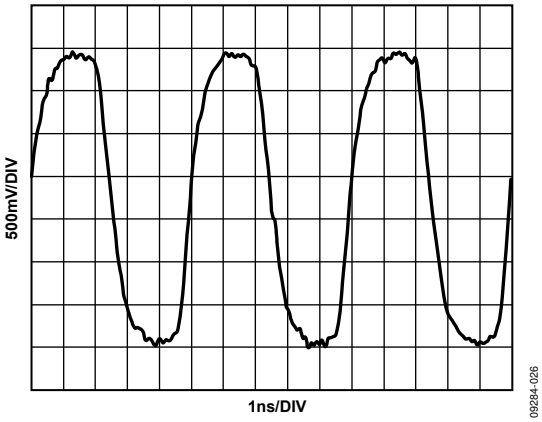

Figure 22. Typical CMOS Output Trace, 200MHz

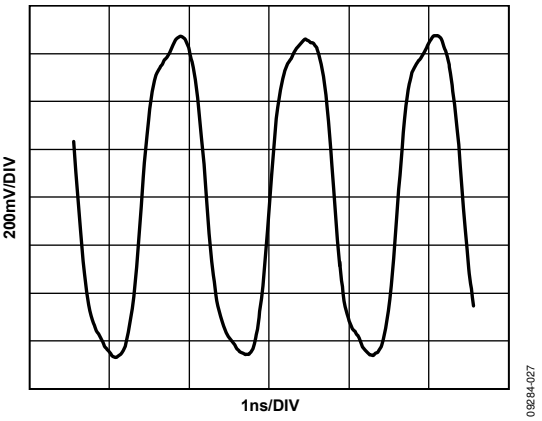

Figure 23. Typical LVPECL Differential Output Trace, 625 MHz

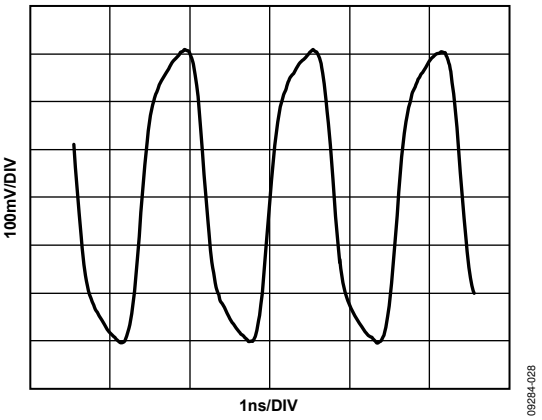

Figure 24. Typical LVDS Differential Output Trace, 625 MHz

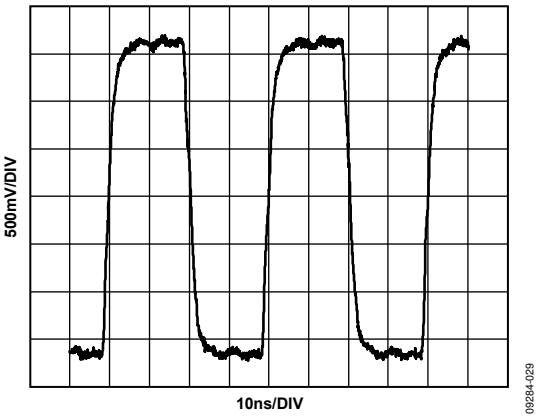

Figure 25. Typical REFOUT Output Trace, 25 MHz

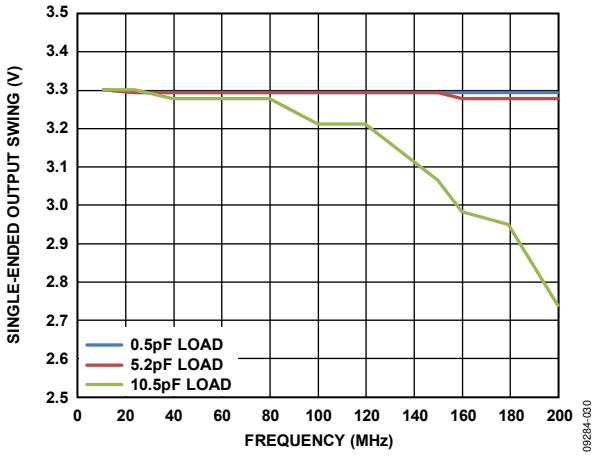

Figure 26. CMOS Single-Ended, Peak-to-Peak Output Swing vs. Frequency, for Loads of 0.5 pF, 5.2 pF, and 10.5 pF, Measured with a Tektronix P7313 Active Probe

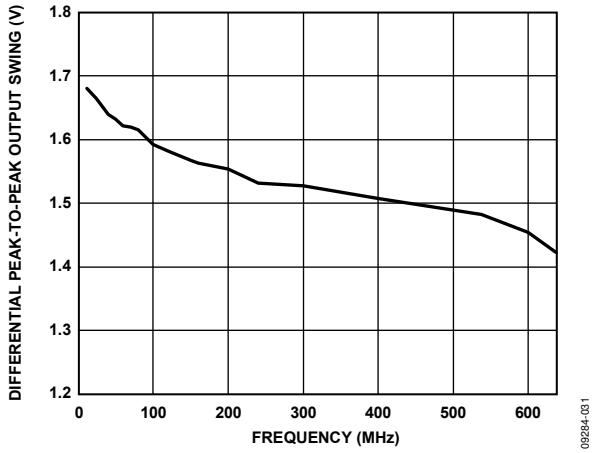

Figure 27. LVPECL Differential, Peak-to-Peak Output Swing vs. Frequency

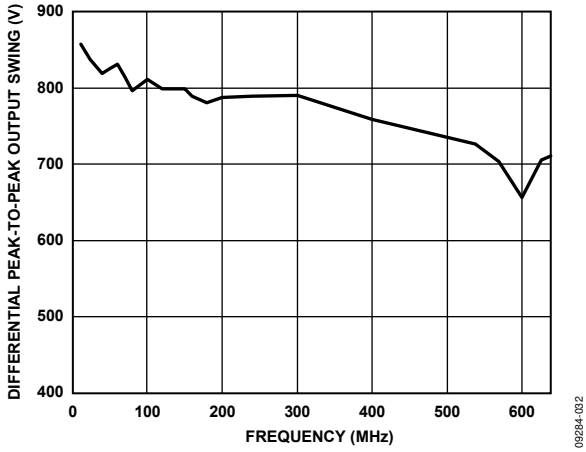

Figure 28. LVDS Differential, Peak-to-Peak Output Swing vs. Frequency

TYPICAL SPREAD SPECTRUM PERFORMANCE CHARACTERISTICS

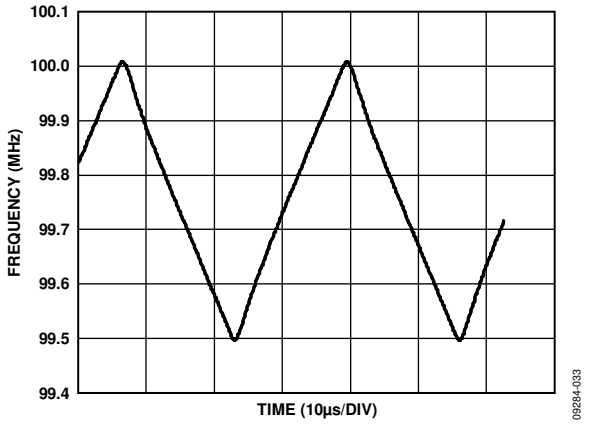

Figure 29. Typical Spread Spectrum Frequency Modulation Profile OUT2, Nb = 96, FRAC = 0, MOD = 1000, CkDiv = 7, NumSteps = 59, FracStep = −8, f_{OUT} = 100 MHz with −0.5% Downspread at 30.2 kHz, MAX_BW set to 0

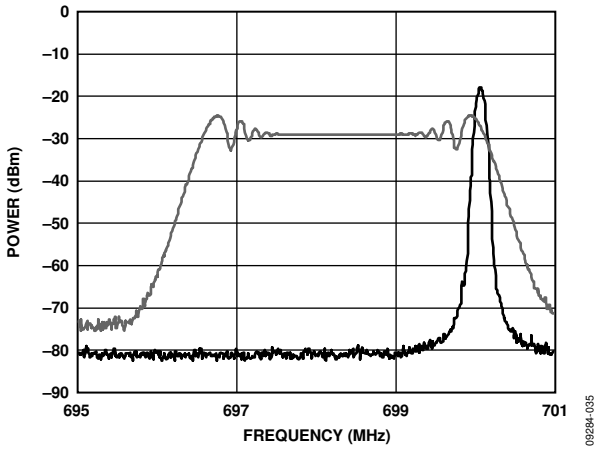

Figure 31. Typical Nonspread and Spread Spectrum Power Spectra, OUT2, Nb = 96, FRAC = 0, MOD = 1000, CkDiv = 7, NumSteps = 59, FracStep = −8, f_{OUT} = 100 MHz with −0.5% Downspread at 30.2 kHz, MAX_BW set to 0, Seventh Harmonic Shown, Spectrum Analyzer Resolution Bandwidth = 120 kHz, Maximum Hold On

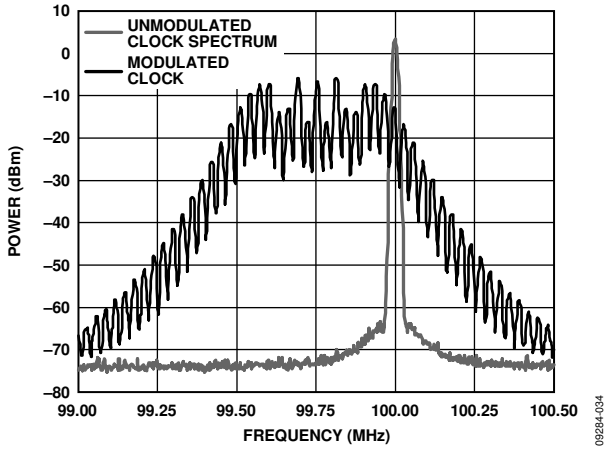

Figure 30. Typical Nonspread and Spread Spectrum Power Spectra, OUT2, Nb = 96, FRAC = 0, MOD = 1000, CkDiv = 7, NumSteps = 59, FracStep = −8, f_{OUT} = 100 MHz with −0.5% Downspread at 30.2 kHz, MAX_BW set to 0, First Harmonic Shown, Spectrum Analyzer Resolution Bandwidth =10 kHz, Maximum Hold On