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Dual PLL Precision Synthesizer

Data Sheet **AD9578**

FEATURES

- Any output frequency precision synthesis
  - 11.8 MHz to 919 MHz
  - Better than 0.1 ppb frequency resolution
- Ultralow rms jitter (12 kHz to 20 MHz)
  - <300 fs rms using integer synthesis
  - <405 fs rms using fractional synthesis
- Dual reference inputs support LVPECL, LVDS, 1.8 V LVCMOS, or fundamental mode AT cut crystals from 22 MHz to 54 MHz or reference clocks from 20 MHz to 60 MHz
- Numerical (NCO) frequency control
  - Dynamically pullable output frequency enables FPGA-based PLLs (HDL available)
  - Fast serial peripheral interface (SPI) bus write speeds up to 100 MHz
  - On-the-fly frequency changes
- Dual PLL in compact 7 mm × 7 mm package
  - Replaces multiple large clock ICs, PLLs, fanout buffers, crystal oscillators (XOs), and voltage controlled crystal oscillators (VCXOs)
- Mix and match output buffers
  - In-circuit programmable LVPECL/LVDS/HCSL/LVCMOS
  - Independent buffer (VDDOx) drives multiple technologies
- Enhanced power supply noise rejection

APPLICATIONS

- FPGA-based jitter attenuators and low jitter PLLs
- Precision disciplined clocks and clock synthesizers
- Multirate clock synthesizers
- Optical: OTN/SDH/SONET
- Broadcast video: 3G SDI, HD SDI, SDI
- Networking and storage: Ethernet/SAS/Fibre Channel
- Wireless infrastructure: OBSAI/CPRI
- Industrial: IEEE 1588
- Numerically controlled oscillators (NCOs)

GENERAL DESCRIPTION

The AD9578 is a programmable synthesizer intended for jitter attenuation and asynchronous clocking applications in high performance telecommunications, networking, data storage, serializer/deserializer (SERDES), and physical layer (PHY) applications. The device incorporates two low jitter PLLs that provide any frequency with precision better than 0.1 ppb, each with two separate output dividers, for a total of four programmable outputs, delivering maximum flexibility and jitter performance. Each output is independently programmable to provide frequencies of up to 919 MHz with <410 fs typical rms jitter (12 kHz to 20 MHz) utilizing compact, low cost fundamental mode crystals (XTALs) that enable a robust supply chain. Using integer frequency synthesis, the AD9578 is capable of achieving rms jitter as low as 290 fs.

The AD9578 is packaged with a factory programmed default power-on configuration. After power-on, all settings including output frequency are reconfigurable through a fast SPI.

The AD9578 architecture permits it to be used as a numerically controlled oscillator (NCO). This allows the user to dynamically change the frequency using the fast SPI bus. FPGAs and other devices can take advantage of this function to implement digital PLLs with configurable loop bandwidths for jitter attenuation applications, precision disciplined clocks that lock to tight stability references, or digitally controlled precision timing applications, such as network timing and IEEE 1588 applications. The SPI bus can operate up to 50 MHz, enabling fast FPGA loops while multiple devices share the same bus. The AD9578 can also be used in multirate precision applications, such as broadcast video or OTN. HDL FPGA code for digital PLL applications is available from Analog Devices, Inc.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

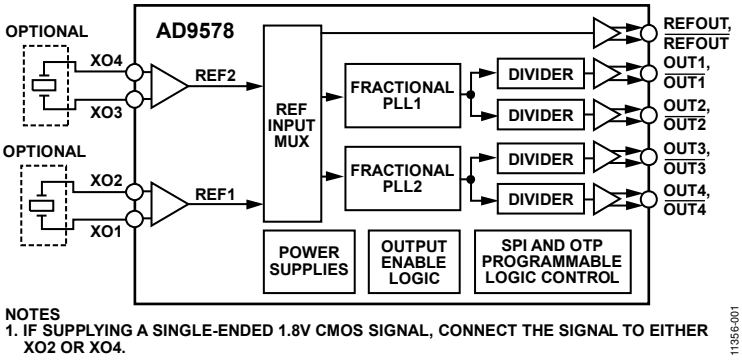

Figure 1.

Rev. B
Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
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EVALUATION KITS

- AD9578 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9578: Dual PLL Precision Synthesizer Data Sheet

DESIGN RESOURCES

- AD9578 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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REVISION HISTORY

1/2017—Rev. A to Rev. B

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10/2016—Rev. 0 to Rev. A

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Added Exposed Pad Notation to Outline Dimensions 44

10/2014—Revision 0: Initial Version

SPECIFICATIONS

SUPPLY VOLTAGE AND CURRENT (2.5 V OPERATION)

V_{DD} = 2.5 V ± 5%, T_A = −25°C to +85°C.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE	V_{DD}	2.375	2.50	2.625	V	
SUPPLY CURRENT	I_{DD}	229	247	265	mA	Using typical configuration in Table 3
		337	365	388	mA	Using all blocks running configuration in Table 3

SUPPLY VOLTAGE AND CURRENT (3.3 V OPERATION)

V_{DD} = 3.3 V ± 10%, T_A = −25°C to +85°C.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE	V_{DD}	2.97	3.30	3.63	V	
	V_{PROG}	5.25	5.5	V_{DD} + 2.5	V	$\overline{CS}$ pin only; used only for one time programmable (OTP) programming; perform OTP programming only with V_{DD} = 3.3 V
SUPPLY CURRENT	I_{DD}		252	268	mA	Using typical configuration in Table 3
			373	397	mA	Using all blocks running configuration in Table 3

POWER DISSIPATION

V_{DD} = 2.5 V ± 5%, T_A = −25°C to +85°C. Maximum power is at V_{DD} = 2.625 V and is usually 11% higher than typical.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION					
Typical Configuration		618	696	mW	XTAL: 25 MHz REFOUT driver: disabled PLL1: one LVPECL driver at 644.53125 MHz PLL2: one single-ended LVCMOS driver (with 80 pF load) at 100 MHz
All Blocks Running		913	1018	mW	XTAL: 49.152 MHz XTAL on both XTAL inputs REFOUT driver: LVPECL mode, 49.152 MHz PLL1: two LVPECL drivers at 693.812 MHz PLL2: two LVPECL drivers at 693.812 MHz
Full Power-Down		67	75	mW	$\overline{PD1}$ pin grounded; Register 0x02 = 0x015555 to disable remainder of chip
Incremental Power Dissipation					Starting with typical configuration; change in power due to the indicated operation
Crystal Reference On/Off		25		mW	
PLL On/Off		259		mW	PLL1 or PLL2 on/off, including output drivers or channel dividers
Output Distribution Driver On/Off					
HCSL (at 644.53 MHz)		75		mW	Each output of a differential pair has 50 Ω to ground
LVDS (at 644.53 MHz)		43		mW	100 Ω across differential pair
LVPECL (at 644.53 MHz)		107		mW	50 Ω to V_{DD} − 2 V
3.3 V LVCMOS (at 25 MHz)		75		mW	A single 3.3 V LVCMOS output with an 80 pF load

LOGIC INPUTS ($\overline{CS}$, $\overline{PD1}$, OEREF, OE1, OE2, OE3, OE4)

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS ($\overline{CS}$ in OTP FUNCTION)					Specifications apply to the $\overline{CS}$ pin while in OTP programming mode
Input Voltage (V_{PROG})	5.25	5.5	V_{DD} + 2.5	V	See V_{PROG} definition in Table 1; OTP programming must be done with V_{DD} = 3.3 V
Input Current		20	25	mA	Current consumed during OTP programming
Time to OTP Program	800			µs	Time required per bit programmed
LOGIC INPUTS ($\overline{PD1}$, OEREF, OE1, OE2, OE3, OE4, $\overline{CS}$)					Numbers are valid for V_{DD} = 2.5 V and 3.3 V
Input Voltage					
High (V_{IH})	2.2			V	
Low (V_{IL})			0.8	V	
Input Current (I_{INH}, I_{INL})		38	60	µA	
Input Capacitance (C_{IN})		3		pF	

REFERENCE INPUTS (XO1, XO2, XO3, XO4)

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE INPUT DRIVEN BY CRYSTAL RESONATOR					
Crystal Resonator Frequency Range	20		60	MHz	Fundamental mode, AT cut crystal
Crystal Motional Resistance			100	Ω	Guaranteed by design
REFERENCE INPUT DRIVEN BY A DIFFERENTIAL CLOCK					This input is a source follower and must be either dc-coupled 1.8 V LVCMOS on the XO2 or XO4 pin, or ac-coupled
Input Frequency Range	20		60	MHz	Assumes ac-coupled LVDS (494 mV p-p across the differential pair)
Input Slew Rate	133			V/µs	Minimum limit imposed for jitter performance
Differential Input Voltage Sensitivity	250			mV p-p	Minimum voltage across pins required to ensure switching between logic states; the instantaneous voltage on either pin must not exceed the supply rails; can accommodate single-ended input by ac grounding of complementary input
REFERENCE INPUT DRIVEN BY A SINGLE-ENDED CLOCK					The XO2 pin (for PLL1) and XO4 pin (for PLL2) input accepts dc-coupled 1.8 V LVCMOS
Input Frequency Range	20		60	MHz	DC-coupled
Input Slew Rate	67			V/µs	Minimum limit imposed for jitter performance
Single-Ended Input (XO2, XO4 Pins Only)					
Input Voltage				V	
High (V_{IH})	1.48				
Low (V_{IL})			0.98	V	

DISTRIBUTION CLOCK OUTPUTS (INCLUDING REFOUT/$\overline{\text{REFOUT}}$)

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
3.3 V LVPECL MODE					V_{DD} = 3.3V; 50 Ω to V_{DD} − 2 V termination at output pins
Output Frequency	11.8		919	MHz	REFOUT/$\overline{\text{REFOUT}}$ limited to 60 MHz
Rise Time (20% to 80%)		130	183	ps	
Fall Time (80% to 20%)		142	203	ps	
Duty Cycle, OUTPUT1 and OUTPUT4					
111.8 ≤ f_{OUT} ≤ 357 MHz	50	52	54	%	Output divider settings other than 4.5
357 < f_{OUT} ≤ 919 MHz	43	47	51	%	Output divider settings other than 4.5
Output Divider = 4.5	46	50	54	%	Measured at 765 MHz
Duty Cycle, OUTPUT2 and OUTPUT3					
111.8 ≤ f_{OUT} ≤ 357 MHz	49	51	53	%	Output divider settings other than 4.5
357 < f_{OUT} ≤ 919 MHz	45	49	51	%	Output divider settings other than 4.5
Output Divider = 4.5	51	57	63	%	Measured at 765 MHz
Differential Output Voltage Swing	700	850	1000	mV	Voltage across pins at minimum output frequency; if a differential probe is used, peak-to-peak voltage (V_{PP}) is 2× this value
Common-Mode Output Voltage	1.81	1.91	2.01	V	
2.5 V LVPECL MODE					V_{DD} = 2.5 V; 50 Ω to V_{DD} − 2 V termination at output pins
Output Frequency	11.8		919	MHz	REFOUT/$\overline{\text{REFOUT}}$ limited to 60 MHz
Rise Time (20% to 80%)		137	186	ps	
Fall Time (80% to 20%)		148	209	ps	
Duty Cycle, OUTPUT1 and OUTPUT4					
111.8 ≤ f_{OUT} ≤ 357 MHz	50	52	54	%	Output divider settings other than 4.5
357 < f_{OUT} ≤ 919 MHz	49	51	54	%	Output divider settings other than 4.5
Output Divider = 4.5	46	50	54	%	Measured at 765 MHz
Duty Cycle, OUTPUT2 and OUTPUT3					
111.8 ≤ f_{OUT} ≤ 357 MHz	43	48	51	%	Output divider settings other than 4.5
357 < f_{OUT} ≤ 919 MHz	44	48	52	%	Output divider settings other than 4.5
Output Divider = 4.5	51	57	63	%	Measured at 765 MHz
Differential Output Voltage Swing	700	850	1000	mV	Voltage across pins at minimum output frequency; if a differential probe is used, V_{PP} is 2× this value
Common-Mode Output Voltage	1.05	1.15	1.25	V	
3.3 V HCSL MODE					50 Ω to ground termination at output pins
Output Frequency	11.8		919	MHz	REFOUT/$\overline{\text{REFOUT}}$ limited to 60 MHz
Rise Time (20% to 80%)		180	266	ps	
Fall Time (80% to 20%)		186	286	ps	
Duty Cycle, OUTPUT1 and OUTPUT4					
111.8 ≤ f_{OUT} ≤ 357 MHz	51	52	54	%	Output divider settings other than 4.5
357 < f_{OUT} ≤ 919 MHz	48	51	54	%	Output divider settings other than 4.5
Output Divider = 4.5	49	52	56	%	Measured at 765 MHz
Duty Cycle, OUTPUT2 and OUTPUT3					
111.8 ≤ f_{OUT} ≤ 357 MHz	50	53	54	%	Output divider settings other than 4.5
357 < f_{OUT} ≤ 919 MHz	48	51	53	%	Output divider settings other than 4.5
Output Divider = 4.5	53	59	67	%	Measured at 765 MHz
Output High Voltage	624	750	850	mV	
Output Low Voltage	−50	0	+50	mV	
Output Voltage Swing (V_{SWING})	624	750	850	mV	Voltage across pins at minimum output frequency; when a differential probe is used, V_{PP} is 2× this value
Absolute Crossing Point (V_{OX})	295	360	400	mV	
Short-Circuit Output Current		14	17	mA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
2.5 V HCSL MODE					50 Ω to ground termination at output pins
Output Frequency	11.8		919	MHz	REFOUT/$\overline{\text{REFOUT}}$ limited to 60 MHz
Rise Time (20% to 80%)					
OUTPUT1, OUTPUT2, OUTPUT3		199	275	ps	Output divider settings other than 4.5
OUTPUT4		243	370	ps	Output divider settings other than 4.5
Fall Time (80% to 20%)					
OUTPUT1, OUTPUT2, OUTPUT3		191	287	ps	Output divider settings other than 4.5
OUTPUT4		226	329	ps	Output divider settings other than 4.5
Duty Cycle, OUTPUT1 and OUTPUT4					
111.8 ≤ f_{OUT} ≤ 357 MHz	50	52	54	%	Output divider settings other than 4.5
357 < f_{OUT} ≤ 919 MHz	47	50	53	%	Output divider settings other than 4.5
Output Divider = 4.5	39	52	55	%	Measured at 765 MHz
Duty Cycle, OUTPUT2 and OUTPUT3					
111.8 ≤ f_{OUT} ≤ 357 MHz	50	52	54	%	Output divider settings other than 4.5
357 < f_{OUT} ≤ 919 MHz	48	50	53	%	Output divider settings other than 4.5
Output Divider = 4.5	45	59	65	%	Measured at 765 MHz
Output High Voltage	624	750	850	mV	
Output Low Voltage	-50	0	50	mV	
Output Voltage Swing (V_{SWING})	624	750	850	mV	Voltage across pins at minimum output frequency; if a differential probe is used, V_{PP} is 2× this value
Absolute Crossing Point (V_{OX})	295	360	400	mV	
Short-Circuit Output Current		14	17	mA	
LVDS MODE (V_{DD} = 3.3 V and 2.5 V)					100 Ω termination across the output pair
Output Frequency	11.8		919	MHz	REFOUT/$\overline{\text{REFOUT}}$ limited to 54 MHz
Rise Time (20% to 80%)		173	215	ps	
Fall Time (80% to 20%)		177	223	ps	
OUTPUT1 and OUTPUT4 Duty Cycle					
111.8 ≤ f_{OUT} ≤ 357 MHz	50	52	54	%	Output divider settings other than 4.5
357 < f_{OUT} ≤ 919 MHz	46	50	54	%	Output divider settings other than 4.5
Output Divider = 4.5	49	52	55	%	Measured at 765 MHz
OUTPUT2 and OUTPUT3 Duty Cycle					
111.8 ≤ f_{OUT} ≤ 357 MHz	50	52	54	%	Output divider settings other than 4.5
357 < f_{OUT} ≤ 919 MHz	46	50	53	%	Output divider settings other than 4.5
Output Divider = 4.5	51	59	66	%	Measured at 765 MHz
Differential Output Voltage Swing					
Balanced, V_{OD}	247		454	mV	Voltage across pins at minimum output frequency; if a differential probe is used, V_{PP} is 2× this value
Unbalanced, ΔV_{OD}			50	mV	Absolute difference between voltage swing of true pin and complementary pin
Offset Voltage					
Common Mode, V_{OS}	1.08	1.26	1.375	V	
Common-Mode Difference, ΔV_{OS}			50	mV	Voltage difference between pins at minimum output frequency
Short-Circuit Output Current		16	24	mA	
LVCMOS MODE (V_{DD} = 3.3 V and 2.5 V)					
Output Frequency	11.8		250	MHz	REFOUT limited to 60 MHz
Rise Time (20% to 80%)					Capacitor load (C_{LOAD}) = 10 pF
330 Ω Pull-Down Resistor		1.3	1.9	ns	
3.3 kΩ Pull-Down Resistor		1.2	1.7	ns	
Fall Time (20% to 80%)					C_{LOAD} = 10 pF
330 Ω Pull-Down Resistor		1.3	2	ns	
3.3 kΩ Pull-Down Resistor		1.5	2.4	ns	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Duty Cycle (20% to 80%)				ns	C_{LOAD} = 10 pF
330 Ω Pull-Down Resistor	43	52	62	%	
3.3 kΩ Pull-Down Resistor	44	53	63	%	
Output Voltage High (V_{OH})					At minimum output frequency; outputs terminated 50 Ω to V_{DD}/2
V_{DD} = 3.3 V	3.0	3.1	3.35	V	
V_{DD} = 2.5 V	1.9	2.0	2.1	V	
Output Voltage Low (V_{OL})					At minimum output frequency; outputs terminated 50 Ω to V_{DD}/2
V_{DD} = 3.3 V	0.22	0.32	0.42	V	
V_{DD} = 2.5 V	0.2	0.3	0.4	V	
OUTPUT TIMING SKEW					OUTPUT2 lags OUTPUT1; OUTPUT3 lags OUTPUT4
LVPECL					
Between OUTPUT1 and OUTPUT2 Drivers		90		ps	LVPECL mode on both drivers; rising edge only; any divide value
Between OUTPUT3 and OUTPUT4 Drivers		102		ps	LVPECL mode on both drivers; rising edge only; any divide value
LVDS					
Between OUTPUT1 and OUTPUT2 Drivers		94		ps	LVDS mode on both drivers; rising edge only; any divide value
Between OUTPUT3 and OUTPUT4 Drivers		100		ps	LVDS mode on both drivers; rising edge only; any divide value
HCSL					
Between OUTPUT1 and OUTPUT2 Drivers		48		ps	HCSL mode on both drivers; rising edge only; any divide value
Between OUTPUT3 and OUTPUT4 Drivers		59		ps	HCSL mode on both drivers; rising edge only; any divide value
LVCMOS					
Between OUTPUT1 and OUTPUT2 Drivers		64		ps	LVCMOS mode on both drivers; rising edge only; any divide value
Between OUTPUT3 and OUTPUT4 Drivers		59		ps	LVCMOS mode on both drivers; rising edge only; any divide value

SERIAL PORT

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{CS}$					See Table 4 for using $\overline{CS}$ while in OTP programming mode
Input Voltage					
Logic 1	2.2			V	
Logic 0			1.2	V	
Input Current		44		µA	
Logic 1					
Logic 0		88		µA	
Input Capacitance		2		pF	
SCK					Internal 30 kΩ pull-down resistor
Input Voltage					
Logic 1	2.2			V	
Logic 0		0.8	1.2	V	
Input Current					
Logic 1		200		µA	
Logic 0		1		µA	
Input Capacitance		2		pF	
SDI					
Input Voltage					
Logic 1	2.2			V	
Logic 0			1.2	V	
Input Current					
Logic 1		1		µA	
Logic 0		1		µA	
Input Capacitance		2		pF	
SDO/LOL					
Output Logic 1 Voltage	V_{DD} – 0.6			V	1 mA load current
Output Logic 0 Voltage			0.4	V	1 mA load current
TIMING					See Figure 2
SCK					
Clock Rate, $1/t_{CLK}$			50	MHz	SDO/LOL pin maximum speed may be limited by excess capacitance on the receiver connected to the SDO/LOL pin
Write Only			100	MHz	
Pulse Width High, t_{HIGH}	2			ns	
Pulse Width Low, t_{LOW}	2			ns	
SDI to SCK Setup, t_{DS}	1.5			ns	
SCK to SDI Hold, t_{DH}	2			ns	
SCK to Valid SDO, t_{DV}			8	ns	SDO function of SDO/LOL pin (see Figure 33)
$\overline{CS}$ to SCK Setup, t_S	65			ns	$\overline{CS}$ is normally held low during a complete SPI transaction
$\overline{CS}$ to SCK Hold, t_C	0			ns	
$\overline{CS}$ Minimum Pulse Width High	65			ns	

Timing Diagram

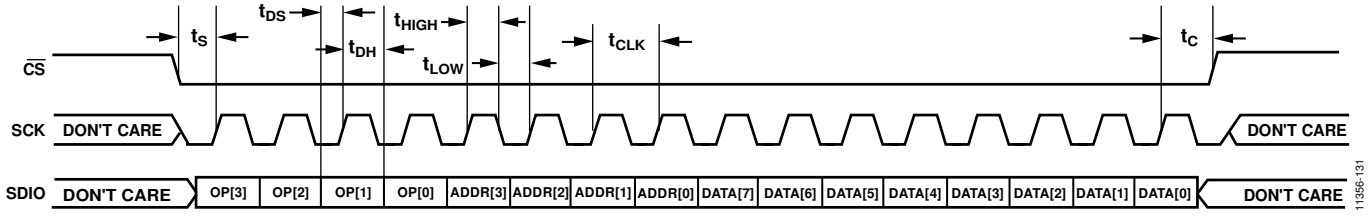


Figure 2. Serial Port Timing Diagram

DIGITAL PLL

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY STEP SIZE	0.1			ppb	

DIGITAL FUNCTIONS TIMING

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OTP PROGRAMMING TIME, PER BIT	0.8	1	2	ms	See Table 4 for using $\overline{CS}$ while in OTP programming mode (the AD9578 has 444 bits; therefore, the total programming time is <1 sec)
POWER-ON RESET TIME	4			ms	Do not access serial port during power-on reset.

JITTER GENERATION USING 49.152 MHZ CRYSTAL

Both PLLs are generating the same output frequency and use a 49.152 MHz crystal for the input reference. The loop bandwidth is set to the default value of 300 kHz. Where multiple driver types are listed, there is no significant difference between driver types.

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
JITTER GENERATION					Fractional mode on, f_{REF} = 49.152 MHz XTAL
LVPECL, HCSL, LVDS Driver					
f_{OUT} = 622.08 MHz					
Bandwidth: 12 kHz to 20 MHz		320		fs rms	
Bandwidth: 20 kHz to 80 MHz		370		fs rms	
f_{OUT} = 693.48 MHz					
Bandwidth: 12 kHz to 20 MHz		403		fs rms	
Bandwidth: 20 kHz to 80 MHz		408		fs rms	
f_{OUT} = 174.703 MHz					
Bandwidth: 12 kHz to 20 MHz		403		fs rms	
Bandwidth: 20 kHz to 80 MHz		410		fs rms	
f_{OUT} = 161.1328 MHz					
Bandwidth: 12 kHz to 20 MHz		361		fs rms	
Bandwidth: 20 kHz to 80 MHz		363		fs rms	
LVPECL, HCSL, LVDS, LVCMOS Driver					
f_{OUT} = 156.25 MHz					
Bandwidth: 12 kHz to 20 MHz		350		fs rms	
Bandwidth: 1.875 MHz to 20 MHz		77		fs rms	
Bandwidth: 20 kHz to 80 MHz		352		fs rms	

JITTER GENERATION USING 25 MHZ SQUARE WAVE

Both PLLs are generating the same output frequency and use a 25 MHz square wave for the input reference. The loop bandwidth is set to the default value of 300 kHz. Where multiple driver types are listed, there is no significant difference between driver types. Fractional mode turned on, unless otherwise stated.

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
JITTER GENERATION					f_{REF} = 25 MHz square wave
LVPECL, HCSL, LVDS Driver					
f_{OUT} = 622.08 MHz					
Bandwidth: 12 kHz to 20 MHz		515		fs rms	
Bandwidth: 20 kHz to 80 MHz		516		fs rms	
f_{OUT} = 693.48 MHz					
Bandwidth: 12 kHz to 20 MHz		504		fs rms	
Bandwidth: 20 kHz to 80 MHz		505		fs rms	
f_{OUT} = 174.703 MHz					
Bandwidth: 12 kHz to 20 MHz		517		fs rms	
Bandwidth: 20 kHz to 80 MHz		523		fs rms	
f_{OUT} = 161.1328 MHz					
Bandwidth: 12 kHz to 20 MHz		527		fs rms	
Bandwidth: 20 kHz to 80 MHz		530		fs rms	
LVPECL, HCSL, LVDS, LVCMOS Driver					
f_{OUT} = 156.25 MHz					Integer mode operation
Bandwidth: 12 kHz to 20 MHz		290		fs rms	
Bandwidth: 1.875 MHz to 20 MHz		61		fs rms	
Bandwidth: 20 kHz to 80 MHz		292		fs rms	

ABSOLUTE MAXIMUM RATINGS

Table 12.

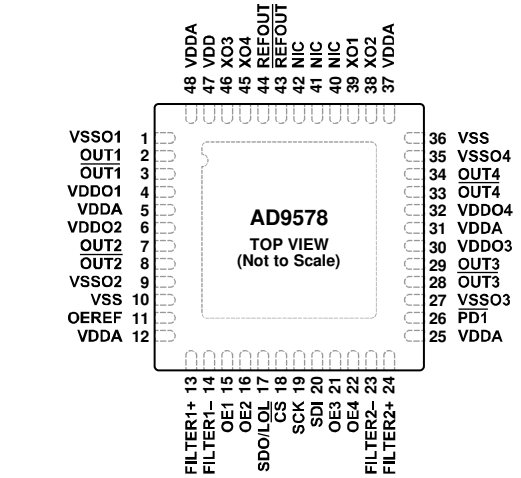
Parameter	Rating
Supply Voltage (V_{DD})	4.6 V
Inputs (V_{IN}) (Except for $\overline{CS}$ Pin)	−0.50 V to V_{DD} + 0.5 V
$\overline{CS}$ Pin	V_{DD} + 2.5 V
Outputs (V_{OUT})	−0.50 V to V_{DD} + 0.5 V
Operating Temperature Range (T_A) Industrial	−25°C to +85°C
Storage Temperature Range (T_S)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NOT INTERNALLY CONNECTED. LEAVE THIS PIN UNCONNECTED.
2. THE EXPOSED PAD ON THE BOTTOM OF THE PACKAGE MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

11356-002

Figure 3. Pin Configuration

Table 13. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	VSSO1	Negative power	Return Path Ground for Clock Output 1.
2	OUT1	Output	Clock Output 1 Derived from PLL1. Supports frequencies up to the device maximum. OUT1 is a selectable[1] pin. When used in LVCMOS mode, OUT1 is the active pin.
3	$\overline{\text{OUT1}}$	Output	Active Low Clock Output 1 Derived from PLL1. Supports frequencies up to the device maximum. $\overline{\text{OUT1}}$ is a selectable[1] pin. $\overline{\text{OUT1}}$ is not used in LVCMOS mode; it is high-Z in LVCMOS mode.
4	VDDO1	Supply, positive power	Power Supply for Clock Output 1.
5, 12, 25, 31, 37, 48	VDDA	Supply, positive power	2.5 V or 3.3 V Analog Power Supply.
6	VDDO2	Supply, positive power	Power Supply for Clock Output 2.
7	OUT2	Output	Clock Output 2 Derived from PLL1. Supports frequencies up to the device maximum. OUT2 is a selectable[1] pin. When used in LVCMOS mode, OUT2 is the active pin.
8	$\overline{\text{OUT2}}$	Output	Active Low Clock Output 2 Derived from PLL1. Supports frequencies up to the device maximum. $\overline{\text{OUT1}}$ is a selectable[1] pin. $\overline{\text{OUT2}}$ is not used in LVCMOS mode; it is high-Z in LVCMOS mode.
9	VSSO2	Negative power	Return Path Ground for Clock Output 2.
10, 36	VSS	Negative power	Device Ground.
11	OEREF	Input	Output Enable for REFOUT and $\overline{\text{REFOUT}}$ Pins, LVCMOS. Active high. This pin has an internal 75 kΩ pull-down resistor.
13	FILTER1+	Filter	Phase-Locked Loop 1 (PLL1) Filter Node, Positive Side. Connect a 220 nF capacitor between this pin and Pin 14.
14	FILTER1−	Filter	PLL1 Filter Node, Negative Side. Connect a 220 nF capacitor between this pin and Pin 13.
15	OE1	Input	Output Enable 1 for Clock Output 1, LVCMOS. Places OUT1 and $\overline{\text{OUT1}}$ in a high-Z state. Active high. This pin has an internal 75 kΩ pull-up resistor.
16	OE2	Input	Output Enable 2 for Clock Output 2, LVCMOS. Places OUT2 and $\overline{\text{OUT2}}$ in a high-Z state. Active high. This pin has an internal 75 kΩ pull-up resistor.
17	SDO/LOL	Output	Serial Data Output for SPI Control/Loss of Lock, LVCMOS.
18	$\overline{\text{CS}}$	Input	Chip Select for SPI Control, LVCMOS. Active low. When this pin is set to 5 V, OTP programming is enabled (see Table 4 and the OTP Programming section). This pin has an internal 75 kΩ pull-up resistor.
19	SCK	Input	Serial Clock Input for SPI Control, LVCMOS.

Pin No.	Mnemonic	Type	Description
20	SDI	Input	Serial Data Input for SPI Control, LVCMOS.
21	OE3	Input	Output Enable 3 for Clock Output 3, LVCMOS. Places OUT3 and $\overline{\text{OUT3}}$ in a high-Z state. Active high is the default but active low is programmable. This pin has an internal 75 kΩ pull-up resistor.
22	OE4	Input	Output Enable 4 for Clock Output 4, LVCMOS. Places OUT4 and $\overline{\text{OUT4}}$ in a high-Z state. Active high is the default but active low is programmable. This pin has an internal 75 kΩ pull-up resistor.
23	FILTER2−	Filter	PLL2 Filter Node, Negative Side. Connect a 220 nF capacitor between this pin and Pin 24.
24	FILTER2+	Filter	PLL2 Filter Node, Positive Side. Connect a 220 nF capacitor between this pin and Pin 23.
26	$\overline{\text{PD1}}$	Input	Active Low Power-Down for PLL1, LVCMOS. This pin has an internal 75 kΩ pull-up resistor.
27	VSSO3	Negative power	Return Path Ground for Clock Output 3.
28	$\overline{\text{OUT3}}$	Output	Active Low Clock Output 3 Derived from PLL2. Supports frequencies up to the device maximum. $\overline{\text{OUT3}}$ is a selectable[1] pin. $\overline{\text{OUT3}}$ is not used in LVCMOS mode; it is high-Z in LVCMOS mode.
29	OUT3	Output	Clock Output 3 Derived from PLL2. Supports frequencies up to the device maximum. OUT3 is a selectable[1] pin. When used in LVCMOS mode, OUT3 is the active pin.
30	VDDO3	Supply, positive power	Power Supply for Clock Output 3.
32	VDDO4	Supply, positive power	Power Supply for Clock Output 4.
33	$\overline{\text{OUT4}}$	Output	Clock Output 4 Derived from PLL2. Supports frequencies up to the device maximum. $\overline{\text{OUT4}}$ is not used in LVCMOS mode and is high-Z. $\overline{\text{OUT4}}$ is a selectable[1] pin.
34	OUT4	Output	Clock Output 4 Derived from PLL2. Supports frequencies up to the device maximum. OUT4 is a selectable[1] pin. When used in LVCMOS mode, OUT4 is the active pin.
35	VSSO4	Negative power	Return Path Ground for Clock Output 4.
38	XO2	Input	Reference Input 1. Connect a crystal across this pin and XO1. Alternatively, the user can connect a 1.8 V LVCMOS clock to this pin only, or connect a differential, ac-coupled LVDS or LVPECL signal across this pin and the XO1 pin. This pin can be a crystal or reference input.
39	XO1	Input	Complementary Reference Input 1. Connect a crystal across this pin and XO2. Alternatively, the user can connect a differential, ac-coupled LVDS or LVPECL signal to this pin and the XO2 pin. This pin can be a crystal or reference input.
40, 41, 42	NIC		No Internal Connection. Leave these pins unconnected.
43	$\overline{\text{REFOUT}}$	Output	Active Low Reference Clock Output. This pin provides a copy of the reference input or crystal input frequency. $\overline{\text{REFOUT}}$ is a selectable[1] pin.
44	REFOUT	Output	Reference Clock Output. This pin provides a copy of the reference input or crystal input frequency. REFOUT is a selectable[1] pin.
45	XO4	Input	Reference Input 2. Connect a crystal across this pin and XO3. Alternatively, connect a 1.8 V LVCMOS clock to this pin only, or connect a differential, ac-coupled LVDS or LVPECL signal across this pin and the XO3 pin. This pin can be a crystal or reference input.
46	XO3	Input	Complementary Reference Input 2. Connect a crystal across this pin and XO4. Alternatively, connect a differential, ac-coupled LVDS or LVPECL signal to this pin and the XO4 pin.
47	VDD	Supply, positive power	2.5 V or 3.3 V Power Supply for Device Core. This pin can be a crystal or reference input.
	EPAD		Exposed Pad. The exposed pad on the bottom of the package must be connected to ground for proper operation.

[1] Selectable pins are factory programmed to a default power-up configuration. The user can override the default programming to support LVCMOS, LVDS, LVPECL, or HCSL mode after power-up using the SPI.

TYPICAL PERFORMANCE CHARACTERISTICS

f_R is the input reference clock frequency; f_{OUT} is the output clock frequency; V_{DD} at nominal supply voltage (3.3 V). 25 MHz square wave input is a dc-coupled 3.3 V LVCMOS signal with 0.8 ns (20% to 80%) rise time.

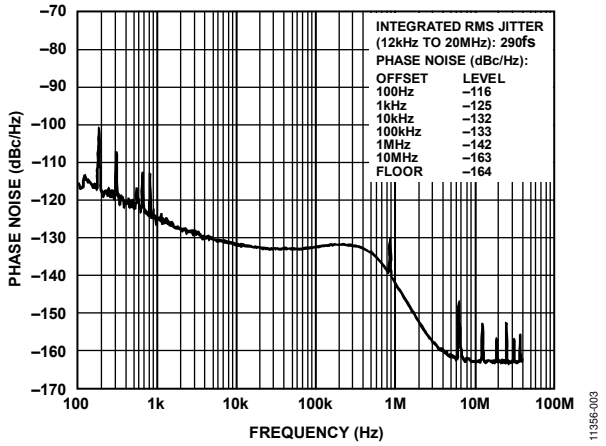


Figure 4. Absolute Phase Noise (Output Driver = LVDS), f_R = 25 MHz Square Wave, f_{OUT} = 156.25 MHz on Both PLLs

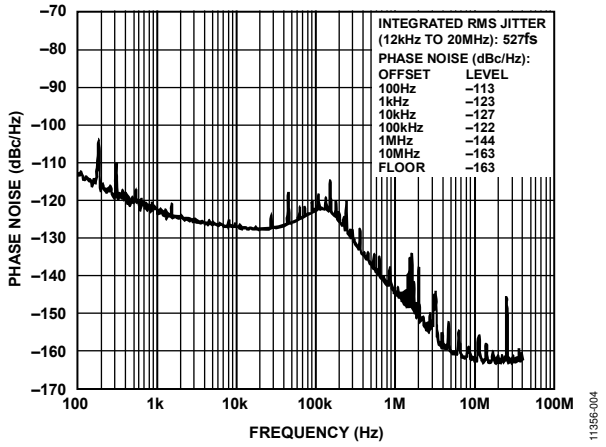


Figure 5. Absolute Phase Noise (Output Driver = LVCMOS), f_R = 25 MHz Square Wave, f_{OUT} = 161.1328125 MHz on Both PLLs

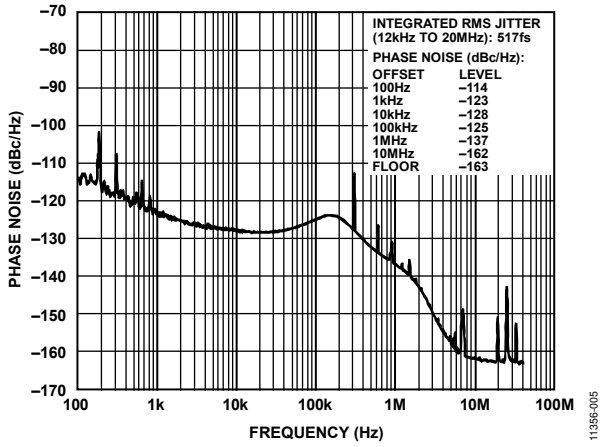


Figure 6. Absolute Phase Noise (Output Driver = LVPECL), f_R = 25 MHz Square Wave, f_{OUT} = 174.703 MHz on Both PLLs

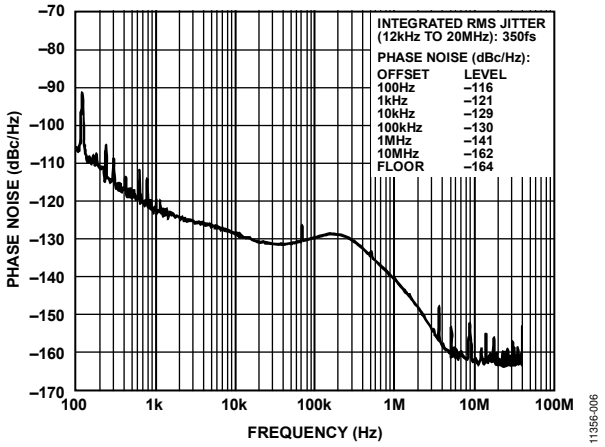


Figure 7. Absolute Phase Noise (Output Driver = LVDS), f_R = 49.152 MHz Crystal, f_{OUT} = 156.25 MHz on Both PLLs

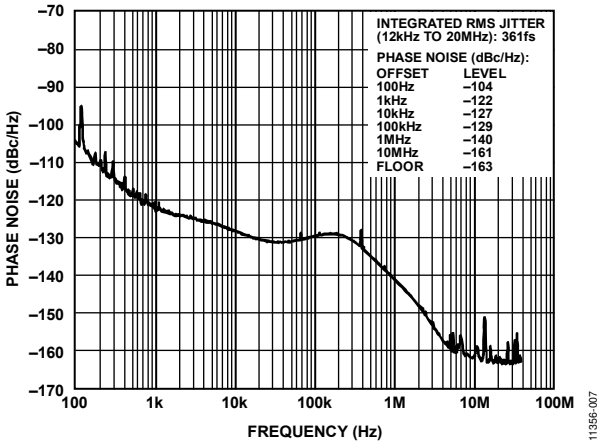


Figure 8. Absolute Phase Noise (Output Driver = 3.3.V LVCMOS), f_R = 49.152 MHz Crystal, f_{OUT} = 161.1328125 MHz on Both PLLs

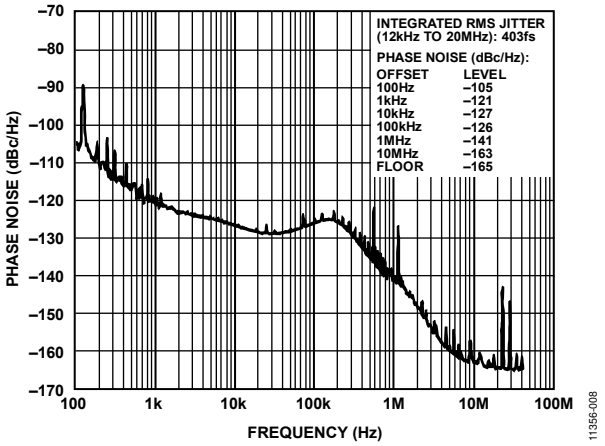


Figure 9. Absolute Phase Noise (Output Driver = LVPECL), f_R = 49.152 MHz Crystal, f_{OUT} = 174.703 MHz on Both PLLs

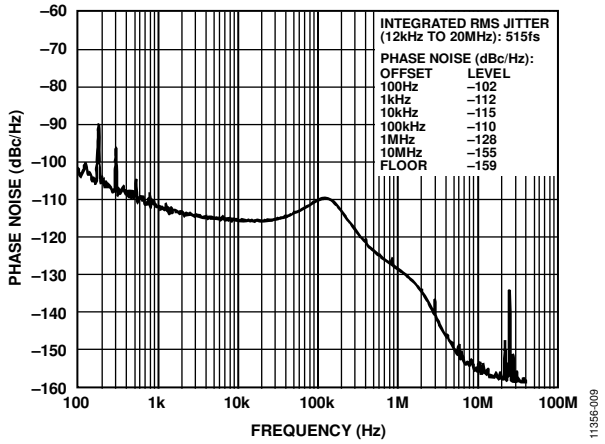


Figure 10. Absolute Phase Noise (Output Driver = LVPECL), f_R = 25 MHz 3.3 V LVCMOS Square Wave, f_{OUT} = 622.08 MHz on Both PLLs

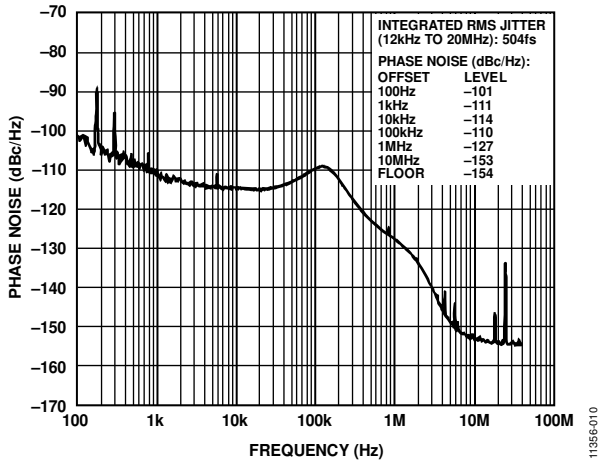


Figure 11. Absolute Phase Noise (Output Driver = LVPECL), f_R = 25 MHz Square Wave, f_{OUT} = 693.482991 MHz on Both PLLs

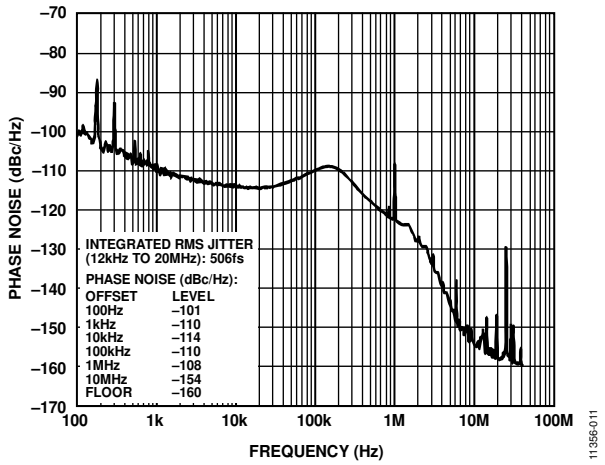


Figure 12. Absolute Phase Noise (Output Driver = LVPECL), f_R = 25 MHz Square Wave on XO1/XO2 Pins, f_{OUT} = 919 MHz on Both PLLs

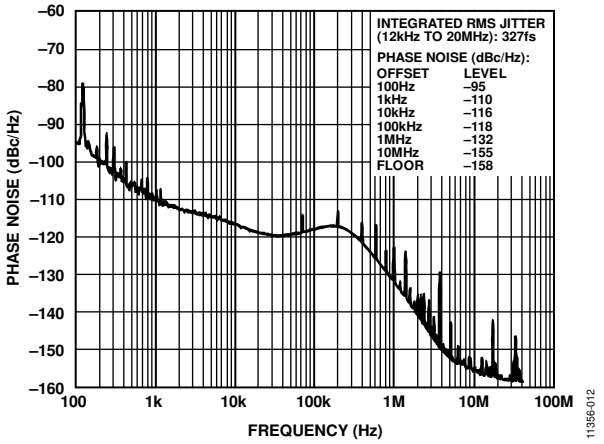


Figure 13. Absolute Phase Noise (Output Driver = LVPECL), f_R = 49.152 MHz Crystal, f_{OUT} = 622.08 MHz on Both PLLs

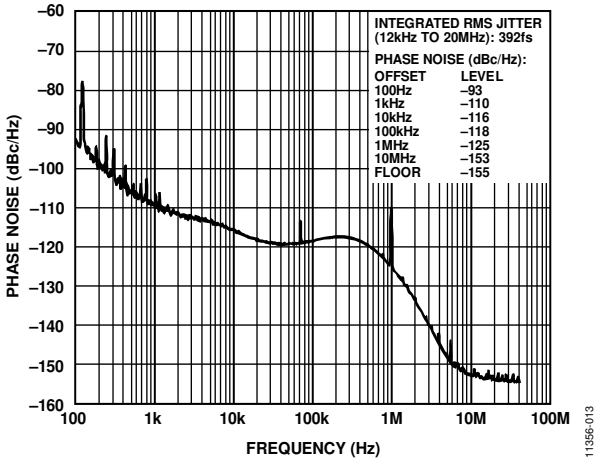


Figure 14. Absolute Phase Noise (Output Driver = LVPECL), f_R = 49.152 MHz Crystal, f_{OUT} = 693.482991 MHz on Both PLLs

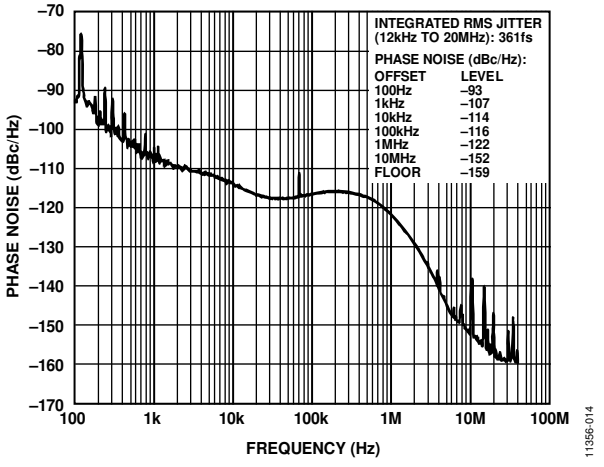


Figure 15. Absolute Phase Noise (Output Driver = LVPECL), f_R = 49.152 MHz Crystal, f_{OUT} = 919 MHz on Both PLLs

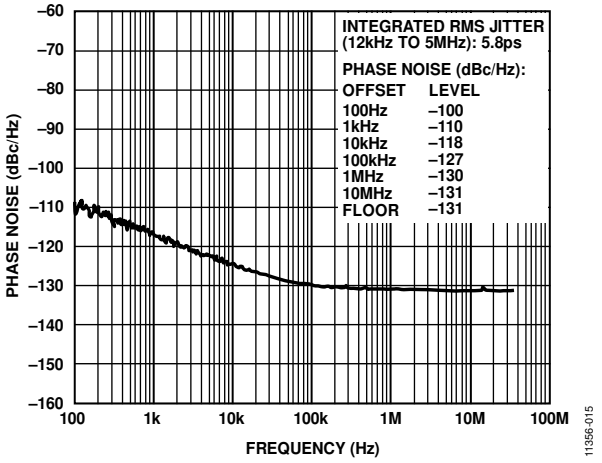


Figure 16. Phase Noise of 25 MHz, 3.3 V LVCMOS Input Clock Used

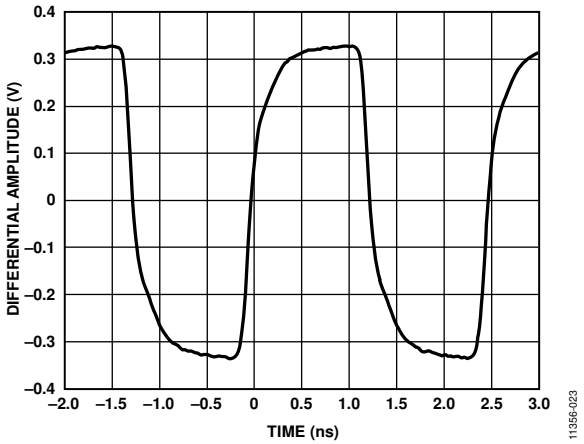


Figure 17. Output Waveform, LVDS (400 MHz)

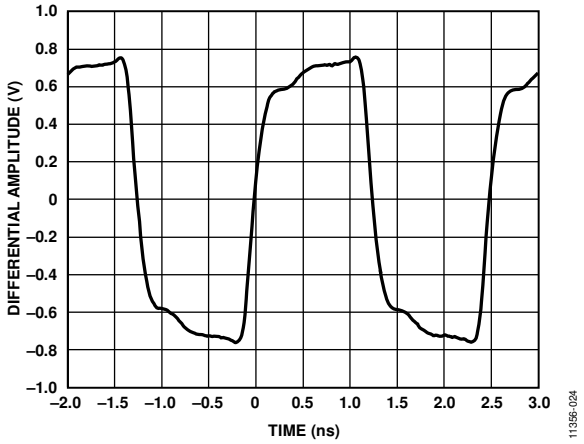


Figure 18. Output Waveform, HCSL (400 MHz)

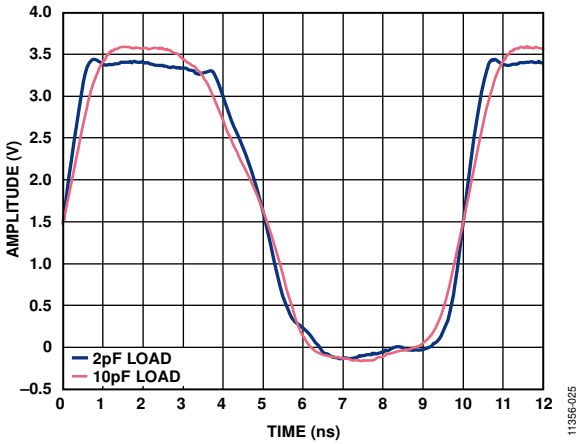


Figure 19. Output Waveform, 3.3 V CMOS (100 MHz)

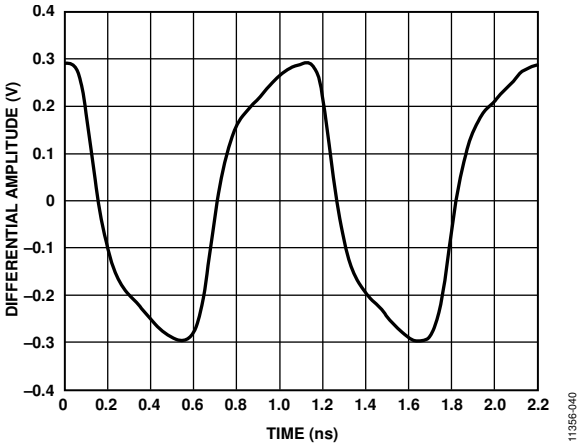


Figure 20. Output Waveform, LVDS (900 MHz)

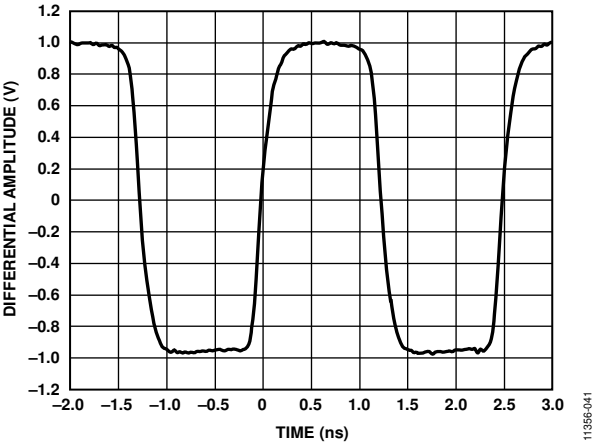


Figure 21. Output Waveform, LVPECL (400 MHz)

TEST SETUP AND CONFIGURATION CIRCUITS

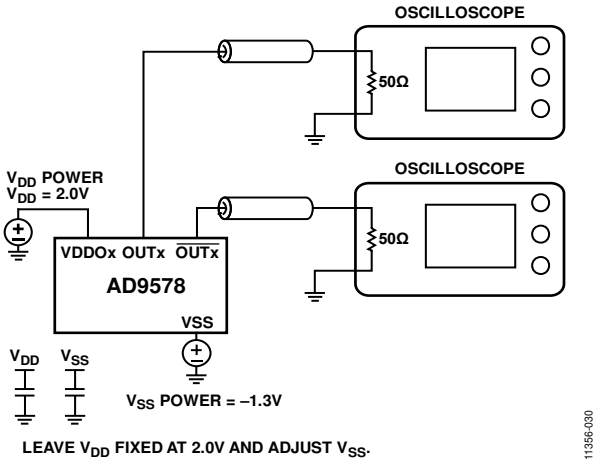


Figure 22. LVPECL Test Circuit

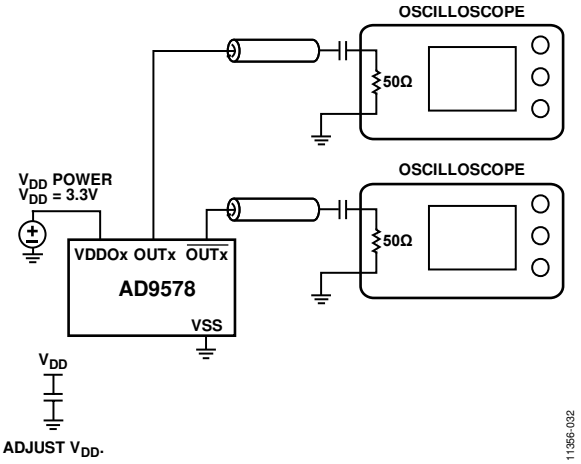


Figure 24. LVDS Test Circuit

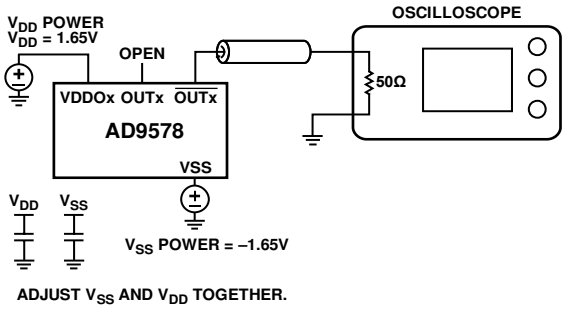


Figure 23. LVCMOS Test Circuit

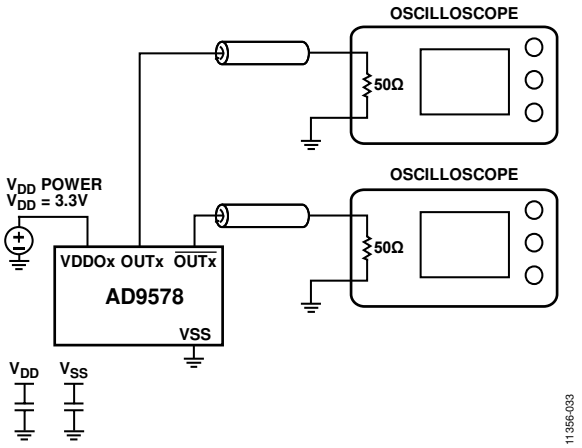


Figure 25. HCSL Test Circuit

INPUT/OUTPUT TERMINATION RECOMMENDATIONS

See Figure 26 to Figure 30 for recommendations on how to connect the outputs.

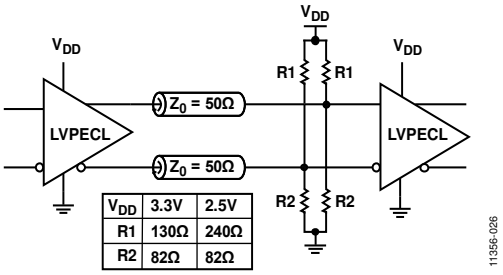


Figure 26. Thevenin Equivalent DC-Coupled LVPECL Termination

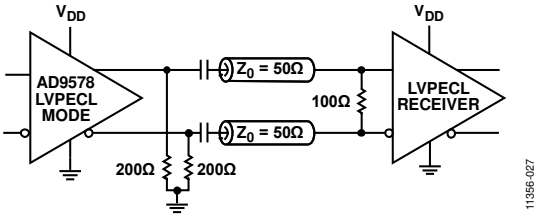


Figure 27. AC-Coupled LVPECL Termination

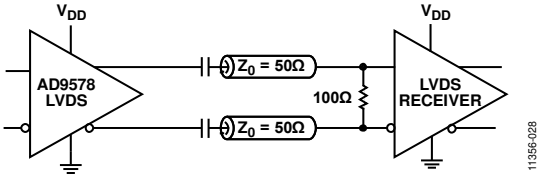


Figure 28. AC-Coupled LVDS

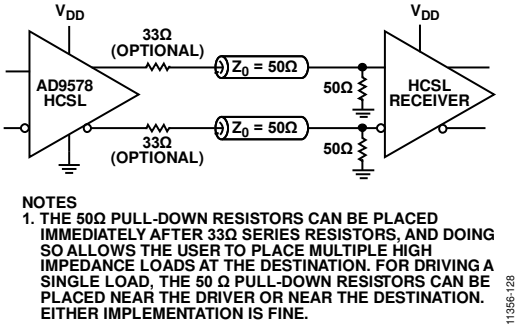


Figure 29. DC-Coupled HCSL

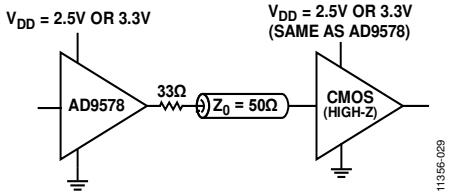


Figure 30. DC-Coupled LVCMOS Termination

GETTING STARTED

CHIP POWER MONITOR AND STARTUP

The AD9578 monitors the voltage on the power supplies at power-up. When power supplies are greater than 2.1 V ± 0.1 V, the device generates an internal reset pulse, at which time, the AD9578 loads the values programmed in OTP memory. Do not use the SPI until 4 ms after power-up to ensure that all registers are correctly loaded from the OTP memory and that all internal voltages are stable.

It is possible for the user to overwrite any value stored in the OTP memory if the security bits in Register 0x00 were not set at the time the OTP programming occurred. Take care not to overwrite the factory programmed calibrations (Register 11 through Register 14).

When programming the device through the serial port, write unused or reserved bits to their default values as listed in the register map.

DEVICE REGISTER PROGRAMMING USING A REGISTER SETUP FILE

The evaluation software contains a programming wizard and a convenient graphical user interface that assists the user in determining the optimal configuration for the device. It generates a register setup file with a .STP extension that is easily readable using a text editor. These registers can be loaded directly into the AD9578.

OTP PROGRAMMING

The AD9578 has 444 bits of OTP memory. OTP stores the nonvolatile default configuration used on power-up.

The default configuration is determined and programmed by the user. Use the SPI to overwrite these bits and change the operation of the AD9578 after power-up. The SPI Programming section describes how the bits affect the device operation and how to use the SPI to modify them.

THEORY OF OPERATION

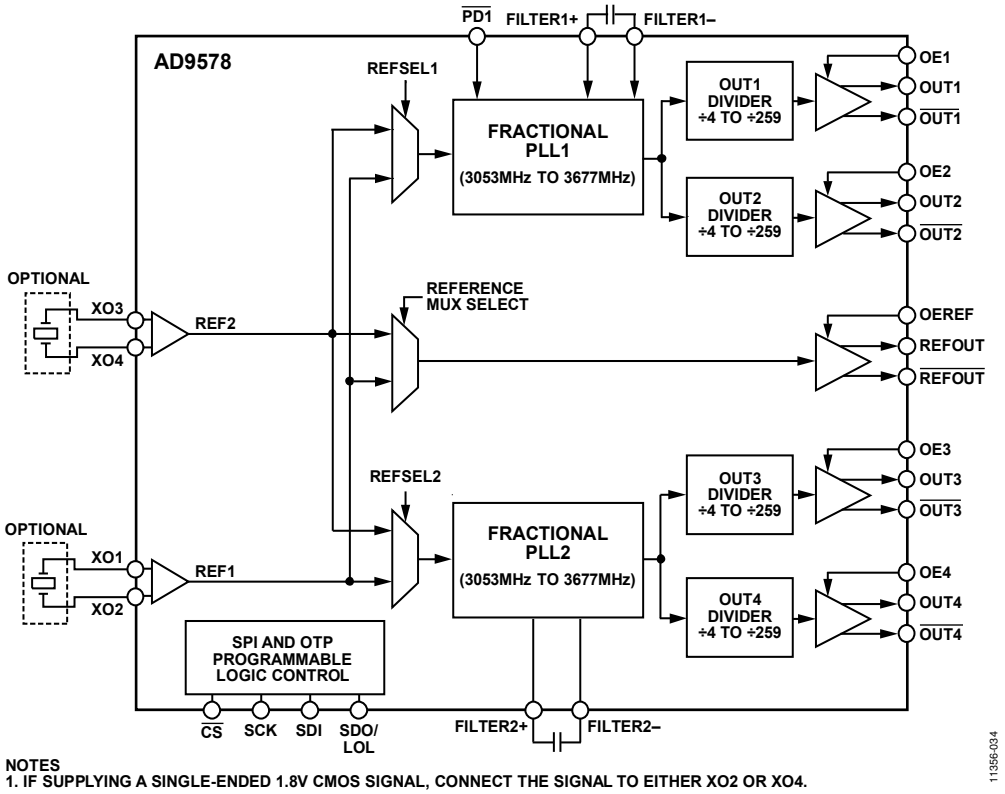


Figure 31. Detailed Block Diagram

OVERVIEW

The AD9578 is a dual synthesizer with four programmable outputs. Two PLLs, with either a crystal or external reference input frequency, produce up to four unique output frequencies. Output format standards on each output include LVCMOS, LVDS, LVPECL, and HCSL. The input crystal is a low cost fundamental mode type, and the AD9578 provides programmable gain and load capacitors. Alternatively, an input reference clock can be used for either or both PLLs. The crystal or external reference frequency is available on the REFOUT/$\overline{\text{REFOUT}}$ pins.

The PLLs operate independently but may share the input reference, if desired. Three modes of operation can be selected: integer mode, fractional mode, and rational mode. The integer mode provides the lowest noise and behaves like a conventional PLL with whole number dividers. The fractional mode allows the feedback divider to have an 8-bit integer part and a 28-bit fractional part, resulting in a frequency resolution of 0.1 ppb or better. Rotary traveling wave oscillator (RTWO)-based VCOs operate at rates from 3053 MHz to 3677 MHz. Rational mode is similar to fractional mode, but allows the user to specify the feedback divider in terms of one integer divided by another. There are two output dividers on each VCO, with a range of 4 to 259. To prevent an output frequency gap between 750.8 MHz and 777.25 MHz, a special divide by 4.5 mode is also included. Any output frequency between 11.8 MHz and 919 MHz can be produced with a frequency error of 0.1 ppb or better.

Additional features include loss of lock indicators, smooth change of output frequency for small frequency steps, and SPI control. The AD9578 can be configured through the SPI, factory programmed, user programmed, or any combination thereof. The AD9578 ships with a default power-up configuration programmed into OTP memory. All settings can be reprogrammed after power-up using the SPI.

At offset frequencies below the PLL bandwidth (which is typically 300 kHz), the PLL tracks and multiplies the reference phase noise. The crystal input offers a very low phase noise reference, ensuring that the output phase noise near the carrier is low. When selecting the reference input signal, ensure that the phase noise of the reference input is low enough to meet the system noise requirements.

PLL AND OUTPUT DRIVER CONTROL

Table 14. Register 2 Bits

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
[23:16]	Unused				MR (master reset)	MR enable (set to 1 to enable MR)	REFOUT	REFOUT enable (override OEREF pin)
[15:8]	OUTPUT4	Override OE4 pin	OUTPUT3	Override OE3 pin	OUTPUT2	Override OE2 pin	OUTPUT1	Override OE1 pin
[7:0]	REFSEL2	REFSEL2 enable (set to 1 to enable REFSEL2)	REFSEL1	REFSEL1 enable (set to 1 to enable REFSEL1)	PLL2	PLL2 enable (set to 1 to enable PLL2)	PLL1	PLL1 enable (override $\overline{PD1}$ pin)

Table 15. Register 4 Bits

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
[15:8]	XTAL frequency trim	XTAL Capacitance Value[2:0]			Unused	XTAL Gain[2:0]		
[7:0]	OUTPUT4 Mode[1:0]		OUTPUT3 Mode[1:0]		OUTPUT2 Mode[1:0]		OUTPUT1 Mode[1:0]	

OVERVIEW

The AD9578 has five output drivers: OUTPUT1, OUTPUT2, OUTPUT3, OUTPUT4, and REFOUT. Each output can be individually configured as LVCMOS, LVDS, LVPECL, or HCSL.

Each output has an output enable pin (OEx). Pin control of the outputs is enabled when the corresponding override OEx pin bit in Register 2 is low. When configured this way, the OUTPUTx bit is read only and indicates the status of the OEx pin.

When the override OEx pin (where x = 1 to 4) bit is high, the OUTPUTx bit in Register 2 turns OUTPUTx on and off. See Table 14 for the contents of Register 2.

The AD9578 ships with the default start-up output enable and output format functionality selected by the user. After power-up, the user can override the default programming through the SPI.

PLL ENABLE/DISABLE

Each output is enabled only if the associated PLL is powered up. Bits[3:0] in Register 2 control this function. There are two ways to power up/down PLL1. If the PLLx enable bit is 0, the user can power down PLL1 by pulling the $\overline{PD1}$ pin low. If the PLLx enable bit is high, PLL1 is powered up/down using the PLL1 bit (Bit 1). PLL2 is under software control only. Therefore, always set Bit 2 to 1. The PLL2 bit (Bit 3) powers up/down PLL2.

Reading the Hardware OEx Pin States

By default, the AD9578 OEx pins determine which outputs are enabled. If the corresponding override OEx pin bits are not set in Register 2, the user can read the states of these pins by reading Register 2. Note that the OE1, OE2, OE3, and OE4 pins have 75 kΩ pull-up resistors.

Disabling Hardware OEx Pin Control

To disable the hardware pin control, the associated override OEx pin bit can be set in Register 2 (see Table 14). The override OEx pin bits are OTP, allowing the device to power up with any output forced on, forced off, or controlled by the OEx pin. In Register 2, when the override OEx pin bit is set to 1, the corresponding OEx pin is ignored, and the OUTPUTx bit enables or disables an input or output. To enable an output, both the override OEx pin bit and the OUTPUTx bit in Register 2 must be set to 1.

Glitch-Free Output Enable

When an output changes from disabled to enabled, there is an approximate 2 µs delay before switching begins. During this delay, the outputs settle to the appropriate dc differential levels according to the configured mode. After this initial delay, the outputs begin toggling without glitches or runt pulses.

Output Disable Sequence

When an output changes from enabled to disabled, it stops switching at the appropriate dc levels according to the configured mode. After it has stopped switching, the biases are disabled and the output is set to high impedance.

OUTPUT DRIVER FORMAT

The default power-up output mode is factory programmed to single-ended LVCMOS. The user can override the defaults using the serial port, and the drivers can be programmed simultaneously.

Table 16. Output Driver Modes[1]

OUTPUTx Mode[1:0]	Output Mode
00	LVCMOS
01	LVDS
10	LVPECL
11	HCSL

[1] To disable any output through the SPI, the corresponding override OEx pin bit and OUTPUTx bit must be set to 1 and 0, respectively. This prevents any condition of the external OEx pin from affecting the state of the output driver. In OTP programming, setting the override bit to 1 disables the output pin permanently.

Note that all of the output modes are differential except LVCMOS mode. When LVCMOS is selected, the positive output pin is LVCMOS, and the negative (complementary) output pin is high impedance. The LVCMOS output driver mode can be used for output frequencies ≤250 MHz, and a series termination resistor is recommended (see Figure 30). Place a series termination 33 Ω resistor within 7 mm of the AD9578. A 50 Ω transmission line configured this way is impedance matched. However, differential output modes are preferred over single-ended modes to preserve the high performance of the AD9578 and to reduce noise pickup and generation.

OUTPUT CONFIGURATION EXAMPLE

Table 17 and Table 18 show how Register 2 and Register 4, respectively, are used to configure the AD9578 inputs and outputs.

PLL1 and PLL2 are enabled so that the output drivers connected to them are also enabled.

The OE1 and OE2 pins are ignored, OUTPUT1 is enabled and in LVCMOS mode, and OUTPUT2 is disabled. The OE3 and OE4 pins determine the state of OUTPUT3 and OUTPUT4, respectively. The REFOUT driver is disabled, OUTPUT3 is LVDS, and OUTPUT4 is LVPECL.

The X in Table 17 and Table 18 indicates that the register bit is not related to output driver configuration.

Table 17. Example of Output Driver Configuration Using Register 2

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
[23:16]	Unused = XXXX				MR (master reset) = 0	MR enable = 1	REFOUT = 0	REFOUT enable (override OEREF pin) = 1
[15:8]	OUTPUT4 = X	Override OE4 pin = 0	OUTPUT3 = X	Override OE3 pin = 0	OUTPUT2 = 0	Override OE2 pin = 1	OUTPUT1 = 1	Override OE1 pin = 1
[7:0]	REFSEL2 = X	REFSEL2 enable = X	REFSEL1 = X	REFSEL1 enable = X	PLL2 = 1	PLL2 enable =1	PLL1 = 1	PLL enable (override PD1 pin) = 1

Table 18. Example of Output Driver Configuration Using Register 4

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
[15:8]	XTAL1 frequency trim = X	XTAL1 Capacitance Value[2:0] = XXX			Unused = X	XTAL1 Gain[2:0] = XXX		
[7:0]	OUTPUT4 Mode[1:0] = 10		OUTPUT3 Mode[1:0] = 01		OUTPUT2 Mode[1:0] = XX		OUTPUT1 Mode[1:0] = 00	

REFERENCE INPUT

Table 19. Register 2 Bits

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
[23:16]	Unused				MR (master reset)	MR enable (set to 1 to enable MR bit)	REFOUT	REFOUT enable (override OEREF pin)
[15:8]	OUTPUT4	Override OE4 pin	OUTPUT3	Override OE3 pin	OUTPUT2	Override OE2 pin	OUTPUT1	Override OE1 pin
[7:0]	REFSEL2	REFSEL2 enable (set to 1 to enable REFSEL2 bit)	REFSEL1	REFSEL1 enable (set to 1 to enable REFSEL1 bit)	PLL2	PLL2 enable (set to 1 to enable PLL2 bit)	PLL1	PLL1 enable (override $\overline{\text{PD1}}$ pin) (set to 1 to enable PLL1 bit)

Table 20. Register 3 Bits

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
[31:24]	REFOUT mode[1:0]		Unused	Enable activity detect (set to 1)	Reference mux select	Enable XTAL1	Unused	
[23:16]	Unused				Enable OUTPUT4 divider	Enable OUTPUT3 divider	Enable OUTPUT2 divider	Enable OUTPUT1 divider
[15:8]	Unused	LVCMOS Edge Trim[2:0]			Enable OUTPUT4 4.5 mode	Enable OUTPUT3 4.5 mode	Enable OUTPUT2 4.5 mode	Enable OUTPUT1 4.5 mode
[7:0]	Exponent[3:0]				Mantissa[3:0]			

OVERVIEW

Two reference inputs are available for the PLLs. The user can connect either a crystal or an input clock to the XO1/XO2 pins or the XO3/XO4 pins. The allowable reference input logic types are 1.8 V LVCMOS, ac-coupled LVDS, and ac-coupled LVPECL. The crystal oscillators accept standard crystals from 22 MHz to 54 MHz. Either reference can be used by either PLL through the internal selectors. Likewise, either reference can be buffered to the REFOUT driver, which supports LVCMOS, LVDS, LVPECL, or HCSL format. OTP fuses are available to automatically load the user settings loaded each time the chip powers up or resets.

Register 2 contains the reference input control bits, Bits[7:4], and is shown in Table 19. Register 3 contains the configuration bits for the input reference buffer, and reference output, shown in Table 20. See the PLL and Output Driver Control section for information about the control of the reference output buffer.

REFERENCE INPUT

Table 21. PLL1 Reference Selection

Register 2		Register 3	
REFSEL1 Enable	REFSEL1	Enable XTAL1	PLLx Reference
0	X[1]	X[1]	Reference 1 (XO1, XO2)
1	0	X[1]	Reference 1 (XO1, XO2)
1	1	X[1]	Reference 2 (XO3, XO4)

[1] X = don't care.

Table 22. PLL2 Reference Selection

Register 2		Register 10	
REFSEL2 Enable	REFSEL2	Enable XTAL2	PLLx Reference
0	X[1]	X[1]	Reference 1 (XO1, XO2)
1	0	X[1]	Reference 1 (XO1, XO2)
1	1	X[1]	Reference 2 (XO3, XO4)

[1] X = don't care.

CRYSTAL OSCILLATOR AMPLIFIER ENABLE

The crystal oscillator amplifier is automatically enabled when either the PLLx or REFOUT bit in Register 2 uses the crystal oscillator for either Reference 1 or Reference 2. Otherwise, the crystal oscillator amplifier is disabled if neither the PLLx nor REFOUT bit selects that input. However, this setting can be overridden with the enable XTAL1 bit in Register 3 and enable XTAL2 bit in Register 10. Setting these bits forces the corresponding crystal oscillator on.

These bits are useful to allow a crystal to power up and stabilize before it is needed. However, these bits are usually set to 0 under normal operation.

REFOUT/$\overline{\text{REFOUT}}$ SOURCE SELECTION

The REFOUT/$\overline{\text{REFOUT}}$ pins can be used to buffer the crystal oscillator signal. Like the other outputs, it can be set to LVPECL, LVDS, HCSL, or LVCMOS format (see the PLL and Output Driver Control section for more information).