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12-Bit, 2.6 GSPS/2.5 GSPS/2.0 GSPS, 1.3 V/2.5 V Analog-to-Digital Converter

Data Sheet **AD9625**

FEATURES

- 12-bit 2.5 GSPS ADC, no missing codes
- SFDR = 79 dBc, AIN up to 1 GHz at −1 dBFS, 2.5 GSPS
- SFDR = 77 dBc, AIN up to 1.8 GHz at −1 dBFS, 2.5 GSPS
- SNR = 57.6 dBFS, AIN up to 1 GHz at −1 dBFS, 2.5 GSPS
- SNR = 57 dBFS, AIN up to 1.8 GHz at −1 dBFS, 2.5 GSPS
- Noise spectral density = −149.5 dBFS/Hz at 2.5 GSPS
- Differential analog input: 1.2 V p-p
- Differential clock input
- 3.2 GHz analog input bandwidth, full power
- High speed 6- or 8-lane JESD204B serial output at 2.6 GSPS
  - Subclass 1: 6.5 Gbps at 2.6 GSPS
- Two independent decimate by 8 or decimate by 16 filters with 10-bit NCOs
- Supply voltages: 1.3 V, 2.5 V
- Serial port control
  - Flexible digital output modes
  - Built-in selectable digital test patterns
- Timestamp feature
- Conversion error rate < 10^{-15}

APPLICATIONS

- Spectrum analyzers
- Military communications
- Radar
- High performance digital storage oscilloscopes
- Active jamming/antijamming
- Electronic surveillance and countermeasures

FUNCTIONAL BLOCK DIAGRAM

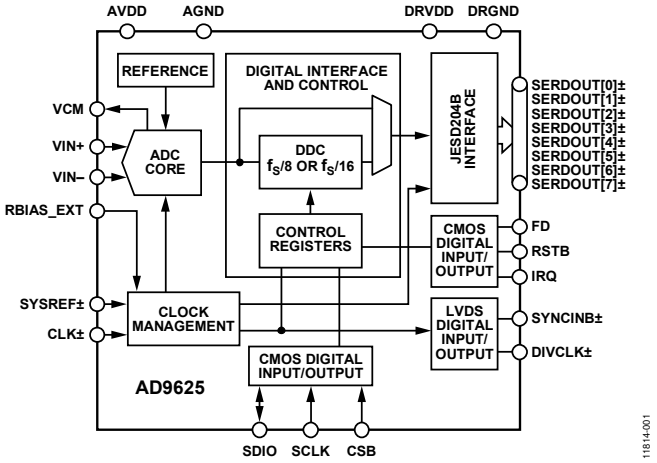

Figure 1.

GENERAL DESCRIPTION

The AD9625 is a 12-bit monolithic sampling analog-to-digital converter (ADC) that operates at conversion rates of up to 2.6 giga samples per second (GSPS). This product is designed for sampling wide bandwidth analog signals up to the second Nyquist zone. The combination of wide input bandwidth, high sampling rate, and excellent linearity of the AD9625 is ideally suited for spectrum analyzers, data acquisition systems, and a wide assortment of military electronics applications, such as radar and electronic countermeasures.

The analog input, clock, and SYSREF± signals are differential inputs. The JESD204B-based high speed serialized output is configurable in a variety of one-, two-, four-, six-, or eight-lane configurations. The product is specified over the industrial temperature range of −40°C to +85°C, measured at the case.

PRODUCT HIGHLIGHTS

1. High performance: exceptional SFDR in high sample rate applications, direct RF sampling, and on-chip reference.
2. Flexible digital data output formats based on the JESD204B specification.
3. Control path SPI interface port that supports various product features and functions, such as data formatting, gain, and offset calibration values.

Rev. C
Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
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AD9625* PRODUCT PAGE QUICK LINKS

Last Content Update: 03/25/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- 2 AD9625 ADC's running at 2.5GSPS with an effective sampling rate of 5GSPS
- AD9625 Evaluation and Synchronization
- AD9625 Evaluation Board
- ADA4961 & AD9625 Analog Signal Chain Evaluation and Converter Synchronization
- ADL5567 & AD9625 Analog Signal Chain Evaluation and ADF4355-2 Wideband Synthesizer with VCO

DOCUMENTATION

Data Sheet

- AD9625: 12-Bit, 2.6 GSPS/2.5 GSPS/2.0 GSPS, 1.3 V/2.5 V Analog-to-Digital Converter Data Sheet

User Guides

- AD-FMCADC2-EBZ FMC Board User Guide

TOOLS AND SIMULATIONS

- Visual Analog
- AD9625 AMI Model

REFERENCE MATERIALS

Informational

- JESD204 Serial Interface

Press

- 2.6-GHz A/D Converter in High-Reliability Package Meets Specific Sample Rate and Dynamic Range Requirements of Aerospace/Defense Applications
- Analog Devices Unveils 2.5-GSPS A/D Converter, Driver Amplifier and Rapid Prototyping FMC Module
- Global Leader in Converter Technology Releases Industry's Highest Performing 2-GSPS Data Converter
- New PLLs Deliver Widest Frequency Range Coverage and Lowest VCO Phase Noise in a Single Device

Technical Articles

- A Test Method for Synchronizing Multiple GSPS Converters
- Designing High Speed Analog Signal Chains from DC to Wideband
- MS-2660: Understanding Spurious-Free Dynamic Range in Wideband GSPS ADCs
- MS-2670-1: The Demand for Digital: Challenges and Solutions for High Speed Analog-to-Digital Converters and Radar Systems
- MS-2672: JESD204B Subclasses - Part 1: An Introduction to JESD204B Subclasses and Deterministic Latency
- MS-2677: JESD204B Subclasses - Part 2: Subclass 1 vs. Subclass 2 System Considerations
- MS-2702: Gigasample ADCs Run Fast to Solve New Challenges
- MS-2708: GSPS Data Converters to the Rescue for Electronics Surveillance and Warfare Systems
- MS-2714: Understanding Layers in the JESD204B Specificaton: A High Speed ADC Perspective, Part 1
- MS-2728: Demystifying the Conversion Error Rate of High Speed ADCs
- MS-2735: Maximizing the Dynamic Range of Software-Defined Radio
- Taming the Wideband Conundrum with RF Sampling ADCs

DESIGN RESOURCES

- AD9625 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9625 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

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Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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5/2014—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = DVDD1 = DRVDD1 = 1.3 V, AVDD2 = DVDD2 = DRVDD2 = 2.5 V, specified maximum sampling rate, 1.2 V internal reference, AIN = −1.0 dBFS, default SPI settings, dc-coupled output data, unless otherwise noted.

Table 1.

Parameter	Test Conditions/ Comments	Temperature[1]	AD9625-2.0			AD9625-2.5			AD9625-2.6			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION			12			12			12			Bits
ACCURACY												
No Missing Codes		Full		Guaranteed			Guaranteed			Guaranteed		
Offset Error		Full	−7	±0.5	+6.4	−7	±0.5	+6.4	−8.5	±0.5	+7.0	LSB
Gain Error		Full	−8		+8	−10.8		+14.2	−13.8		+20.9	%FSR
Differential Nonlinearity (DNL)		Full	−0.7	±0.3	+0.7	−0.5	±0.3	+0.7	−0.6	±0.3	+0.7	LSB
Integral Nonlinearity (INL)		Full	−3.6	±0.9	+3.6	−2.1	±1.0	+2.1	−2.7	±1.0	+2.3	LSB
ANALOG INPUTS												
Differential Input												
Voltage Range	Internal V_{REF} = 1.2 V	Full		1.1			1			1		V p-p
Resistance		25°C		100			100			100		Ω
Capacitance		25°C		1.5			1.5			1.5		pF
Internal Common-Mode Voltage (V_{CM})		Full	492	525	563	492	525	563	492	525	563	mV
Analog Full-Power Bandwidth[2]	Internal termination	25°C		3.2			3.2			3.2		GHz
Input Referred Noise		25°C		2			2			2		LSB_{RMS}
POWER SUPPLIES												
AVDD1		Full	1.26	1.3	1.32	1.26	1.3	1.32	1.26	1.3	1.32	V
AVDD2		Full	2.4	2.5	2.6	2.4	2.5	2.6	2.4	2.5	2.6	V
DRVDD1		Full	1.26	1.3	1.32	1.26	1.3	1.32	1.26	1.3	1.32	V
DRVDD2		Full	2.4	2.5	2.6	2.4	2.5	2.6	2.4	2.5	2.6	V
DVDD1		Full	1.26	1.3	1.32	1.26	1.3	1.32	1.26	1.3	1.32	V
DVDD2		Full	2.4	2.5	2.6	2.4	2.5	2.6	2.4	2.5	2.6	V
DVDDIO		Full	2.4	2.5	3.3	2.4	2.5	3.3	2.4	2.5	3.3	V
SPI_VDDIO		Full	2.4	2.5	3.3	2.4	2.5	3.3	2.4	2.5	3.3	V
I_{AVDD1}		Full		1120	1222		1250	1351		1267	1390	mA
I_{AVDD2}		Full		383	460		427	491		432	492	mA
I_{DRVDD1}		Full		456	470		476	518		497	544	mA
I_{DRVDD2}		Full		9	10		9	10		9	10	mA
I_{DVDD1}		Full		410	430		425	473		441	503	mA
I_{DVDD2}		Full		<1			<1			<1		mA
I_{DVDDIO}		Full		<1			<1			<1		mA
I_{SPI_VDDIO}		Full		<1			<1			<1		mA
Power Dissipation	Eight lane mode	Full		3.48	3.8		3.90	4.2		4.0	4.3	W
Power-Down Dissipation				125	3.8		125			125		mW

[1] Full temperature range is −40°C to +85°C measured at the case (T_C).
[2] See Figure 75 and Figure 76 for networks.

AC SPECIFICATIONS

AVDD1 = DVDD1 = DRVDD1 = 1.3 V, AVDD2 = DVDD2 = DRVDD2 = 2.5 V, specified maximum sampling, 1.2 V internal reference, AIN = −1.0 dBFS, sample clock input = 1.65 V p-p differential, default SPI settings, unless otherwise noted.

Table 2.

Parameter	Test Conditions/ Comments	Temperature[1]	AD9625-2.0			AD9625-2.5			AD9625-2.6			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SPEED GRADE					2.0			2.5			2.6	GSPS
ANALOG INPUT	Full scale	Full		1.1			1.2			1.1		V p-p
NOISE DENSITY		25°C		−149.0			−149.5			−150.0		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)												
f_{IN} = 100 MHz		25°C		59.5			58.3			58.1		dBFS
f_{IN} = 500 MHz		25°C		59.4			58.0			58.0		dBFS
f_{IN} = 1000 MHz		25°C		59.0			57.6			57.5		dBFS
f_{IN} = 1800 MHz		Full	55.4	58.2		54.1	57.0		55.0	56.6		dBFS
SIGNAL-TO-NOISE AND DISTORTION (SINAD)												
f_{IN} = 100 MHz		25°C		58.4			57.2			57.0		dBc
f_{IN} = 500 MHz		25°C		58.4			57.0			56.9		dBc
f_{IN} = 1000 MHz		25°C		58.0			56.5			56.4		dBc
f_{IN} = 1800 MHz		Full	54.1	57.2		53.1	55.9		53.9	55.6		dBc
EFFECTIVE NUMBER OF BITS (ENOB)												
f_{IN} = 100 MHz		25°C		9.4			9.2			9.2		Bits
f_{IN} = 500 MHz		25°C		9.4			9.2			9.2		Bits
f_{IN} = 1000 MHz		25°C		9.3			9.1			9.1		Bits
f_{IN} = 1800 MHz		25°C		9.2			9.0			8.9		Bits
SPURIOUS FREE DYNAMIC RANGE (SFDR)	Including second or thrid harmonic											
f_{IN} = 100 MHz		25°C		80			77			80.5		dBc
f_{IN} = 500 MHz		25°C		81			76			79.6		dBc
f_{IN} = 1000 MHz		25°C		80			79			77.3		dBc
f_{IN} = 1800 MHz		Full	67	76		70	77		65	75.4		dBc
WORST OTHER SPUR	Excluding second or third harmonic											
f_{IN} = 100 MHz		25°C		−80			−77			−81		dBc
f_{IN} = 500 MHz		25°C		−86			−76			−83		dBc
f_{IN} = 1000 MHz		25°C		−83			−82			−80		dBc
f_{IN} = 1800 MHz		Full		−85	−73		−78	−70		−78.0	−66.0	dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)	At −7 dBFS per tone											
f_{IN1} = 728.5 MHz, f_{IN2} = 731.5 MHz		25°C		−82.8			−81.2			−78.3		dBc
f_{IN1} = 1805.5 MHz, f_{IN2} = 1808.5 MHz		25°C		−77.6			−76.3			−77.7		dBc

[1] Full temperature range is −40°C to +85°C measured at the case (T_C).

DIGITAL SPECIFICATIONS

AVDD1 = DVDD1 = DRVDD1 = 1.3 V, AVDD2 = DVDD2 = DRVDD2 = 2.5 V, specified maximum sampling rate, 1.2 V internal reference, AIN = −1.0 dBFS, default SPI settings, unless otherwise noted.

Table 3.

Parameter	Temperature[1]	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Differential Input Voltage	Full	500		1800	mV p-p
Common-Mode Input Voltage	Full		0.88		V
Input Resistance (Differential)	Full		40		kΩ
Input Capacitance	Full		1.5		pF
SYSREF INPUTS (SYSREF+, SYSREF−)					
Differential Input Voltage	Full	500		1800	mV p-p
Common-Mode Input Voltage	Full		0.88		V
Input Resistance (Differential)	Full		40		kΩ
Input Capacitance	Full		1.5		pF
LOGIC INPUTS (SDIO, SCLK, CSB)					
Logic Compliance			CMOS		
Voltage					
Logic 1	Full	0.8 × SPI_DVDDIO			V
Logic 0	Full			0.5	V
Input Resistance	Full		30		kΩ
Input Capacitance	Full		0.5		pF
SYNCB+/SYNCB− INPUT					
Logic Compliance	Full		LVDS		
Input Voltage					
Differential	Full	250		1200	mV p-p
Common Mode	Full		1.2		V
Input Resistance (Differential)	Full		100		Ω
Input Capacitance	Full		2.5		pF
LOGIC OUTPUT (SDIO)					
Logic Compliance			CMOS		
Voltage					
Logic 1 (I_{OH} = 800 µA)	Full		0.8 × SPI_VDDIO		V
Logic 0 (I_{OL} = 50 µA)	Full		0.3		V
DIGITAL OUTPUTS (SERDOUT[x]±)					
Compliance	Full		CML		
Output Voltage					
Differential	Full	360	700	800	mV p-p
Offset	Full		DRVDD/2		mV p-p
Differential Return Loss (RL_{DIFF})[2]	25°C	8			dB
Common-Mode Return Loss (RL_{CM})	25°C	6			dB
Differential Termination Impedance	25°C			100	Ω
RESET (RSTB)					
Voltage					
Logic 1	Full	0.8 × DVDDIO			V
Logic 0	Full			0.5	V
Input Resistance (Differential)	Full		20		kΩ
Input Capacitance	Full		2.5		pF
FAST DETECT (FD), PWDN, AND INTERRUPT (IRQ)					
Logic Compliance			CMOS		
Voltage					
Logic 1	Full	0.8 × DVDDIO			V
Logic 0	Full			0.5	V
Input Resistance (Differential)	Full		20		kΩ
Input Capacitance	Full		2.5		pF

[1] Full temperature range is −40°C to +85°C measured at the case (T_C).
[2] Differential and common-mode return loss measured from 100 MHz to 0.75 × baud rate.

SWITCHING SPECIFICATIONS

AVDD1 = DVDD1 = DRVDD1 = 1.3 V, AVDD2 = DVDD2 = DRVDD2 = 2.5 V, specified maximum sampling rate, 1.2 V internal reference, AIN = −1.0 dBFS, default SPI settings, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Temperature[1]	Min	Typ	Max	Unit
CLOCK (CLK)						
Maximum Clock Rate		Full			2600	MSPS
Minimum Clock Rate		Full	330[2]			MSPS
Clock Pulse Width High		Full	50 ± 5			% duty cycle
Clock Pulse Width Low		Full	50 ± 5			% duty cycle
SYSREF (SYSREF±)[3]						
Setup Time (t_{SU_SR})		25°C		+200		ps
Hold Time (t_{H_SR})		25°C		−100		ps
FAST DETECT OUTPUT (FD)						
Latency		Full		82		Clock cycles
OUTPUT PARAMETERS (SERDOUT[x]±)						
Rise Time		25°C		70		ps
Fall Time		25°C		70		ps
Pipeline Latency	Eight lane mode	25°C		226		Clock cycles
SYNCB± Falling Edge to First K.28 Characters		25°C	4			Multiframes
CGS Phase K.28 Characters Duration		25°C	1			Multiframes
Differential Termination Resistance		25°C		100		Ω
APERTURE						
Delay		Full		200		ps
Uncertainty (Jitter)		Full		80		f_S rms
Out-of-Range Recovery Time		Full		2		Clock cycles

[1] Full temperature range is −40°C to +85°C measured at the case (T_C).
[2] Must use a two-lane, generic output lane configuration for minimum sample rate. For more information, see the lane table in the JESD204B specification document.
[3] SYSREF± setup and hold times are defined with respect to the rising SYSREF± edge and rising clock edge. Positive setup time leads the clock edge. Negative hold time also leads the clock edge.

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPI TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK should be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK should be in a logic low state	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10			ns

Timing Diagrams

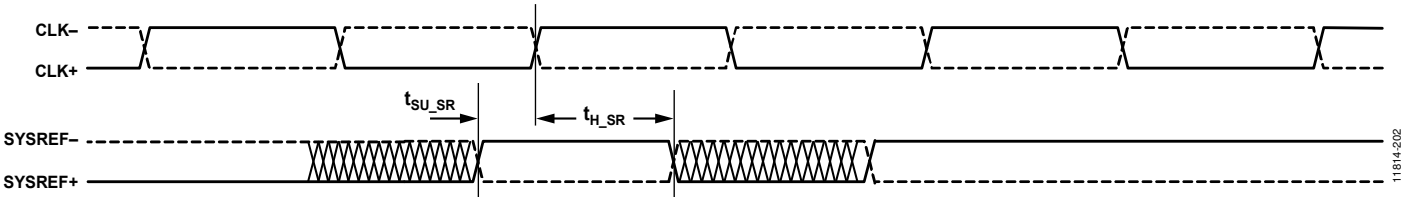

Figure 2. SYSREF± Setup and Hold Timing

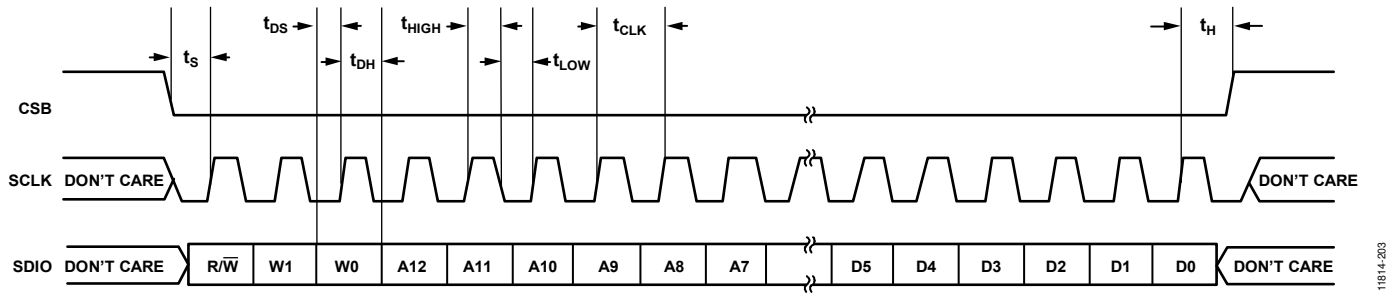

Figure 3. Serial Port Interface Timing Diagram (MSB First)

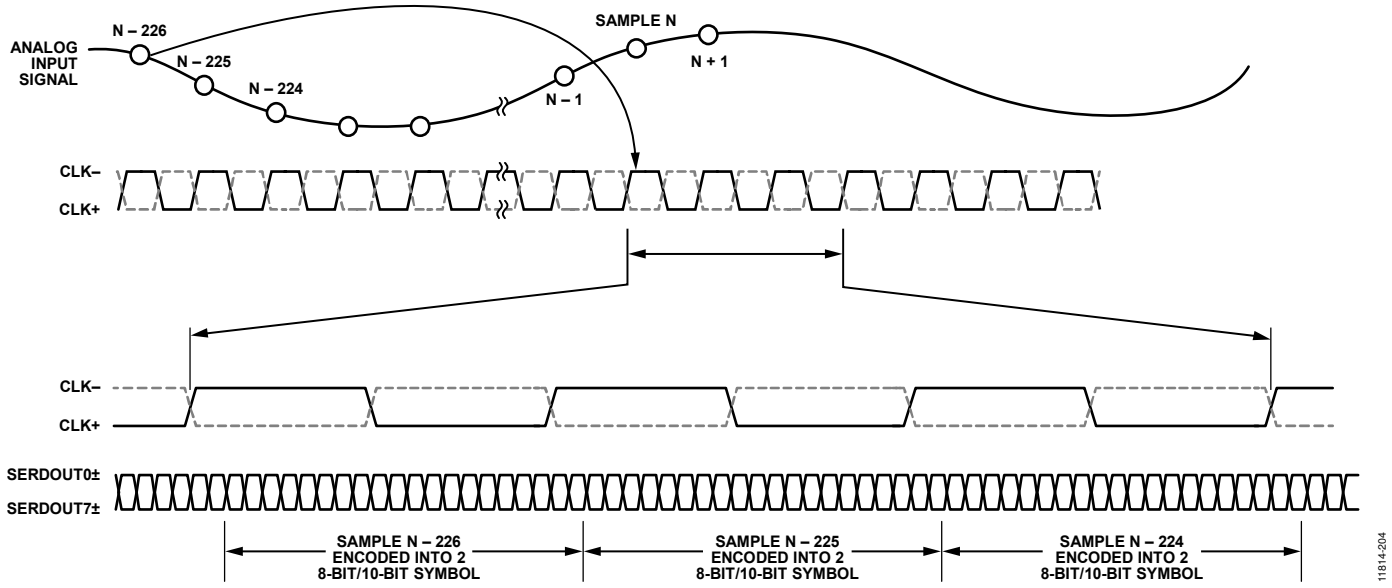

Figure 4. Data Output Timing for Eight Lane Mode

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD1 to AGND	−0.3 V to +1.32 V
AVDD2 to AGND	−0.3 V to +2.75 V
DRVDD1 to DRGND	−0.3 V to +1.32 V
DRVDD2 to DRGND	−0.3 V to +2.75 V
DVDD1 to DGND	−0.3 V to +1.32 V
DVDD2 to DGND	−0.3 V to +2.75 V
DVDDIO to DGND	−0.3 V to +3.63 V
SPI_VDDIO to DGND	−0.3 V to +3.63 V
AGND to DRGND	−0.3 V to +0.3 V
VIN± to AGND	−0.3 V to AVDD1 + 0.2 V
VCM to AGND	−0.3 V to AVDD1 + 0.2 V
VMON to AGND	−0.3 V to AVDD1 + 0.2 V
CLK± to AGND	−0.3 V to AVDD1 + 0.2 V
SYSREF± to AGND	−0.3 V to AVDD1 + 0.2 V
SYNCINB± to DRGND	−0.3 V to DRVDD2 + 0.2 V
SCLK to DRGND	−0.3 V to SPI_VDDIO + 0.2 V
SDIO to DRGND	−0.3 V to SPI_VDDIO + 0.2 V
IRQ to DRGND	−0.3 V to DVDDIO + 0.2 V
RSTB to DRGND	−0.3 V to DVDDIO + 0.2 V
CSB to DRGND	−0.3 V to SPI_VDDIO + 0.2 V
FD to DRGND	−0.3 V to DVDDIO + 0.2 V
DIVCLK± to DRGND	−0.3 V to DRVDD2 + 0.2 V
SERDOUT[x]± to DRGND	−0.3 V to DRVDD1 + 0.2 V
Environmental	
Storage Temperature Range	−60°C to +150°C
Operating Case Temperature Range	−40°C to +85°C (measured at case)
Maximum Junction Temperature	110°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

The following characteristics are for a 4-layer and 10-layer printed circuit board (PCB).

Table 7. Thermal Resistance

PCB	T_A (°C)	θ_{JA} (°C/W)	Ψ_{JT} (°C/W)	Ψ_{JB} (°C/W)	θ_{JC} (°C/W)
4-Layer	85.0	18.7	0.61	6.1	1.4
10-Layer	85.0	11.5	0.61	4.1	N/A[1]

[1] N/A means not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

AD9625
TOP VIEW
(Not to Scale)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	AGND	AGND	AGND	AVDD1	AGND	AVDD2	VCM	AGND	VIN+	VIN–	AGND	VM_BYP	AVDD2	AVDD2
B	AGND	AGND	AGND	AGND	AVDD1	AGND	AVDD2	AGND	AGND	AGND	AGND	AVDD2	AGND	AGND
C	AGND	AGND	AGND	AGND	AGND	AVDD1	AGND	AVDD2	AGND	AGND	AVDD2	AGND	AGND	AVDD1
D	DVDD1	DVDD1	DVDD1	DNC	AGND	AGND	AVDD1	AVDD2	AGND	AGND	AVDD2	AVDD1	AVDD1	AVDD1
E	DGND	DGND	DGND	DVDD2	VMON	AGND	AVDD1	AVDD2	AGND	AGND	AVDD2	AVDD1	AGND	AGND
F	DVDD1	DVDD1	DVDD1	SPI_VDDIO	DVDDIO	AGND	AVDD1	AVDD2	AGND	AGND	AVDD2	AVDD1	AGND	CLK+
G	DGND	DGND	DGND	CSB	DVDDIO	AGND	AVDD1	AVDD2	AGND	AGND	AVDD2	AVDD1	AGND	CLK–
H	DVDD1	DVDD1	DVDD1	SCLK	IRQ	AGND	AVDD1	AVDD2	AGND	AGND	AVDD2	AVDD1	AGND	AGND
J	DGND	DGND	DGND	SDIO	FD	RBIAS_EXT	AVDD1	AVDD2	AGND	AGND	AVDD2	AVDD1	AGND	SYSREF+
K	DVDD1	DVDD1	RSTB	PWDN	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	SYSREF–
L	DGND	DNC	SYNCINB–	SYNCINB+	DGND	DGND	DGND	DGND	DGND	DNC	DNC	DNC	AGND	AGND
M	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRVDD1	REXT	DRGND	DRGND
N	DRVDD1	SERDOUT [7]+	SERDOUT [6]+	SERDOUT [5]+	SERDOUT [4]+	DRVDD1	SERDOUT [3]+	SERDOUT [2]+	SERDOUT [1]+	SERDOUT [0]+	DRVDD1	VP_BYP	DRVDD2	DRVDD2
P	DRVDD1	SERDOUT [7]–	SERDOUT [6]–	SERDOUT [5]–	SERDOUT [4]–	DRVDD1	SERDOUT [3]–	SERDOUT [2]–	SERDOUT [1]–	SERDOUT [0]–	DRVDD1	DRGND	DIVCLK–	DIVCLK+

NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN. LEAVE THIS PIN FLOATING.

11814-009

Figure 5. Pin Configuration

Table 8. Pin Function Descriptions (By Pin Number)

Pin No.	Mnemonic	Type	Description
A1 to A3	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
A4	AVDD1	Power	ADC Analog Power Supply (1.30 V).
A5	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
A6	AVDD2	Power	ADC Analog Power Supply (2.50 V).
A7	VCM	Output	Analog Input, Common Mode (0.525 V).
A8	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
A9	VIN+	Input	Differential Analog Input, True.
A10	VIN−	Input	Differential Analog Input, Complement.
A11	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
A12	VM_BYP	Input	Voltage Bypass.
A13	AVDD2	Power	ADC Analog Power Supply (2.50 V).
A14	AVDD2	Power	ADC Analog Power Supply (2.50 V).
B1 to B4	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
B5	AVDD1	Power	ADC Analog Power Supply (1.30 V).
B6	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
B7	AVDD2	Power	ADC Analog Power Supply (2.50 V).
B8 to B11	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
B12	AVDD2	Power	ADC Analog Power Supply (2.50 V).
B13, B14	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
C1 to C5	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
C6	AVDD1	Power	ADC Analog Power Supply (1.30 V).
C7	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
C8	AVDD2	Power	ADC Analog Power Supply (2.50 V).
C9, C10	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
C11	AVDD2	Power	ADC Analog Power Supply (2.50 V).
C12, C13	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
C14	AVDD1	Power	ADC Analog Power Supply (1.30 V).
D1 to D3	DVDD1	Power	ADC Digital Power Supply (1.30 V).
D4	DNC	N/A[1]	Do Not Connect. Do not connect to this pin. Leave this pin floating.
D5, D6	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
D7	AVDD1	Power	ADC Analog Power Supply (1.30 V).
D8	AVDD2	Power	ADC Analog Power Supply (2.50 V).
D9, D10	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
D11	AVDD2	Power	ADC Analog Power Supply (2.50 V).
D12 to D14	AVDD1	Power	ADC Analog Power Supply (1.30 V).
E1 to E3	DGND	Ground	Digital Control Ground Supply. These pins connect to the digital ground plane.
E4	DVDD2	Power	ADC Digital Power Supply (2.5 V).
E5	VMON	Output	CTAT Voltage Monitor Output.
E6	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
E7	AVDD1	Power	ADC Analog Power Supply (1.30 V).
E8	AVDD2	Power	ADC Analog Power Supply (2.50 V).
E9, E10	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
E11	AVDD2	Power	ADC Analog Power Supply (2.50 V).
E12	AVDD1	Power	ADC Analog Power Supply (1.30 V).
E13, E14	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
F1 to F3	DVDD1	Power	ADC Digital Power Supply (1.30 V).
F4	SPI_VDDIO	Power	SPI Digital Power Supply (2.50 V).
F5	DVDDIO	Power	Digital I/O Power Supply (2.50 V).
F6	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
F7	AVDD1	Power	ADC Analog Power Supply (1.30 V).
F8	AVDD2	Power	ADC Analog Power Supply (2.50 V).
F9, F10	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.

Pin No.	Mnemonic	Type	Description
F11	AVDD2	Power	ADC Analog Power Supply (2.50 V).
F12	AVDD1	Power	ADC Analog Power Supply (1.30 V).
F13	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
F14	CLK+	Input	ADC Clock Input, True.
G1 to G3	DGND	Ground	Digital Control Ground Supply. These pins connect to the digital ground plane.
G4	CSB	Input	SPI Chip Select CMOS Input. Active low.
G5	DVDDIO	Power	Digital I/O Power Supply (2.50 V).
G6	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
G7	AVDD1	Power	ADC Analog Power Supply (1.30 V).
G8	AVDD2	Power	ADC Analog Power Supply (2.50 V).
G9, G10	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
G11	AVDD2	Power	ADC Analog Power Supply (2.50 V).
G12	AVDD1	Power	ADC Analog Power Supply (1.30 V).
G13	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
G14	CLK–	Input	ADC Clock Input, Complement.
H1 to H3	DVDD1	Power	ADC Digital Power Supply (1.30 V).
H4	SCLK	Input	SPI Serial Clock CMOS Input.
H5	IRQ	Output	Interrupt Request Output Signal.
H6	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
H7	AVDD1	Power	ADC Analog Power Supply (1.30 V).
H8	AVDD2	Power	ADC Analog Power Supply (2.50 V).
H9, H10	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
H11	AVDD2	Power	ADC Analog Power Supply (2.50 V).
H12	AVDD1	Power	ADC Analog Power Supply (1.30 V).
H13, H14	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
J1 to J3	DGND	Ground	Digital Control Ground Supply. These pins connect to the digital ground plane.
J4	SDIO	I/O	SPI Serial Data CMOS Input/Output; Scan Output 1.
J5	FD	Output	Fast Detect Output. This pin requires an external 10 kΩ resistor connected to ground.
J6	RBIAS_EXT	Input	Reference Bias. This pin requires an external 10 kΩ resistor connected to ground.
J7	AVDD1	Power	ADC Analog Power Supply (1.30 V).
J8	AVDD2	Power	ADC Analog Power Supply (2.50 V).
J9, J10	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
J11	AVDD2	Power	ADC Analog Power Supply (2.50 V).
J12	AVDD1	Power	ADC Analog Power Supply (1.30 V).
J13	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
J14	SYSREF+	Input	System Reference Chip Synchronization, True.
K1 to K2	DVDD1	Power	ADC Digital Power Supply (1.30 V).
K3	RSTB	Input	Chip Digital Reset, Active Low.
K4	PWDN	Input	Power-down.
K5 to K13	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
K14	SYSREF–	Input	System Reference Chip Synchronization, Complement.
L1	DGND	Ground	Digital Control Ground Supply. This pin connects to the digital ground plane.
L2	DNC	N/A[1]	Do Not Connect. Do not connect to this pin. Leave this pin floating.
L3	SYNCINB–	Input	Synchronization, Complement.
L4	SYNCINB+	Input	Synchronization, True. SYNCINB LVDS input (active low, true).
L5 to L9	DGND	Ground	Digital Control Ground Supply. These pins connect to the digital ground plane.
L10 to L12	DNC	N/A[1]	Do Not Connect. Do not connect to these pins. Leave these pins floating.
L13, L14	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
M1 to M10	DRGND	Ground	Digital Driver Ground Supply. These pins connect to the digital driver ground plane.
M11	DRVDD1	Power	Power Supply (1.3 V) Reference Clock Divider, VCO, and Synthesizer.
M12	REXT	Input	External Resistor, 10 kΩ to Ground.
M13, M14	DRGND	Ground	Digital Driver Ground Supply. This pin connects to the digital driver ground plane.

Pin No.	Mnemonic	Type	Description
N1	DRVDD1	Power	Serial Digital Power Supply (1.3 V).
N2	SERDOUT[7]+	Output	Lane 7 CML Output Data, True.
N3	SERDOUT[6]+	Output	Lane 6 CML Output Data, True.
N4	SERDOUT[5]+	Output	Lane 5 CML Output Data, True.
N5	SERDOUT[4]+	Output	Lane 4 CML Output Data, True.
N6	DRVDD1	Power	Serial Digital Power Supply (1.3 V).
N7	SERDOUT[3]+	Output	Lane 3 CML Output Data, True.
N8	SERDOUT[2]+	Output	Lane 2 CML Output Data, True.
N9	SERDOUT[1]+	Output	Lane 1 CML Output Data, True.
N10	SERDOUT[0]+	Output	Lane 0 CML Output Data, True.
N11	DRVDD1	Power	Serial Digital Power Supply (1.3 V).
N12	VP_BYP	Input	Voltage Bypass.
N13, N14	DRVDD2	Power	Power Supply (2.5 V) Reference Clock Divider for SYNCINB±, DIVCLK±.
P1	DRVDD1	Power	Serial Digital Power Supply (1.3 V).
P2	SERDOUT[7]–	Output	Lane 7 CML Output Data, Complement.
P3	SERDOUT[6]–	Output	Lane 6 CML Output Data, Complement.
P4	SERDOUT[5]–	Output	Lane 5 CML Output Data, Complement.
P5	SERDOUT[4]–	Output	Lane 4 CML Output Data, Complement.
P6	DRVDD1	Power	Serializer Digital Power Supply (1.30 V).
P7	SERDOUT[3]–	Output	Lane 3 CML Output Data, Complement.
P8	SERDOUT[2]–	Output	Lane 2 CML Output Data, Complement.
P9	SERDOUT[1]–	Output	Lane 1 CML Output Data, Complement.
P10	SERDOUT[0]–	Output	Lane 0 CML Output Data, Complement.
P11	DRVDD1	Power	Serializer Digital Power Supply (1.30 V).
P12	DRGND	Ground	Digital Driver Ground Supply. This pin connects to the digital driver ground plane.
P13	DIVCLK–	Output	Divide-by-4 Reference Clock LVDS, Complement.
P14	DIVCLK+	Output	Divide-by-4 Reference Clock LVDS, True.

[1] N/A means not applicable.

Table 9. Pin Function Descriptions (By Function)[1]

Pin No.	Mnemonic	Type	Description
General Power and Ground Supply Pins			
A1 to A3, A5, A8, A11, B1 to B4, B6, B8 to B11, B13, B14, C1 to C5, C7, C9, C10, C12, C13, D5, D6, D9, D10, E6, E9, E10, E13, E14, F6, F9, F10, F13, G6, G9, G10, G13, H6, H9, H10, H13, H14, J9, J10, J13, K5 to K13, L13, L14	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
J6	RBIAS_EXT	Input	Reference Bias. This pin requires an external 10 kΩ resistor connected to ground.
Clock Pins			
F14	CLK+	Input	ADC Clock Input, True.
G14	CLK–	Input	ADC Clock Input, Complement.
ADC Analog Power and Ground Supplies Pins			
A6, A13, A14, B7, B12, C8, C11, D8, D11, E8, E11, F8, F11, G8, G11, H8, H11, J8, J11	AVDD2	Power	ADC Analog Power Supply (2.50 V).
A4, B5, C6, C14, D7, D12 to D14, E7, E12, F7, F12, G7, G12, H7, H12, J7, J12	AVDD1	Power	ADC Analog Power Supply (1.30 V).
A12	VM_BYP	Input	Voltage Bypass.
A1 to A3, A5, A8, A11, B1 to B4, B6, B8 to B11, B13, B14, C1 to C5, C7, C9, C10, C12, C13,D5, D6, D9, D10, E6, E9, E10, E13, E14, F6, F9, F10, F13, G6, G9, G10, G13, H6, H9, H10, H13, H14, J9, J10, J13, K5 to K13, L13, L14	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.

Pin No.	Mnemonic	Type	Description
ADC Analog Input and Outputs Pins			
A9	VIN+	Input	Differential Analog Input, True.
A10	VIN−	Input	Differential Analog Input, Complement.
A7	VCM	Output	Analog Input, Common Mode (0.525 V).
E5	VMON	Output	CTAT Voltage Monitor Output (Diode Temperature Sensor).
JESD204B High Speed Power and Ground Pins			
N1, N6, N11, P1, P6, P11	DRVDD1	Power	Serial Digital Power Supply (1.3 V).
M1 to M10, M13, M14, P12	DRGND	Ground	Digital Driver Ground Supply. These pins connect to the digital driver ground plane.
N13, N14	DRVDD2	Power	Power Supply (2.5 V) Reference Clock Divider, SYNCINB±, DIVCLK±.
M11	DRVDD1	Power	Power Supply (1.3 V) Reference Clock Divider, VCO, and Synthesizer.
N12	VP_BYP	Input	Voltage Bypass.
L2	DNC	N/A[2]	Do Not Connect. Do not connect to this pin.
JESD204B High Speed Serial I/O Pins			
J14	SYSREF+	Input	System Reference Chip Synchronization, True.
K14	SYSREF−	Input	System Reference Chip Synchronization, Complement.
L4	SYNCINB+	Input	Synchronization, True. SYNCINB LVDS input (active low, true).
L3	SYNCINB−	Input	Synchronization, Complement. SYNCINB LVDS input (active low, complement).
N10	SERDOUT[0]+	Output	Lane 0 CML Output Data, True.
P10	SERDOUT[0]−	Output	Lane 0 CML Output Data, Complement.
N9	SERDOUT[1]+	Output	Lane 1 CML Output Data, True.
P9	SERDOUT[1]−	Output	Lane 1 CML Output Data, Complement.
N8	SERDOUT[2]+	Output	Lane 2 CML Output Data, True.
P8	SERDOUT[2]−	Output	Lane 2 CML Output Data, Complement.
N7	SERDOUT[3]+	Output	Lane 3 CML Output Data, True.
P7	SERDOUT[3]−	Output	Lane 3 CML Output Data, Complement.
N5	SERDOUT[4]+	Output	Lane 4 CML Output Data, True.
P5	SERDOUT[4]−	Output	Lane 4 CML Output Data, Complement.
N4	SERDOUT[5]+	Output	Lane 5 CML Output Data, True.
P4	SERDOUT[5]−	Output	Lane 5 CML Output Data, Complement.
N3	SERDOUT[6]+	Output	Lane 6 CML Output Data, True.
P3	SERDOUT[6]−	Output	Lane 6 CML Output Data, Complement.
N2	SERDOUT[7]+	Output	Lane 7 CML Output Data, True.
P2	SERDOUT[7]−	Output	Lane 7 CML Output Data, Complement.
P14	DIVCLK+	Output	Divide-by-4 Reference Clock LVDS, True.
P13	DIVCLK−	Output	Divide-by-4 Reference Clock LVDS, Complement.
Digital Supply and Ground Pins			
D1 to D3, F1 to F3, H1 to H3, K1 to K2	DVDD1	Power	ADC Digital Power Supply (1.3 V).
F5, G5	DVDDIO	Power	Digital I/O Power Supply (2.5 V).
F4	SPI_VDDIO	Power	SPI Digital Power Supply (2.5 V).
E4	DVDD2	Power	ADC Digital Power Supply (2.5 V).
E1 to E3, G1 to G3, J1 to J3, L1, L5 to L9	DGND	Ground	Digital Control Ground Supply. These pins connect to the digital ground plane.
D4	DNC	N/A[2]	Do Not Connect. Do not connect to this pin. Leave this pin floating.
Digital Control Pins			
K3	RSTB	Input	Chip Digital Reset, Active Low.
K4	PWDN	Input	Power-down for the AD9625.
M12	REXT	Input	External Resistor, 10 kΩ to Ground.
G4	CSB	Input	SPI Chip Select CMOS Input. Active low.
H4	SCLK	Input	SPI Serial Clock CMOS Input.

Pin No.	Mnemonic	Type	Description
J4	SDIO	I/O	SPI Serial Data CMOS Input/Output.
J5	FD	Output	Fast Detect Output. This pin requires an external 10 kΩ resistor connected to ground.
H5	IRQ	Output	Interrupt Request Output Signal.
L10 to L12	DNC	N/A[2]	Do Not Connect. Do not connect to these pins. Leave these pins floating.

[1] Note that when pins are relevant to multiple categories, they are repeated in Table 9. Pins may not appear in alphanumeric order within Table 9.
[2] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

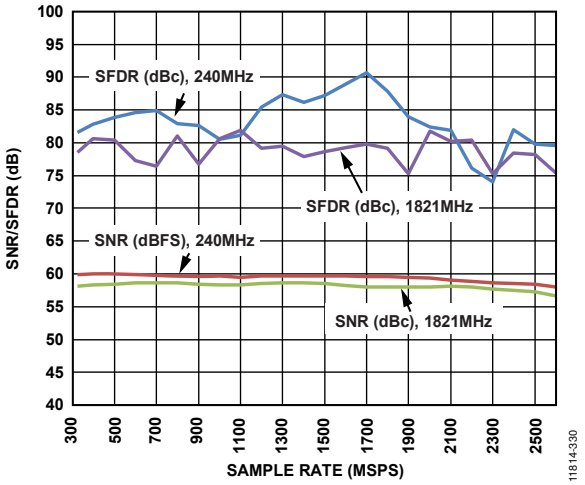

Figure 6. SNR/SFDR vs. Sample Rate

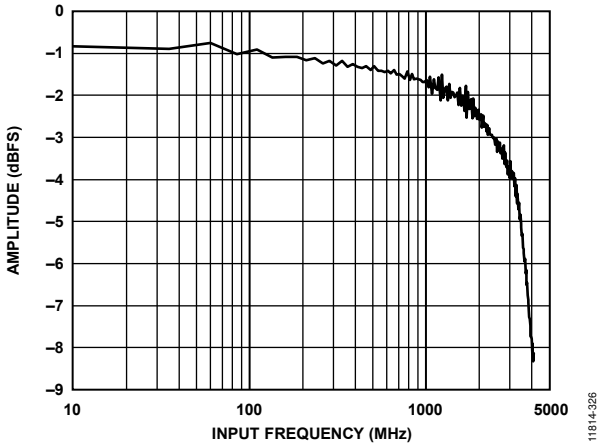

Figure 8. Full Power Input Bandwidth (Input Network in Figure 76 Used >2 GHz, Input Network in Figure 75 Used <2 GHz)

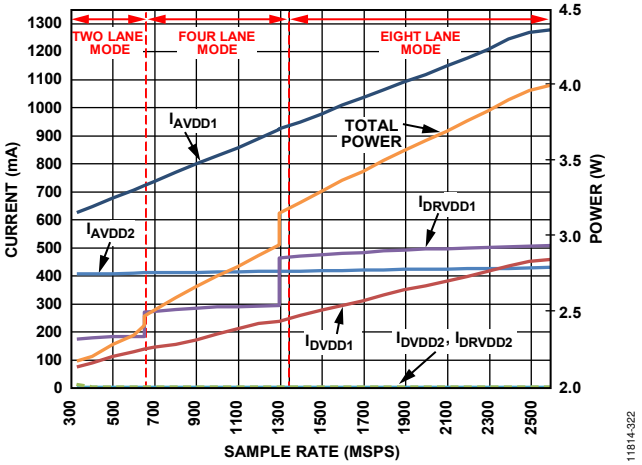

Figure 7. Current and Power vs. Sample Rate: Two Lane, Four Lane, and Eight Lane Output Modes

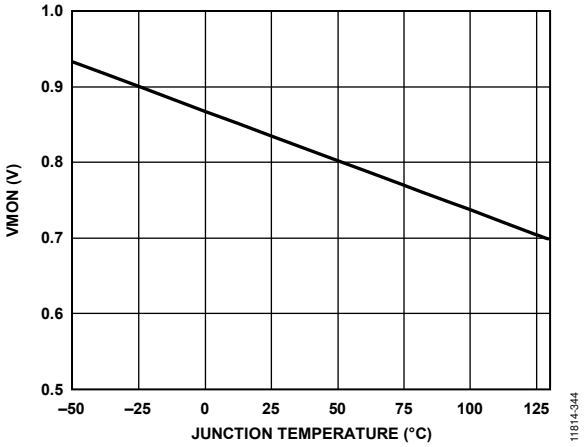

Figure 9. VMON Output Voltage vs. Junction Temperature VMON (V) = −0.0013 × TEMP(C) + 0.8675

AD9625-2.0

For the AD9625-2.0 model, the full-scale range used is 1.1 V.

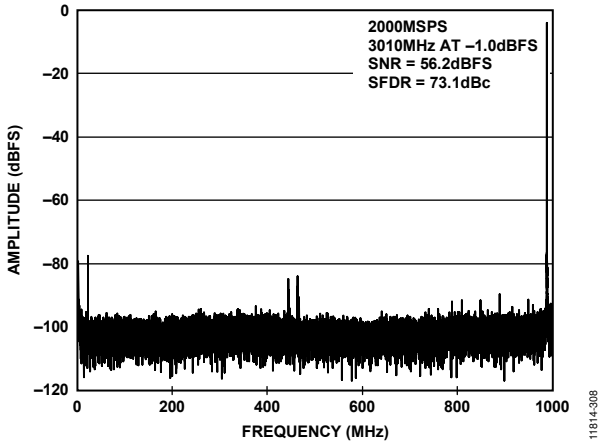

Figure 10. FFT Plot at 2.0 GSPS, f_{IN} = 3010 MHz at AIN (SFDR = 73.1 dBc, SNR = 56.2 dBFS) (Input Network in Figure 76 Used)

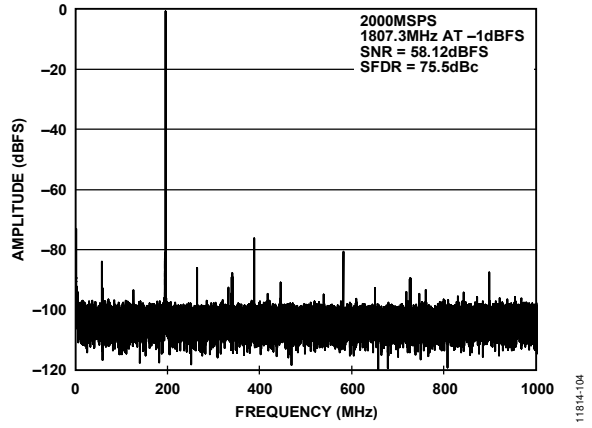

Figure 11. FFT Plot at 2.0 GSPS, f_{IN} = 1807.3 MHz at AIN (SFDR = 75.5 dBc, SNR = 58.12 dBFS)

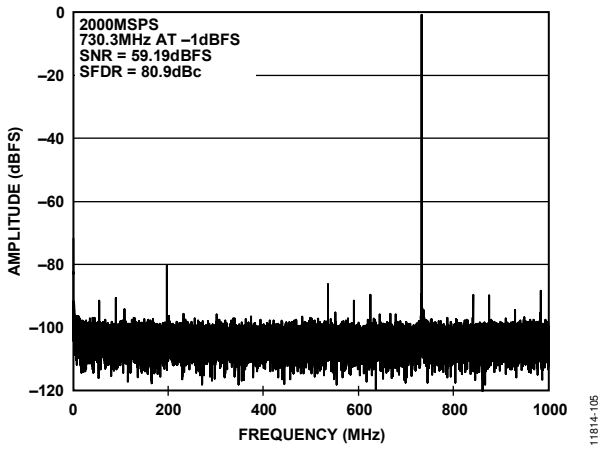

Figure 12. FFT Plot at 2.0 GSPS, f_{IN} = 730.3 MHz at AIN (SFDR = 80.9 dBc, SNR = 59.19 dBFS)

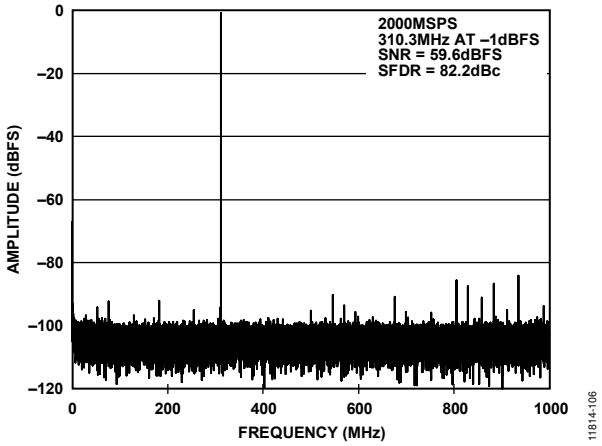

Figure 13. FFT Plot at 2.0 GSPS, f_{IN} = 310.3 MHz at AIN (SFDR = 82.2 dBc, SNR = 59.6 dBFS)

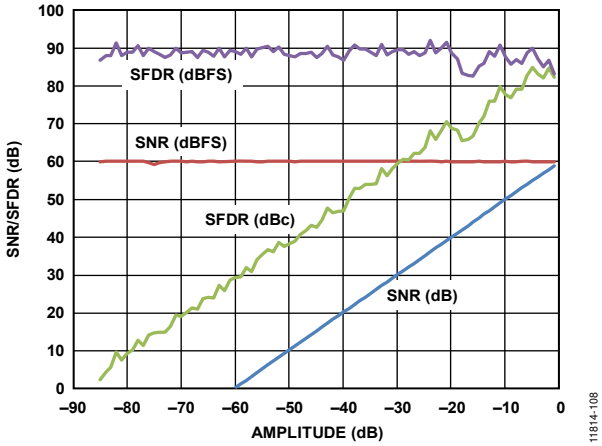

Figure 14. SNR/SFDR vs. Analog Input Amplitude at 2.0 GSPS, f_{IN} = 241.1 MHz at AIN

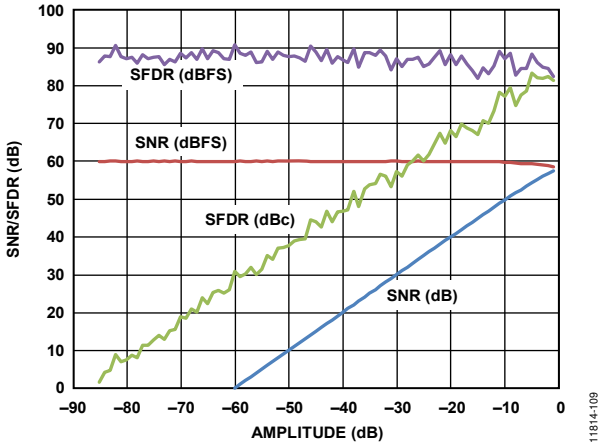

Figure 15. SNR/SFDR vs. Analog Input Amplitude at 2.0 GSPS, f_{IN} = 1811.3 MHz at AIN

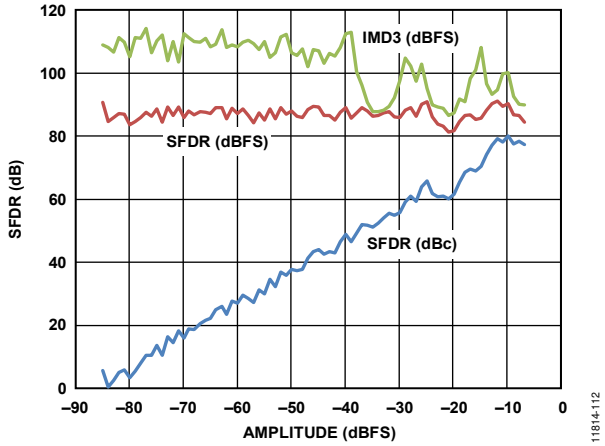

Figure 16. Two Tone SFDR and IMD3 vs. Analog Input Amplitude at 2.0 GSPS at 1800 MHz AIN

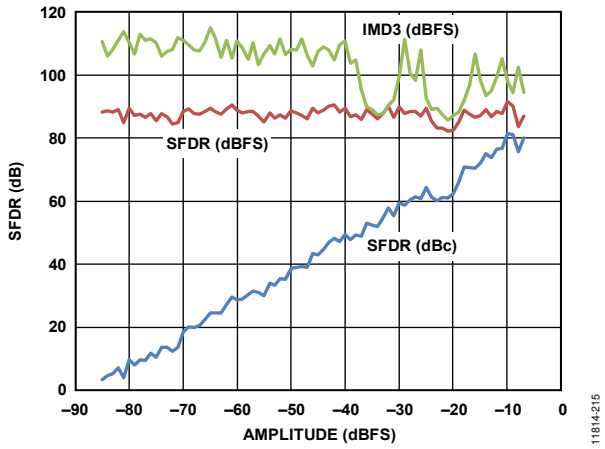

Figure 17. Two Tone SFDR and IMD3 vs. Analog Input Amplitude at 2.0 GSPS at 230 MHz AIN

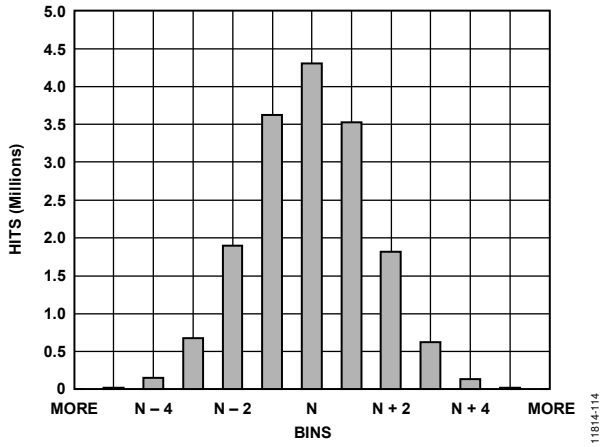

Figure 18. Input Referred Noise Histogram with 2.0 GSPS

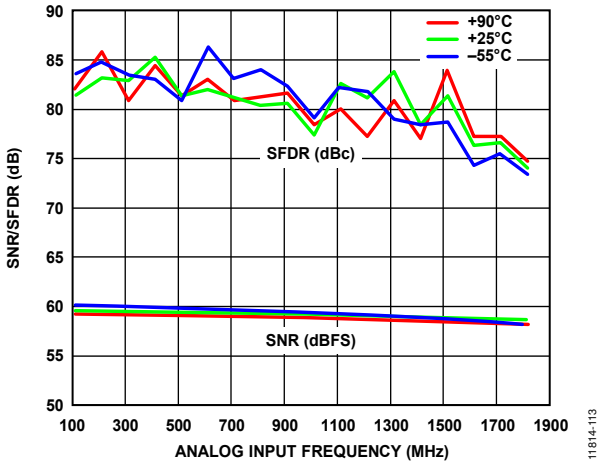

Figure 19. SNR/SFDR vs. Analog Input Frequency at Different Temperatures at 2.0 GSPS

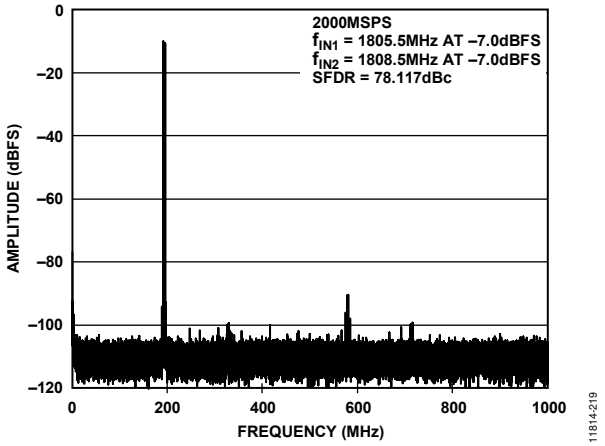

Figure 20. Two Tone FFT Plot at 2.0 GSPS, f_{IN1} = 1805.5 MHz and f_{IN2} = 1808.5 MHz at AIN, –7.0 dBFS (SFDR = 78.117 dBc)

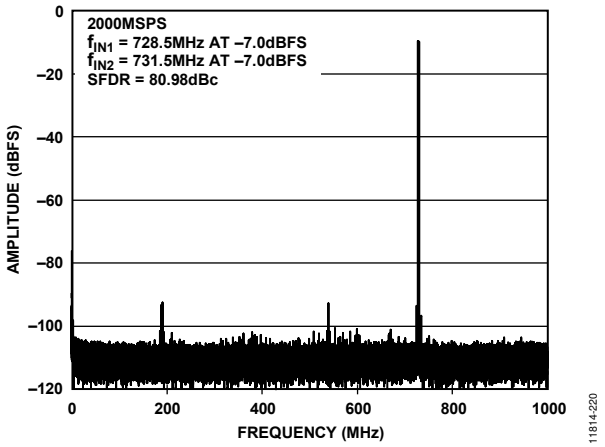

Figure 21. Two Tone FFT Plot at 2.0 GSPS, f_{IN1} = 728.5 MHz and f_{IN2} = 731.5 MHz at AIN, –7.0 dBFS (SFDR = 80.98 dBc)

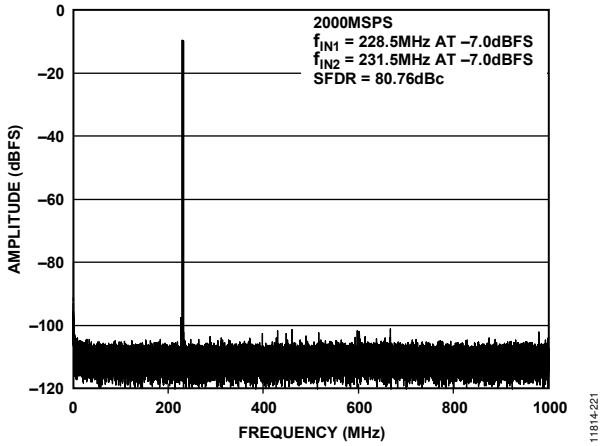

Figure 22. Two Tone FFT Plot at 2.0 GSPS, f_{IN1} = 228.5 MHz and f_{IN2} = 231.5 MHz at AIN, −7.0 dBFS (SFDR = 80.76 dBc)

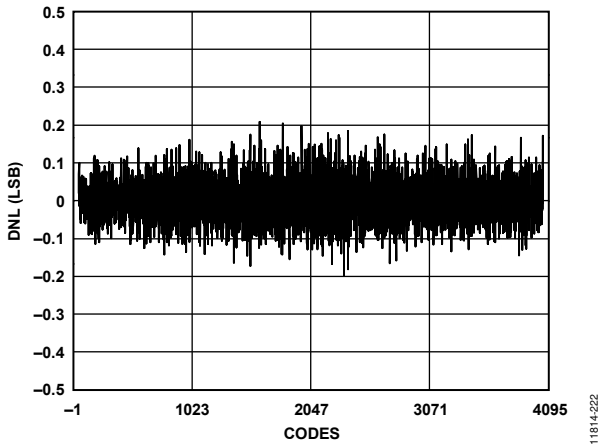

Figure 23. Differential Nonlinearity (DNL), ±0.2 LSB at 2.0 GSPS

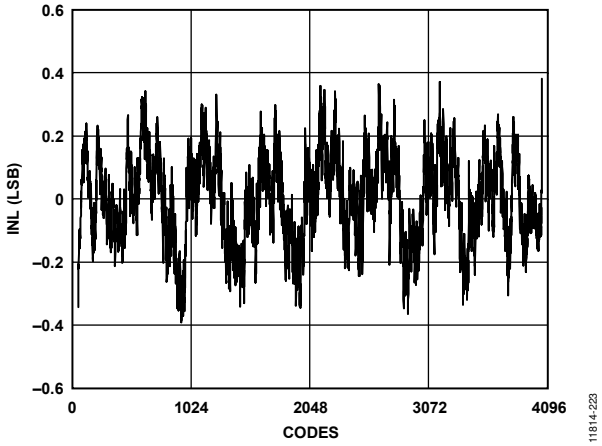

Figure 24. Integral Nonlinearity (INL), ±0.4 LSB at 2.0 GSPS

AD9625-2.5

For the AD9625-2.5 model, full-scale range used is 1.2 V.

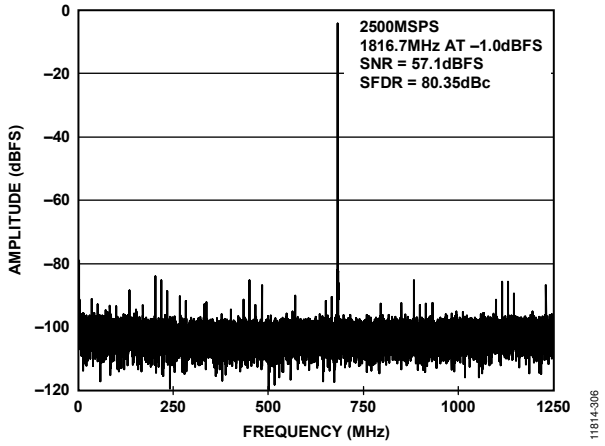

Figure 25. FFT Plot at 2.5 GSPS, f_{IN} = 1816.7 MHz at AIN (SFDR = 80.35 dBc, SNR = 57.1 dBFS)

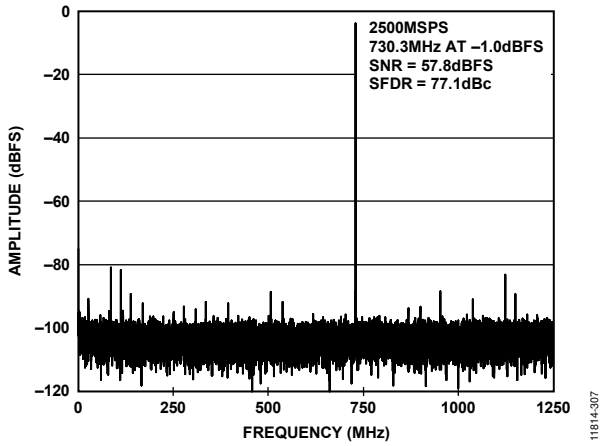

Figure 26. FFT Plot at 2.5 GSPS, f_{IN} = 730.3 MHz at AIN (SFDR = 77.1 dBc, SNR = 57.8 dBFS)

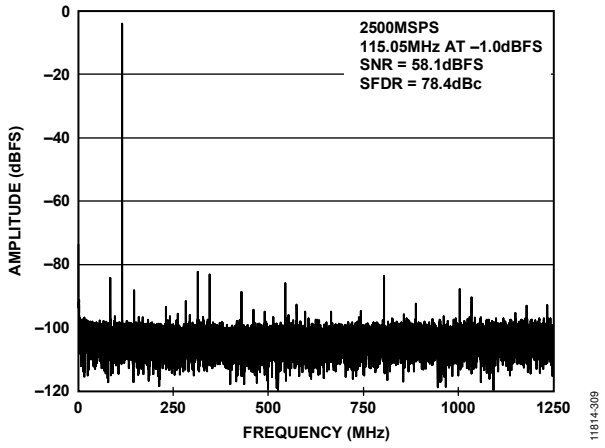

Figure 27. FFT Plot at 2.5 GSPS, f_{IN} = 115.05 MHz at AIN (SFDR = 78.4 dBc, SNR = 58.1 dBFS)

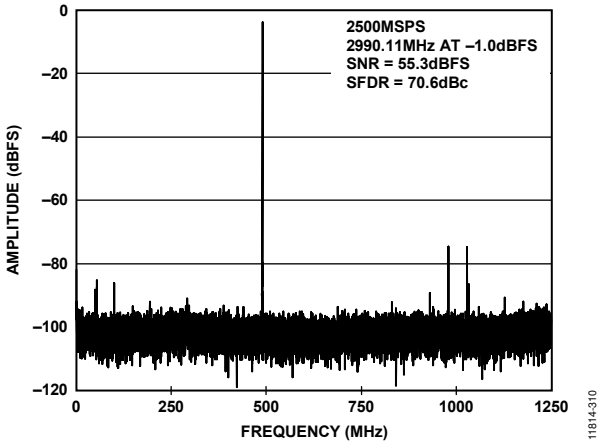

Figure 28. FFT Plot at 2.5 GSPS, f_{IN} = 2990.11 MHz at AIN (SFDR = 70.6 dBc, SNR = 55.3 dBFS) (Input Network in Figure 75 Used)

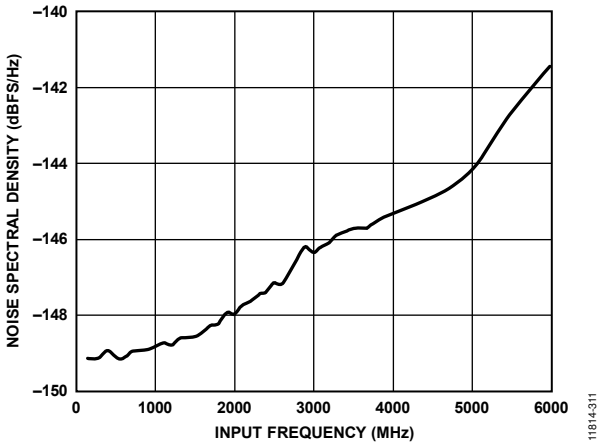

Figure 29. Noise Specrtal Density (NSD) vs. AIN at 2.5 GSPS (Input Network in Figure 76 Used <2 GHz, Input Network in Figure 75 Used >2 GHz)

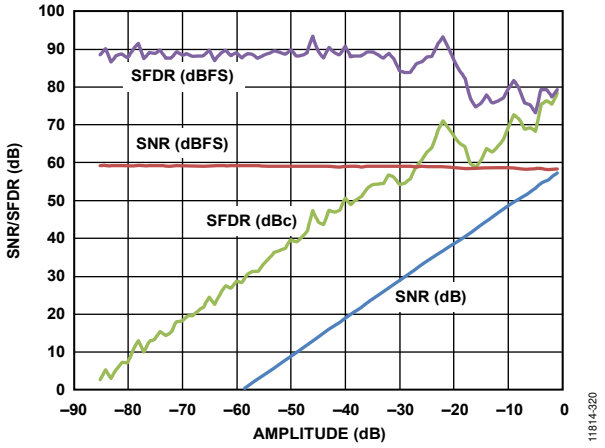

Figure 30. SNR/SFDR vs. Analog Input Amplitude at 2.5 GSPS, f_{IN} = 241 MHz at AIN

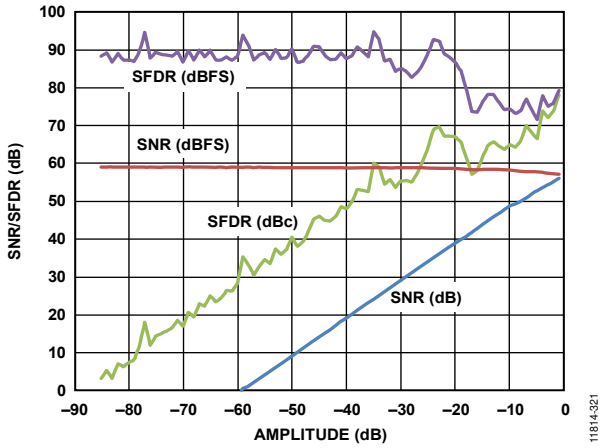

Figure 31. SNR/SFDR vs. Analog Input Amplitude at 2.5 GSPS, f_{IN} = 1811 MHz at AIN

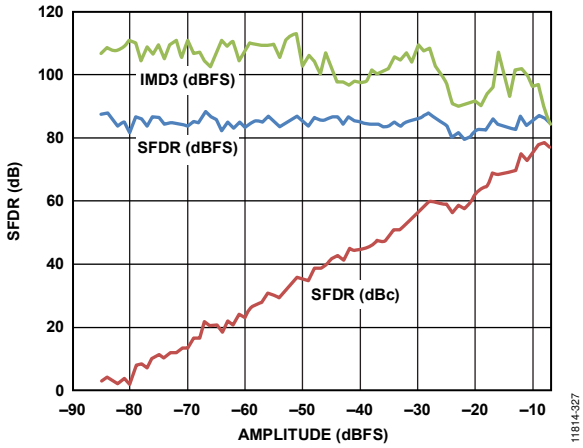

Figure 34. Two Tone SFDR and IMD3 vs. Analog Input Amplitude at 2.5 GSPS at 1800 MHz AIN

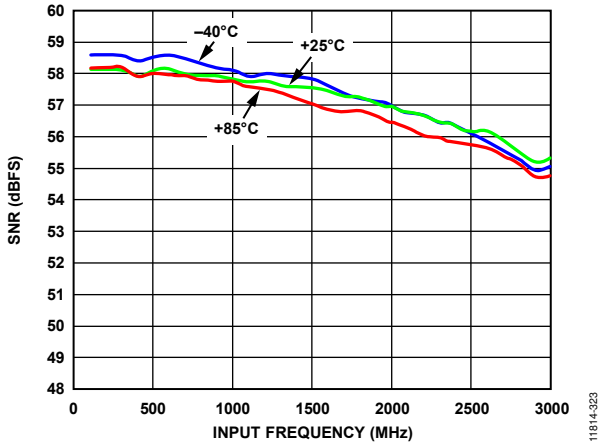

Figure 32. SNR at 2.5 GSPS vs. Temperature (Input Network in Figure 76 Used <2 GHz, Input Network in Figure 75 Used >2 GHz)

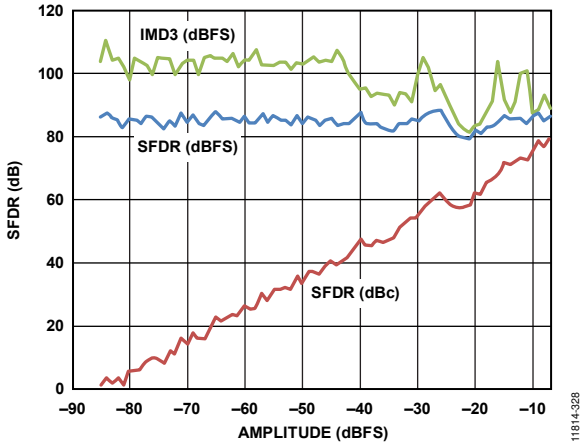

Figure 35. Two Tone SFDR and IMD3 vs. Analog Input Amplitude at 2.5 GSPS at 230 MHz AIN

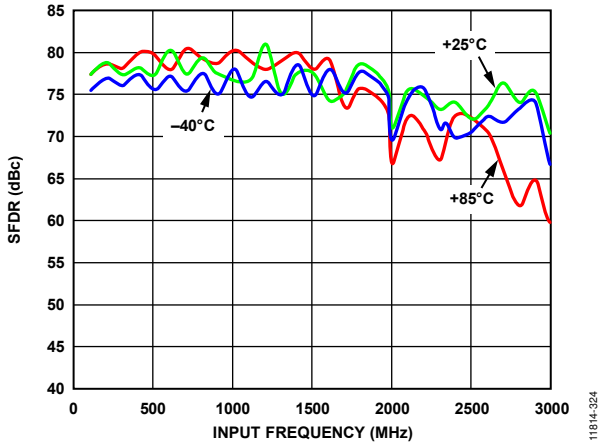

Figure 33. SFDR at 2.5 GSPS vs. Temperature (Input Network in Figure 76 Used <2 GHz, Input Network in Figure 75 Used >2 GHz)

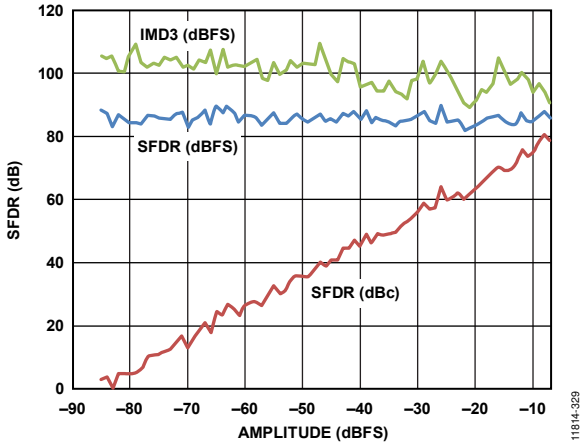

Figure 36. Two Tone SFDR and IMD3 vs. Analog Input Amplitude at 2.5 GSPS at 730 MHz AIN

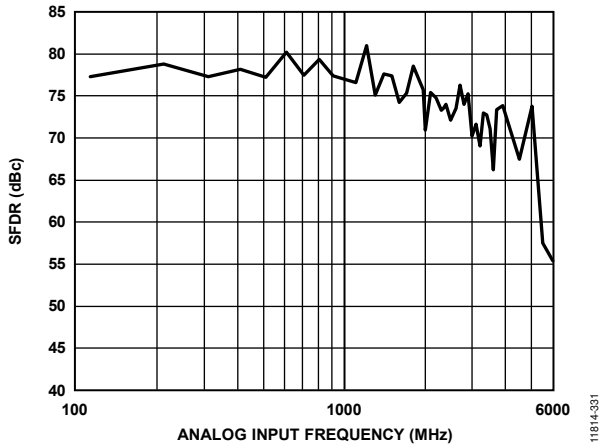

Figure 37. SFDR vs. AIN Frequency at 2.5 GSPS (Input Network in Figure 76 Used <2 GHz, Input Network in Figure 75 used >2 GHz)

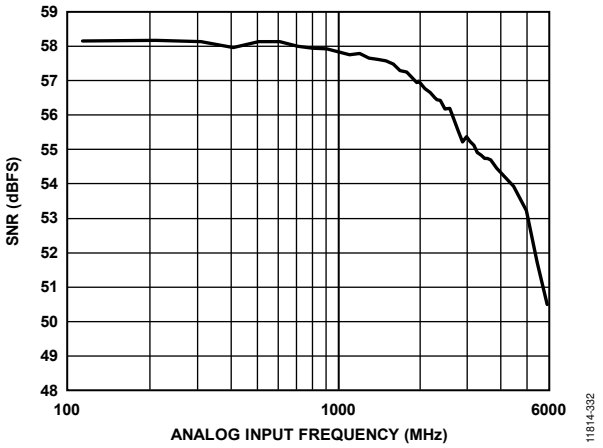

Figure 40. SNRFS vs. AIN Frequency at 2.5 GSPS (Input Network in Figure 76 Used <2 GHz, Input Network in Figure 75 Used >2 GHz)

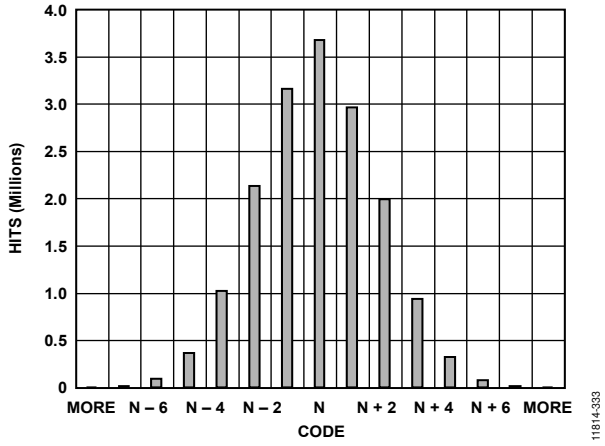

Figure 38. Input Referred Noise Histogram with 2.5 GSPS

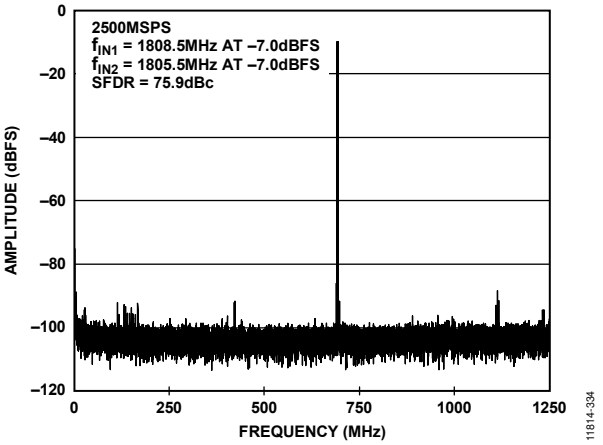

Figure 41. Two Tone FFT Plot at 2.5 GSPS, f_{IN1} = 1808.5 MHz and f_{IN2} = 1805.5 MHz at AIN, −7.0 dBFS (SFDR = 75.9 dBc)

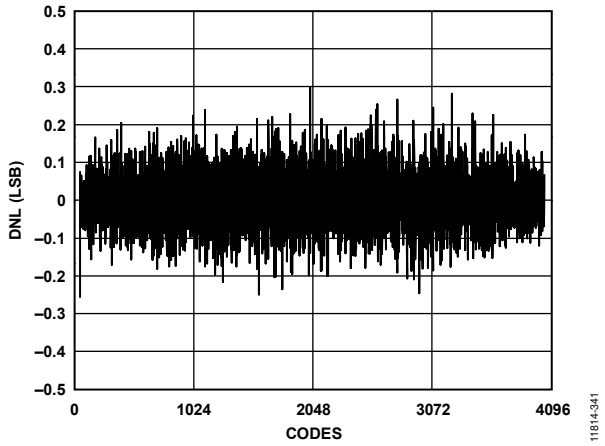

Figure 39. Differential Nonlinearity (DNL), ±0.3 LSB at 2.5 GSPS

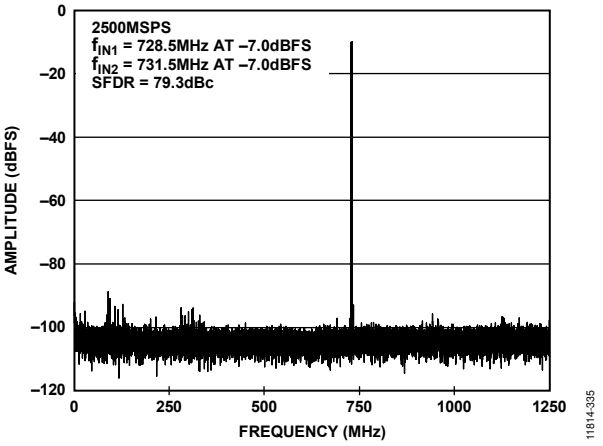

Figure 42. Two Tone FFT Plot at 2.5 GSPS, f_{IN1} = 728.5 MHz and f_{IN2} = 731.5 MHz at AIN, −7.0 dBFS (SFDR = 79.3 dBc)

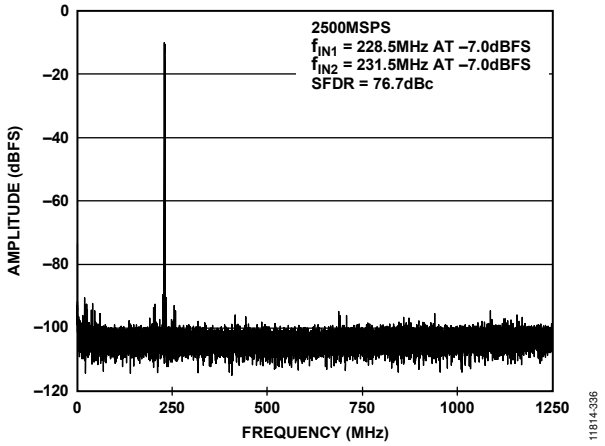

Figure 43. Two Tone FFT Plot at 2.5 GSPS, f_{IN1} = 228.5 MHz and f_{IN2} = 231.5 MHz at AIN, −7.0 dBFS (SFDR = 76.7 dBc)

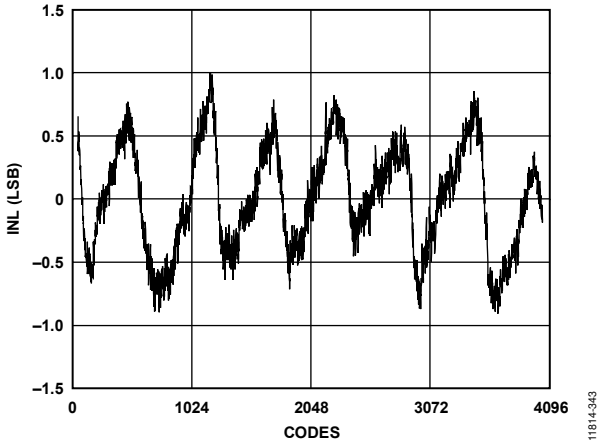

Figure 44. Integral Nonlinearity (INL), ±1.0 LSB at 2.5 GSPS