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12-Bit, 170 MSPS/210 MSPS/250 MSPS, 1.8 V Analog-to-Digital Converter

AD9626

FEATURES

SNR = 64.8 dBFS @ f_{IN} up to 70 MHz @ 250 MSPS
ENOB of 10.5 @ f_{IN} up to 70 MHz @ 250 MSPS (−1.0 dBFS)
SFDR = 80 dBc @ f_{IN} up to 70 MHz @ 250 MSPS (−1.0 dBFS)
Excellent linearity
- **DNL = ±0.3 LSB typical**
- **INL = ±0.7 LSB typical**

CMOS outputs
- **Single data port at up to 250 MHz**
- **Interleaved dual port @ ½ sample rate up to 125 MHz**

700 MHz full power analog bandwidth
On-chip reference, no external decoupling required
Integrated input buffer and track-and-hold
Low power dissipation
- **272 mW @ 170 MSPS**
- **364 mW @ 250 MSPS**

Programmable input voltage range
- **1.0 V to 1.5 V, 1.25 V nominal**

1.8 V analog and digital supply operation
Selectable output data format (offset binary, twos complement, Gray code)
Clock duty cycle stabilizer
Integrated data capture clock

APPLICATIONS

Wireless and wired broadband communications
Cable reverse path
Communications test equipment
Radar and satellite subsystems
Power amplifier linearization

FUNCTIONAL BLOCK DIAGRAM

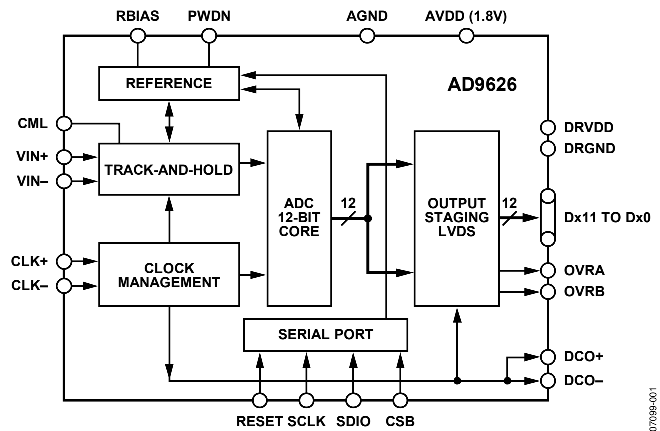

Figure 1.

GENERAL DESCRIPTION

The AD9626 is a 12-bit monolithic sampling analog-to-digital converter optimized for high performance, low power, and ease of use. The product operates at up to a 250 MSPS conversion rate and is optimized for outstanding dynamic performance in wideband carrier and broadband systems. All necessary functions, including a track-and-hold (T/H) and voltage reference, are included on the chip to provide a complete signal conversion solution.

The ADC requires a 1.8 V analog voltage supply and a differential clock for full performance operation. The digital outputs are CMOS compatible and support either twos complement, offset binary format, or Gray code. A data clock output is available for proper output data timing.

Fabricated on an advanced CMOS process, the AD9626 is available in a 56-lead LFCSP, specified over the industrial temperature range (−40°C to +85°C).

PRODUCT HIGHLIGHTS

1. High Performance—Maintains 64.9 dBFS SNR @ 250 MSPS with a 70 MHz input.
2. Low Power—Consumes only 364 mW @ 250 MSPS.
3. Ease of Use—CMOS output data and output clock signal allow interface to current FPGA technology. The on-chip reference and sample-and-hold provide flexibility in system design. Use of a single 1.8 V supply simplifies system power supply design.
4. Serial Port Control—Standard serial port interface supports various product functions, such as data formatting, clock duty cycle stabilizer, power-down, gain adjust, and output test pattern generation.
5. Pin-Compatible Family—10-bit pin-compatible family offered as the AD9601.

Rev. 0

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AD9626* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9626 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-282: Fundamentals of Sampled Data Systems
- AN-586: LVDS Outputs for High Speed A/D Converters
- AN-715: A First Approach to IBIS Models: What They Are and How They Are Generated
- AN-737: How ADIsimADC Models an ADC
- AN-741: Little Known Characteristics of Phase Noise
- AN-742: Frequency Domain Response of Switched-Capacitor ADCs
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-807: Multicarrier WCDMA Feasibility
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-812: MicroController-Based Serial Port Interface (SPI) Boot Circuit
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-878: High Speed ADC SPI Control Software
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual

Data Sheet

- AD9626: 12-Bit, 170 MSPS/210 MSPS/250 MSPS, 1.8 V Analog-to-Digital Converter Data Sheet

TOOLS AND SIMULATIONS

- Visual Analog
- AD9626 IBIS Models

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9626 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9626 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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TABLE OF CONTENTS

REVISION HISTORY

11/07—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = −40°C, T_{MAX} = +85°C, f_{IN} = −1.0 dBFS, full scale = 1.25 V, single port output mode, DCS enabled, unless otherwise noted.

Table 1.

		AD9626-170			AD9626-210			AD9626-250			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION			12			12			12		Bits
ACCURACY											
No Missing Codes	Full		Guaranteed			Guaranteed			Guaranteed		
Offset Error	25°C		4.0			4.0			4.0		mV
	Full	−12		+12	−12		+12	−12		+12	mV
Gain Error	25°C		1.4			1.4			1.4		% FS
	Full	−2.1		+4.5	−2.1		+4.5	−2.1		+4.5	% FS
Differential Nonlinearity (DNL)	25°C		0.3			0.3			0.3		LSB
	Full	−0.6		+0.6	−0.6		+0.6	−0.6		+0.6	LSB
Integral Nonlinearity (INL)	25°C		0.7			0.6			0.7		LSB
	Full	−1.4		+1.4	−1.1		+1.1	−1.7		+1.7	LSB
TEMPERATURE DRIFT											
Offset Error	Full		±8			±8			±8		µV/°C
Gain Error	Full		0.021			0.021			0.021		%/°C
ANALOG INPUTS (VIN+, VIN−)											
Differential Input Voltage Range[2]	Full	0.98	1.25	1.5	0.98	1.25	1.5	0.98	1.25	1.5	V p-p
Input Common-Mode Voltage	Full		1.4			1.4			1.4		V
Input Resistance (Differential)	Full		4.3			4.3			4.3		kΩ
Input Capacitance	25°C		2			2			2		pF
POWER SUPPLY											
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.58	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
Supply Currents											
I_{AVDD}[3]	Full		134	143		151	161		178	191	mA
I_{DRVDD}[3]/Single Port Mode[4]	Full		17	18.5		21	22		24	25.5	mA
I_{DRVDD}[3]/Interleaved Mode[5]	Full		15			18			20		mA
Power Dissipation[3]	Full										mW
Single Port Mode[4]	Full		272	291		310	330		364	390	mW
Interleaved Mode[5]	Full		268			304			357		mW
Power-Down Mode Supply Currents											
I_{AVDD}	Full		40			40			40		µA
I_{DRVDD}	Full		170			170	22		170		µA
Standby Mode Supply Currents											
I_{AVDD}	Full		19			19			19		mA
I_{DRVDD}	Full		170			170	22		170		µA

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] The input range is programmable through the SPI, and the range specified reflects the nominal values of each setting. See the Memory Map section.
[3] I_{AVDD} and I_{DRVDD} are measured with a −1 dBFS, 10.3 MHz sine input at rated sample rate.
[4] Single data rate mode; this is the default mode of the AD9626.
[5] Interleaved mode; user-programmable feature. See the Memory Map section.

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = −40°C, T_{MAX} = +85°C, f_{IN} = −1.0 dBFS, full scale = 1.25 V, , Single Port Output mode, DCS enabled, unless otherwise noted.[1]

Table 2.

		AD9626-170			AD9626-210			AD9626-250			
Parameter[2]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SNR											
f_{IN} = 10 MHz	25°C		64.5			64.4			64.0		dB
	Full			63.6			63.0				dB
f_{IN} = 70 MHz	25°C		64.4			64.2			63.8		dB
	Full			63.0			62.3				dB
SINAD											
f_{IN} = 10 MHz	25°C		64.5			64.4			64.0		dB
	Full			63.5			62.8				dB
f_{IN} = 70 MHz	25°C		64.2			64.0			63.4		dB
	Full			62.6			62.0				dB
EFFECTIVE NUMBER OF BITS (ENOB)											
f_{IN} = 10 MHz	25°C		10.6			10.6			10.5		Bits
f_{IN} = 70 MHz	25°C		10.5			10.5			10.5		Bits
WORST HARMONIC (SECOND OR THIRD)											
f_{IN} = 10 MHz	25°C		84			86			83		dBc
	Full			75			77			73	dBc
f_{IN} = 70 MHz	25°C		79			79			80		dBc
	Full			71			73			71	dBc
WORST OTHER (SFDR EXCLUDING SECOND AND THIRD)											
f_{IN} = 10 MHz	25°C		92			90			84		dBc
	Full			85			79			76	dBc
f_{IN} = 70 MHz	25°C		92			87			84		dBc
	Full			81			77			73	dBc
TWO-TONE IMD											
140.2 MHz/141.3 MHz @ −7 dBFS	25°C		80								dBFS
170.2 MHz/171.3 MHz @ −7 dBFS	25°C					83			83		dBc
ANALOG INPUT BANDWIDTH	25°C		700			700			700		MHz

[1] All ac specifications tested by driving CLK+ and CLK− differentially.
[2] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = −40°C, T_{MAX} = +85°C, f_{IN} = −1.0 dBFS, full scale = 1.25 V, DCS enabled, unless otherwise noted.

Table 3.

		AD9626-170			AD9626-210			AD9626-250			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUTS											
Logic Compliance	Full		CMOS/LVDS/LVPECL			CMOS/LVDS/LVPECL			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		1.2			1.2			1.2		V
Differential Input Voltage	Full	0.2		6	0.2		6	0.2		6	V p-p
Input Voltage Range	Full	AVDD − 0.3		AVDD + 1.6	AVDD − 0.3		AVDD + 1.6	AVDD − 0.3		AVDD + 1.6	V
Input Common-Mode Range	Full	1.1		AVDD	1.1		AVDD	1.1		AVDD	V
High Level Input Voltage (V_{IH})	Full	1.2		3.6	1.2		3.6	1.2		3.6	V
Low Level Input Voltage (V_{IL})	Full	0		0.8	0		0.8	0		0.8	V
Input Resistance (Differential)	Full	16	20	24	16	20	24	16	20	24	kΩ
Input Capacitance	Full		4			4			4		pF
LOGIC INPUTS											
Logic 1 Voltage	Full	0.8 × AVDD			0.8 × AVDD			0.8 × AVDD			V
Logic 0 Voltage	Full			0.2 × AVDD			0.2 × AVDD			0.2 × AVDD	V
Logic 1 Input Current (SDIO)	Full		0			0			0		µA
Logic 0 Input Current (SDIO)	Full		−60			−60			−60		µA
Logic 1 Input Current (SCLK, PDWN, CSB, RESET)	Full		55			55			50		µA
Logic 0 Input Current (SCLK, PDWN, CSB, RESET)	Full		0			0			0		µA
Input Capacitance	25°C		4			4			4		pF
LOGIC OUTPUTS[2]											
High Level Output Voltage	Full	DRVDD − 0.05			DRVDD − 0.05			DRVDD − 0.05			V
Low Level Output Voltage	Full		GND + 0.05			GND + 0.05			GND + 0.05		V
Output Coding		Twos complement, Gray code, or offset binary (default)									

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] LVDS $R_{TERMINATION}$ = 100 Ω.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = −40°C, T_{MAX} = +85°C, f_{IN} = −1.0 dBFS, full scale = 1.25 V, DCS enabled, unless otherwise noted.

Table 4.

		AD9626-170			AD9626-210			AD9626-250			
Parameter (Conditions)	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Maximum Conversion Rate	Full	170			210			250			MSPS
Minimum Conversion Rate	Full			40			40			40	MSPS
CLK+ Pulse Width High (t_{CH})	Full	2.65	2.9		2.15	2.4		1.8	2.0		ns
CLK+ Pulse Width Low (t_{CL})	Full	2.65	2.9		2.15	2.4		1.8	2.0		ns
Output, Single Data Port Mode[1]											
Data Propagation Delay (t_{PD})	25°C		3.7			3.7			3.7		ns
DCO Propagation Delay (t_{CPD})	25°C		3.4			3.4			3.4		ns
Data to DCO Skew (t_{SKEW})	Full	0	0.3	0.55	0	0.3	0.55	0	0.3	0.55	ns
Latency	Full		6			6			6		Cycles
Output, Interleaved Mode[2]											
Data Propagation Delay (t_{PDA}, t_{PDB})	25°C		3.5			3.5			3.5		ns
DCO Propagation Delay (t_{CPDA}, t_{CPDB})	25°C		3.0			3.0			3.0		ns
Data to DCO Skew (t_{SKEWA}, t_{SKEWB})	Full	0	0.5	1.1	0	0.5	1.1	0	0.5	1.1	ns
Latency	Full		6			6			6		Cycles
Standby Recovery	25°C		250			250			250		ns
Power-Down Recovery			50			50			50		µs
Aperture Delay (t_A)	25°C		0.1			0.1			0.1		ns
Aperture Uncertainty (Jitter, t_J)	25°C		0.2			0.2			0.2		ps rms

[1] See Figure 2.
[2] See Figure 3.

TIMING DIAGRAMS

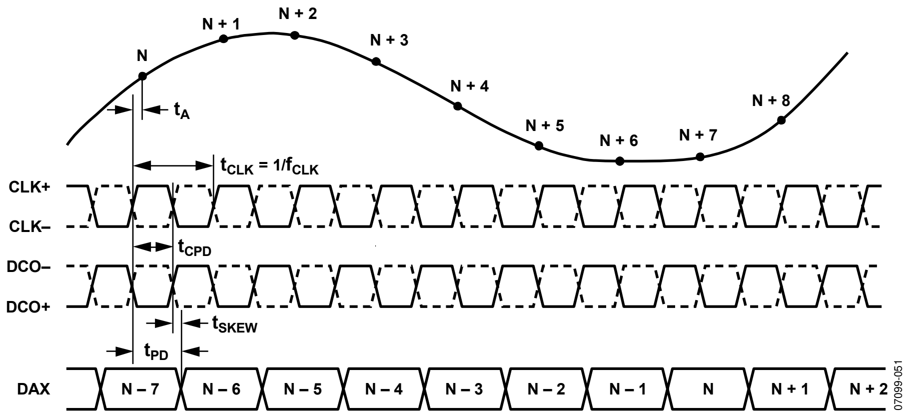


Figure 2. Single Port Mode

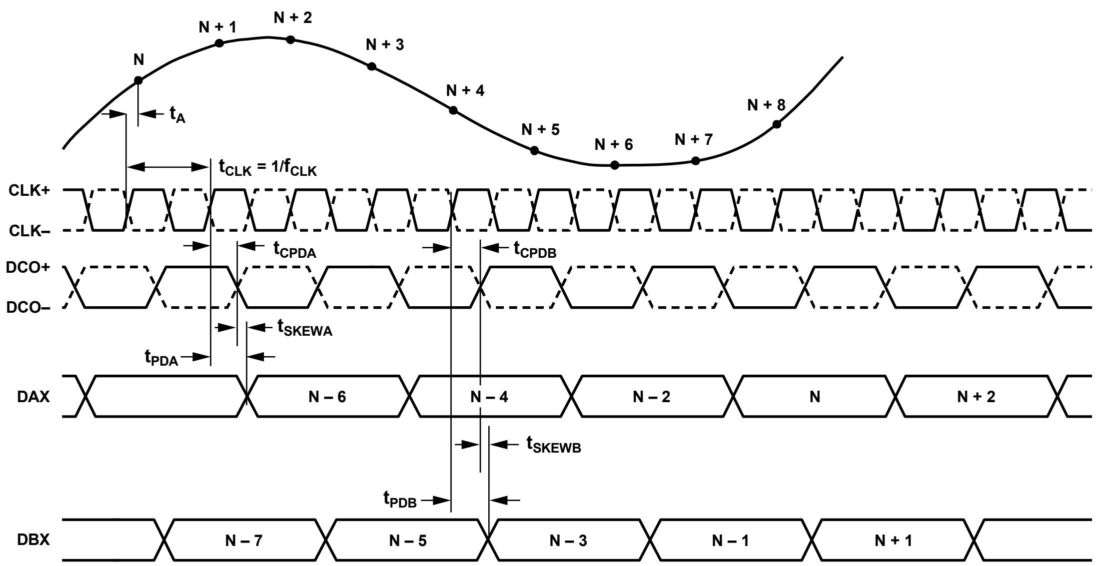


Figure 3. Interleaved Mode

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
ELECTRICAL	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to DRGND	−0.3 V to +2.0 V
AGND to DRGND	−0.3 V to +0.3 V
AVDD to DRVDD	−2.0 V to +2.0 V
Dx0 Through Dx11 to DRGND	−0.3 V to DRVDD + 0.3 V
DCO+/DCO− to DRGND	−0.3 V to DRVDD + 0.3 V
OVRA/OVRB to DGND	−0.3 V to DRVDD + 0.3 V
CLK+ to AGND	−0.3 V to +3.6 V
CLK− to AGND	−0.3 V to +3.6 V
VIN+ to AGND	−0.3 V to AVDD + 0.2 V
VIN− to AGND	−0.3 V to AVDD + 0.2 V
SDIO/DCS to DGND	−0.3 V to DRVDD + 0.3 V
PDWN to AGND	−0.3 V to +3.6 V
CSB to AGND	−0.3 V to +3.6 V
SCLK/DFS to AGND	−0.3 V to +3.6 V
ENVIRONMENTAL	
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

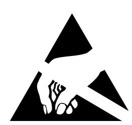
The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the customer board increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 6.

Package Type	θ_{JA}	θ_{JC}	Unit
56-Lead LFCSP (CP-56-2)	30.4	2.9	°C/W

Typical θ_{JA} and θ_{JC} are specified for a 4-layer board in still air. Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, and through holes, ground, and power planes reduces the θ_{JA}.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

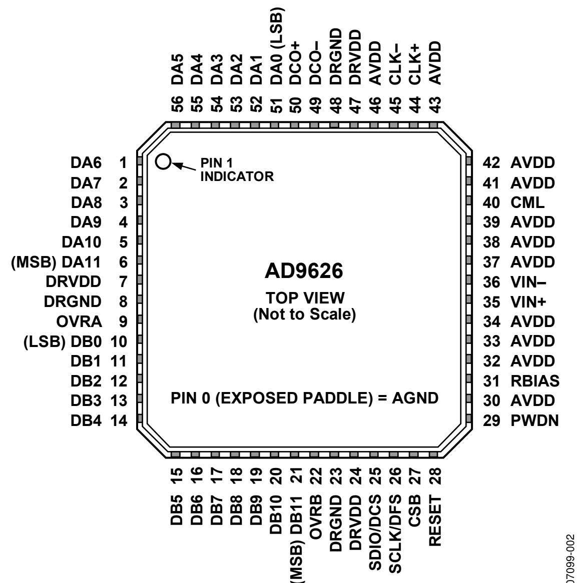


Figure 4. Pin Configuration

Table 7. Single Data Rate Mode Pin Function Descriptions

Pin No.	Mnemonic	Description
30, 32, 33, 34, 37, 38, 39, 41, 42, 43, 46	AVDD	1.8 V Analog Supply.
7, 24, 47	DRVDD	1.8 V Digital Output Supply.
0	AGND[1]	Analog Ground.
8, 23, 48	DRGND[1]	Digital Output Ground.
35	VIN+	Analog Input—True.
36	VIN–	Analog Input—Complement.
40	CML	Common-Mode Output Pin. Enabled through the SPI, this pin provides a reference for the optimized internal bias voltage for VIN+/VIN–.
44	CLK+	Clock Input—True.
45	CLK–	Clock Input—Complement.
31	RBIAS	Set Pin for Chip Bias Current. (Place 1% 10 kΩ resistor terminated to ground.) Nominally 0.5 V.
28	RESET	CMOS-Compatible Chip Reset (Active Low).
25	SDIO/DCS	Serial Port Interface (SPI) Data Input/Output (Serial Port Mode); Duty Cycle Stabilizer Select (External Pin Mode).
26	SCLK/DFS	Serial Port Interface Clock (Serial Port Mode); Data Format Select Pin (External Pin Mode).
27	CSB	Serial Port Chip Select (Active Low).
29	PWDN	Chip Power-Down.
49	DCO–	Data Clock Output—Complement.
50	DCO+	Data Clock Output—True.
51	DA0 (LSB)	Output Port A Output Bit 0 (LSB).
52	DA1	Output Port A Output Bit 1.
53	DA2	Output Port A Output Bit 2.
54	DA3	Output Port A Output Bit 3.
55	DA4	Output Port A Output Bit 4.
56	DA5	Output Port A Output Bit 5.
1	DA6	Output Port A Output Bit 6.
2	DA7	Output Port A Output Bit 7.

Pin No.	Mnemonic	Description
3	DA8	Output Port A Output Bit 8.
4	DA9	Output Port A Output Bit 9.
5	DA10	Output Port A Output Bit 10.
6	DA11 (MSB)	Output Port A Output Bit 11 (MSB).
9	OVRA	Output Port A Overrange Output Bit.
10	DB0 (LSB)	Output Port B Output Bit 0 (LSB).
11	DB1	Output Port B Output Bit 1.
12	DB2	Output Port B Output Bit 2.
13	DB3	Output Port B Output Bit 3.
14	DB4	Output Port B Output Bit 4.
15	DB5	Output Port B Output Bit 5.
16	DB6	Output Port B Output Bit 6.
17	DB7	Output Port B Output Bit 7.
18	DB8	Output Port B Output Bit 8.
19	DB9	Output Port B Output Bit 9.
20	DB10	Output Port B Output Bit 10.
21	DB11 (MSB)	Output Port B Output Bit 11 (MSB).
22	OVRB	Output Port B Overrange Output Bit.

[1] AGND and DRGND should be tied to a common quiet ground plane.

EQUIVALENT CIRCUITS

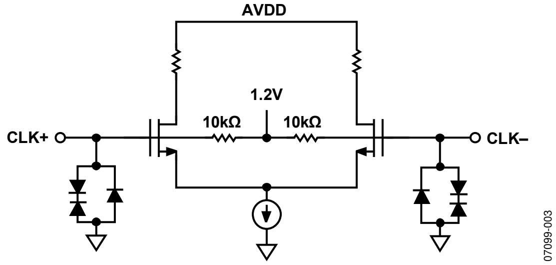


Figure 5. Clock Inputs

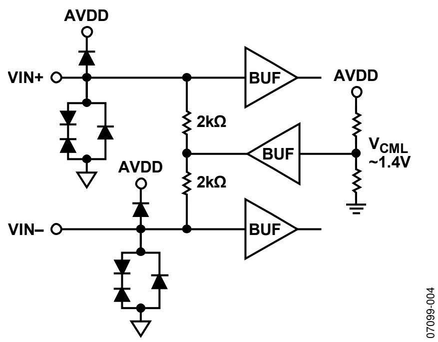


Figure 6. Analog Inputs (V_{CML} = ~1.4 V)

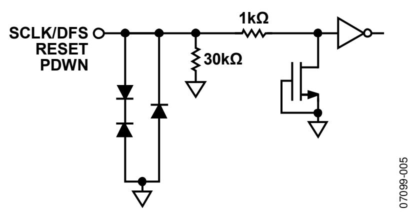


Figure 7. Equivalent SCLK/DFS, RESET, PDWN Input Circuit

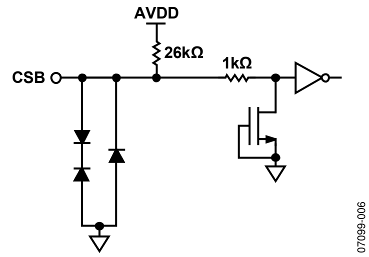


Figure 8. Equivalent CSB Input Circuit

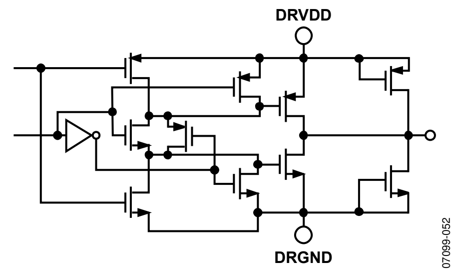


Figure 9. CMOS Outputs (Dx, OVRA, OVRB, DCO+, DCO−)

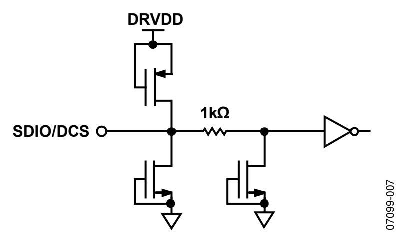


Figure 10. Equivalent SDIO/DCS Input Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, rated sample rate, DCS enabled, T_A = 25°C, 1.25 V p-p differential input, AIN = −1 dBFS, unless otherwise noted.

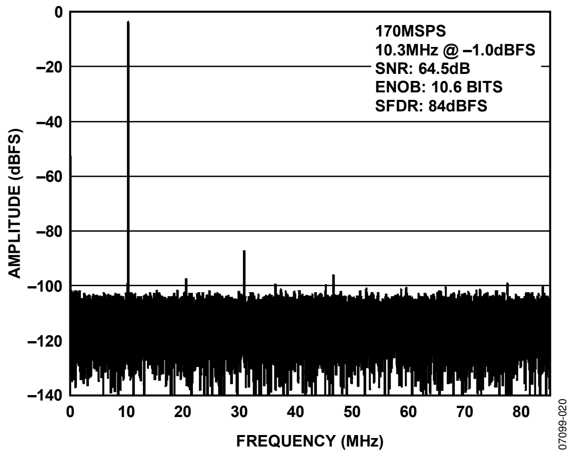


Figure 11. AD9626-170 64k Point Single-Tone FFT; 170 MSPS, 10.3 MHz

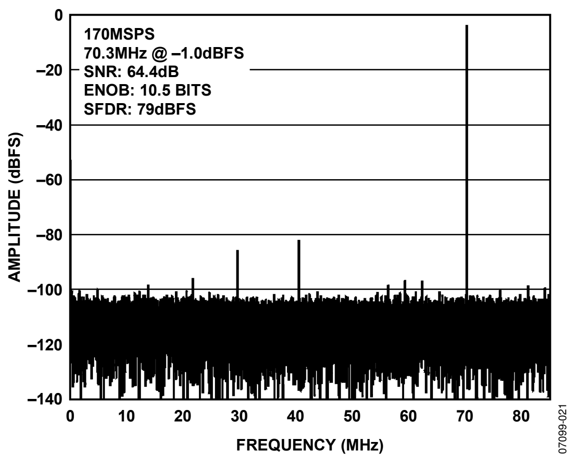


Figure 12. AD9626-170 64k Point Single-Tone FFT; 170 MSPS, 70.3 MHz

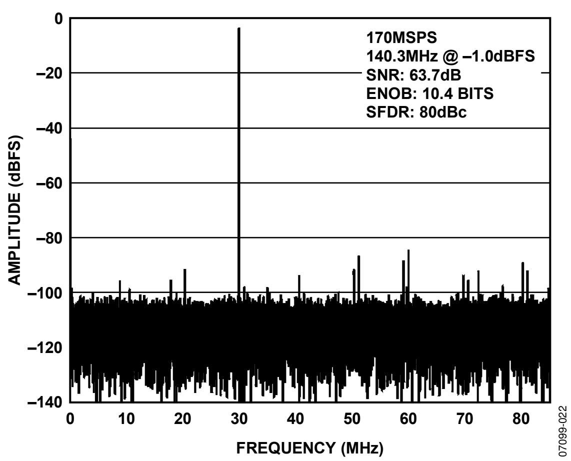


Figure 13. AD9626-170 64k Point Single-Tone FFT; 170 MSPS, 140.3 MHz

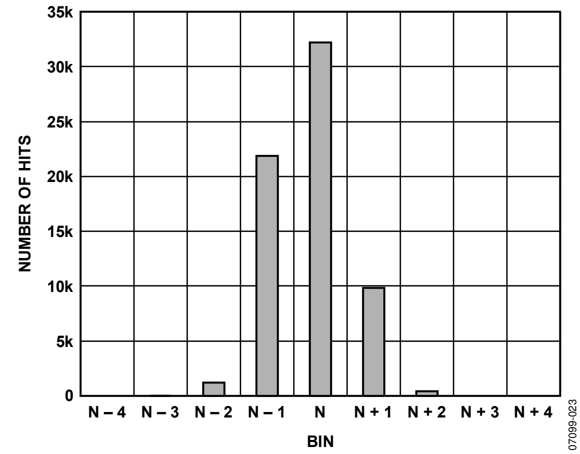


Figure 14. AD9626-170 Grounded Input Histogram; 170 MSPS

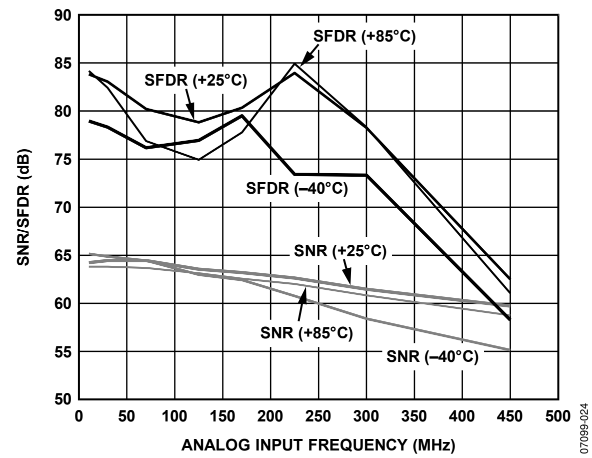


Figure 15. AD9626-170 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 1.25 V p-p Full Scale; 170 MSPS

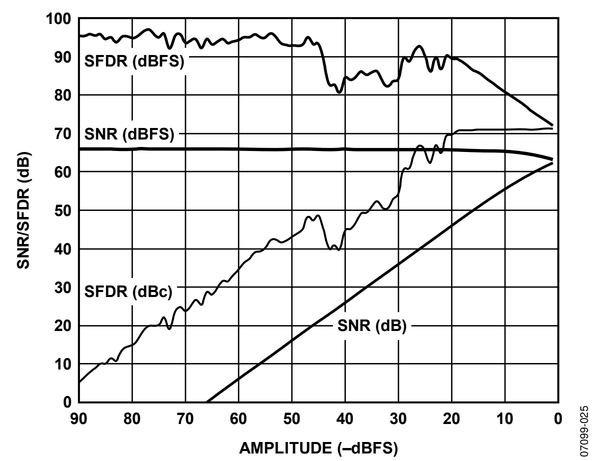


Figure 16. AD9626-170 SNR/SFDR vs. Input Amplitude; 140.3 MHz

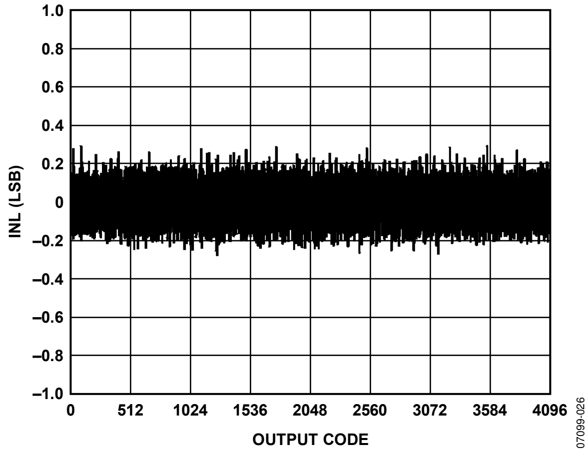


Figure 17. AD9626-170 INL; 170 MSPS

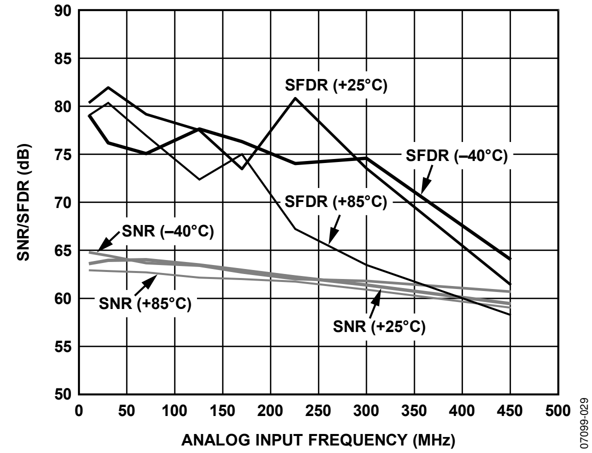


Figure 20. SNR/SFDR vs. Analog Input Frequency, Interleaved Mode vs. Temperature

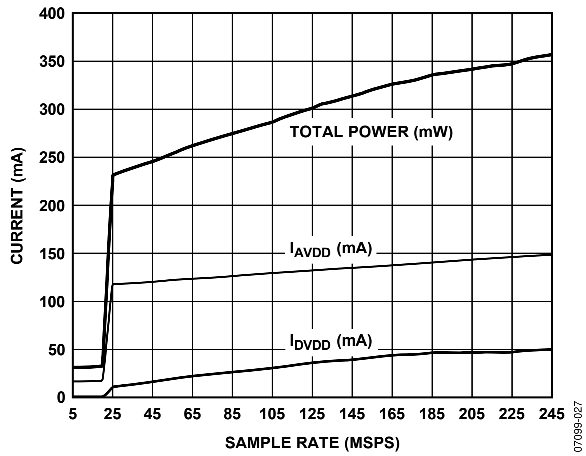


Figure 18. AD9626-170 Power Supply Current vs. Sample Rate

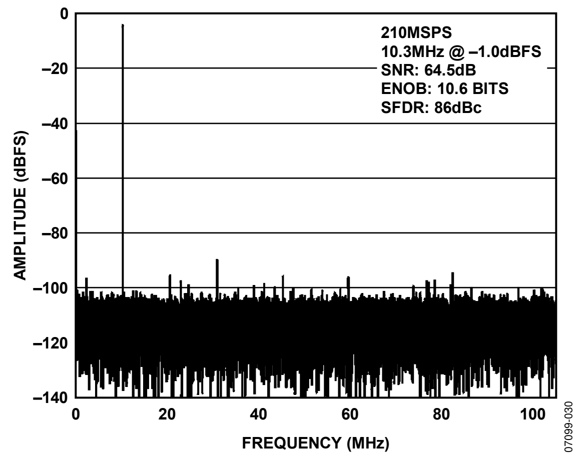


Figure 21. AD9626-210 64k Point Single-Tone FFT; 210 MSPS, 10.3 MHz

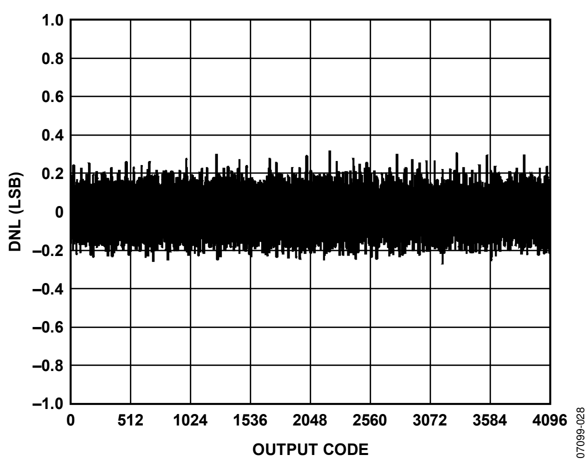


Figure 19. AD9626-170 DNL; 170 MSPS

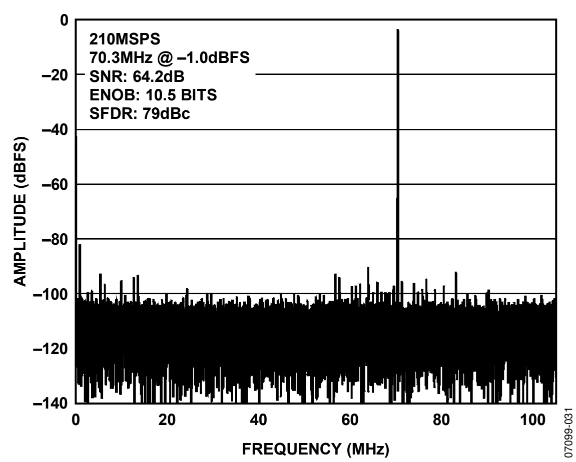


Figure 22. AD9626-210 64k Point Single-Tone FFT; 210 MSPS, 70.3 MHz

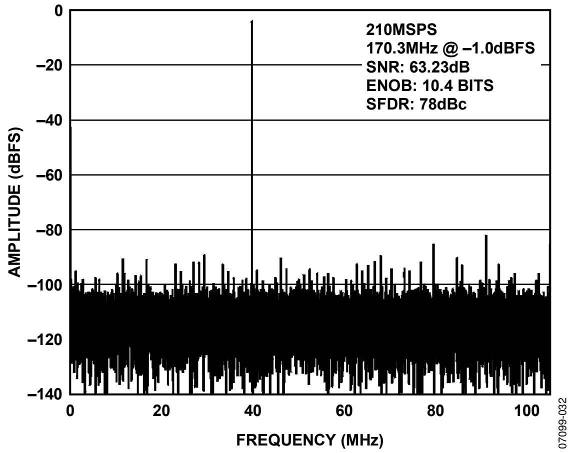


Figure 23. AD9626-210 64k Point Single-Tone FFT; 210 MSPS, 170.3 MHz

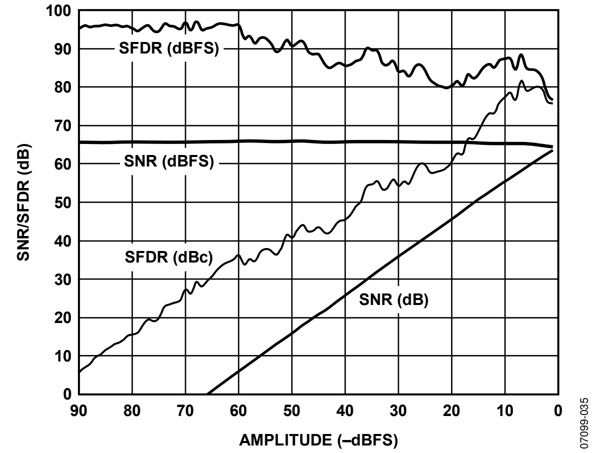


Figure 26. AD9626-210 SNR/SFDR vs. Input Amplitude; 210 MSPS, 170.3 MHz

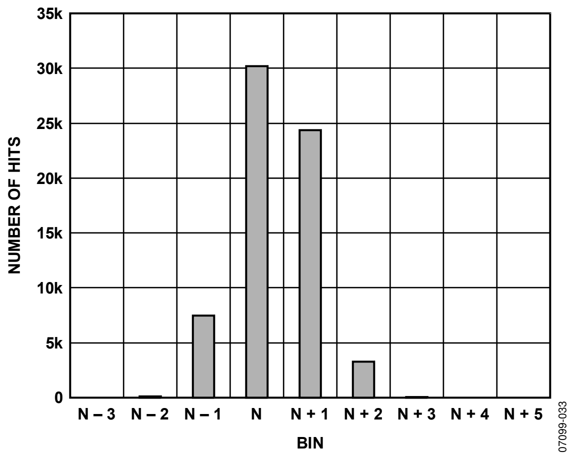


Figure 24. AD9626-210 Grounded Input Histogram; 210 MSPS

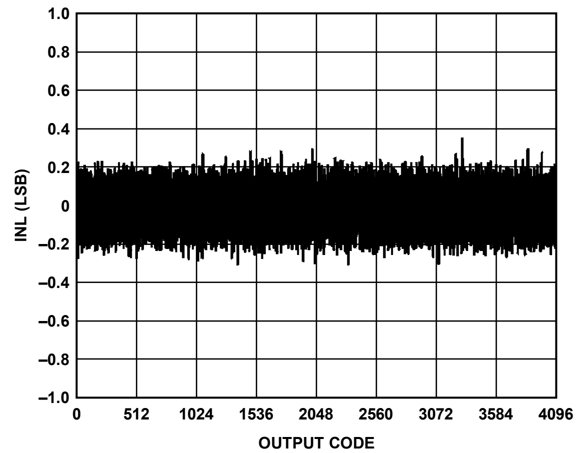


Figure 27. AD9626-210 INL; 210 MSPS

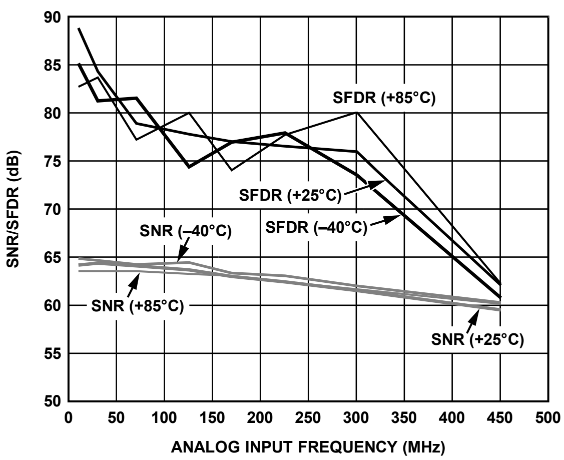


Figure 25. AD9626-210 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 1.25 V p-p Full Scale; 210 MSPS

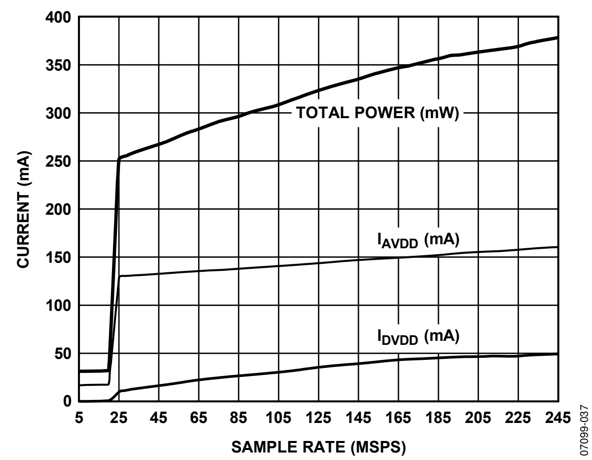


Figure 28. AD9626-210 Power Supply Current vs. Sample Rate

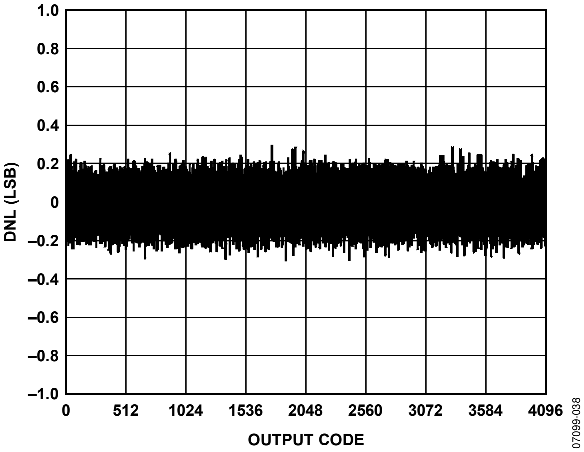


Figure 29. AD9626-210 DNL; 210 MSPS

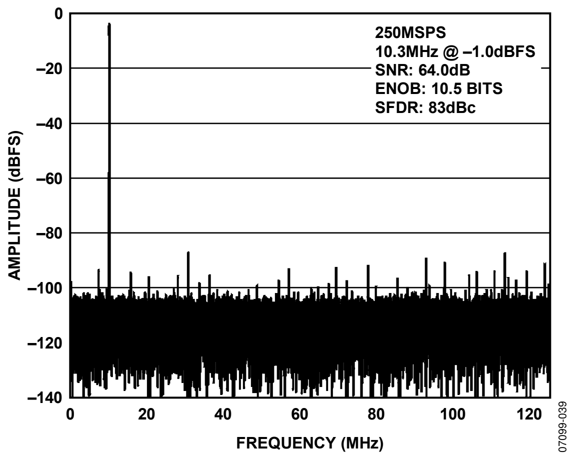


Figure 30. AD9626-250 64k Point Single-Tone FFT; 250 MSPS, 10.3 MHz

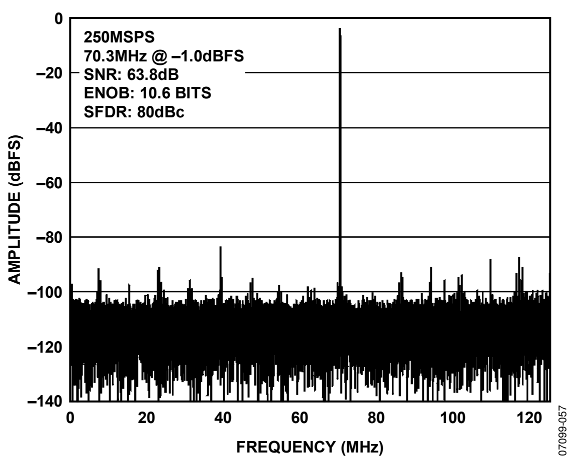


Figure 31. AD9626-250 64k Point Single-Tone FFT; 250 MSPS, 70.3 MHz

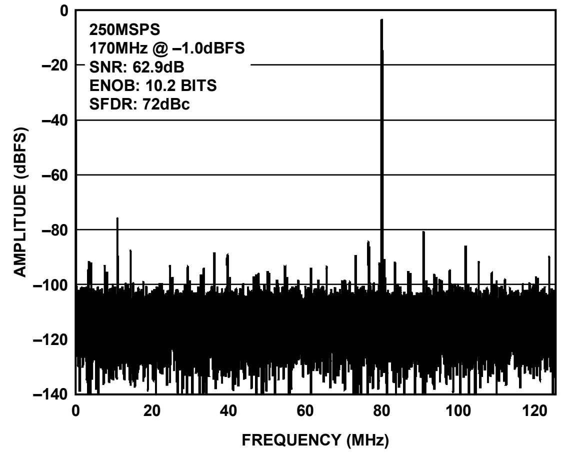


Figure 32. AD9626-250 64k Point Single-Tone FFT; 250 MSPS, 170.3 MHz

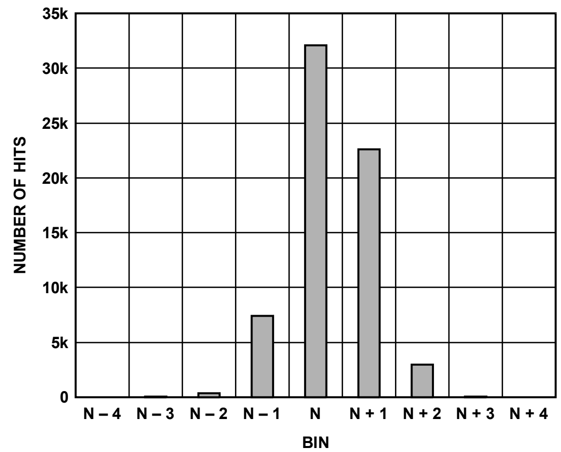


Figure 33. AD9626-250 Grounded Input Histogram; 250 MSPS

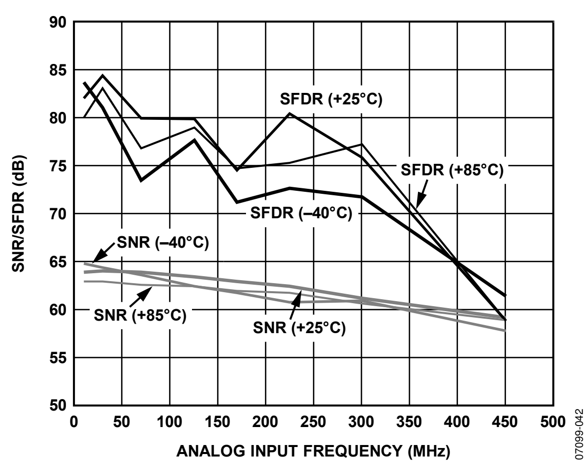


Figure 34. AD9626-250 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 1.25 V p-p Full Scale; 250 MSPS

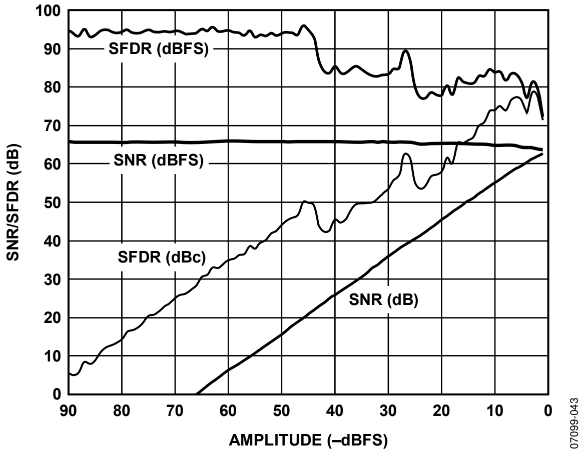


Figure 35. AD9626-250 SNR/SFDR vs. Input Amplitude; 250 MSPS, 170.3 MHz

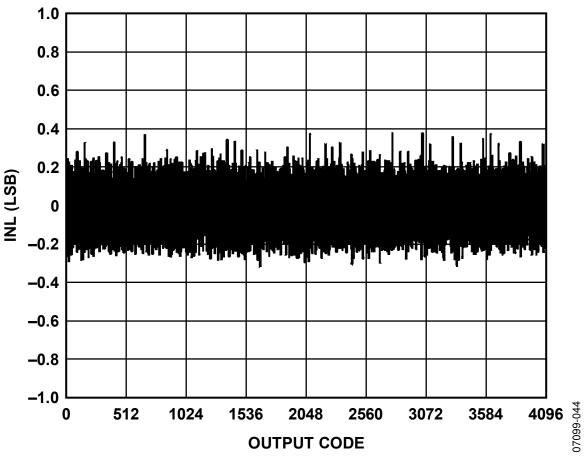


Figure 36. AD9626-250 INL; 250 MSPS

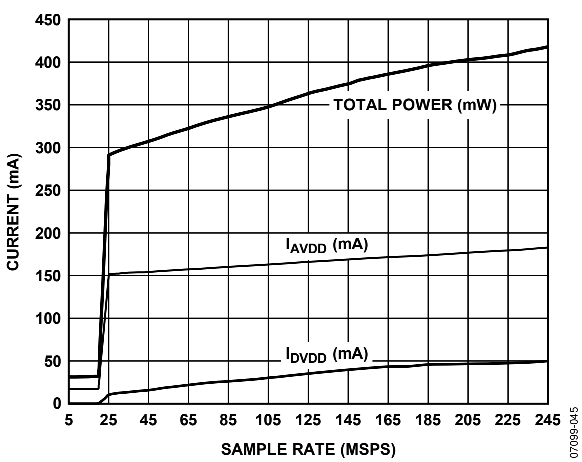


Figure 37. AD9626 Power Supply Current vs. Sample Rate

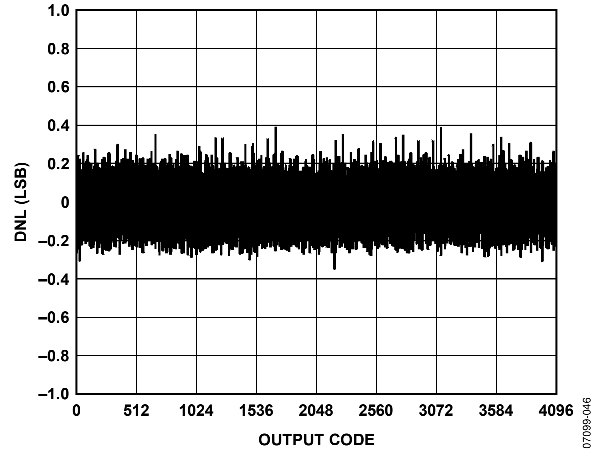


Figure 38. AD9626-250 DNL; 250 MSPS

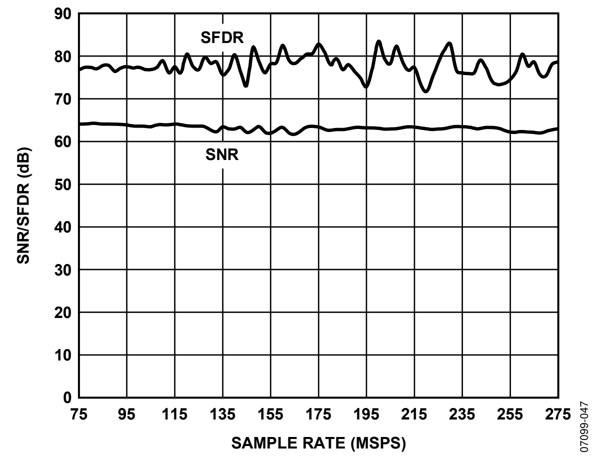


Figure 39. SNR/SFDR vs. Sample Rate; 250 MSPS, 170.3 MHz @ −1 dBFS

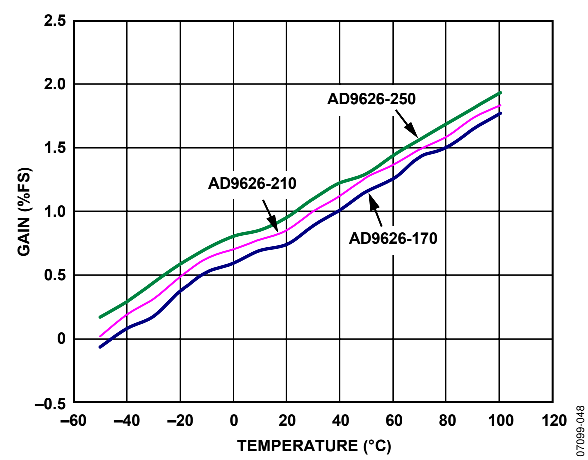


Figure 40. Gain vs. Temperature

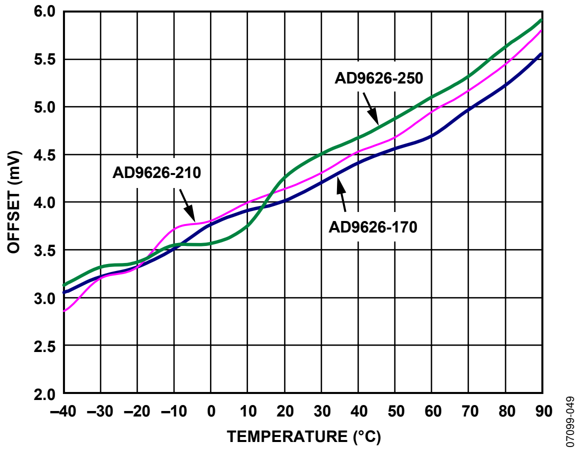


Figure 41. Offset vs. Temperature

THEORY OF OPERATION

The AD9626 architecture consists of a front-end sample-and-hold amplifier (SHA) followed by a pipelined switched capacitor ADC. The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample, while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage contains a differential SHA that can be ac- or dc-coupled. The output-staging block aligns the data, carries out the error correction, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing. During power-down, the output buffers go into a high impedance state.

ANALOG INPUT AND VOLTAGE REFERENCE

The analog input to the AD9626 is a differential buffer. For best dynamic performance, the source impedances driving VIN+ and VIN− should be matched such that common-mode settling errors are symmetrical. The analog input is optimized to provide superior wideband performance and requires that the analog inputs be driven differentially.

A wideband transformer, such as Mini-Circuits® ADT1-1WT, can provide the differential analog inputs for applications that require a single-ended-to-differential conversion. Both analog inputs are self-biased by an on-chip resistor divider to a nominal 1.4 V.

An internal differential voltage reference creates positive and negative reference voltages that define the 1.25 V p-p fixed span of the ADC core. This internal voltage reference can be adjusted by means of SPI control. See the AD9626 Configuration Using the SPI section for more details.

Differential Input Configurations

Optimum performance is achieved while driving the AD9626 in a differential input configuration. For baseband applications, the AD8138 differential driver provides excellent performance and a flexible interface to the ADC. The output common-mode voltage of the AD8138 is easily set to AVDD/2 + 0.5 V, and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

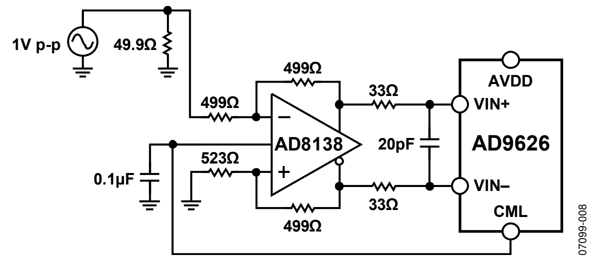


Figure 42. Differential Input Configuration Using the AD8138

At input frequencies in the second Nyquist zone and above, the performance of most amplifiers may not be adequate to achieve the true performance of the AD9626. This is especially true in IF undersampling applications where frequencies in the 70 MHz to 100 MHz range are being sampled. For these applications, differential transformer coupling is the recommended input configuration. The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few millihertz, and excessive signal power can also cause core saturation, which leads to distortion.

In any configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

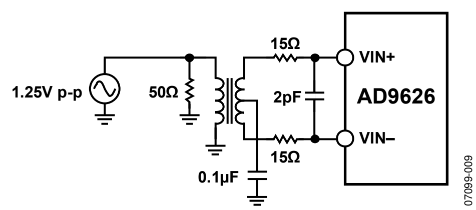


Figure 43. Differential Transformer-Coupled Configuration

As an alternative to using a transformer-coupled input at frequencies in the second Nyquist zone, the AD8352 differential driver can be used (see Figure 44).

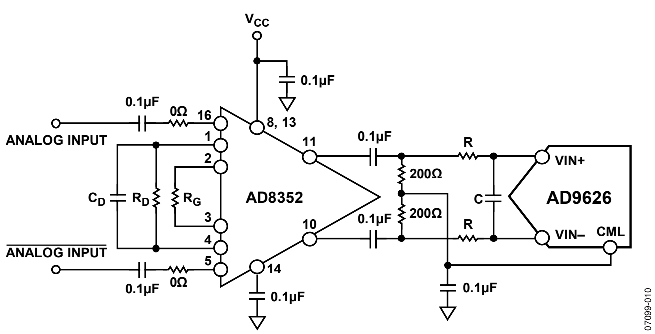


Figure 44. Differential Input Configuration Using the AD8352

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9626 sample clock inputs (CLK+ and CLK−) should be clocked with a differential signal. This signal is typically ac-coupled into the CLK+ pin and the CLK− pin via a transformer or capacitors. These pins are biased internally and require no additional bias.

Figure 45 shows one preferred method for clocking the AD9626. The low jitter clock source is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the secondary transformer limit clock excursions into the AD9626 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9626 and preserves the fast rise and fall times of the signal, which are critical to low jitter performance.

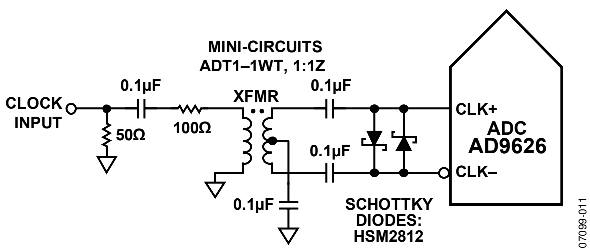


Figure 45. Transformer-Coupled Differential Clock

If a low jitter clock is available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 46. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515 family of clock drivers offers excellent jitter performance.

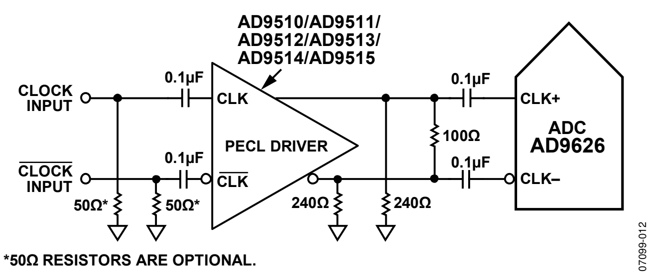


Figure 46. Differential PECL Sample Clock

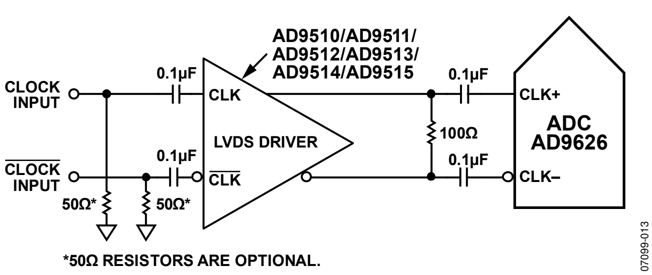


Figure 47. Differential LVDS Sample Clock

In some applications, it is acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, CLK+ should be directly driven from a CMOS gate, and the CLK− pin should be bypassed to ground with a 0.1 µF capacitor in parallel with a 39 kΩ resistor (see Figure 48). Although the CLK+ input circuit supply is AVDD (1.8 V), this input is designed to withstand input voltages up to 3.3 V, making the selection of the drive logic voltage very flexible.

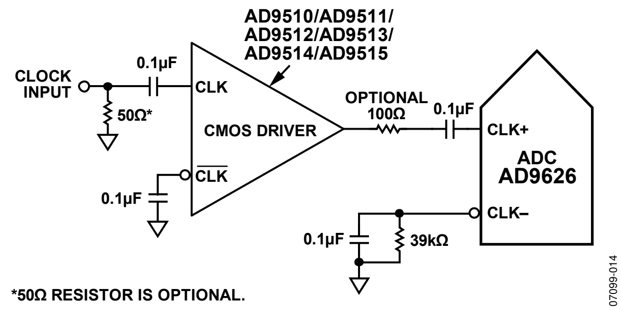


Figure 48. Single-Ended 1.8 V CMOS Sample Clock

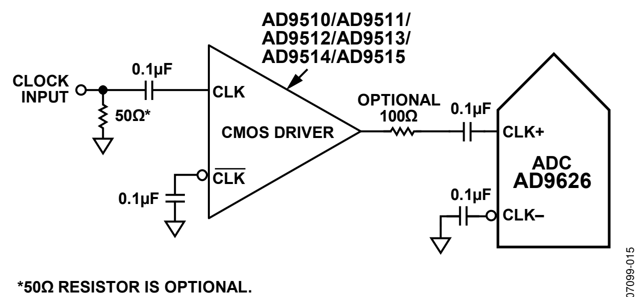


Figure 49. Single-Ended 3.3 V CMOS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to the clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9626 contains a duty cycle stabilizer (DCS) that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9626. When the DCS is on, noise and distortion performance are nearly flat for a wide range of duty cycles. However, some applications may require the DCS function to be off. If so, keep in mind that the dynamic range performance can be affected when operated in this mode. See the AD9626 Configuration Using the SPI section for more details on using this feature.

The duty cycle stabilizer uses a delay-locked loop (DLL) to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately eight clock cycles to allow the DLL to acquire and lock to the new rate.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR for a full-scale input signal at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated by

$$SNR\ Degradation = 20 \times \log_{10}[1/2 \times \pi \times f_A \times t_J]$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 50).

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9626. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

Refer to the AN-501 Application Note and the AN-756 Application Note for more in-depth information about jitter performance as it relates to ADCs (visit www.analog.com).

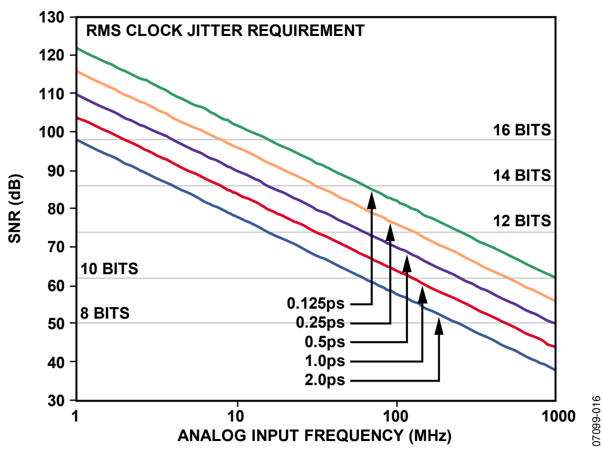


Figure 50. Ideal SNR vs. Input Frequency and Jitter for 0 dBFS input Signal

POWER DISSIPATION AND POWER-DOWN MODE

As shown in Figure 37, the power dissipated by the AD9626 is proportional to its sample rate. The digital power dissipation does not vary much because it is determined primarily by the DRVDD supply and bias current of the LVDS output drivers.

By asserting PDWN (Pin 29) high, the AD9626 is placed in standby mode or full power-down mode, as determined by the contents of Serial Port Register 08. Reasserting the PDWN pin low returns the AD9626 into its normal operational mode.

An additional standby mode is supported by means of varying the clock input. When the clock rate falls below 50 MHz, the AD9626 assumes a standby state. In this case, the biasing network and internal reference remain on, but digital circuitry is powered down. Upon reactivating the clock, the AD9626 resumes normal operation after allowing for the pipeline latency.

DIGITAL OUTPUTS

Digital Outputs and Timing

The off-chip drivers on the AD9626 are CMOS-compatible output levels. The outputs are biased from a separate supply (DRVDD), allowing isolation from the analog supply and easy interface to external logic. The outputs are CMOS devices that swing from ground to DRVDD (with no dc load). It is recommended to minimize the capacitive load the ADC drives by keeping the output traces short (<1 inch, for a total C_{LOAD} < 5 pF). When operating in CMOS mode, it is also recommended to place low value (20 Ω) series damping resistors on the data lines to reduce switching transient effects on performance.

The format of the output data is offset binary by default. An example of the output coding format can be found in Table 11. If it is desired to change the output data format to twos complement, see the AD9626 Configuration Using the SPI section.

An output clock signal is provided to assist in capturing data from the AD9626. The DCO+/DCO– signal is used to clock the output data and is equal to the sampling clock (CLK) rate in single port mode, and one-half the clock rate in interleaved output mode. See the timing diagrams shown in Figure 2 and Figure 3 for more information.

Out-of-Range

An out-of-range condition exists when the analog input voltage is beyond the input range of the ADC. OVRA/OVRB is a digital output that is updated along with the data output corresponding to the particular sampled input voltage. Thus, OVRA/OVRB has the same pipeline latency as the digital data. OVRA/OVRB is low when the analog input voltage is within the analog input range and high when the analog input voltage exceeds the input range, as shown in Figure 51. OVRA/OVRB remains high until the analog input returns to within the input range and another conversion is completed. By logically AND-ing OVRA/OVRB with the MSB and its complement, overrange high or underrange low conditions can be detected.

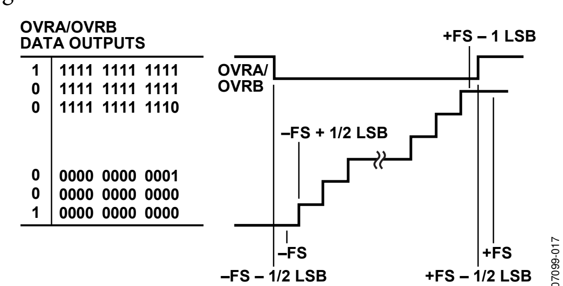


Figure 51. OVRA/OVRB Relation to Input Voltage and Output Data

TIMING—SINGLE PORT MODE

In single port mode, the CMOS output data is available from Data Port A (DA0 to DA11). The outputs for Port B (DB0 to DB11) are unused, and are high impedance in this mode. The Port A outputs and the differential output data clock (DCO+/DCO−) switch nearly simultaneously during the rising edge of DCO+. In this mode, it is recommended to use the rising edge of DCO− to capture the data from Port A. The setup and hold time depends on the input sample clock period, and is approximately $1/f_{CLK} \pm t_{SKEW}$.

TIMING—INTERLEAVED MODE

In interleaved mode, the output data of the AD9626 is demultiplexed onto two data port buses, Port A (DA0 to DA11) and Port B (DB0− to DB11). The output data and differential data capture clock switch at one-half the rate of the sample clock input (CLK+/CLK−), increasing the setup and hold time for the external data capture circuit relative to single port mode (see Figure 3, interleaved mode timing diagram). The two ports switch on alternating sample clock cycles, with the data for Port A being valid during the rising edge of DCO+, and the data for Port B being valid during the rising edge of DCO−. The pipeline latency for both ports is six sample clock cycles. Due to the random nature of the ÷2 circuit that generates the timing for the output stage in interleaved mode, the first data sample during power up can be assigned to either Data Port A or Port B. The user cannot control the polarity of the output data clock relative to the input sample clock. In this mode, it is recommended to use the rising edge of DCO+ to capture the data from Port A, and the rising edge of DCO− to capture the data from Port B. In both cases, the setup and hold time depends on the input sample clock period, and both are approximately $2/f_S \pm t_{SKEW}$.

f_S/2 Spurious

Because the AD9626 output data rate is at one-half the sampling frequency in interleaved output mode, there is significant $f_S/2$ energy in the outputs of the part, and there will be significant energy in the ADC output spectrum at f_S /2. Care must be taken to be certain that this $f_S/2$ energy does not couple into either the clock circuit or the analog inputs of the AD9626. When $f_S/2$ energy is coupled in this fashion, it appears as a spurious tone reflected around $f_S/4$, $3f_S/4$, $5f_S/4$, and so on. For example, in a 125 MSPS sampling application with a 90 MHz single-tone analog input, this energy generates a tone at 97.5 MHz.

$$[(3 \times 125\ \text{MSPS}/4 - 90\ \text{MHz}) + 3 \times 125\ \text{MSPS}/4]$$

Depending on the relationship of the IF frequency to the center of the Nyquist zone, this spurious tone may or may not be in the user's band of interest. Some residual $f_S/2$ energy is present in the AD9601, and the level of this spur is typically below the level of the harmonics at clock rates. Figure 20 shows a plot of the $f_S/2$ spur level vs. the analog input frequency for the AD9626-250. For the specifications provided in Table 2, the $f_S/2$ spur effect is not a factor, as the device is specified in single port output mode.

LAYOUT CONSIDERATIONS

POWER AND GROUND RECOMMENDATIONS

When connecting power to the AD9626, it is recommended that two separate supplies be used: one for analog (AVDD, 1.8 V nominal) and one for digital (DRVDD, 1.8 V nominal). If only a single 1.8 V supply is available, it is routed to AVDD first, then tapped off and isolated with a ferrite bead or filter choke with decoupling capacitors proceeding connection to DRVDD. The user can employ several different decoupling capacitors to cover both high and low frequencies. These should be located close to the point of entry at the PC board level and close to the parts with minimal trace length.

A single PCB ground plane is sufficient when using the AD9626. With proper decoupling and smart partitioning of analog, digital, and clock sections of the PCB, optimum performance is easily achieved.

Exposed Paddle Thermal Heat Slug Recommendations

It is required that the exposed paddle on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance of the AD9626. An exposed, continuous copper plane on the PCB should mate to the AD9626 exposed paddle, Pin 0. The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be solder-filled or plugged.

To maximize the coverage and adhesion between the ADC and PCB, partition the continuous plane by overlaying a silkscreen on the PCB into several uniform sections. This provides several tie points between the two during the reflow process. Using one continuous plane with no partitions guarantees only one tie point between the ADC and PCB. See Figure 52 for a PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, see Application Note AN-772, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package*.

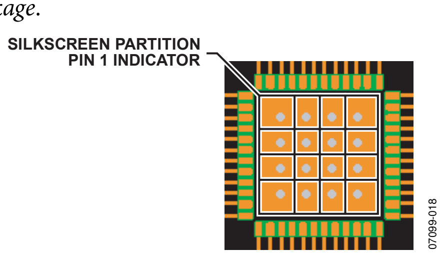


Figure 52. Typical PCB Layout

CML

The CML pin should be decoupled to ground with a 0.1 µF capacitor, as shown in Figure 54.

RBIAS

The AD9626 requires the user to place a 10 kΩ resistor between the RBIAS pin and ground. This resistor sets the master current reference of the ADC core and should have at least a 1% tolerance.

AD9626 CONFIGURATION USING THE SPI

The AD9626 SPI allows the user to configure the converter for specific functions or operations through a structured register space inside the ADC. This gives the user added flexibility to customize device operation depending on the application. Addresses are accessed (programmed or read back) serially in one-byte words. Each byte can be further divided down into fields, which are documented in the Memory Map section.

There are three pins that define the serial port interface or SPI to this particular ADC. They are the SPI SCLK/DFS, SPI SDIO/DCS, and CSB pins. The SCLK/DFS (serial clock) is used to synchronize the read and write data presented the ADC. The SDIO/DCS (serial data input/output) is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB is an active low control that enables or disables the read and write cycles (see Table 8).

Table 8. Serial Port Pins

Mnemonic	Function
SCLK	SCLK (Serial Clock) is the serial shift clock in. SCLK is used to synchronize serial interface reads and writes.
SDIO	SDIO (Serial Data Input/Output) is a dual-purpose pin. The typical role for this pin is an input and output depending on the instruction being sent and the relative position in the timing frame.
CSB	CSB (Chip Select Bar) is an active low control that gates the read and write cycles.
RESET	Master Device Reset. When asserted, device assumes default settings. Active low.

The falling edge of the CSB, in conjunction with the rising edge of the SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 53 and Table 10.

During an instruction phase, a 16-bit instruction is transmitted. Data then follows the instruction phase and is determined by the W0 and W1 bits, which is 1 or more bytes of data. All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether this is a read or write command. This allows the serial data input/output (SDIO) pin to change direction from an input to an output.

Data can be sent in MSB or in LSB first mode. MSB first is default on power-up and can be changed by changing the configuration register. For more information about this feature and others, see *Interfacing to High Speed ADCs via SPI* at www.analog.com.

HARDWARE INTERFACE

The pins described in Table 8 comprise the physical interface between the user's programming device and the serial port of the AD9626. All serial pins are inputs, which is an open-drain output and should be tied to an external pull-up or pull-down resistor (suggested value of 10 kΩ).

This interface is flexible enough to be controlled by either PROMS or PIC mirocontrollers as well. This provides the user with an alternate method to program the ADC other than a SPI controller.

If the user chooses not to use the SPI interface, some pins serve a dual function and are associated with a specific function when strapped externally to AVDD or ground during device power-on. The Configuration Without the SPI section describes the strappable functions supported on the AD9626.

CONFIGURATION WITHOUT THE SPI

In applications that do not interface to the SPI control registers, the SPI SDIO/DCS and SPI SCLK/DFS pins can alternately serve as standalone CMOS-compatible control pins. When the device is powered up, it is assumed that the user intends to use the pins as static control lines for the duty cycle stabilizer. In this mode, the SPI CSB chip select should be connected to ground, which disables the serial port interface.

Table 9. Mode Selection

Mnemonic	External Voltage	Configuration
SPI SDIO/DCS	AVDD	Duty cycle stabilizer enabled
	AGND	Duty cycle stabilizer disabled
SPI SCLK/DFS	AVDD	Twos complement enabled
	AGND	Offset binary enabled

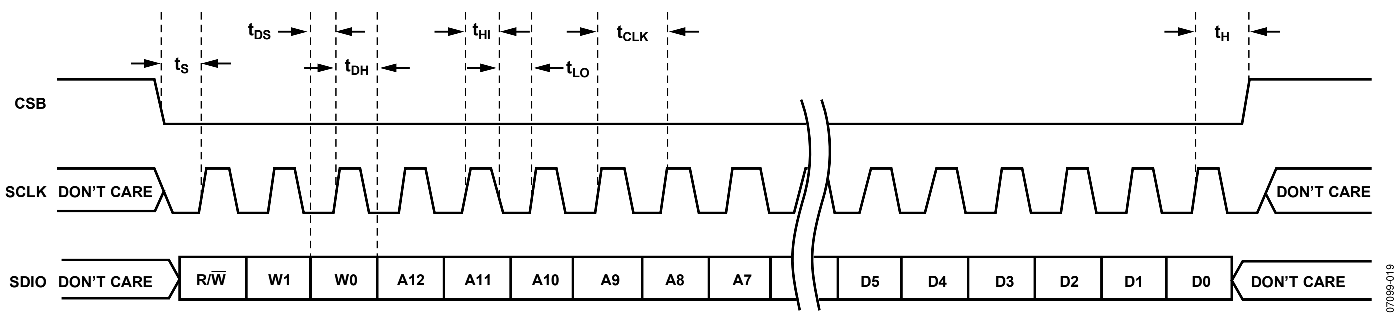


Figure 53. Serial Port Interface Timing Diagram

Table 10. Serial Timing Definitions

Parameter	Timing (minimum, ns)	Description
t_{DS}	5	Setup time between the data and the rising edge of SCLK
t_{DH}	2	Hold time between the data and the rising edge of SCLK
t_{CLK}	40	Period of the clock
t_S	5	Setup time between CSB and SCLK
t_H	2	Hold time between CSB and SCLK
t_{HI}	16	Minimum period that SCLK should be in a logic high state
t_{LO}	16	Minimum period that SCLK should be in a logic low state
t_{EN_SDIO}	1	Minimum time for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 53)
t_{DIS_SDIO}	5	Minimum time for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 53)

Table 11. Output Data Format

Input (V)	Condition (V)	Offset Binary Output Mode D11 to D0	Twos Complement Mode D11 to D0	Gray Code Mode (SPI Accessible) D11 to D0	OR
VIN+ − VIN−	< 0.62	0000 0000 0000	0000 0000 0000	0000 0000 0000	1
VIN+ − VIN−	= 0.62	0000 0000 0000	0000 0000 0000	0000 0000 0000	0
VIN+ − VIN−	= 0	0000 0000 0000	0000 0000 0000	0000 0000 0000	0
VIN+ − VIN−	= 0.62	1111 1111 1111	1111 1111 1111	0000 0000 0000	0
VIN+ − VIN−	> 0.62 + 0.5 LSB	1111 1111 1111	1111 1111 1111	0000 0000 0000	1