Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

12-Bit, 80 MSPS/105 MSPS/125 MSPS/150 MSPS, 1.8 V Dual Analog-to-Digital Converter

AD9627

FEATURES

- SNR = 69.4 dBc (70.4 dBFS) to 70 MHz @ 125 MSPS
- SFDR = 85 dBc to 70 MHz @ 125 MSPS
- Low power: 750 mW @ 125 MSPS
- SNR = 69.2 dBc (70.2 dBFS) to 70 MHz @ 150 MSPS
- SFDR = 84 dBc to 70 MHz @ 150 MSPS
- Low power: 820 mW @ 150 MSPS
- 1.8 V analog supply operation
- 1.8 V to 3.3 V CMOS output supply or 1.8 V LVDS output supply
- Integer 1-to-8 input clock divider
- IF sampling frequencies to 450 MHz
- Internal ADC voltage reference
- Integrated ADC sample-and-hold inputs
- Flexible analog input range: 1 V p-p to 2 V p-p
- Differential analog inputs with 650 MHz bandwidth
- ADC clock duty cycle stabilizer
- 95 dB channel isolation/crosstalk
- Serial port control
- User-configurable, built-in self-test (BIST) capability
- Energy-saving power-down modes
- Integrated receive features
  - Fast detect/threshold bits
  - Composite signal monitor

APPLICATIONS

- Communications
- Diversity radio systems
- Multimode digital receivers (3G)
  - GSM, EDGE, WCDMA, CDMA2000, WiMAX, TD-SCDMA
- I/Q demodulation systems
- Smart antenna systems
- General-purpose software radios
- Broadband data applications

FUNCTIONAL BLOCK DIAGRAM

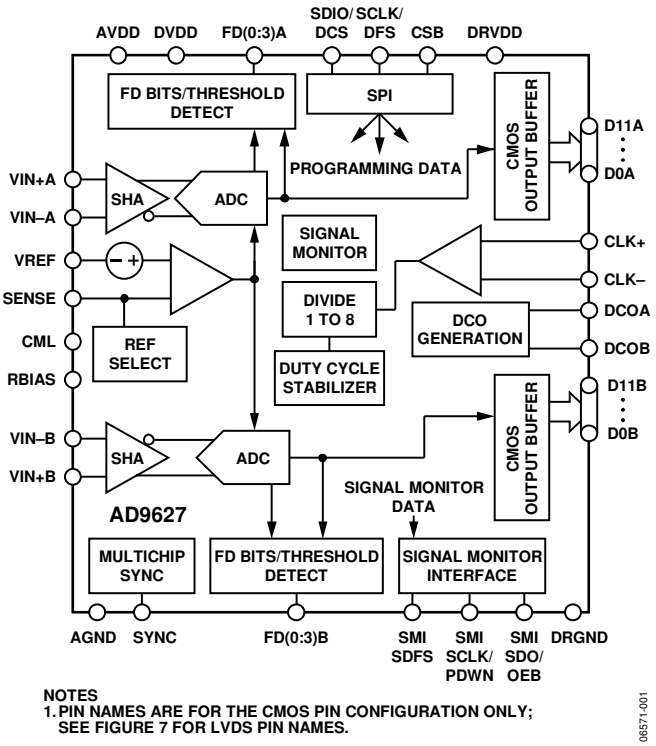

Figure 1.

PRODUCT HIGHLIGHTS

1. Integrated dual, 12-bit, 80 MSPS/105 MSPS/125 MSPS/ 150 MSPS ADC.
2. Fast overrange detect and signal monitor with serial output.
3. Signal monitor block with dedicated serial output mode.
4. Proprietary differential input that maintains excellent SNR performance for input frequencies up to 450 MHz.
5. Operation from a single 1.8 V supply and a separate digital output driver supply to accommodate 1.8 V to 3.3 V logic families.
6. Standard serial port interface (SPI) that supports various product features and functions, such as data formatting (offset binary, twos complement, or gray coding), enabling the clock DCS, power-down, test modes, and voltage reference mode.
7. Pin compatibility with the AD9640, AD9627-11, and AD9600 for a simple migration from 12 bits to 14 bits, 11 bits, or 10 bits.

Rev. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

AD9627* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9627 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-282: Fundamentals of Sampled Data Systems
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-715: A First Approach to IBIS Models: What They Are and How They Are Generated
- AN-737: How ADIsimADC Models an ADC
- AN-742: Frequency Domain Response of Switched-Capacitor ADCs
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-807: Multicarrier WCDMA Feasibility
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-812: MicroController-Based Serial Port Interface (SPI) Boot Circuit
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design
- AN-878: High Speed ADC SPI Control Software
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD9627: 12-Bit, 80 MSPS/105 MSPS/125 MSPS/150 MSPS, 1.8 V Dual Analog-to-Digital Converter Data Sheet

TOOLS AND SIMULATIONS

- Visual Analog
- AD9627 IBIS Models
- AD9627/AD9640 S-Parameters

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9627 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9627 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

5/10—Rev. A to Rev. B

Deleted CP-64-3 Package ..... Universal
Added CP-64-6 Package ..... Universal
Changed AD9627BCPZ-80 to AD9267-80 and
AD9627BCPZ-105 to AD9627-105 Throughout.....5
Changed AD9627BCPZ-125 to AD9267-125 and
AD9627BCPZ-150 to AD9627-150 Throughout.....6
Changes to Figure 6.....16
Changes to Figure 7.....18
Updated Outline Dimensions.....74
Changes to Ordering Guide.....74

6/09—Rev. 0 to Rev. A

Changes to Table 6 11
Changes to Table 7 12
Changes to Figure 3.....14
Changes to Figure 11, Figure 12, and Figure 14.....20
Changes to Table 15 32
Changes to Configuration Using the SPI Section 41
Change to Table 25.....46
Change to Signal Monitor Period (Register 0x113
to Register 0x115) Section.....49
Updated Outline Dimensions.....74

10/07—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9627 is a dual, 12-bit, 80 MSPS/105 MSPS/125 MSPS/ 150 MSPS analog-to-digital converter (ADC). The AD9627 is designed to support communications applications where low cost, small size, and versatility are desired.

The dual ADC core features a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth differential sample-and-hold analog input amplifiers supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

The AD9627 has several functions that simplify the automatic gain control (AGC) function in the system receiver. The fast detect feature allows fast overrange detection by outputting four bits of input level information with very short latency.

In addition, the programmable threshold detector allows monitoring of the incoming signal power, using the four fast detect bits of the ADC with very low latency. If the input signal level exceeds the programmable threshold, the coarse upper threshold indicator goes high. Because this threshold indicator has very low latency, the user can quickly turn down the system gain to avoid an overrange condition.

The second AGC-related function is the signal monitor. This block allows the user to monitor the composite magnitude of the incoming signal, which aids in setting the gain to optimize the dynamic range of the overall system.

The ADC output data can be routed directly to the two external 12-bit output ports. These outputs can be set from 1.8 V to 3.3 V CMOS or 1.8 V LVDS.

Flexible power-down options allow significant power savings, when desired.

Programming for setup and control is accomplished using a 3-bit SPI-compatible serial interface.

The AD9627 is available in a 64-lead LFCSP and is specified over the industrial temperature range of −40°C to +85°C.

SPECIFICATIONS

ADC DC SPECIFICATIONS—AD9627-80/AD9627-105

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 3.3 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, fast detect output pins disabled, and signal monitor disabled, unless otherwise noted.

Table 1.

		AD9627-80			AD9627-105			
Parameter	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	12			12			Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	Full		±0.2	±0.6		±0.3	±0.7	% FSR
Gain Error	Full	+0.1	−1.8	−3.7	−0.5	−2.2	−3.7	% FSR
Differential Nonlinearity (DNL)[1]	Full			±0.4			±0.4	LSB
	25°C		±0.2			±0.2		LSB
Integral Nonlinearity (INL)[1]	Full			±0.9			±0.9	LSB
	25°C		±0.4			±0.4		LSB
MATCHING CHARACTERISTIC								
Offset Error	Full		±0.2	±0.6		±0.3	±0.7	% FSR
Gain Error	Full		±0.2	±0.75		±0.2	±0.75	% FSR
TEMPERATURE DRIFT								
Offset Error	Full		±15			±15		ppm/°C
Gain Error	Full		±95			±95		ppm/°C
INTERNAL VOLTAGE REFERENCE								
Output Voltage Error (1 V Mode)	Full		±5	±16		±5	±16	mV
Load Regulation @ 1.0 mA	Full		7			7		mV
INPUT REFERRED NOISE								
VREF = 1.0 V	25°C		0.3			0.3		LSB rms
ANALOG INPUT								
Input Span, VREF = 1.0 V	Full		2			2		V p-p
Input Capacitance[2]	Full		8			8		pF
VREF INPUT RESISTANCE	Full		6			6		kΩ
POWER SUPPLIES								
Supply Voltage								
AVDD, DVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD (CMOS Mode)	Full	1.7	3.3	3.6	1.7	3.3	3.6	V
DRVDD (LVDS Mode)	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
Supply Current								
I_{AVDD}[1, 3]	Full		233	278		310	365	mA
I_{DVDD}[1, 3]	Full		26			34		mA
I_{DRVDD}[1] (3.3 V CMOS)	Full		23			34		mA
I_{DRVDD}[1] (1.8 V CMOS)	Full		11			15		mA
I_{DRVDD}[1] (1.8 V LVDS)	Full		47			47		mA
POWER CONSUMPTION								
DC Input	Full		452	490		600	650	mW
Sine Wave Input[1] (DRVDD = 1.8 V)	Full		495			657		mW
Sine Wave Input[1] (DRVDD = 3.3 V)	Full		550			740		mW
Standby Power[4]	Full		52			68		mW
Power-Down Power	Full		2.5	6		2.5	6	mW

[1] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND. See Figure 8 for the equivalent analog input structure.
[3] The maximum limit applies to the combination of I_{AVDD} and I_{DVDD} currents.
[4] Standby power is measured with a dc input and with the CLK pins inactive (set to AVDD or AGND).

ADC DC SPECIFICATIONS—AD9627-125/AD9627-150

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 3.3 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, fast detect output pins disabled, and signal monitor disabled, unless otherwise noted.

Table 2.

		AD9627-125			AD9627-150			
Parameter	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	12			12			Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	Full		±0.3	±0.6		±0.2	±0.6	% FSR
Gain Error	Full	−0.7	−2.7	−3.9	−0.9	−3.2	−5.2	% FSR
Differential Nonlinearity (DNL)[1]	Full			±0.4			±0.9	LSB
	25°C		±0.2			±0.2		LSB
Integral Nonlinearity (INL)[1]	Full			±0.9			±1.3	LSB
	25°C		±0.4			±0.5		LSB
MATCHING CHARACTERISTIC								
Offset Error	25°C		±0.3	±0.6		±0.2	±0.7	% FSR
Gain Error	25°C		±0.1	±0.75		±0.2	±0.8	% FSR
TEMPERATURE DRIFT								
Offset Error	Full		±15			±15		ppm/°C
Gain Error	Full		±95			±95		ppm/°C
INTERNAL VOLTAGE REFERENCE								
Output Voltage Error (1 V Mode)	Full		±5	±16		±5	±16	mV
Load Regulation @ 1.0 mA	Full		7			7		mV
INPUT REFERRED NOISE								
VREF = 1.0 V	25°C		0.3			0.3		LSB rms
ANALOG INPUT								
Input Span, VREF = 1.0 V	Full		2			2		V p-p
Input Capacitance[2]	Full		8			8		pF
VREF INPUT RESISTANCE	Full		6			6		kΩ
POWER SUPPLIES								
Supply Voltage								
AVDD, DVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD (CMOS Mode)	Full	1.7	3.3	3.6	1.7	3.3	3.6	V
DRVDD (LVDS Mode)	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
Supply Current								
I_{AVDD}[1, 3]	Full		385	455		419	495	mA
I_{DVDD}[1, 3]	Full		42			50		mA
I_{DRVDD}[1] (3.3 V CMOS)	Full		36			42		mA
I_{DRVDD}[1] (1.8 V CMOS)	Full		18			22		mA
I_{DRVDD}[1] (1.8 V LVDS)	Full		48			49		mA
POWER CONSUMPTION								
DC Input	Full		750	800		820	890	mW
Sine Wave Input[1] (DRVDD = 1.8 V)	Full		814			895		mW
Sine Wave Input[1] (DRVDD = 3.3 V)	Full		900			995		mW
Standby Power[4]	Full		77			77		mW
Power-Down Power	Full		2.5	6		2.5	6	mW

[1] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND. See Figure 8 for the equivalent analog input structure.
[3] The maximum limit applies to the combination of I_{AVDD} and I_{DVDD} currents.
[4] Standby power is measured with a dc input and with the CLK pins inactive (set to AVDD or AGND).

ADC AC SPECIFICATIONS—AD9627-80/AD9627-105

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 3.3 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, fast detect output pins disabled, and signal monitor disabled, unless otherwise noted.

Table 3.

		AD9627-80			AD9627-105			
Parameter[1]	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE RATIO (SNR)								
f_{IN} = 2.3 MHz	25°C		69.7			69.6		dB
f_{IN} = 70 MHz	25°C		69.5			69.4		dB
	Full	68.1			68.6			dB
f_{IN} = 140 MHz	25°C		69.2			69.1		dB
f_{IN} = 220 MHz	25°C		68.5			68.4		dB
SIGNAL-TO-NOISE AND DISTORTION (SINAD)								
f_{IN} = 2.3 MHz	25°C		69.6			69.5		dB
f_{IN} = 70 MHz	25°C		69.4			69.3		dB
	Full	67.4			68.0			dB
f_{IN} = 140 MHz	25°C		69.0			69.0		dB
f_{IN} = 220 MHz	25°C		68.3			68.1		dB
EFFECTIVE NUMBER OF BITS (ENOB)								
f_{IN} = 2.3 MHz	25°C		11.5			11.4		Bits
f_{IN} = 70 MHz	25°C		11.4			11.4		Bits
f_{IN} = 140 MHz	25°C		11.4			11.4		Bits
f_{IN} = 220 MHz	25°C		11.3			11.2		Bits
WORST SECOND OR THIRD HARMONIC								
f_{IN} = 2.3 MHz	25°C		−87			−87		dBc
f_{IN} = 70 MHz	25°C		−85			−85		dBc
	Full			−74			−74	dBc
f_{IN} = 140 MHz	25°C		−84			−84		dBc
f_{IN} = 220 MHz	25°C		−83			−83		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
f_{IN} = 2.3 MHz	25°C		87			87		dBc
f_{IN} = 70 MHz	25°C		85			85		dBc
	Full	74			74			dBc
f_{IN} = 140 MHz	25°C		84			84		dBc
f_{IN} = 220 MHz	25°C		83			83		dBc
WORST OTHER HARMONIC OR SPUR								
f_{IN} = 2.3 MHz	25°C		−92			−92		dBc
f_{IN} = 70 MHz	25°C		−89			−88		dBc
	Full			−82			−82	dBc
f_{IN} = 140 MHz	25°C		−89			−87		dBc
f_{IN} = 220 MHz	25°C		−89			−86		dBc
TWO-TONE SFDR								
f_{IN} = 29.1 MHz, 32.1 MHz (−7 dBFS)	25°C		85			85		dBc
f_{IN} = 169.1 MHz, 172.1 MHz (−7 dBFS)	25°C		82			82		dBc
CROSSTALK[2]	Full		−95			−95		dB
ANALOG INPUT BANDWIDTH	25°C		650			650		MHz

[1] See Application Note AN-835, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Crosstalk is measured at 100 MHz with −1 dBFS on one channel and with no input on the alternate channel.

ADC AC SPECIFICATIONS—AD9627-125/AD9627-150

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 3.3 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, fast detect output pins disabled, and signal monitor disabled, unless otherwise noted.

Table 4.

		AD9627-125			AD9627-150			
Parameter[1]	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE RATIO (SNR)								
f_{IN} = 2.3 MHz	25°C		69.5			69.4		dB
f_{IN} = 70 MHz	25°C		69.4			69.2		dB
	Full	68.1			67.1			dB
f_{IN} = 140 MHz	25°C		69.1			68.8		dB
f_{IN} = 220 MHz	25°C		68.8			68.2		dB
SIGNAL-TO-NOISE AND DISTORTION (SINAD)								
f_{IN} = 2.3 MHz	25°C		69.4			69.3		dB
f_{IN} = 70 MHz	25°C		69.3			69.1		dB
	Full	67.9			65.9			dB
f_{IN} = 140 MHz	25°C		69.0			68.7		dB
f_{IN} = 220 MHz	25°C		68.3			67.8		dB
EFFECTIVE NUMBER OF BITS (ENOB)								
f_{IN} = 2.3 MHz	25°C		11.4			11.4		Bits
f_{IN} = 70 MHz	25°C		11.4			11.4		Bits
f_{IN} = 140 MHz	25°C		11.3			11.3		Bits
f_{IN} = 220 MHz	25°C		11.3			11.2		Bits
WORST SECOND OR THIRD HARMONIC								
f_{IN} = 2.3 MHz	25°C		−86.5			−86.5		dBc
f_{IN} = 70 MHz	25°C		−85			−84		dBc
	Full			−74			−73	dBc
f_{IN} = 140 MHz	25°C		−84			−83.5		dBc
f_{IN} = 220 MHz	25°C		−83			−77		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
f_{IN} = 2.3 MHz	25°C		86.5			86.5		dBc
f_{IN} = 70 MHz	25°C		85			84		dBc
	Full	74			73			dBc
f_{IN} = 140 MHz	25°C		84			83.5		dBc
f_{IN} = 220 MHz	25°C		83			77		dBc
WORST OTHER HARMONIC OR SPUR								
f_{IN} = 2.3 MHz	25°C		−92			−92		dBc
f_{IN} = 70 MHz	25°C		−89			−88		dBc
	Full			−81			−80	dBc
f_{IN} = 140 MHz	25°C		−89			−88		dBc
f_{IN} = 220 MHz	25°C		−89			−88		dBc
TWO-TONE SFDR								
f_{IN} = 29.1 MHz, 32.1 MHz (−7 dBFS)	25°C		85			85		dBc
f_{IN} = 169.1 MHz, 172.1 MHz (−7 dBFS)	25°C		82			82		dBc
CROSSTALK[2]	Full		−95			−95		dB
ANALOG INPUT BANDWIDTH	25°C		650			650		MHz

[1] See Application Note AN-835, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Crosstalk is measured at 100 MHz with −1 dBFS on one channel and with no input on the alternate channel.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 3.3 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, and DCS enabled, unless otherwise noted.

Table 5.

Parameter	Temperature	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK–)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		1.2		V
Differential Input Voltage	Full	0.2		6	V p-p
Input Voltage Range	Full	GND − 0.3		AVDD + 1.6	V
Input Common-Mode Range	Full	1.1		AVDD	V
High Level Input Voltage	Full	1.2		3.6	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	−10		+10	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
SYNC INPUT					
Logic Compliance			CMOS		
Internal Bias	Full		1.2		V
Input Voltage Range	Full	GND − 0.3		AVDD + 1.6	V
High Level Input Voltage	Full	1.2		3.6	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	−10		+10	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
LOGIC INPUT (CSB)[1]					
High Level Input Voltage	Full	1.22		3.6	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	40		132	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SCLK/DFS)[2]					
High Level Input Voltage	Full	1.22		3.6	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current (VIN = 3.3 V)	Full	−92		−135	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUTS/OUTPUTS (SDIO/DCS, SMI SDFS)[1]					
High Level Input Voltage	Full	1.22		3.6	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	38		128	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
LOGIC INPUTS/OUTPUTS (SMI SDO/OEB, SMI SCLK/PDWN)[2]					
High Level Input Voltage	Full	1.22		3.6	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current (VIN = 3.3 V)	Full	−90		−134	µA
Low Level Input Current	Full	−10		+10	µA

Parameter	Temperature	Min	Typ	Max	Unit
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS					
CMOS Mode—DRVDD = 3.3 V					
High Level Output Voltage					
I_{OH} = 50 µA	Full	3.29			V
I_{OH} = 0.5 mA	Full	3.25			V
Low Level Output Voltage					
I_{OL} = 1.6 mA	Full			0.2	V
I_{OL} = 50 µA	Full			0.05	V
CMOS Mode—DRVDD = 1.8 V					
High Level Output Voltage					
I_{OH} = 50 µA	Full	1.79			V
I_{OH} = 0.5 mA	Full	1.75			V
Low Level Output Voltage					
I_{OL} = 1.6 mA	Full			0.2	V
I_{OL} = 50 µA	Full			0.05	V
LVDS Mode—DRVDD = 1.8 V					
Differential Output Voltage (V_{OD}), ANSI Mode	Full	250	350	450	mV
Output Offset Voltage (V_{OS}), ANSI Mode	Full	1.15	1.25	1.35	V
Differential Output Voltage (V_{OD}), Reduced Swing Mode	Full	150	200	280	mV
Output Offset Voltage (V_{OS}), Reduced Swing Mode	Full	1.15	1.25	1.35	V

[1] Pull up.
[2] Pull down.

SWITCHING SPECIFICATIONS—AD9627-80/AD9627-105

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 3.3 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, and DCS enabled, unless otherwise noted.

Table 6.

		AD9627-80			AD9627-105			
Parameter	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUT PARAMETERS								
Input Clock Rate	Full			625			625	MHz
Conversion Rate								
DCS Enabled[1]	Full	20		80	20		105	MSPS
DCS Disabled[1]	Full	10		80	10		105	MSPS
CLK Period—Divide-by-1 Mode (t_{CLK})	Full	12.5			9.5			ns
CLK Pulse Width High								
Divide-by-1 Mode, DCS Enabled	Full	3.75	6.25	8.75	2.85	4.75	6.65	ns
Divide by-1-Mode, DCS Disabled	Full	5.63	6.25	6.88	4.28	4.75	5.23	ns
Divide-by-2 Mode, DCS Enabled	Full	1.6			1.6			ns
Divide-by-3 Through Divide-by-8 Modes, DCS Enabled	Full	0.8			0.8			ns
DATA OUTPUT PARAMETERS (DATA, FD)								
CMOS Mode—DRVDD = 3.3 V								
Data Propagation Delay (t_{PD})[2]	Full	2.2	4.5	6.4	2.2	4.5	6.4	ns
DCO Propagation Delay (t_{DCO})	Full	3.8	5.0	6.8	3.8	5.0	6.8	ns
Setup Time (t_S)	Full		6.25			5.25		ns
Hold Time (t_H)	Full		5.75			4.25		ns
CMOS Mode—DRVDD = 1.8 V								
Data Propagation Delay (t_{PD})[2]	Full	2.4	5.2	6.9	2.4	5.2	6.9	ns
DCO Propagation Delay (t_{DCO})	Full	4.0	5.6	7.3	4.0	5.6	7.3	ns
Setup Time (t_S)	Full		6.65			5.15		ns
Hold Time (t_H)	Full		5.85			4.35		ns
LVDS Mode—DRVDD = 1.8 V								
Data Propagation Delay (t_{PD})[2]	Full	2.0	4.8	6.3	2.0	4.8	6.3	ns
DCO Propagation Delay (t_{DCO})	Full	5.2	7.3	9.0	5.2	7.3	9.0	ns
CMOS Mode Pipeline Delay (Latency)	Full		12			12		Cycles
LVDS Mode Pipeline Delay (Latency) Channel A/Channel B	Full		12/12.5			12/12.5		Cycles
Aperture Delay (t_A)	Full		1.0			1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.1			0.1		ps rms
Wake-Up Time[3]	Full		350			350		µs
OUT-OF-RANGE RECOVERY TIME	Full		2			2		Cycles

[1] Conversion rate is the clock rate after the divider.
[2] Output propagation delay is measured from CLK 50% transition to DATA 50% transition, with 5 pF load.
[3] Wake-up time is dependent on the value of the decoupling capacitors.

SWITCHING SPECIFICATIONS—AD9627-125/AD9627-150

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 3.3 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, and DCS enabled, unless otherwise noted.

Table 7.

		AD9627-125			AD9627-150			
Parameter	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUT PARAMETERS								
Input Clock Rate	Full			625			625	MHz
Conversion Rate								
DCS Enabled[1]	Full	20		125	20		150	MSPS
DCS Disabled[1]	Full	10		125	10		150	MSPS
CLK Period—Divide-by-1 Mode (t_{CLK})	Full	8			6.66			ns
CLK Pulse Width High								
Divide-by-1 Mode, DCS Enabled	Full	2.4	4	5.6	2.0	3.33	4.66	ns
Divide-by-1 Mode, DCS Disabled	Full	3.6	4	4.4	3.0	3.33	3.66	ns
Divide-by-2 Mode, DCS Enabled	Full	1.6			1.6			ns
Divide-by-3-Through-8 Mode, DCS Enabled	Full	0.8			0.8			ns
DATA OUTPUT PARAMETERS (DATA, FD)								
CMOS Mode—DRVDD = 3.3 V								
Data Propagation Delay (t_{PD})[2]	Full	2.2	4.5	6.4	2.2	4.5	6.4	ns
DCO Propagation Delay (t_{DCO})	Full	3.8	5.0	6.8	3.8	5.0	6.8	ns
Setup Time (t_S)	Full		4.5			3.83		ns
Hold Time (t_H)	Full		3.5			2.83		ns
CMOS Mode—DRVDD = 1.8 V								
Data Propagation Delay (t_{PD})[2]	Full	2.4	5.2	6.9	2.4	5.2	6.9	ns
DCO Propagation Delay (t_{DCO})	Full	4.0	5.6	7.3	4.0	5.6	7.3	ns
Setup Time (t_S)	Full		4.4			3.73		ns
Hold Time (t_H)	Full		3.6			2.93		ns
LVDS Mode—DRVDD = 1.8 V								
Data Propagation Delay (t_{PD})[2]	Full	2.0	4.8	6.3	2.0	4.8	6.3	ns
DCO Propagation Delay (t_{DCO})	Full	5.2	7.3	9.0	5.2	7.3	9.0	ns
CMOS Mode Pipeline Delay (Latency)	Full		12			12		Cycles
LVDS Mode Pipeline Delay (Latency) Channel A/Channel B	Full		12/12.5			12/12.5		Cycles
Aperture Delay (t_A)	Full		1.0			1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.1			0.1		ps rms
Wake-Up Time[3]	Full		350			350		µs
OUT-OF-RANGE RECOVERY TIME	Full		3			3		Cycles

[1] Conversion rate is the clock rate after the divider.
[2] Output propagation delay is measured from CLK 50% transition to DATA 50% transition, with 5 pF load.
[3] Wake-up time is dependent on the value of the decoupling capacitors.

TIMING SPECIFICATIONS

Table 8.

Parameter	Conditions	Min	Typ	Max	Unit
SYNC TIMING REQUIREMENTS					
t_{SSYNC}	SYNC to rising edge of CLK setup time		0.24		ns
t_{HSYNC}	SYNC to rising edge of CLK hold time		0.40		ns
SPI TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	SCLK pulse width high	10			ns
t_{LOW}	SCLK pulse width low	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10			ns
SPORT TIMING REQUIREMENTS					
t_{CSSCLK}	Delay from rising edge of CLK+ to rising edge of SMI SCLK	3.2	4.5	6.2	ns
$t_{SSCLKSDO}$	Delay from rising edge of SMI SCLK to SMI SDO	−0.4	0	0.4	ns
$t_{SSCLKSDFS}$	Delay from rising edge of SMI SCLK to SMI SDFS	−0.4	0	0.4	ns

Timing Diagrams

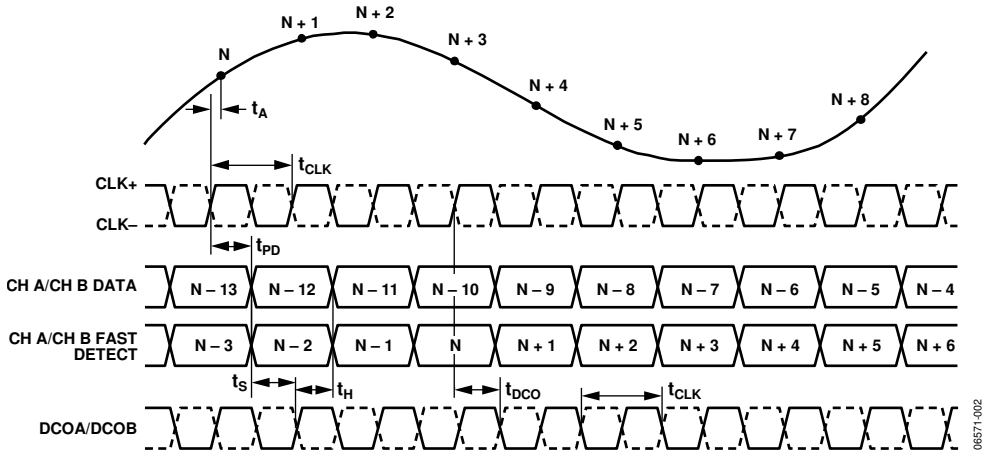

Figure 2. CMOS Output Mode Data and Fast Detect Output Timing (Fast Detect Mode Select Bits = 000)

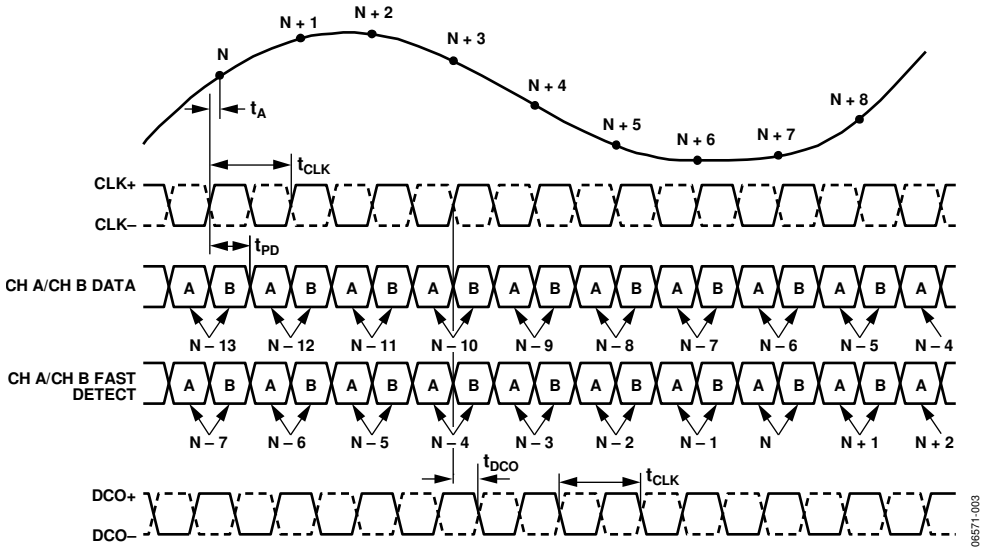

Figure 3. LVDS Mode Data and Fast Detect Output Timing (Fast Detect Mode Select Bits = 001 Through Fast Detect Mode Select Bits = 100)

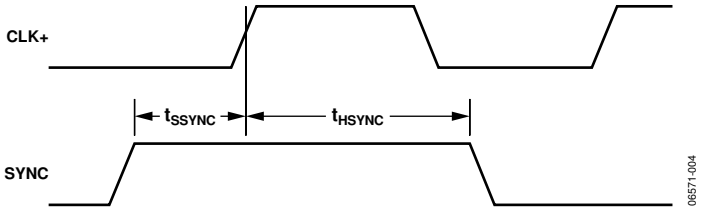

Figure 4. SYNC Input Timing Requirements

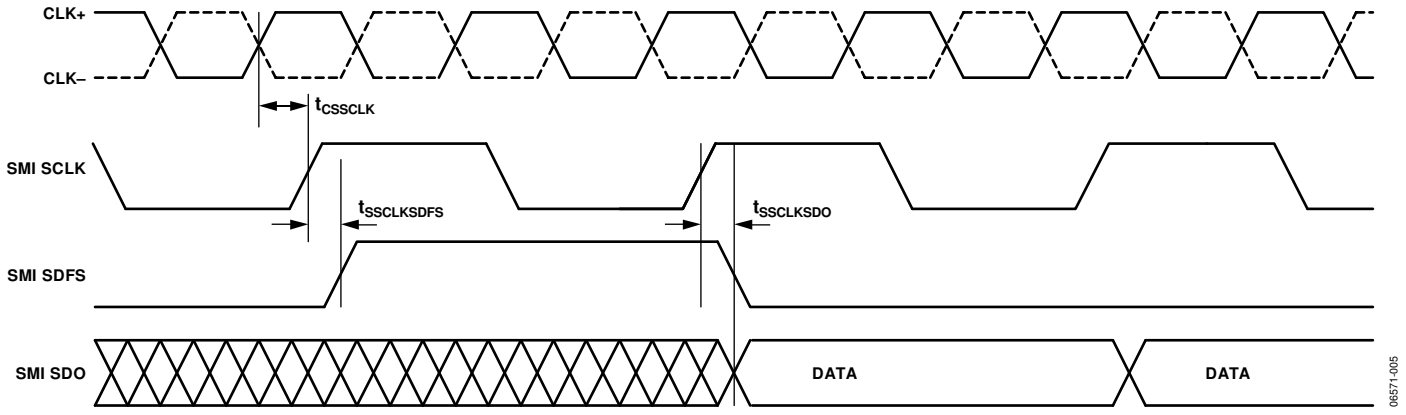

Figure 5. Signal Monitor SPORT Output Timing (Divide-by-2 Mode)

ABSOLUTE MAXIMUM RATINGS

Table 9.

Parameter	Rating
ELECTRICAL	
AVDD, DVDD to AGND	−0.3 V to +2.0 V
DRVDD to DRGND	−0.3 V to +3.9 V
AGND to DRGND	−0.3 V to +0.3 V
AVDD to DRVDD	−3.9 V to +2.0 V
VIN+A/VIN+B, VIN−A/VIN−B to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to +3.9 V
SYNC to AGND	−0.3 V to +3.9 V
VREF to AGND	−0.3 V to AVDD + 0.2 V
SENSE to AGND	−0.3 V to AVDD + 0.2 V
CML to AGND	−0.3 V to AVDD + 0.2 V
RBIAS to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to +3.9 V
SCLK/DFS to DRGND	−0.3 V to +3.9 V
SDIO/DCS to DRGND	−0.3 V to DRVDD + 0.3 V
SMI SDO/OEB	−0.3 V to DRVDD + 0.3 V
SMI SCLK/PDWN	−0.3 V to DRVDD + 0.3 V
SMI SDFS	−0.3 V to DRVDD + 0.3 V
D0A/D0B through D11A/D11B to DRGND	−0.3 V to DRVDD + 0.3 V
FD0A/FD0B through FD3A/FD3B to DRGND	−0.3 V to DRVDD + 0.3 V
DCOA/DCOB to DRGND	−0.3 V to DRVDD + 0.3 V
ENVIRONMENTAL	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the customer board increases the reliability of the solder joints and maximizes the thermal capability of the package.

Table 10. Thermal Resistance

Package Type	Airflow Velocity (m/s)	θ_{JA}[1,2]	θ_{JC}[1,3]	θ_{JB}[1,4]	Unit
64-Lead LFCSP 9 mm × 9 mm (CP-64-6)	0	18.8	0.6	6.0	°C/W
	1.0	16.5			°C/W
	2.0	15.8			°C/W

[1] Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. As shown, airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes, reduces the θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

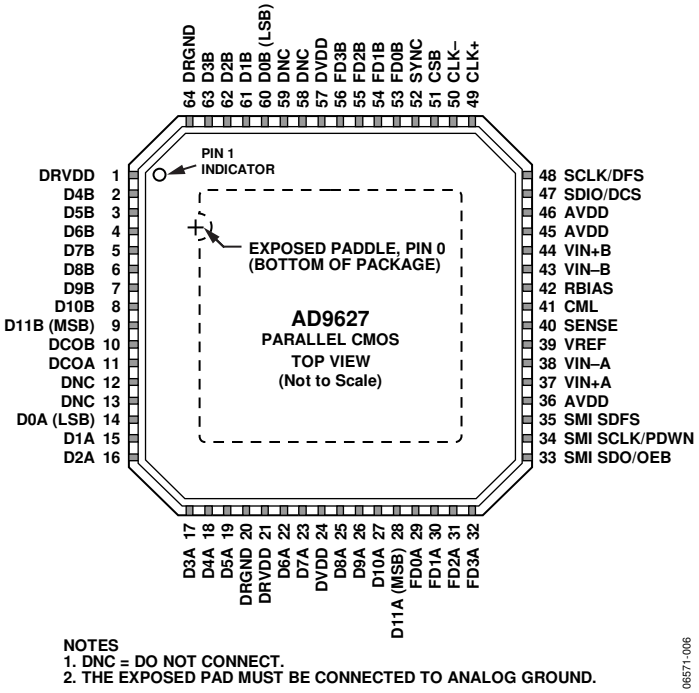

Figure 6. LFCSP Parallel CMOS Pin Configuration (Top View)

Table 11. Pin Function Descriptions (Parallel CMOS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
20, 64	DRGND	Ground	Digital Output Ground.
1, 21	DRVDD	Supply	Digital Output Driver Supply (1.8 V to 3.3 V).
24, 57	DVDD	Supply	Digital Power Supply (1.8 V Nominal).
36, 45, 46	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
0	AGND	Ground	Analog Ground. Pin 0 is the exposed thermal pad on the bottom of the package.
12, 13, 58, 59	DNC		Do Not Connect.
ADC Analog			
37	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
38	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
44	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
43	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
39	VREF	Input/Output	Voltage Reference Input/Output.
40	SENSE	Input	Voltage Reference Mode Select. See Table 14 for details.
42	RBIAS	Input/Output	External Reference Bias Resistor.
41	CML	Output	Common-Mode Level Bias Output for Analog Inputs.
49	CLK+	Input	ADC Clock Input—True.
50	CLK−	Input	ADC Clock Input—Complement.
ADC Fast Detect Outputs			
29	FD0A	Output	Channel A Fast Detect Indicator. See Table 17 for details.
30	FD1A	Output	Channel A Fast Detect Indicator. See Table 17 for details.
31	FD2A	Output	Channel A Fast Detect Indicator. See Table 17 for details.
32	FD3A	Output	Channel A Fast Detect Indicator. See Table 17 for details.
53	FD0B	Output	Channel B Fast Detect Indicator. See Table 17 for details.
54	FD1B	Output	Channel B Fast Detect Indicator. See Table 17 for details.
55	FD2B	Output	Channel B Fast Detect Indicator. See Table 17 for details.
56	FD3B	Output	Channel B Fast Detect Indicator. See Table 17 for details.

Pin No.	Mnemonic	Type	Description
Digital Input			
52	SYNC	Input	Digital Synchronization Pin. Slave mode only.
Digital Outputs			
14	D0A (LSB)	Output	Channel A CMOS Output Data.
15	D1A	Output	Channel A CMOS Output Data.
16	D2A	Output	Channel A CMOS Output Data.
17	D3A	Output	Channel A CMOS Output Data.
18	D4A	Output	Channel A CMOS Output Data.
19	D5A	Output	Channel A CMOS Output Data.
22	D6A	Output	Channel A CMOS Output Data.
23	D7A	Output	Channel A CMOS Output Data.
25	D8A	Output	Channel A CMOS Output Data.
26	D9A	Output	Channel A CMOS Output Data.
27	D10A	Output	Channel A CMOS Output Data.
28	D11A (MSB)	Output	Channel A CMOS Output Data.
60	D0B (LSB)	Output	Channel B CMOS Output Data.
61	D1B	Output	Channel B CMOS Output Data.
62	D2B	Output	Channel B CMOS Output Data.
63	D3B	Output	Channel B CMOS Output Data.
2	D4B	Output	Channel B CMOS Output Data.
3	D5B	Output	Channel B CMOS Output Data.
4	D6B	Output	Channel B CMOS Output Data.
5	D7B	Output	Channel B CMOS Output Data.
6	D8B	Output	Channel B CMOS Output Data.
7	D9B	Output	Channel B CMOS Output Data.
8	D10B	Output	Channel B CMOS Output Data.
9	D11B (MSB)	Output	Channel B CMOS Output Data.
11	DCOA	Output	Channel A Data Clock Output.
10	DCOB	Output	Channel B Data Clock Output.
SPI Control			
48	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
47	SDIO/DCS	Input/Output	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.
51	CSB	Input	SPI Chip Select (Active Low).
Signal Monitor Port			
33	SMI SDO/OEB	Input/Output	Signal Monitor Serial Data Output/Output Enable Input (Active Low) in External Pin Mode.
35	SMI SDFS	Output	Signal Monitor Serial Data Frame Sync.
34	SMI SCLK/PDWN	Input/Output	Signal Monitor Serial Clock Output/Power-Down Input in External Pin Mode.

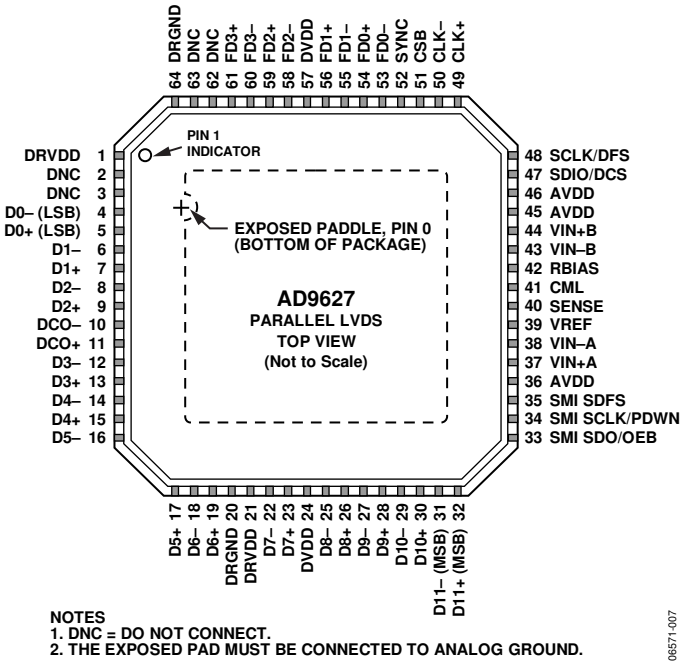

Figure 7. LFCSP Interleaved Parallel LVDS Pin Configuration (Top View)

Table 12. Pin Function Descriptions (Interleaved Parallel LVDS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
20, 64	DRGND	Ground	Digital Output Ground.
1, 21	DRVDD	Supply	Digital Output Driver Supply (1.8 V to 3.3 V).
24, 57	DVDD	Supply	Digital Power Supply (1.8 V Nominal).
36, 45, 46	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
0	AGND	Ground	Analog Ground. Pin 0 is the exposed thermal pad on the bottom of the package.
2, 3, 62, 63	DNC		Do Not Connect.
ADC Analog			
37	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
38	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
44	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
43	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
39	VREF	Input/Output	Voltage Reference Input/Output.
40	SENSE	Input	Voltage Reference Mode Select. See Table 14 for details.
42	RBIAS	Input/Output	External Reference Bias Resistor.
41	CML	Output	Common-Mode Level Bias Output for Analog Inputs.
49	CLK+	Input	ADC Clock Input—True.
50	CLK−	Input	ADC Clock Input—Complement.
ADC Fast Detect Outputs			
54	FD0+	Output	Channel A/Channel B LVDS Fast Detect Indicator 0—True. See Table 17 for details.
53	FD0−	Output	Channel A/Channel B LVDS Fast Detect Indicator 0—Complement. See Table 17 for details.
56	FD1+	Output	Channel A/Channel B LVDS Fast Detect Indicator 1—True. See Table 17 for details.
55	FD1−	Output	Channel A/Channel B LVDS Fast Detect Indicator 1—Complement. See Table 17 for details.
59	FD2+	Output	Channel A/Channel B LVDS Fast Detect Indicator 2—True. See Table 17 for details.
58	FD2−	Output	Channel A/Channel B LVDS Fast Detect Indicator 2—Complement. See Table 17 for details.
61	FD3+	Output	Channel A/Channel B LVDS Fast Detect Indicator 3—True. See Table 17 for details.
60	FD3−	Output	Channel A/Channel B LVDS Fast Detect Indicator 3—Complement. See Table 17 for details.
Digital Input			
52	SYNC	Input	Digital Synchronization Pin. Slave mode only.

Pin No.	Mnemonic	Type	Description
Digital Outputs			
5	D0+ (LSB)	Output	Channel A/Channel B LVDS Output Data 0—True.
4	D0− (LSB)	Output	Channel A/Channel B LVDS Output Data 0—Complement.
7	D1+	Output	Channel A/Channel B LVDS Output Data 1—True.
6	D1−	Output	Channel A/Channel B LVDS Output Data 1—Complement.
9	D2+	Output	Channel A/Channel B LVDS Output Data 2—True.
8	D2−	Output	Channel A/Channel B LVDS Output Data 2—Complement.
13	D3+	Output	Channel A/Channel B LVDS Output Data 3—True.
12	D3−	Output	Channel A/Channel B LVDS Output Data 3—Complement.
15	D4+	Output	Channel A/Channel B LVDS Output Data 4 —True.
14	D4−	Output	Channel A/Channel B LVDS Output Data 4—Complement.
17	D5+	Output	Channel A/Channel B LVDS Output Data 5—True.
16	D5−	Output	Channel A/Channel B LVDS Output Data 5—Complement.
19	D6+	Output	Channel A/Channel B LVDS Output Data 6—True.
18	D6−	Output	Channel A/Channel B LVDS Output Data 6—Complement.
23	D7+	Output	Channel A/Channel B LVDS Output Data 7—True.
22	D7−	Output	Channel A/Channel B LVDS Output Data 7—Complement.
26	D8+	Output	Channel A/Channel B LVDS Output Data 8—True.
25	D8−	Output	Channel A/Channel B LVDS Output Data 8—Complement.
28	D9+	Output	Channel A/Channel B LVDS Output Data 9—True.
27	D9−	Output	Channel A/Channel B LVDS Output Data 9—Complement.
30	D10+	Output	Channel A/Channel B LVDS Output Data 10—True.
29	D10−	Output	Channel A/Channel B LVDS Output Data 10—Complement.
32	D11+ (MSB)	Output	Channel A/Channel B LVDS Output Data 11—True.
31	D11− (MSB)	Output	Channel A/Channel B LVDS Output Data 11—Complement.
11	DCO+	Output	Channel A/Channel B LVDS Data Clock Output—True.
10	DCO−	Output	Channel A/Channel B LVDS Data Clock Output—Complement.
SPI Control			
48	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
47	SDIO/DCS	Input/Output	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.
51	CSB	Input	SPI Chip Select (Active Low).
Signal Monitor Port			
33	SMI SDO/OEB	Input/Output	Signal Monitor Serial Data Output/Output Enable Input (Active Low) in External Pin Mode.
35	SMI SDFS	Output	Signal Monitor Serial Data Frame Sync.
34	SMI SCLK/PDWN	Input/Output	Signal Monitor Serial Clock Output/Power-Down Input in External Pin Mode.

EQUIVALENT CIRCUITS

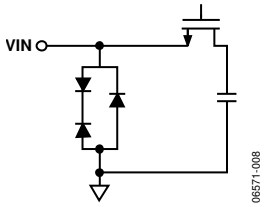

Figure 8. Equivalent Analog Input Circuit

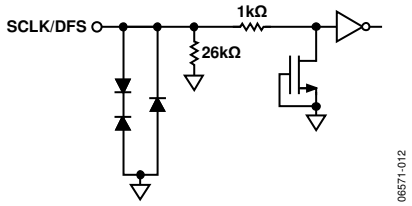

Figure 12. Equivalent SCLK/DFS Input Circuit

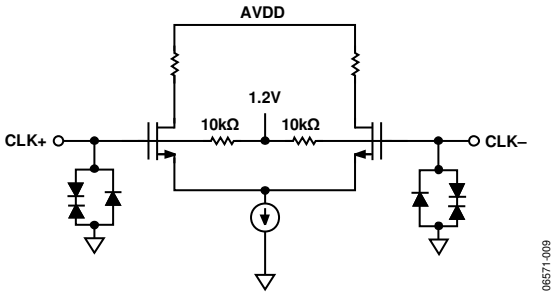

Figure 9. Equivalent Clock Input Circuit

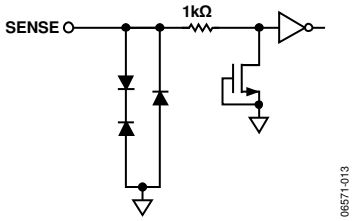

Figure 13. Equivalent SENSE Circuit

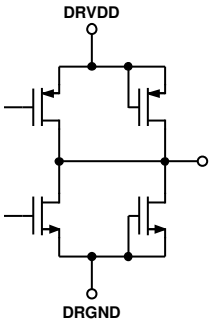

Figure 10. Digital Output

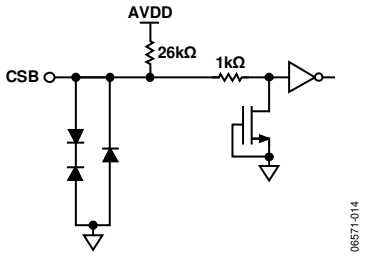

Figure 14. Equivalent CSB Input Circuit

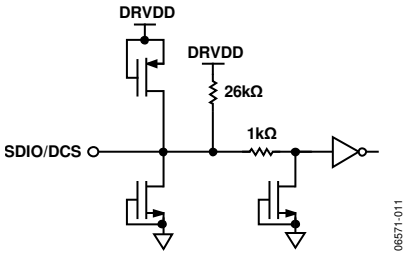

Figure 11. Equivalent SDIO/DCS or SMI SDFS Circuit

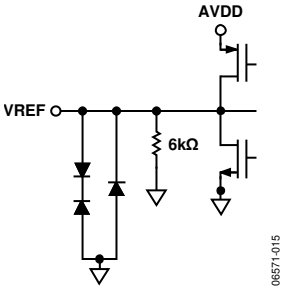

Figure 15. Equivalent VREF Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 3.3 V, sample rate = 150 MSPS, DCS enabled, 1.0 V internal reference, 2 V p-p differential input, VIN = −1.0 dBFS, and 64k sample, T_A = 25°C, unless otherwise noted.

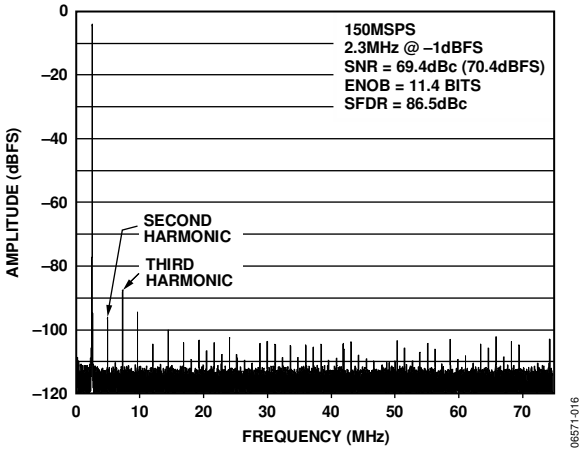

Figure 16. AD9627-150 Single-Tone FFT with f_{IN} = 2.3 MHz

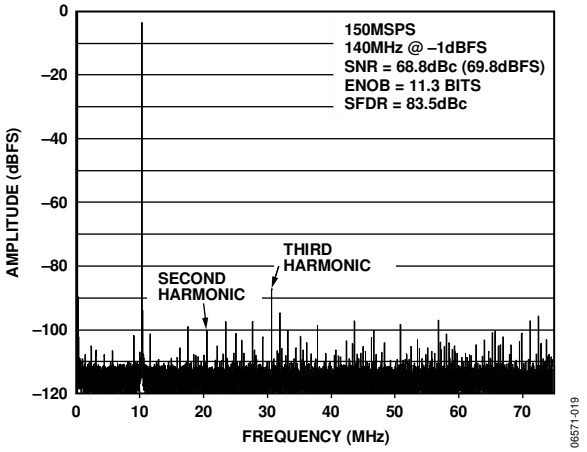

Figure 19. AD9627-150 Single-Tone FFT with f_{IN} = 140 MHz

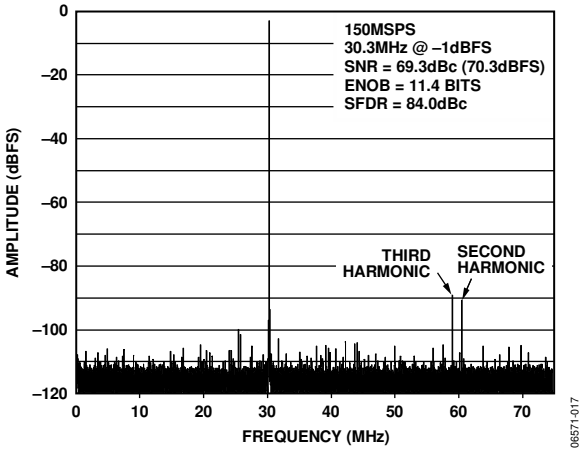

Figure 17. AD9627-150 Single-Tone FFT with f_{IN} = 30.3 MHz

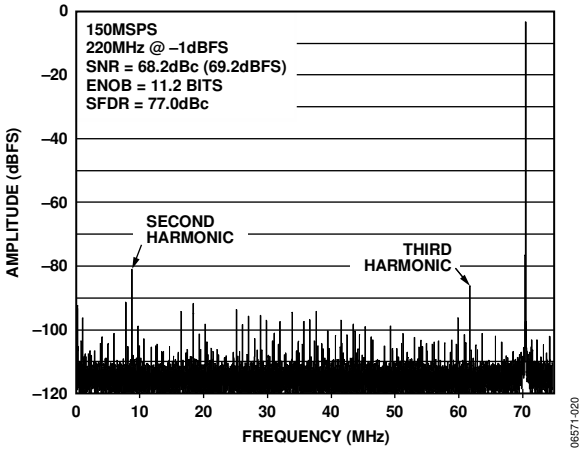

Figure 20. AD9627-150 Single-Tone FFT with f_{IN} = 220 MHz

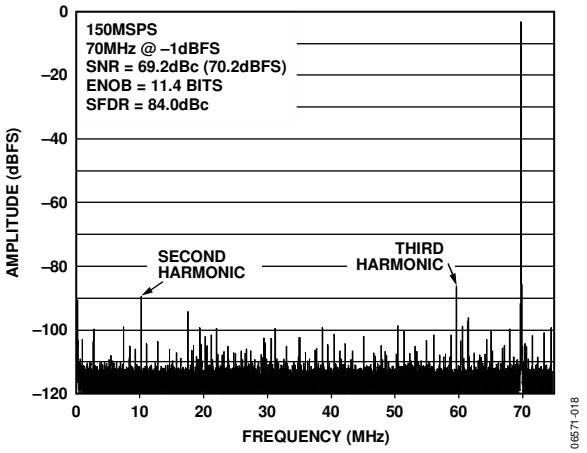

Figure 18. AD9627-150 Single-Tone FFT with f_{IN} = 70 MHz

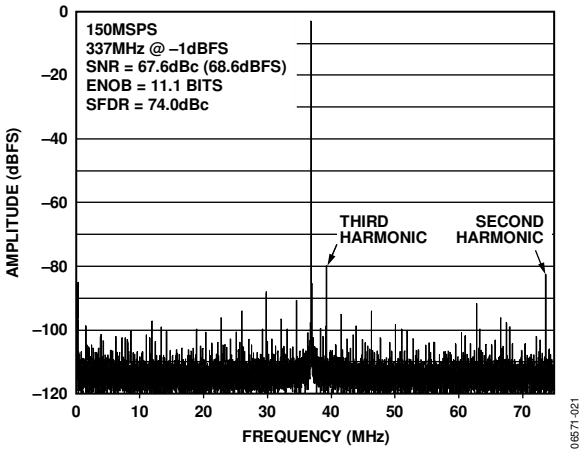

Figure 21. AD9627-150 Single-Tone FFT with f_{IN} = 337 MHz

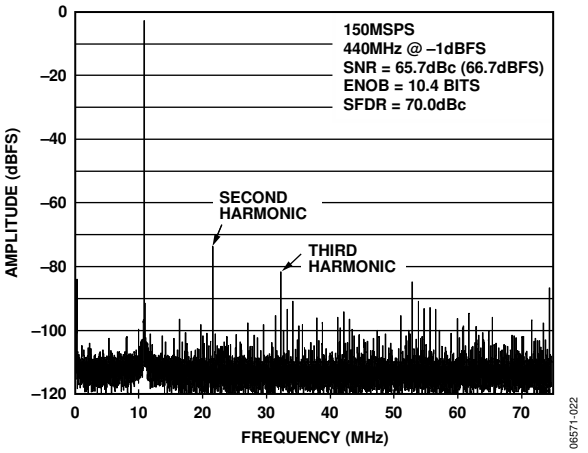

Figure 22. AD9627-150 Single-Tone FFT with f_{IN} = 440 MHz

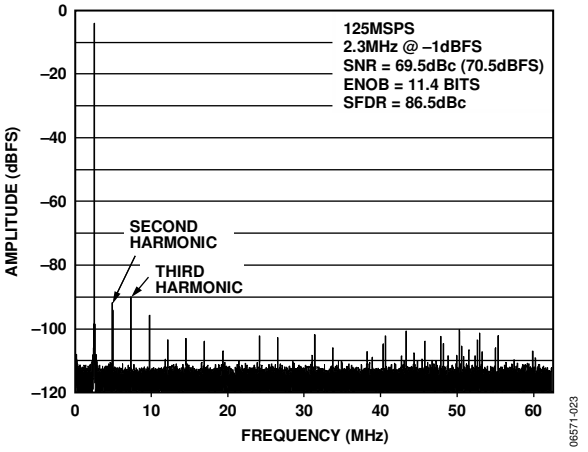

Figure 23. AD9627-125 Single-Tone FFT with f_{IN} = 2.3 MHz

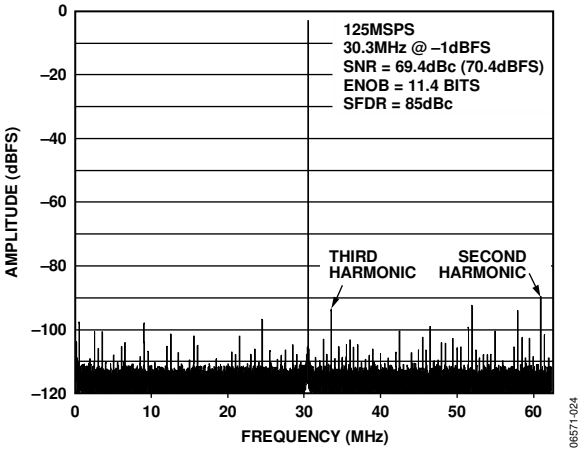

Figure 24. AD9627-125 Single-Tone FFT with f_{IN} = 30.3 MHz

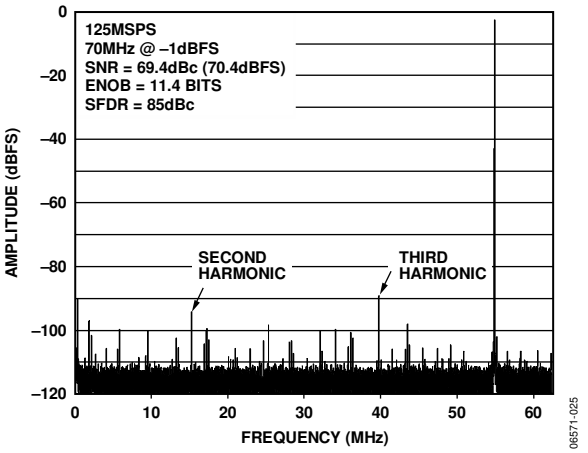

Figure 25. AD9627-125 Single-Tone FFT with f_{IN} = 70 MHz

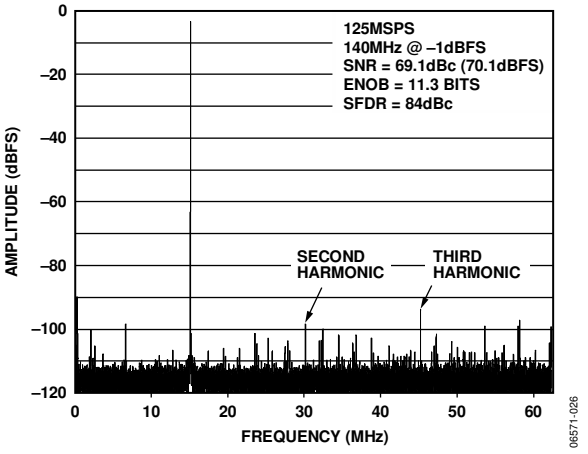

Figure 26. AD9627-125 Single-Tone FFT with f_{IN} = 140 MHz

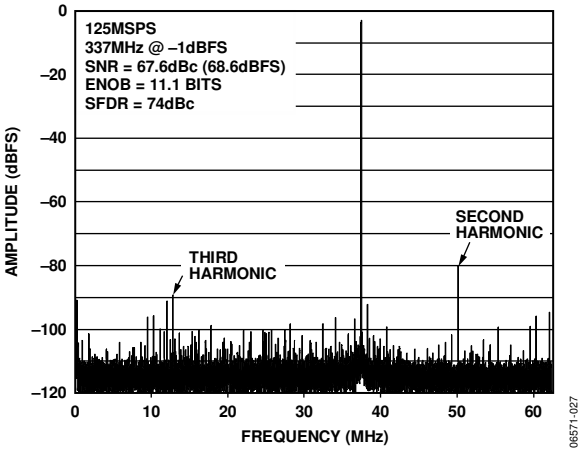

Figure 27. AD9627-125 Single-Tone FFT with f_{IN} = 337 MHz

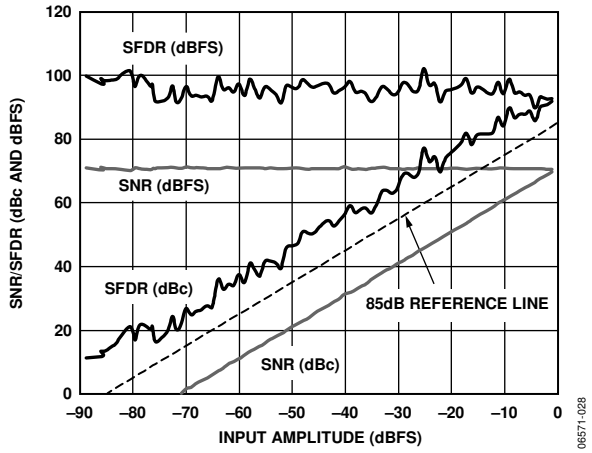

Figure 28. AD9627-150 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 2.4 MHz

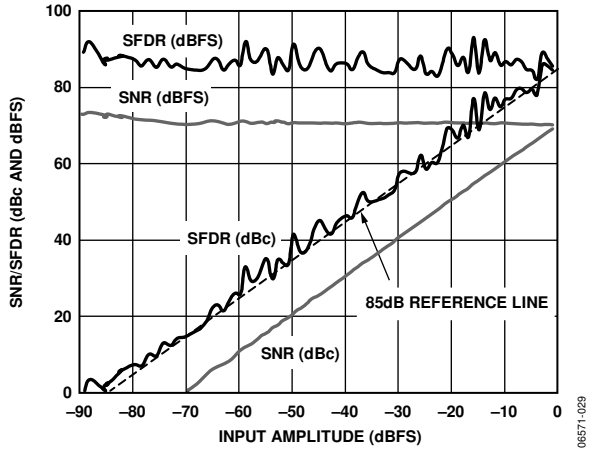

Figure 29. AD9627-150 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 98.12 MHz

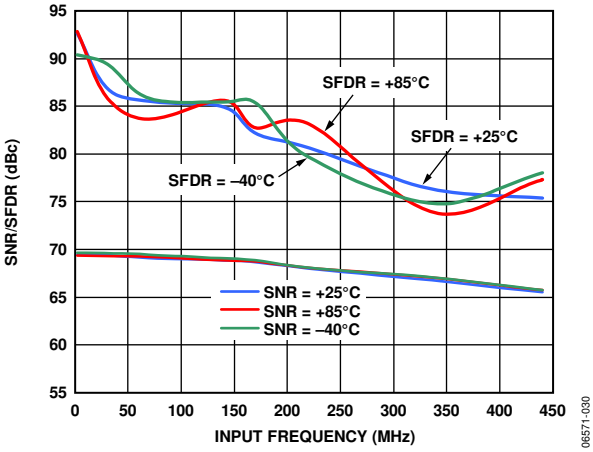

Figure 30. AD9627-150 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 2 V p-p Full Scale

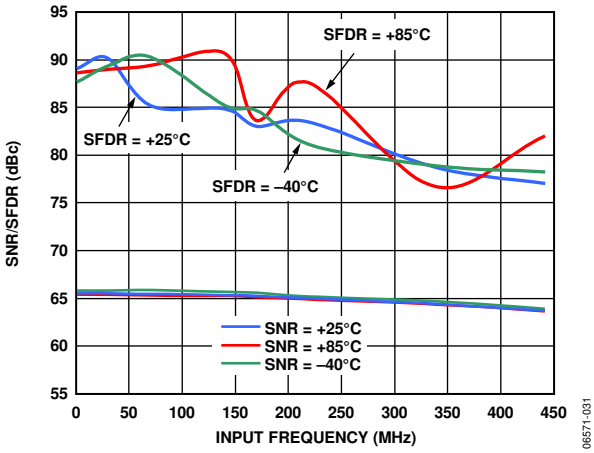

Figure 31. AD9627-150 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 1 V p-p Full Scale

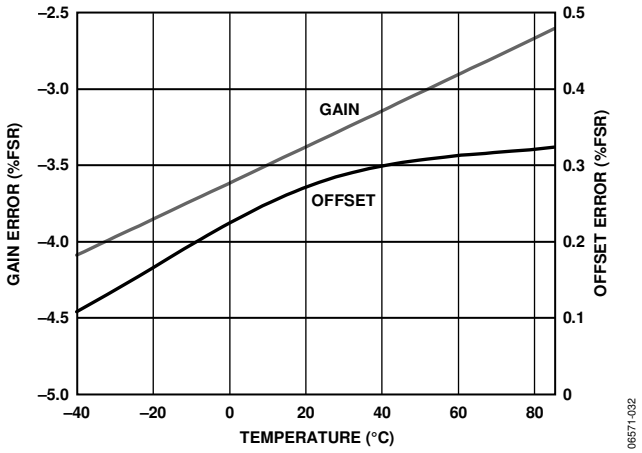

Figure 32. AD9627-150 Gain and Offset vs. Temperature

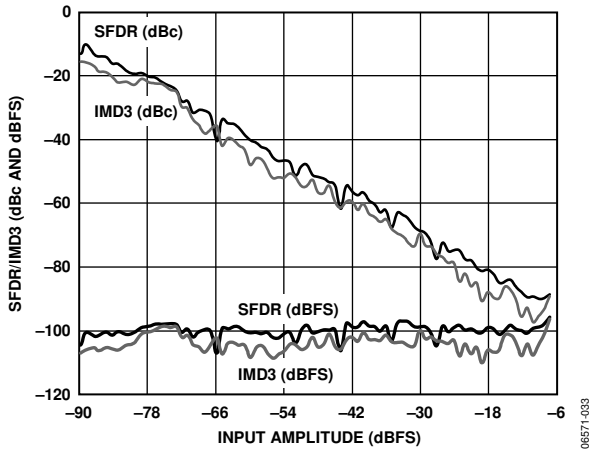

Figure 33. AD9627-150 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 29.1 MHz, f_{IN2} = 32.1 MHz, f_S = 150 MSPS

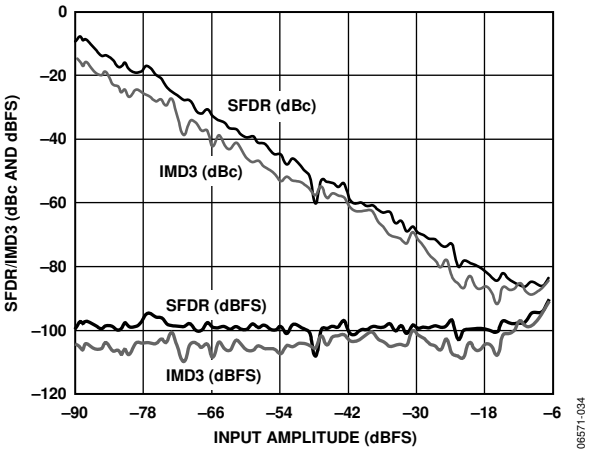

Figure 34. AD9627-150 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 169.1 MHz, f_{IN2} = 172.1 MHz, f_S = 150 MSPS

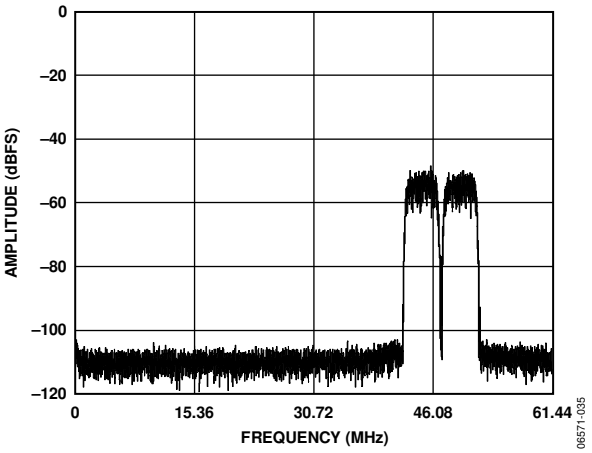

Figure 35. AD9627-125, Two 64k WCDMA Carriers with f_{IN} = 170 MHz, f_S = 122.88 MSPS

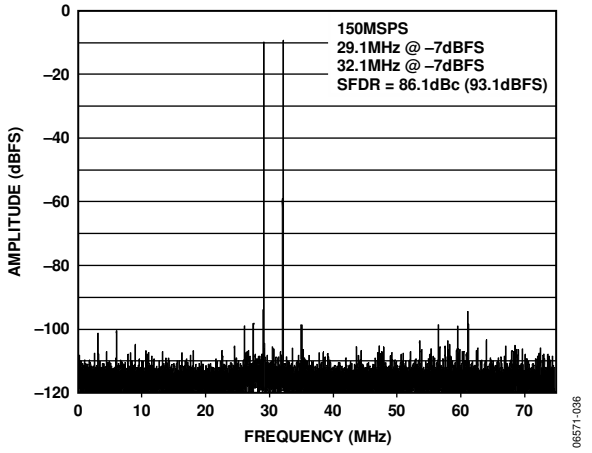

Figure 36. AD9627-150 Two-Tone FFT with f_{IN1} = 29.1 MHz and f_{IN2} = 32.1 MHz

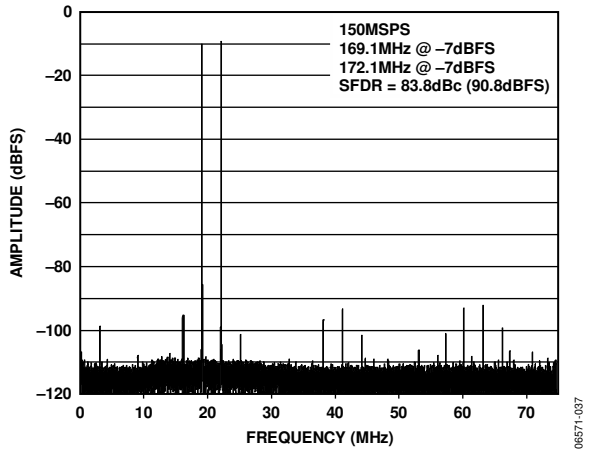

Figure 37. AD9627-150 Two-Tone FFT with f_{IN1} = 169.1 MHz and f_{IN2} = 172.1 MHz

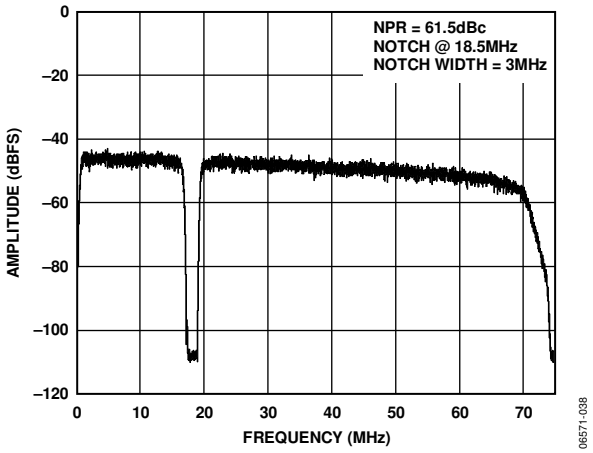

Figure 38. AD9627-150 Noise Power Ratio (NPR)

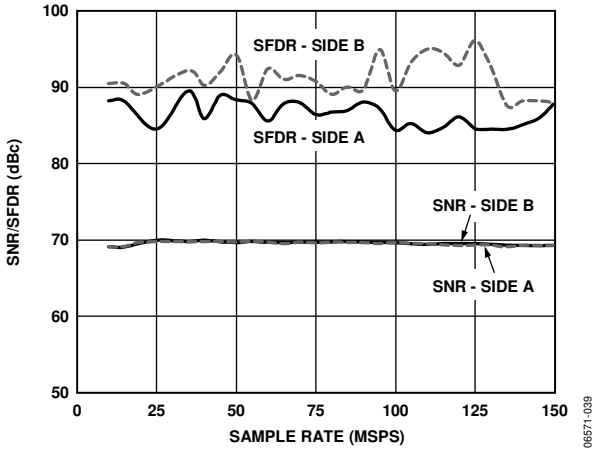

Figure 39. AD9627-150 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 2.3 MHz