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FEATURES

- 1.8 V supply operation**
- Low power: 100 mW per channel at 125 MSPS with scalable power options**
- SNR = 71 dB (to Nyquist)**
- SFDR = 91 dBc (to Nyquist)**
- DNL = ± 0.3 LSB (typical); INL = ± 0.5 LSB (typical)**
- Serial LVDS (ANSI-644, default) and low power, reduced signal option (similar to IEEE 1596.3)**
- 650 MHz full power analog bandwidth**
- 2 V p-p input voltage range**
- Serial port control**
 - Full chip and individual channel power-down modes
 - Flexible bit orientation
 - Built-in and custom digital test pattern generation
 - Multichip sync and clock divider
 - Programmable output clock and data alignment
 - Programmable output resolution
 - Standby mode

APPLICATIONS

- Medical ultrasound
- High speed imaging
- Quadrature radio receivers
- Diversity radio receivers
- Test equipment

GENERAL DESCRIPTION

The **AD9633** is a quad, 12-bit, 80 MSPS/105 MSPS/125 MSPS analog-to-digital converter (ADC) with an on-chip sample-and-hold circuit designed for low cost, low power, small size, and ease of use. The product operates at a conversion rate of up to 125 MSPS and is optimized for outstanding dynamic performance and low power in applications where a small package size is critical.

The ADC requires a single 1.8 V power supply and LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock output (DCO) for capturing data on the output and a frame clock output (FCO) for signaling a new output byte are provided. Individual-channel power-down is supported and typically consumes less than 2 mW when all channels are disabled.

Rev. B

Document Feedback

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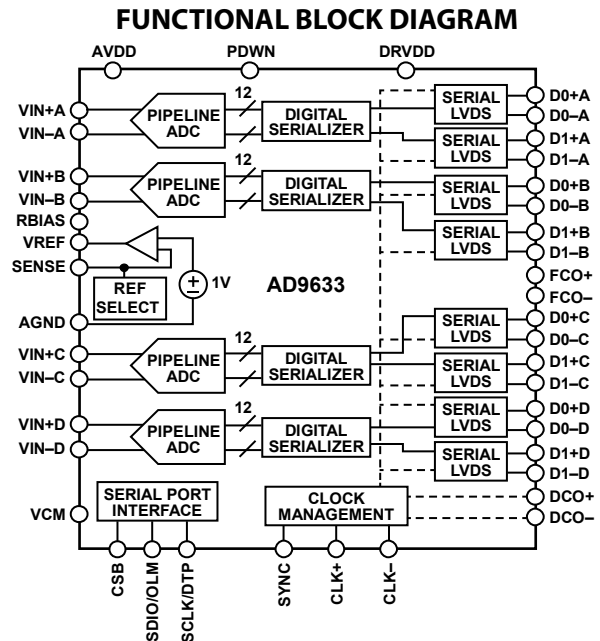


Figure 1.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable output clock and data alignment and digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

The **AD9633** is available in a RoHS-compliant, 48-lead LFCSP. It is specified over the industrial temperature range of -40°C to $+85^{\circ}\text{C}$. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Small Footprint. Four ADCs are contained in a small, space-saving package.
2. Low power of 100 mW/channel at 125 MSPS with scalable power options.
3. Pin compatible to the **AD9253** 14-bit quad ADC.
4. Ease of Use. A data clock output (DCO) operates at frequencies of up to 375 MHz and supports double data rate (DDR) operation.
5. User Flexibility. The SPI control offers a wide range of flexible features to meet specific system requirements.

AD9633* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9633 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-737: How ADIsimADC Models an ADC
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-878: High Speed ADC SPI Control Software
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD9633: Quad, 12-Bit, 80 MSPS/105 MSPS/125 MSPS, Serial LVDS 1.8 V ADC Data Sheet

User Guides

- Evaluating the AD9253/AD9633/AD9653 Analog-to-Digital Converters

TOOLS AND SIMULATIONS

- Visual Analog
- AD9633 IBIS Model

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9633 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9633 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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10/15—Rev. A to Rev. B

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9/14—Rev. 0 to Rev. A

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Added Propagation Delay Parameters of 1.5 ns (min) and 3.1 ns (max); Table 4.....	6
Changed t_{SSYNC} from 0.24 ns Typ to 1.2 ns Min and Changed t_{HSYNC} from 0.40 ns Typ to -0.2 ns Min; Table 5 and Changes to Figure 2	7
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10/11—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = -1.0 dBFS, unless otherwise noted.

Table 1.

Parameter ¹	Temp	AD9633-80			AD9633-105			AD9633-125			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION		12			12			12			Bits
ACCURACY		Guaranteed			Guaranteed			Guaranteed			
No Missing Codes	Full	Guaranteed			Guaranteed			Guaranteed			
Offset Error	Full	-0.7	-0.3	+0.1	-0.7	-0.3	+0.1	-0.7	-0.3	+0.1	% FSR
Offset Matching	Full	-0.6	+0.2	+0.6	-0.6	+0.2	+0.6	-0.6	+0.2	+0.6	% FSR
Gain Error	Full	-10	-5	0	-10	-5	0	-10	-5	0	% FSR
Gain Matching	Full	1		1.5	1		1.8	1		1.5	% FSR
Differential Nonlinearity (DNL)	Full	-0.6		+0.6	-0.6		+0.6	-0.6		+0.6	LSB
	25°C	±0.3			±0.3			±0.3			LSB
Integral Nonlinearity (INL)	Full	-1.4		+1.6	-1.4		+1.6	-1.4		+1.6	LSB
	25°C	±0.5			±0.5			±0.5			LSB
TEMPERATURE DRIFT											
Offset Error	Full	±2			±2			±2			ppm/°C
INTERNAL VOLTAGE REFERENCE											
Output Voltage (1 V Mode)	Full	0.98	1.0	1.02	0.98	1.0	1.02	0.98	1.0	1.02	V
Load Regulation at 1.0 mA (V _{REF} = 1 V)	Full	2			2			2			mV
Input Resistance	Full	7.5			7.5			7.5			kΩ
INPUT-REFERRED NOISE											
V _{REF} = 1.0 V	25°C	0.25			0.25			0.25			LSB rms
ANALOG INPUTS											
Differential Input Voltage (V _{REF} = 1 V)	Full	2			2			2			V p-p
Common-Mode Voltage	Full	0.9			0.9			0.9			V
Differential Input Resistance		5.2			5.2			5.2			kΩ
Differential Input Capacitance	Full	3.5			3.5			3.5			pF
POWER SUPPLY											
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
I _{AVDD} ²	Full	125		136	151		166	173		191	mA
I _{DRVDD} (ANSI-644 Mode) ²	Full	59		80	63		97	66		101	mA
I _{DRVDD} (Reduced Range Mode) ²	25°C	40			43			46			mA
TOTAL POWER CONSUMPTION											
DC Input	Full	313			360			400			mW
Sine Wave Input (Four Channels Including Output Drivers ANSI-644 Mode)	Full	331		389	385		473	430		526	mW
Sine Wave Input (Four Channels Including Output Drivers Reduced Range Mode)	25°C	297			349			394			mW
Power-Down	Full	2			2			2			mW
Standby ³	Full	174			202			226			mW

¹ See the [AN-835 Application Note](#), *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.

² Measured with a low input frequency, full-scale sine wave on all four channels.

³ Can be controlled via the SPI.

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = -1.0 dBFS, unless otherwise noted.

Table 2.

Parameter ¹	Temp	AD9633-80			AD9633-105			AD9633-125			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SIGNAL-TO-NOISE RATIO (SNR)											
$f_{IN} = 9.7$ MHz	25°C		71.7			71.7			71.8		dBFS
$f_{IN} = 30.5$ MHz	25°C		71.7			71.6			71.4		dBFS
$f_{IN} = 70$ MHz	Full	70.0	70.5		70.2	71.0		70.5	71.1		dBFS
$f_{IN} = 140$ MHz	25°C		70.3			70.2			70.0		dBFS
$f_{IN} = 200$ MHz	25°C		69.4			69.8			69.4		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)											
$f_{IN} = 9.7$ MHz	25°C		71.6			71.6			71.1		dBFS
$f_{IN} = 30.5$ MHz	25°C		71.5			71.5			71.3		dBFS
$f_{IN} = 70$ MHz	Full	70.0	70.4		69.5	70.9		70.5	71.0		dBFS
$f_{IN} = 140$ MHz	25°C		70.2			69.9			69.9		dBFS
$f_{IN} = 200$ MHz	25°C		68.4			68.7			67.4		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)											
$f_{IN} = 9.7$ MHz	25°C		11.6			11.6			11.5		Bits
$f_{IN} = 30.5$ MHz	25°C		11.6			11.6			11.5		Bits
$f_{IN} = 70$ MHz	Full	11.3	11.5		11.3	11.6		11.4	11.5		Bits
$f_{IN} = 140$ MHz	25°C		11.4			11.3			11.3		Bits
$f_{IN} = 200$ MHz	25°C		11.2			11.2			10.9		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)											
$f_{IN} = 9.7$ MHz	25°C		96			94			94		dBc
$f_{IN} = 30.5$ MHz	25°C		90			89			91		dBc
$f_{IN} = 70$ MHz	Full	76	96		75	87		75	91		dBc
$f_{IN} = 140$ MHz	25°C		87			91			86		dBc
$f_{IN} = 200$ MHz	25°C		86			88			86		dBc
WORST HARMONIC (SECOND OR THIRD)											
$f_{IN} = 9.7$ MHz	25°C		-96			-94			-94		dBc
$f_{IN} = 30.5$ MHz	25°C		-90			-89			-91		dBc
$f_{IN} = 70$ MHz	Full		-96	-76		-87	-75		-91	-75	dBc
$f_{IN} = 140$ MHz	25°C		-87			-91			-86		dBc
$f_{IN} = 200$ MHz	25°C		-86			-88			-86		dBc
WORST OTHER (EXCLUDING SECOND OR THIRD)											
$f_{IN} = 9.7$ MHz	25°C		-97			-96			-94		dBc
$f_{IN} = 30.5$ MHz	25°C		-95			-93			-97		dBc
$f_{IN} = 70$ MHz	Full		-96	-82		-94	-82		-96	-84	dBc
$f_{IN} = 140$ MHz	25°C		-97			-93			-92		dBc
$f_{IN} = 200$ MHz	25°C		-96			-93			-90		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)—AIN1 AND AIN2 = -7.0 dBFS											
$f_{IN1} = 70.5$ MHz, $f_{IN2} = 72.5$ MHz	25°C		85			86			87		dBc
CROSSTALK ²	Full		-95			-95			-95		dB
CROSSTALK (OVERRANGE CONDITION) ³	25°C		-89			-89			-89		dB
POWER SUPPLY REJECTION RATIO (PSRR) ^{1,4}											
AVDD	25°C		52			52			52		dB
DRVDD	25°C		75			75			75		dB
ANALOG INPUT BANDWIDTH, FULL POWER	25°C		650			650			650		MHz

¹ See the [AN-835 Application Note, Understanding High Speed ADC Testing and Evaluation](#), for definitions and for details on how these tests were completed.

² Crosstalk is measured at 70 MHz with -1.0 dBFS analog input on one channel and no input on the adjacent channel.

³ Overrange condition is specified as being 3 dB above the full-scale input range.

⁴ PSRR is measured by injecting a sinusoidal signal at 10 MHz to the power supply pin and measuring the output spur on the FFT. PSRR is calculated as the ratio of the amplitudes of the spur voltage over the pin voltage, expressed in decibels.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = -1.0 dBFS, unless otherwise noted.

Table 3.

Parameter ¹	Temp	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK-)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage ²	Full	0.2		3.6	V p-p
Input Voltage Range	Full	AGND - 0.2		AVDD + 0.2	V
Input Common-Mode Voltage	Full		0.9		V
Input Resistance (Differential)	25°C		10		kΩ
Input Capacitance	25°C		4		pF
LOGIC INPUTS (PDWN, SYNC, SCLK)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		2		pF
LOGIC INPUT (CSB)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		2		pF
LOGIC INPUT (SDIO)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		5		pF
LOGIC OUTPUT (SDIO) ³					
Logic 1 Voltage (I _{OH} = 800 μA)	Full		1.79		V
Logic 0 Voltage (I _{OL} = 50 μA)	Full			0.05	V
DIGITAL OUTPUTS (D0±x, D1±x), ANSI-644					
Logic Compliance			LVDS		
Differential Output Voltage (V _{OD})	Full	290	345	400	mV
Output Offset Voltage (V _{OS})	Full	1.15	1.25	1.35	V
Output Coding (Default)			Twos complement		
DIGITAL OUTPUTS (D0±x, D1±x), LOW POWER, REDUCED SIGNAL OPTION					
Logic Compliance			LVDS		
Differential Output Voltage (V _{OD})	Full	160	200	230	mV
Output Offset Voltage (V _{OS})	Full	1.15	1.25	1.35	V
Output Coding (Default)			Twos complement		

¹ See the [AN-835 Application Note, Understanding High Speed ADC Testing and Evaluation](#), for definitions and for details on how these tests were completed.

² This is specified for LVDS and LVPECL only.

³ This is specified for 13 SDIO/OLM pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = -1.0 dBFS, unless otherwise noted.

Table 4.

Parameter ^{1,2}	Temp	Min	Typ	Max	Unit
CLOCK³					
Input Clock Rate	Full	10		1000	MHz
Conversion Rate ⁴	Full	10		80/105/125	MSPS
Clock Pulse Width High (t _{EH})	Full		6.25/4.76/4.00		ns
Clock Pulse Width Low (t _{EL})	Full		6.25/4.76/4.00		ns
OUTPUT PARAMETERS³					
Propagation Delay (t _{PD})	Full	1.5	2.3	3.1	ns
Rise Time (t _r) (20% to 80%)	Full		300		ps
Fall Time (t _f) (20% to 80%)	Full		300		ps
FCO Propagation Delay (t _{FCO})	Full	1.5	2.3	3.1	ns
DCO Propagation Delay (t _{CPD}) ⁵	Full		t _{FCO} + (t _{SAMPLE} /12)		ns
DCO to Data Delay (t _{DATA}) ⁵	Full	(t _{SAMPLE} /12) - 300	(t _{SAMPLE} /12)	(t _{SAMPLE} /12) + 300	ps
DCO to FCO Delay (t _{FRAME}) ⁵	Full	(t _{SAMPLE} /12) - 300	(t _{SAMPLE} /12)	(t _{SAMPLE} /12) + 300	ps
Lane Delay (t _{LD})			90		ps
Data to Data Skew (t _{DATA-MAX} - t _{DATA-MIN})	Full		±50	±200	ps
Wake-Up Time (Standby)	25°C		250		ns
Wake-Up Time (Power-Down) ⁶	25°C		375		μs
Pipeline Latency	Full		16		Clock cycles
APERTURE					
Aperture Delay (t _A)	25°C		1		ns
Aperture Uncertainty (Jitter, t _j)	25°C		135		fs rms
Out-of-Range Recovery Time	25°C		1		Clock cycles

¹ See the [AN-835 Application Note, Understanding High Speed ADC Testing and Evaluation](#), for definitions and for details on how these tests were completed.

² Measured on standard FR-4 material.

³ Can be adjusted via the SPI. The conversion rate is the clock rate after the divider.

⁴ The maximum conversion rate is based on two-lane output mode. See the Digital Outputs and Timing section for the maximum conversion rate in one-lane output mode.

⁵ t_{SAMPLE}/12 is based on the number of bits in two LVDS data lanes. t_{SAMPLE} = 1/f_s.

⁶ Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Description	Limit	Unit
SYNC TIMING REQUIREMENTS			
t_{SSYNC}	SYNC to rising edge of CLK+ setup time	1.2	ns min
t_{HSYNC}	SYNC to rising edge of CLK+ hold time	-0.2	ns min
SPI TIMING REQUIREMENTS			
	See Figure 73		
t_{DS}	Setup time between the data and the rising edge of SCLK	2	ns min
t_{DH}	Hold time between the data and the rising edge of SCLK	2	ns min
t_{CLK}	Period of the SCLK	40	ns min
t_S	Setup time between CSB and SCLK	2	ns min
t_H	Hold time between CSB and SCLK	2	ns min
t_{HIGH}	SCLK pulse width high	10	ns min
t_{LOW}	SCLK pulse width low	10	ns min
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 73)	10	ns min
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 73)	10	ns min

Timing Diagrams

Refer to the Memory Map Register Descriptions section and Table 21 for SPI register settings.

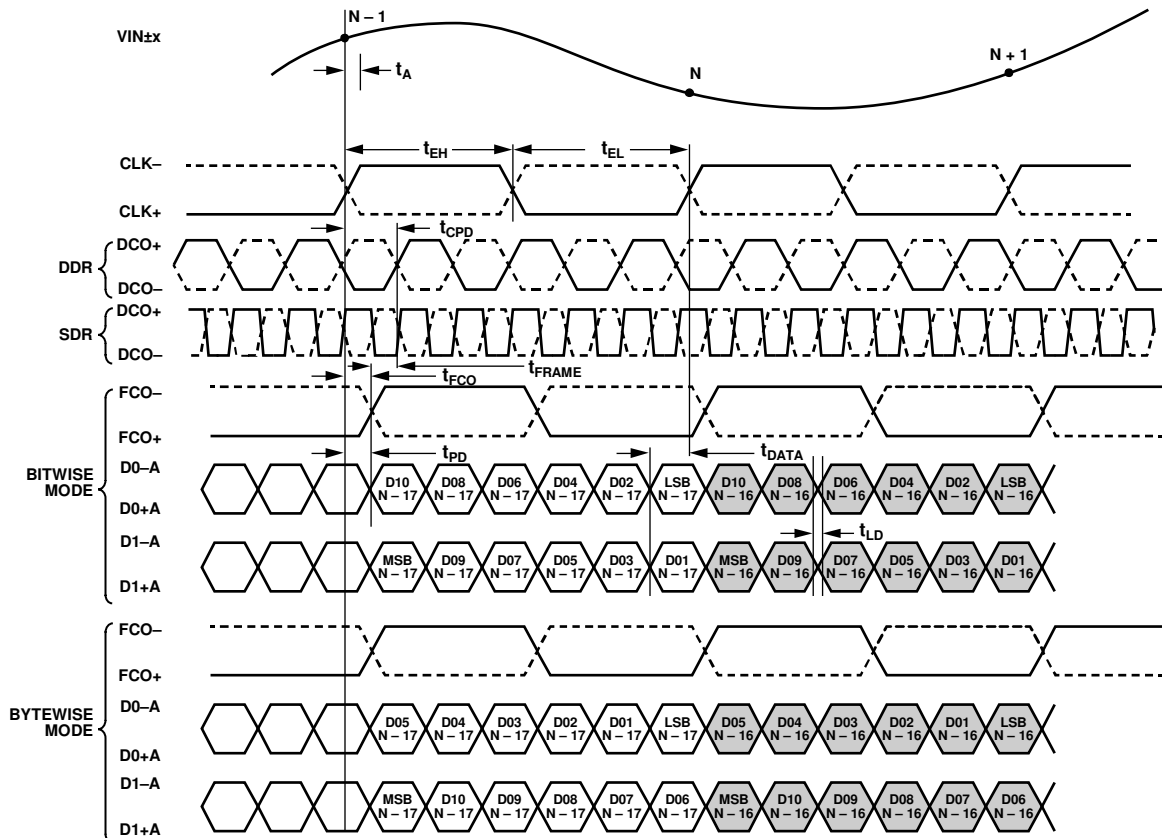


Figure 2. 12-Bit DDR/SDR, Two-Lane, 1x Frame Mode (Default)

10073-004

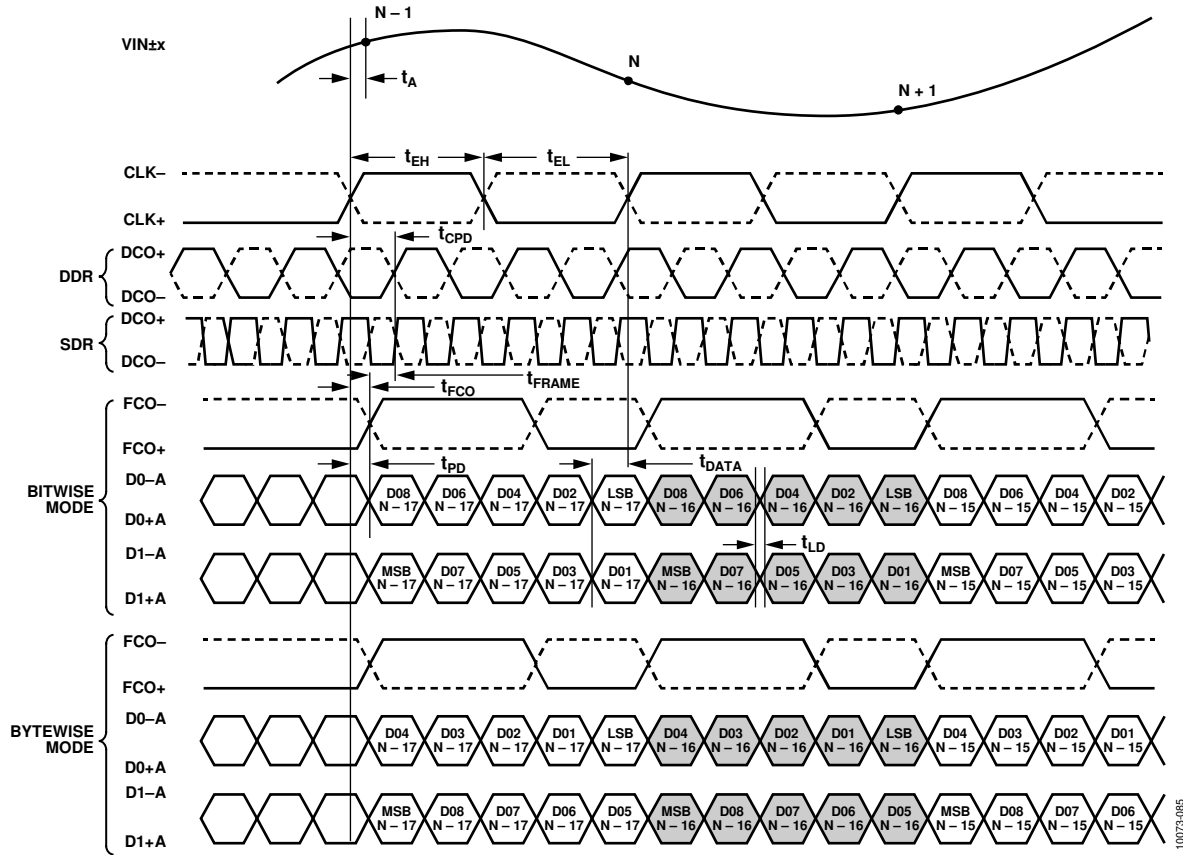


Figure 3. 10-Bit DDR/SDR, Two-Lane, 1x Frame Mode

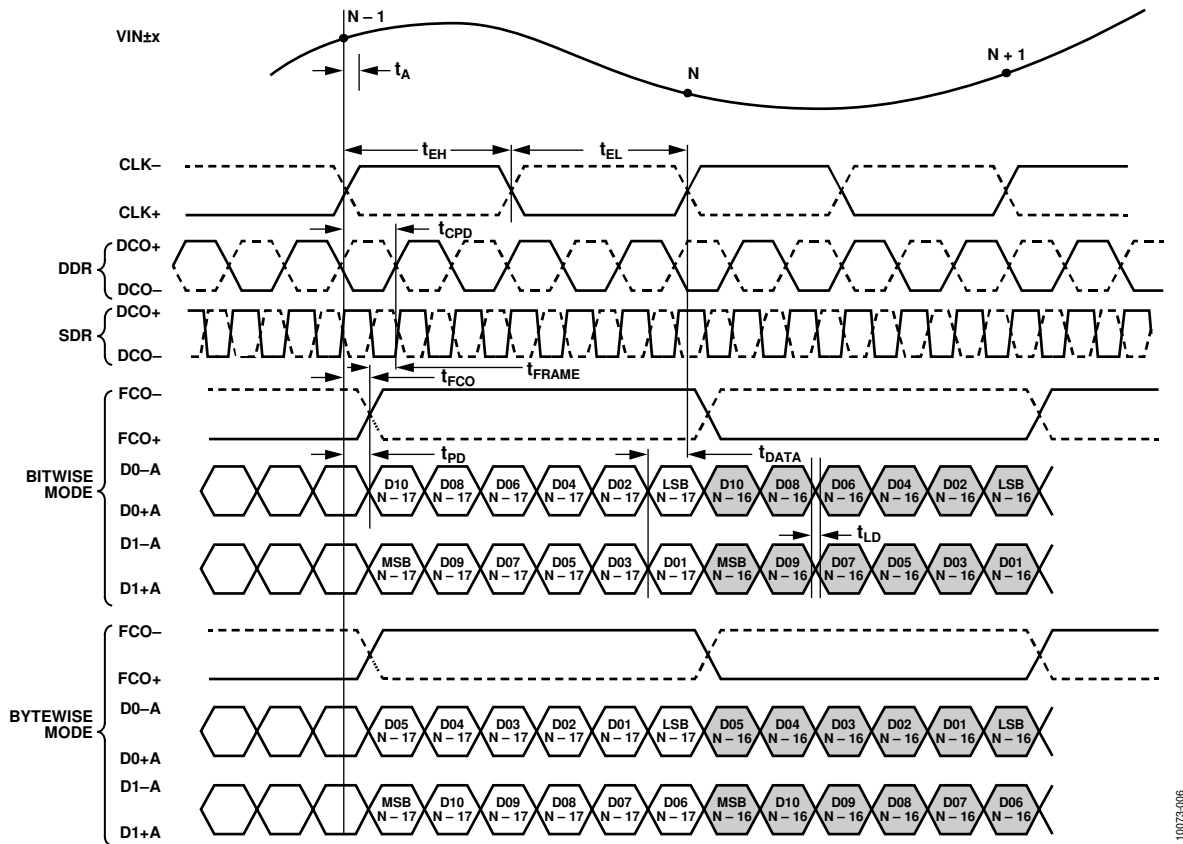


Figure 4. 12-Bit DDR/SDR, Two-Lane, 2x Frame Mode

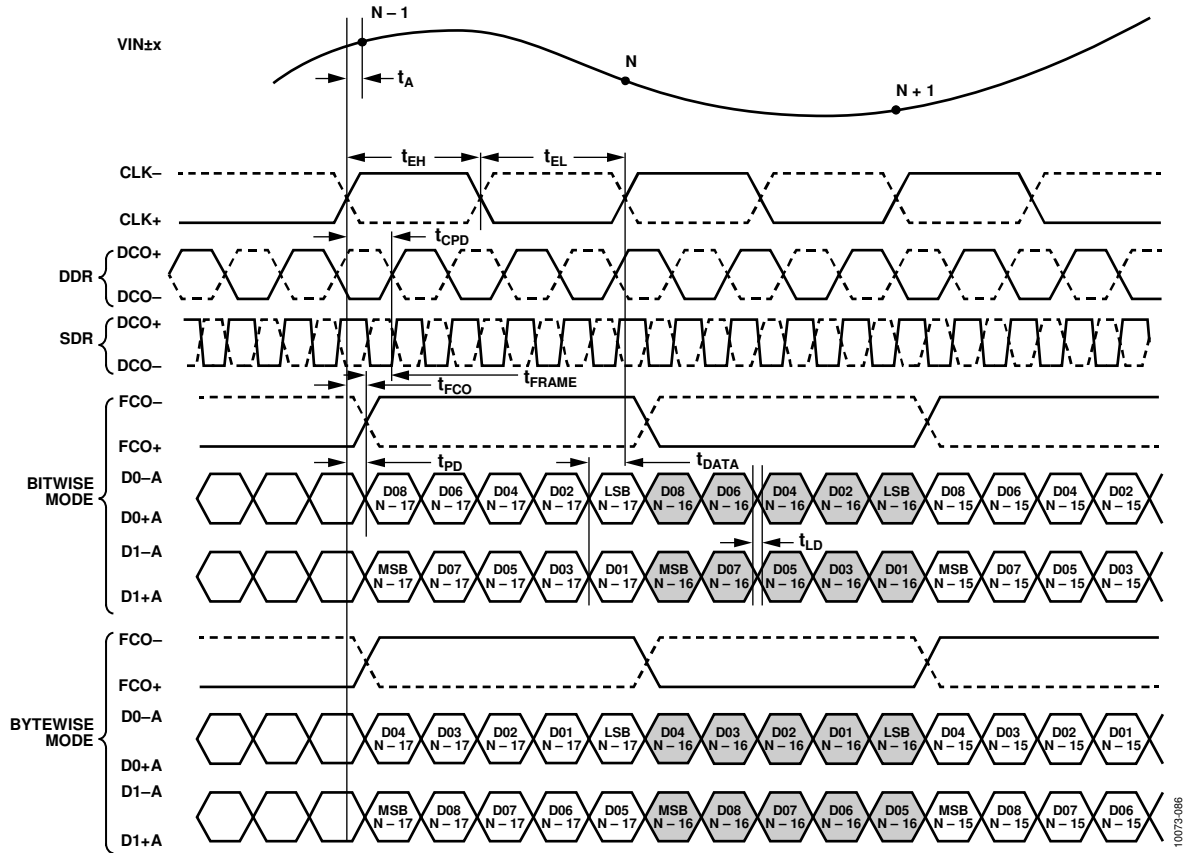


Figure 5. 10-Bit DDR/SDR, Two-Lane, 2x Frame Mode

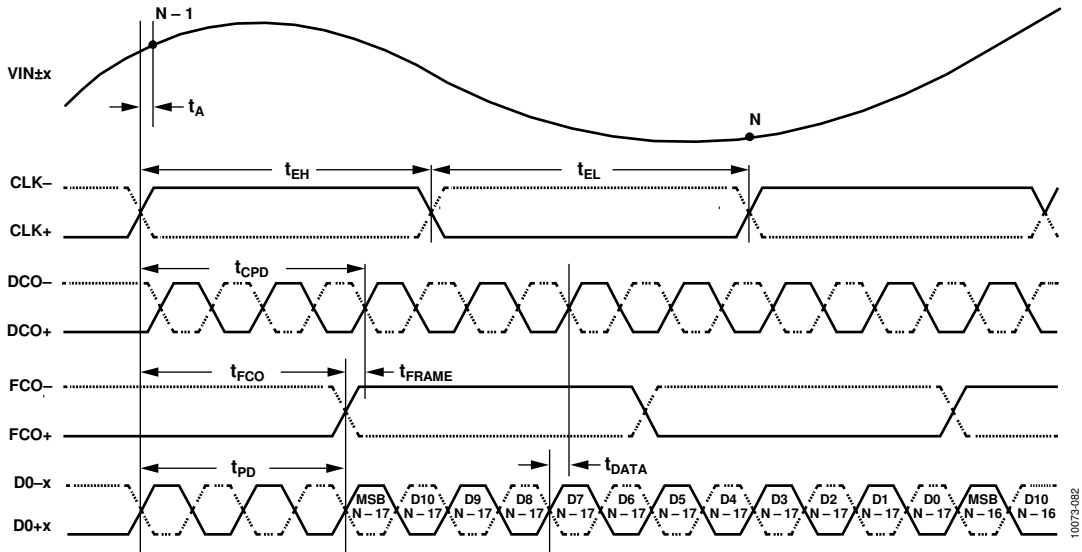


Figure 6. Wordwise DDR, One-Lane, 1x Frame, 12-Bit Output Mode

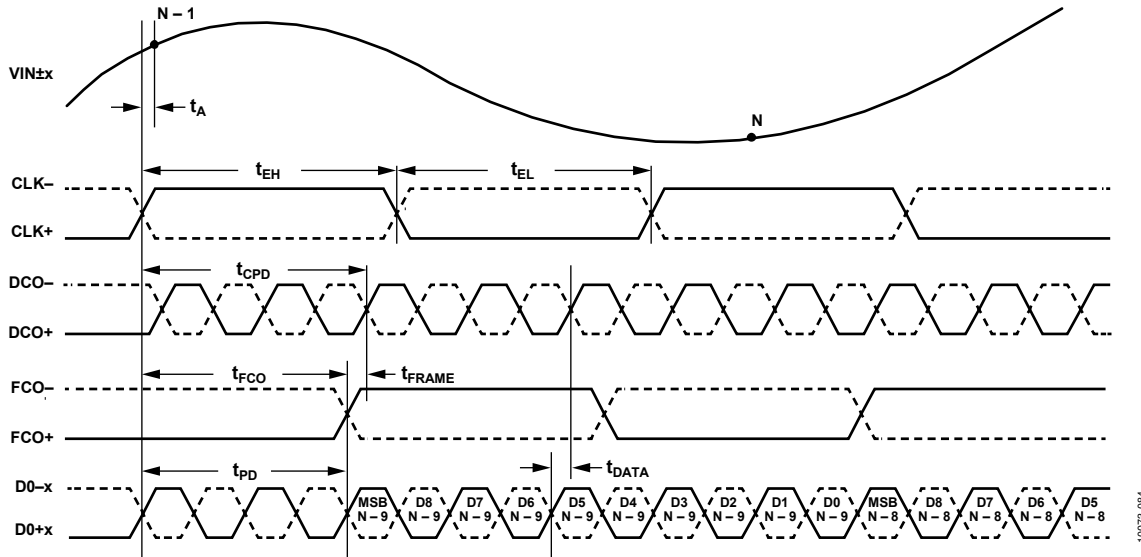


Figure 7. Wordwise DDR, One-Lane, 1x Frame, 10-Bit Output Mode

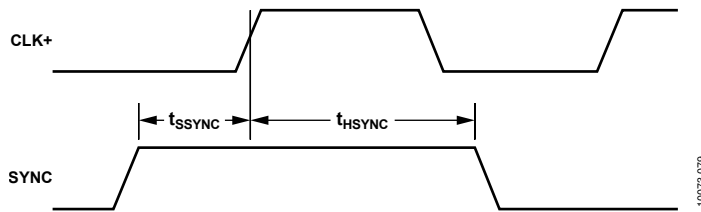


Figure 8. SYNC Input Timing Requirements

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
Digital Outputs (D0±x, D1±x, DCO+, DCO−, FCO+, FCO−) to AGND	−0.3 V to +2.0 V
CLK+, CLK− to AGND	−0.3 V to +2.0 V
VIN+x, VIN−x to AGND	−0.3 V to +2.0 V
SCLK/DTP, SDIO/OLM, CSB to AGND	−0.3 V to +2.0 V
SYNC, PDWN to AGND	−0.3 V to +2.0 V
RBIAS to AGND	−0.3 V to +2.0 V
VREF, SENSE to AGND	−0.3 V to +2.0 V
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 7. Thermal Resistance

Package Type	Air Flow Velocity (m/sec)	θ_{JA}^1	θ_{JB}	θ_{JC}	Unit
48-Lead LFCSP	0.0	23.7	7.8	7.1	°C/W
7 mm × 7 mm	1.0	20.0	N/A	N/A	°C/W
CP-48-13	2.5	18.7	N/A	N/A	°C/W

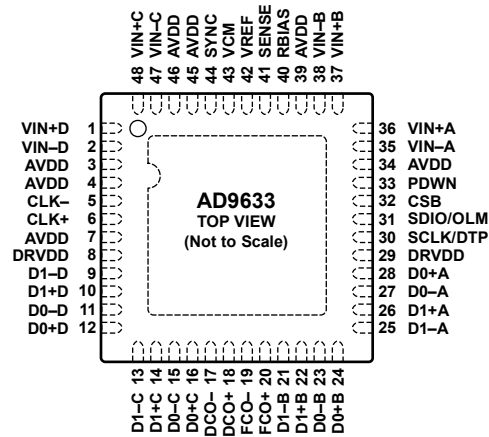
¹ θ_{JA} for a 4-layer PCB with solid ground plane (simulated). Exposed pad soldered to PCB.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES
1. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE PART. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

100793-007

Figure 9. 48-Lead LFCSP Pin Configuration, Top View

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	AGND, Exposed Pad	Analog Ground, Exposed Pad. The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
1	VIN+D	ADC D Analog Input True.
2	VIN-D	ADC D Analog Input Complement.
3, 4, 7, 34, 39, 45, 46	AVDD	1.8 V Analog Supply Pins.
5, 6	CLK-, CLK+	Differential Encode Clock. PECL, LVDS, or 1.8 V CMOS inputs.
8, 29	DRVDD	Digital Output Driver Supply.
9, 10	D1-D, D1+D	Channel D Digital Outputs, (Disabled in One-Lane Mode ¹).
11, 12	D0-D, D0+D	Channel D Digital Outputs, (Disabled in One-Lane Mode ¹).
13, 14	D1-C, D1+C	Channel C Digital Outputs, (Channel D Digital Outputs in One-Lane Mode ¹).
15, 16	D0-C, D0+C	Channel C Digital Outputs.
17, 18	DCO-, DCO+	Data Clock Outputs.
19, 20	FCO-, FCO+	Frame Clock Outputs.
21, 22	D1-B, D1+B	Channel B Digital Outputs.
23, 24	D0-B, D0+B	Channel B Digital Outputs, (Channel A Digital Outputs in One-Lane Mode ¹).
25, 26	D1-A, D1+A	Channel A Digital Outputs, (Disabled in One-Lane Mode ¹).
27, 28	D0-A, D0+A	Channel A Digital Outputs, (Disabled in One-Lane Mode ¹).
30	SCLK/DTP	SPI Clock Input/Digital Test Pattern.
31	SDIO/OLM	SPI Data Input and Output Bidirectional SPI Data/Output Lane Mode.
32	CSB	SPI Chip Select Bar. Active low enable; 30 kΩ internal pull-up.
33	PDWN	Digital Input, 30 kΩ Internal Pull-Down. PDWN high = power-down device. PDWN low = run device, normal operation.
35	VIN-A	ADC A Analog Input Complement.
36	VIN+A	ADC A Analog Input True.
37	VIN+B	ADC B Analog Input True.
38	VIN-B	ADC B Analog Input Complement.
40	RBIAS	Sets Analog Current Bias. Connect to 10 kΩ (1% tolerance) resistor to ground.
41	SENSE	Reference Mode Selection.
42	VREF	Voltage Reference Input and Output.

Pin No.	Mnemonic	Description
43	VCM	Analog Input Common-Mode Voltage.
44	SYNC	Digital Input. SYNC input to clock divider.
47	VIN-C	ADC C Analog Input Complement.
48	VIN+C	ADC C Analog Input True.

¹ Output channel assignments are shown first for default two-lane mode. If one-lane mode is used, output channel assignments change as indicated in parenthesis. Register 0x21 Bits[6:4] invoke one-lane mode.

TYPICAL PERFORMANCE CHARACTERISTICS

AD9633-80

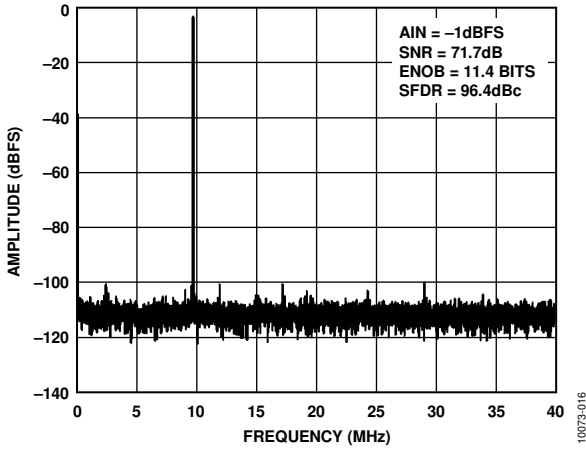


Figure 10. Single-Tone 16k FFT with $f_{IN} = 9.7$ MHz, $f_{SAMPLE} = 80$ MSPS

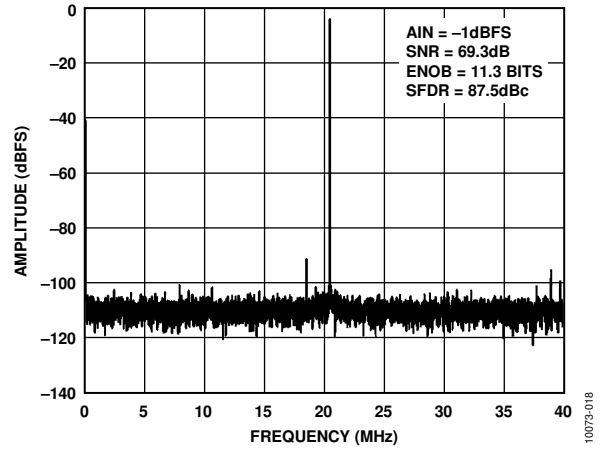


Figure 13. Single-Tone 16k FFT with $f_{IN} = 140$ MHz, $f_{SAMPLE} = 80$ MSPS

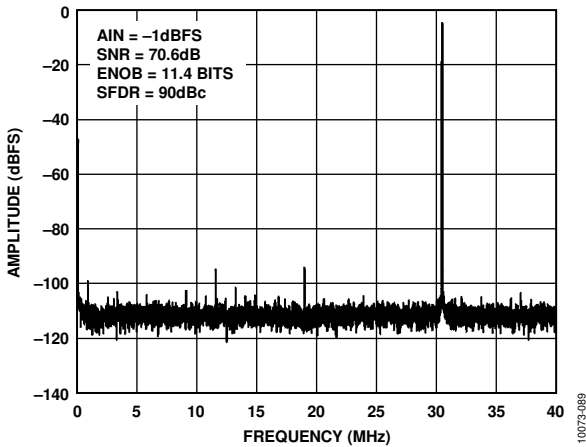


Figure 11. Single-Tone 16k FFT with $f_{IN} = 30.5$ MHz, $f_{SAMPLE} = 80$ MSPS

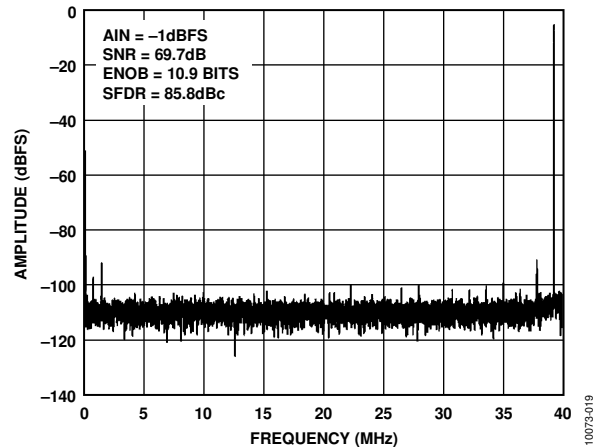


Figure 14. Single-Tone 16k FFT with $f_{IN} = 200$ MHz, $f_{SAMPLE} = 80$ MSPS

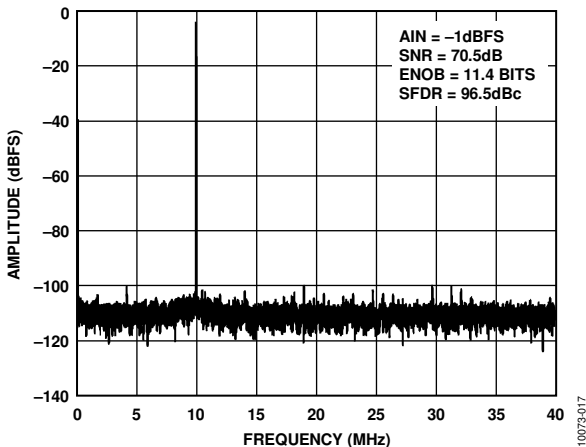


Figure 12. Single-Tone 16k FFT with $f_{IN} = 70$ MHz, $f_{SAMPLE} = 80$ MSPS

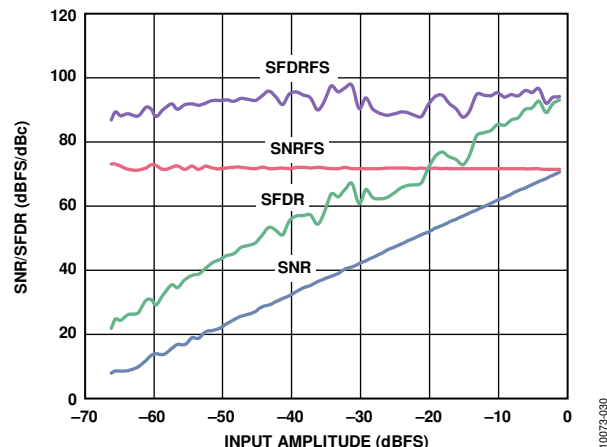


Figure 15. SNR/SFDR vs. Analog Input Level, $f_{IN} = 9.7$ MHz, $f_{SAMPLE} = 80$ MSPS

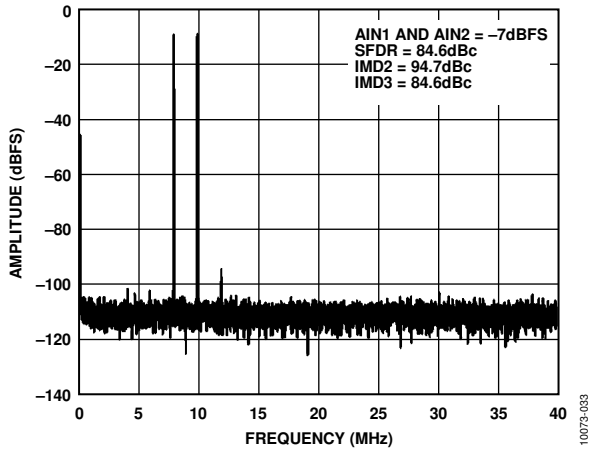


Figure 16. Two-Tone 16k FFT with $f_{IN1} = 70.5$ MHz and $f_{IN2} = 72.5$ MHz, $f_{SAMPLE} = 80$ MSPS

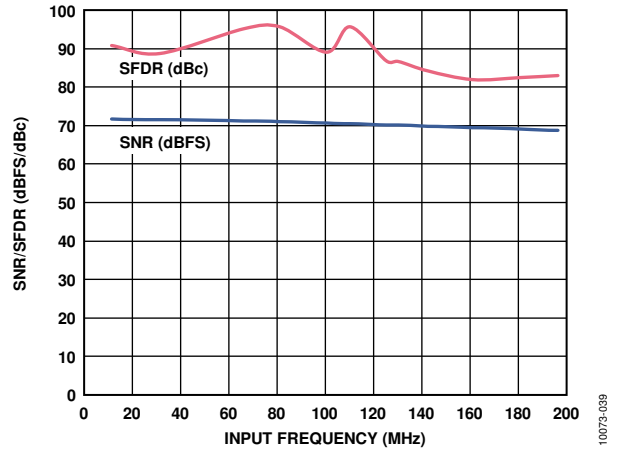


Figure 18. SNR/SFDR vs. f_{IN} , $f_{SAMPLE} = 80$ MSPS

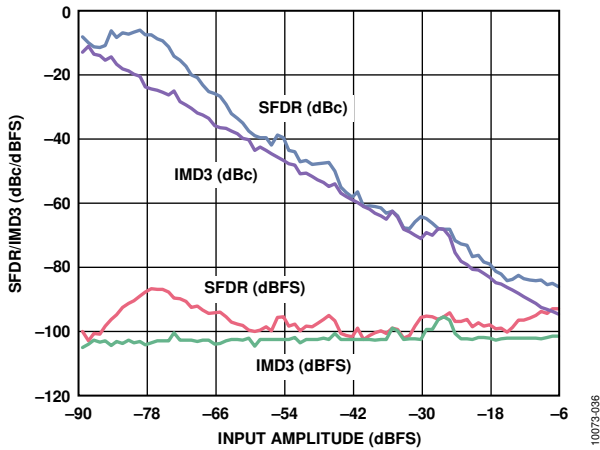


Figure 17. Two-Tone SFDR/IMD3 vs. Input Amplitude (AIN) with $f_{IN1} = 70.5$ MHz and $f_{IN2} = 72.5$ MHz, $f_{SAMPLE} = 80$ MSPS

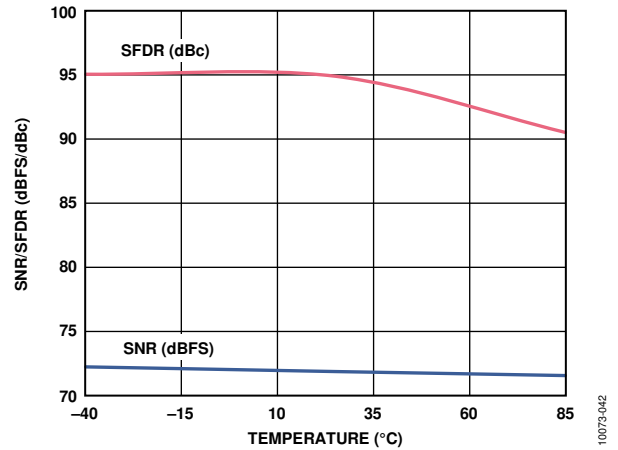


Figure 19. SNR/SFDR vs. Temperature, $f_{IN} = 10.3$ MHz, $f_{SAMPLE} = 80$ MSPS

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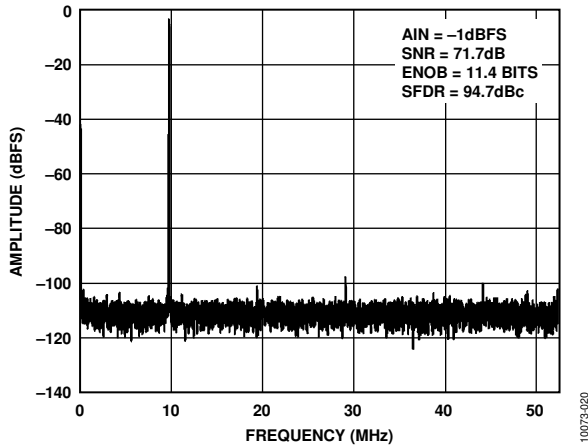


Figure 20. Single-Tone 16k FFT with $f_{IN} = 9.7$ MHz, $f_{SAMPLE} = 105$ MSPS

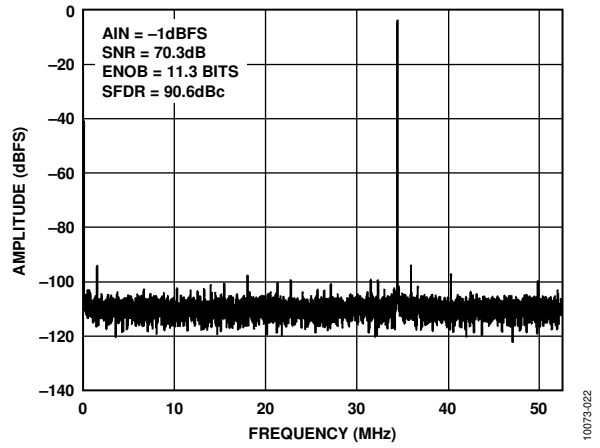


Figure 23. Single-Tone 16k FFT with $f_{IN} = 140$ MHz, $f_{SAMPLE} = 105$ MSPS

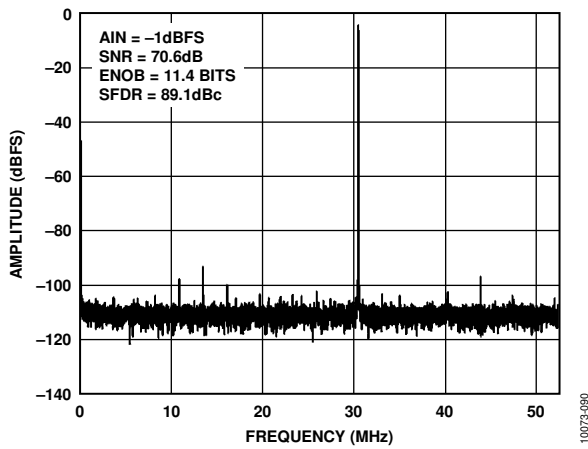


Figure 21. Single-Tone 16k FFT with $f_{IN} = 30.5$ MHz, $f_{SAMPLE} = 105$ MSPS

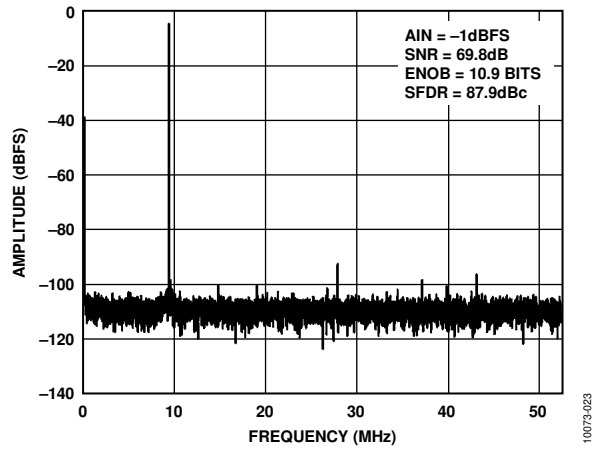


Figure 24. Single-Tone 16k FFT with $f_{IN} = 200$ MHz, $f_{SAMPLE} = 105$ MSPS

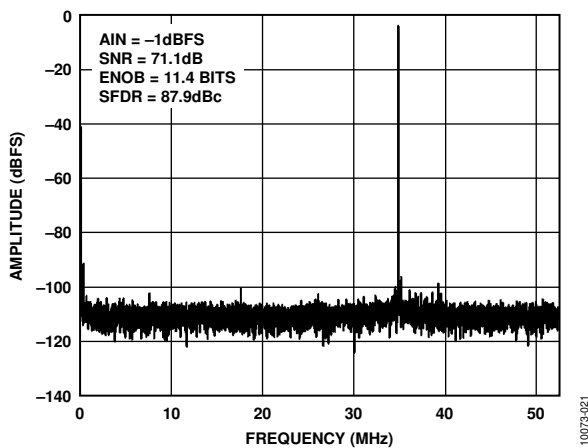


Figure 22. Single-Tone 16k FFT with $f_{IN} = 70$ MHz, $f_{SAMPLE} = 105$ MSPS

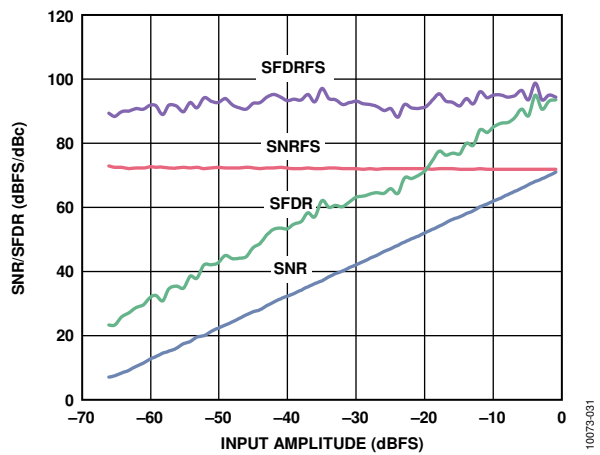


Figure 25. SNR/SFDR vs. Analog Input Level, $f_{IN} = 9.7$ MHz, $f_{SAMPLE} = 105$ MSPS

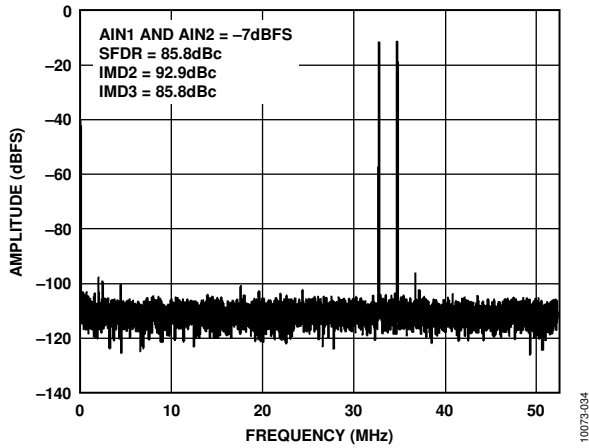


Figure 26. Two-Tone 16k FFT with $f_{IN1} = 70.5$ MHz and $f_{IN2} = 72.5$ MHz, $f_{SAMPLE} = 105$ MSPS

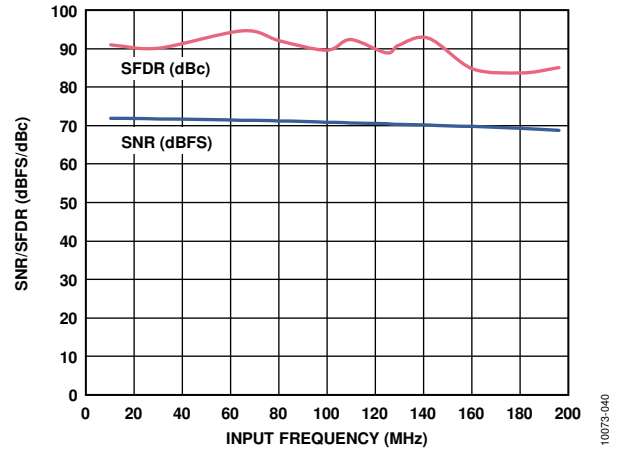


Figure 28. SNR/SFDR vs. f_{IN} , $f_{SAMPLE} = 105$ MSPS

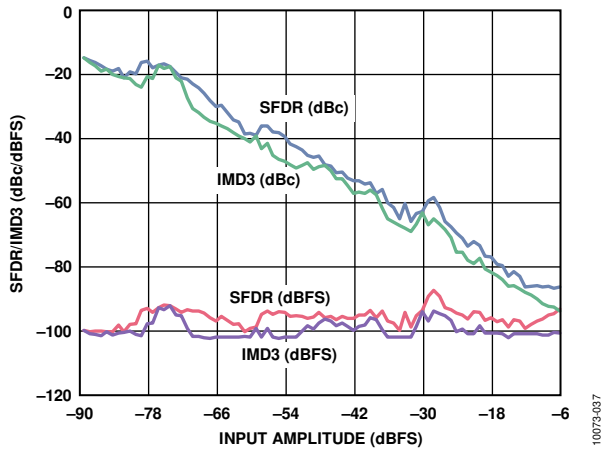


Figure 27. Two-Tone SFDR/IMD3 vs. Input Amplitude (AIN) with $f_{IN1} = 70.5$ MHz and $f_{IN2} = 72.5$ MHz, $f_{SAMPLE} = 105$ MSPS

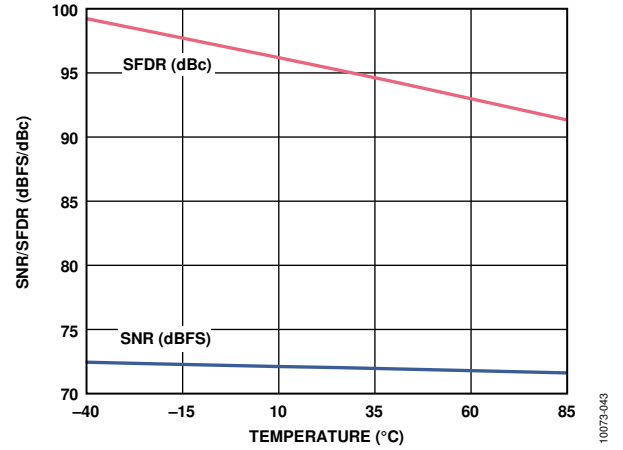


Figure 29. SNR/SFDR vs. Temperature, $f_{IN} = 10.3$ MHz, $f_{SAMPLE} = 105$ MSPS

AD9633-125

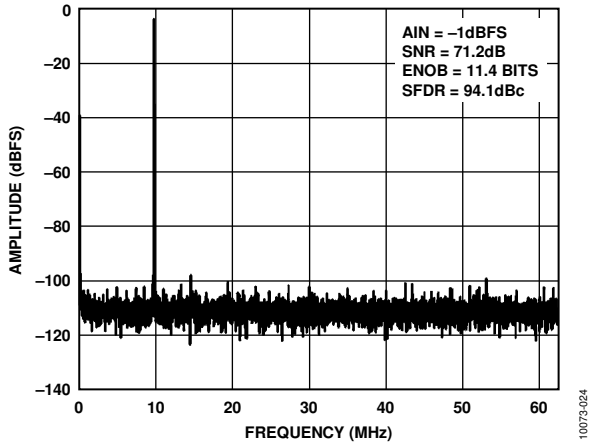


Figure 30. Single-Tone 16k FFT with $f_{IN} = 9.7$ MHz, $f_{SAMPLE} = 125$ MSPS

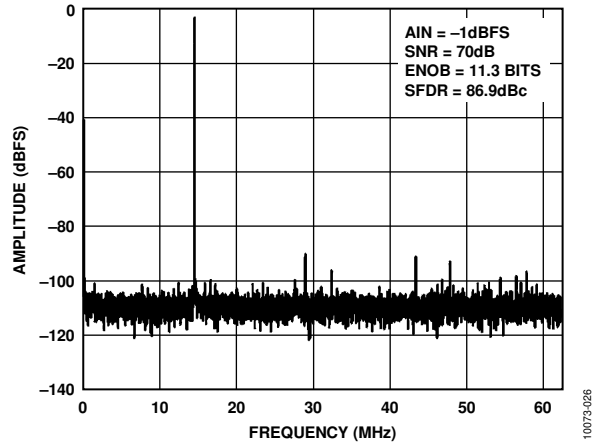


Figure 33. Single-Tone 16k FFT with $f_{IN} = 140$ MHz, $f_{SAMPLE} = 125$ MSPS

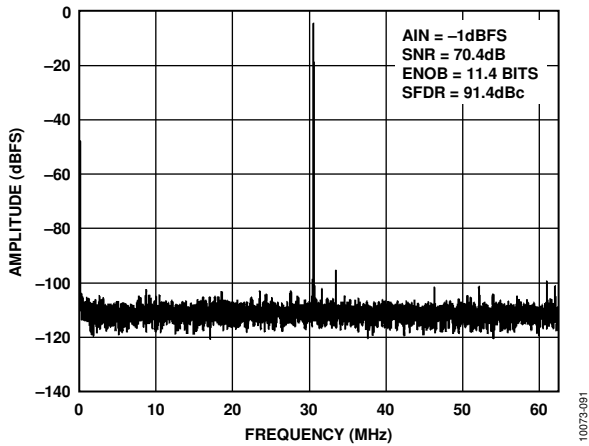


Figure 31. Single-Tone 16k FFT with $f_{IN} = 30.5$ MHz, $f_{SAMPLE} = 125$ MSPS

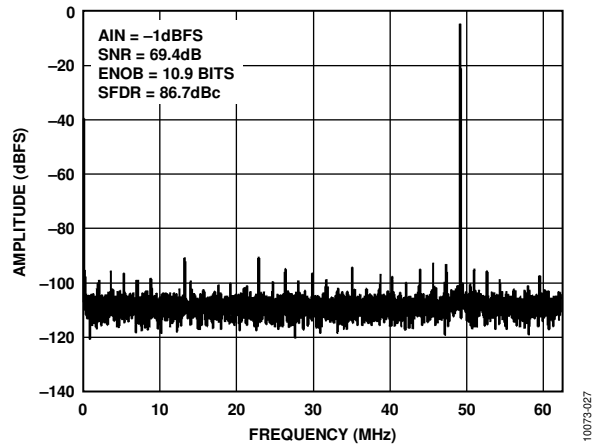


Figure 34. Single-Tone 16k FFT with $f_{IN} = 200$ MHz, $f_{SAMPLE} = 125$ MSPS

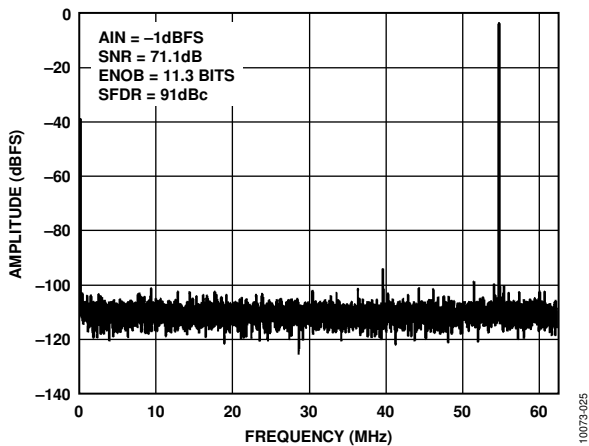


Figure 32. Single-Tone 16k FFT with $f_{IN} = 70$ MHz, $f_{SAMPLE} = 125$ MSPS

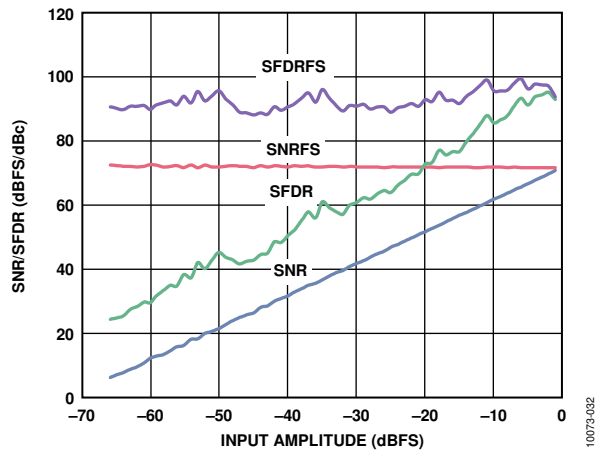


Figure 35. SNR/SFDR vs. Analog Input Level, $f_{IN} = 9.7$ MHz, $f_{SAMPLE} = 125$ MSPS

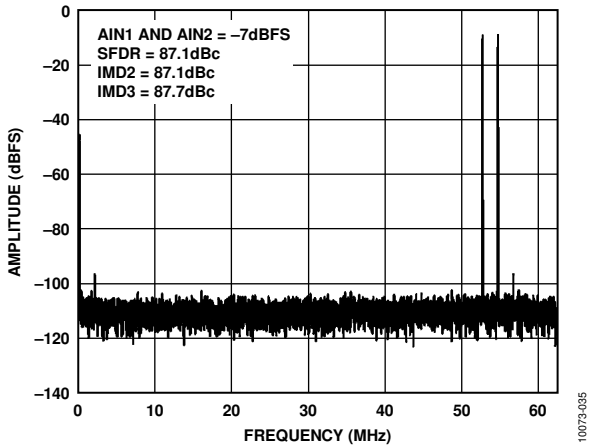


Figure 36. Two-Tone 16k FFT with $f_{IN1} = 70.5$ MHz and $f_{IN2} = 72.5$ MHz, $f_{SAMPLE} = 125$ MSPS

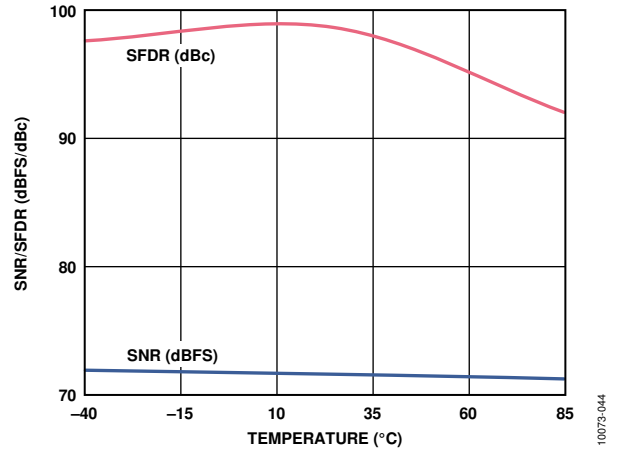


Figure 39. SNR/SFDR vs. Temperature, $f_{IN} = 10.3$ MHz, $f_{SAMPLE} = 125$ MSPS

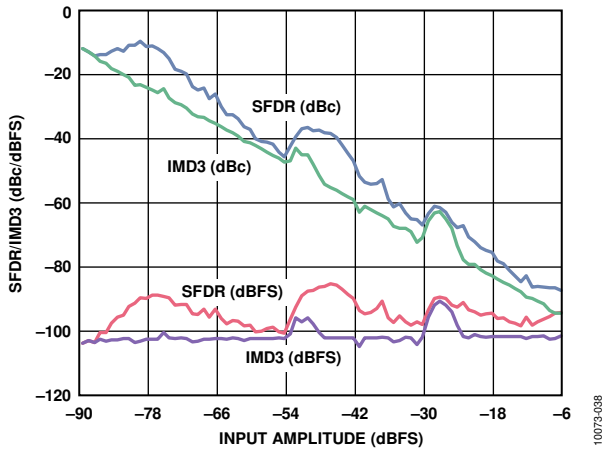


Figure 37. Two-Tone SFDR/IMD3 vs. Input Amplitude (AIN) with $f_{IN1} = 70.5$ MHz and $f_{IN2} = 72.5$ MHz, $f_{SAMPLE} = 125$ MSPS

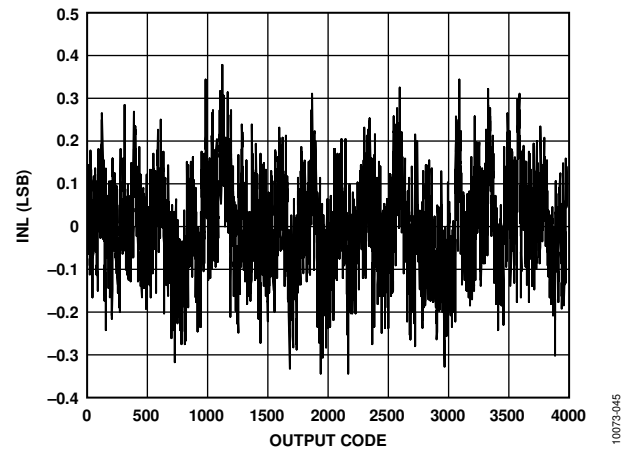


Figure 40. INL, $f_{IN} = 9.7$ MHz, $f_{SAMPLE} = 125$ MSPS

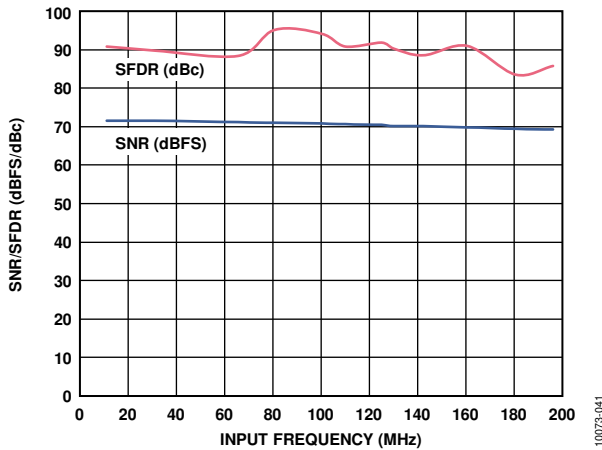


Figure 38. SNR/SFDR vs. f_{IN} , $f_{SAMPLE} = 125$ MSPS

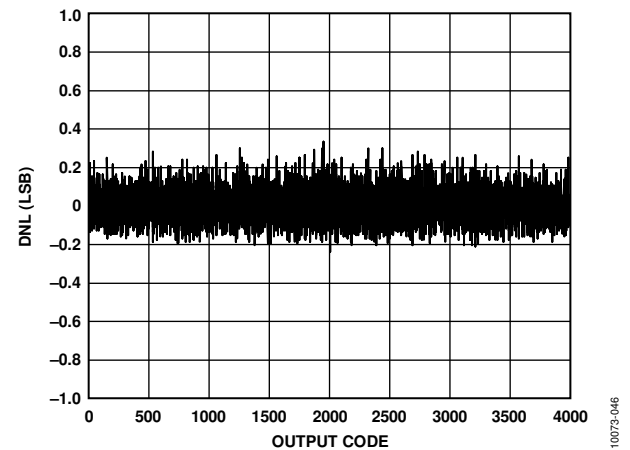


Figure 41. DNL, $f_{IN} = 9.7$ MHz, $f_{SAMPLE} = 125$ MSPS

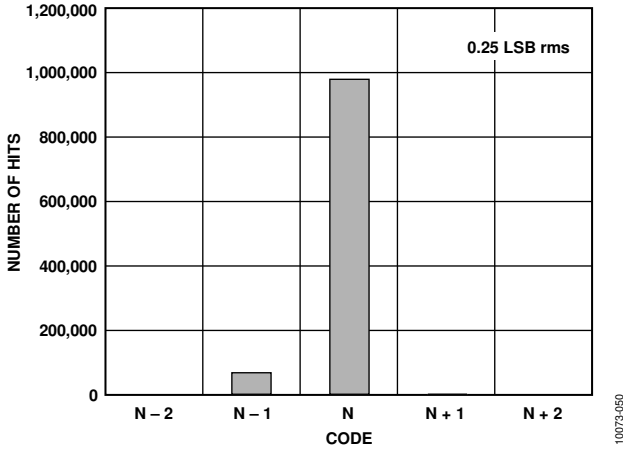


Figure 42. Input-Referred Noise Histogram, $f_{SAMPLE} = 125$ MSPS

10073-050

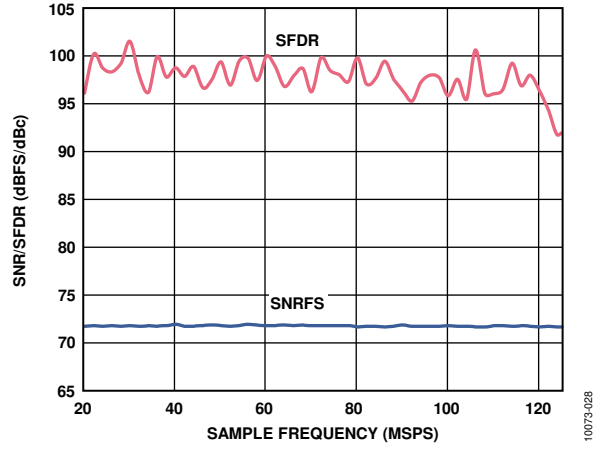


Figure 44. SNR/SFDR vs. Encode, $f_{IN} = 9.7$ MHz, $f_{SAMPLE} = 125$ MSPS

10073-028

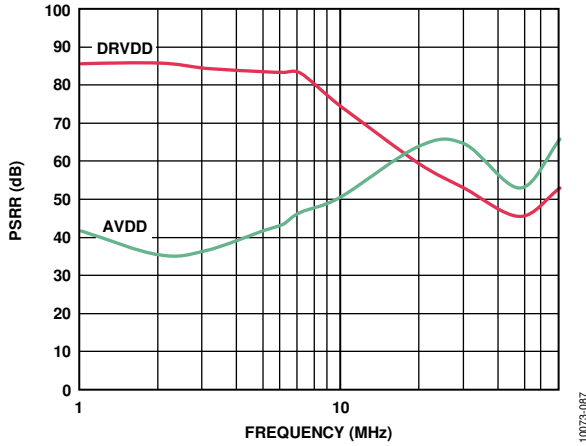


Figure 43. PSRR vs. Frequency, $f_{CLK} = 125$ MHz, $f_{SAMPLE} = 125$ MSPS

10073-087

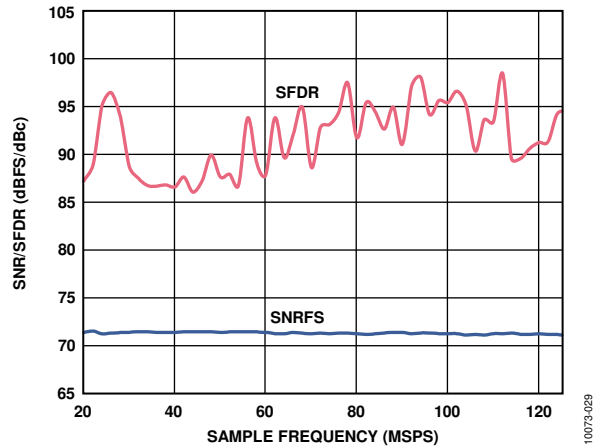


Figure 45. SNR/SFDR vs. Encode, $f_{IN} = 70$ MHz, $f_{SAMPLE} = 125$ MSPS

10073-029

EQUIVALENT CIRCUITS

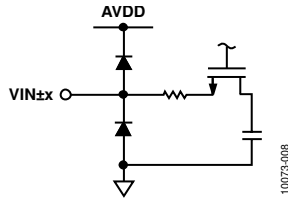


Figure 46. Equivalent Analog Input Circuit

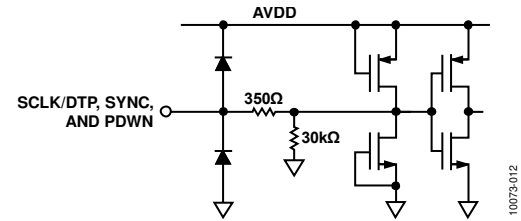


Figure 50. Equivalent SCLK/DTP, SYNC, and PDWN Input Circuit

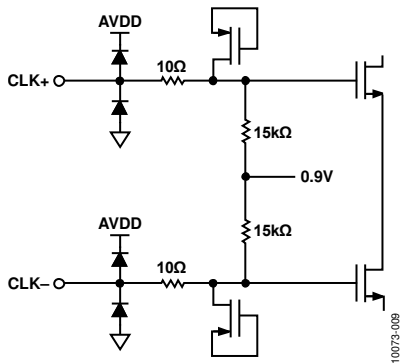


Figure 47. Equivalent Clock Input Circuit

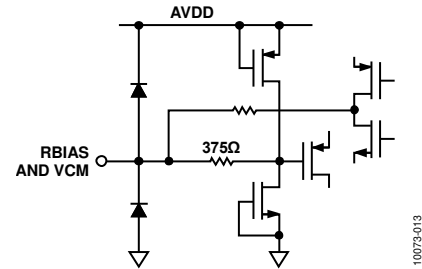


Figure 51. Equivalent RBIAS and VCM Circuit

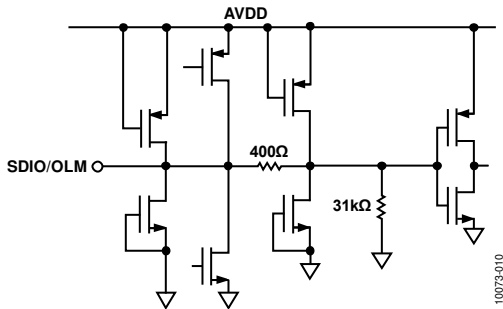


Figure 48. Equivalent SDIO/OLM Input Circuit

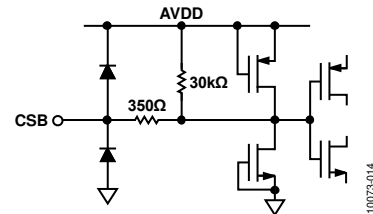


Figure 52. Equivalent CSB Input Circuit

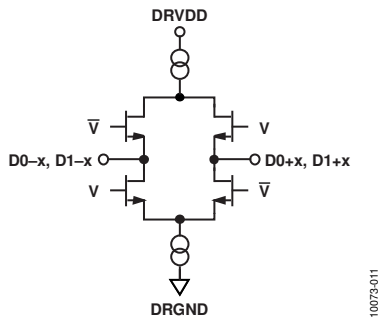


Figure 49. Equivalent Digital Output Circuit

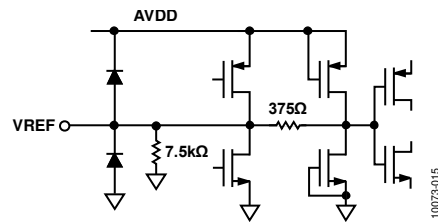


Figure 53. Equivalent VREF Circuit

THEORY OF OPERATION

The AD9633 is a multistage, pipelined ADC. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The data is then serialized and aligned to the frame and data clocks.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9633 is a differential switched-capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. By using an input common-mode voltage of midsupply, users can minimize signal-dependent errors and achieve optimum performance.

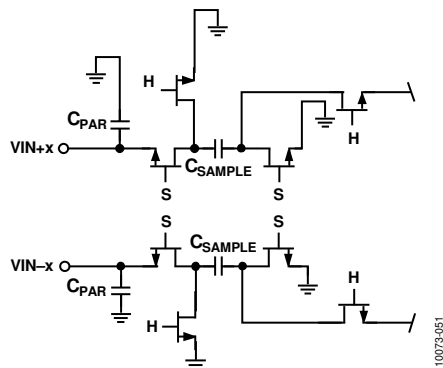


Figure 54. Switched-Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample mode and hold mode (see Figure 54). When the input circuit is switched to sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current injected from

the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and therefore achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Either a differential capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-742 Application Note, the AN-827 Application Note, and the Analog Dialogue article “Transformer-Coupled Front-End for Wideband A/D Converters” (Volume 39, April 2005) for more information. In general, the precise values depend on the application.

Input Common Mode

The analog inputs of the AD9633 are not internally dc-biased. Therefore, in ac-coupled applications, the user must provide this bias externally. Setting the device so that $V_{CM} = AVDD/2$ is recommended for optimum performance, but the device can function over a wider range with reasonable performance, as shown in Figure 55.

An on-chip, common-mode voltage reference is included in the design and is available from the VCM pin. The VCM pin must be decoupled to ground by a 0.1 μ F capacitor, as described in the Applications Information section.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9633, the largest input span available is 2 V p-p.

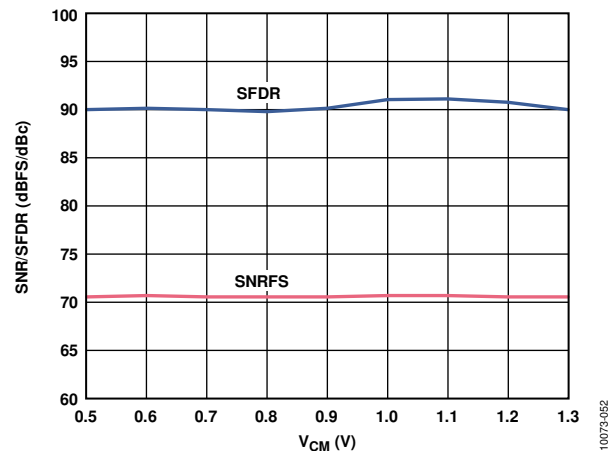


Figure 55. SNR/SFDR vs. Common-Mode Voltage, $f_{IN} = 9.7$ MHz, $f_{SAMPLE} = 125$ MSPS

Differential Input Configurations

There are several ways to drive the AD9633 either actively or passively. However, optimum performance is achieved by driving the analog inputs differentially. Using a differential double balun configuration to drive the AD9633 provides excellent performance and a flexible interface to the ADC (see Figure 57) for baseband applications.

For applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration (see Figure 58), because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9633.

Regardless of the configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

It is not recommended to drive the AD9633 inputs single-ended.

VOLTAGE REFERENCE

A stable and accurate 1.0 V voltage reference is built into the AD9633. VREF can be configured using either the internal 1.0 V reference or an externally applied 1.0 V reference voltage. The various reference modes are summarized in the Internal Reference Connection section and the External Reference Operation section. The VREF pin should be externally decoupled to ground with a low ESR, 1.0 μF capacitor in parallel with a low ESR, 0.1 μF ceramic capacitor.

Internal Reference Connection

A comparator within the AD9633 detects the potential at the SENSE pin and configures the reference into two possible modes, which are summarized in Table 9. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 56), setting VREF to 1.0 V.

Table 9. Reference Configuration Summary

Selected Mode	SENSE Voltage (V)	Resulting VREF (V)	Resulting Differential Span (V p-p)
Fixed Internal Reference	AGND to 0.2	1.0 internal	2.0
Fixed External Reference	AVDD	1.0 applied to external VREF pin	2.0

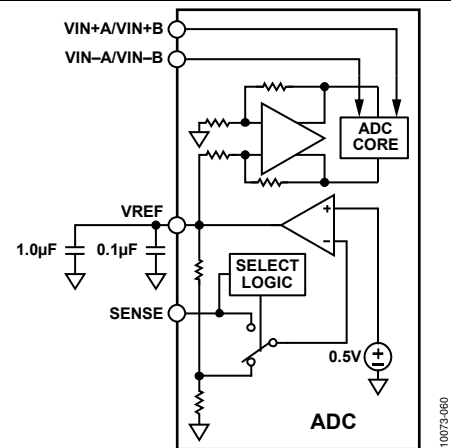


Figure 56. Internal Reference Configuration

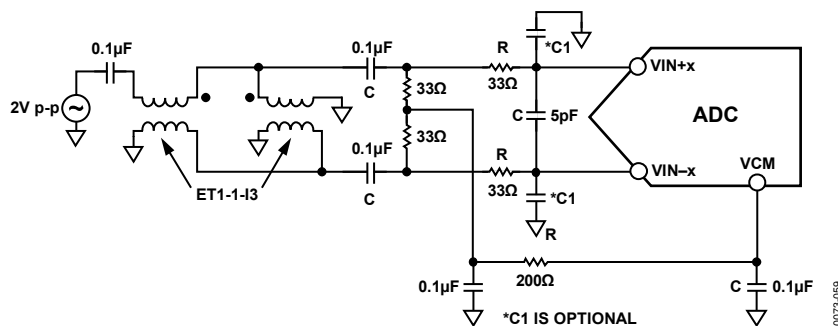


Figure 57. Differential Double Balun Input Configuration for Baseband Applications

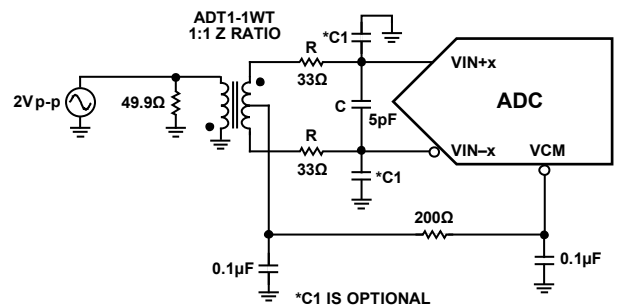


Figure 58. Differential Transformer-Coupled Configuration for Baseband Applications

If the internal reference of the AD9633 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 59 shows how the internal reference voltage is affected by loading.

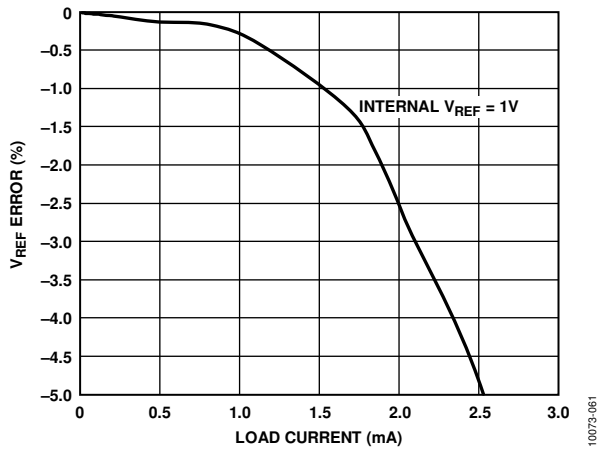


Figure 59. V_{REF} Error vs. Load Current

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 60 shows the typical drift characteristics of the internal reference in 1.0 V mode.

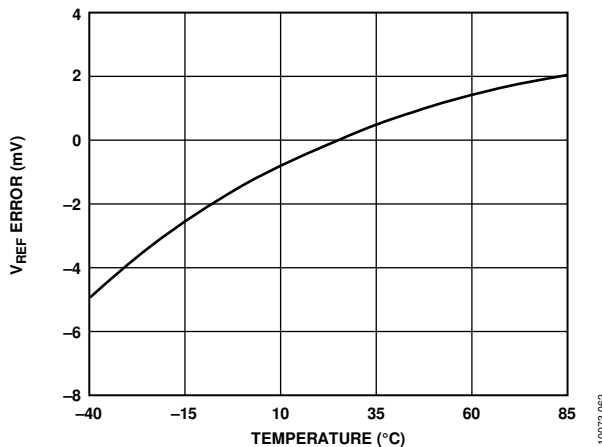


Figure 60. Typical V_{REF} Drift

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7.5 k Ω load (see Figure 53). The internal buffer generates the positive and negative full-scale references for the ADC core. Therefore, the external reference must be limited to a maximum of 1.0 V.

It is not recommended to leave the SENSE pin floating.

CLOCK INPUT CONSIDERATIONS

For optimum performance, clock the AD9633 sample clock inputs, CLK+ and CLK-, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK- pins via a transformer or capacitors. These pins are biased internally (see Figure 47) and require no external bias.

Clock Input Options

The AD9633 has a flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of the most concern, as described in the Jitter Considerations section.

Figure 61 and Figure 62 show two preferred methods for clocking the AD9633 (at clock rates up to 1 GHz prior to internal CLK divider). A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF transformer or an RF balun.

The RF balun configuration is recommended for clock frequencies between 125 MHz and 1 GHz, and the RF transformer is recommended for clock frequencies from 10 MHz to 200 MHz. The antiparallel Schottky diodes across the transformer/balun secondary winding limit clock excursions into the AD9633 to approximately 0.8 V p-p differential.

This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9633 while preserving the fast rise and fall times of the signal that are critical to achieving low jitter performance. However, the diode capacitance comes into play at frequencies above 500 MHz. Care must be taken in choosing the appropriate signal limiting diode.

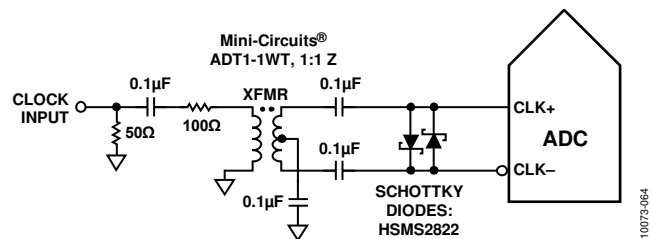


Figure 61. Transformer-Coupled Differential Clock (Up to 200 MHz)

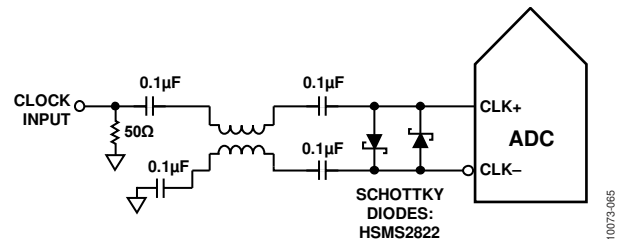


Figure 62. Balun-Coupled Differential Clock (Up to 1 GHz)

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 64. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516-0/AD9516-1/AD9516-2/AD9516-3/AD9516-4/AD9516-5/AD9517-0/AD9517-1/AD9517-2/AD9517-3/AD9517-4 clock drivers offer excellent jitter performance.

A third option is to ac couple a differential LVDS signal to the sample clock input pins, as shown in Figure 65. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516-0/AD9516-1/AD9516-2/AD9516-3/AD9516-4/AD9516-5/