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Octal, 12-Bit, 40/80 MSPS, Serial LVDS, 1.8 V Analog-to-Digital Converter

Data Sheet **AD9637**

FEATURES

- Low power: 60 mW per channel at 80 MSPS with scalable power options
- SNR = 71.5 dBFS (to Nyquist)
- SFDR = 92 dBc (to Nyquist)
- DNL = ±0.4 LSB (typical), INL = ±0.5 LSB (typical)
- Serial LVDS (ANSI-644, default)
  - Low power, reduced signal option (similar to IEEE 1596.3)
- Data and frame clock outputs
- 650 MHz full power analog bandwidth
- 2 V p-p differential input voltage range
- 1.8 V supply operation
- Serial port control
  - Full chip and individual channel power-down modes
  - Flexible bit orientation
  - Built-in and custom digital test pattern generation
  - Programmable clock and data alignment
  - Programmable output resolution
  - Standby mode

APPLICATIONS

- Medical imaging and nondestructive ultrasound
- Portable ultrasound and digital beam-forming systems
- Quadrature radio receivers
- Diversity radio receivers
- Optical networking
- Test equipment

FUNCTIONAL BLOCK DIAGRAM

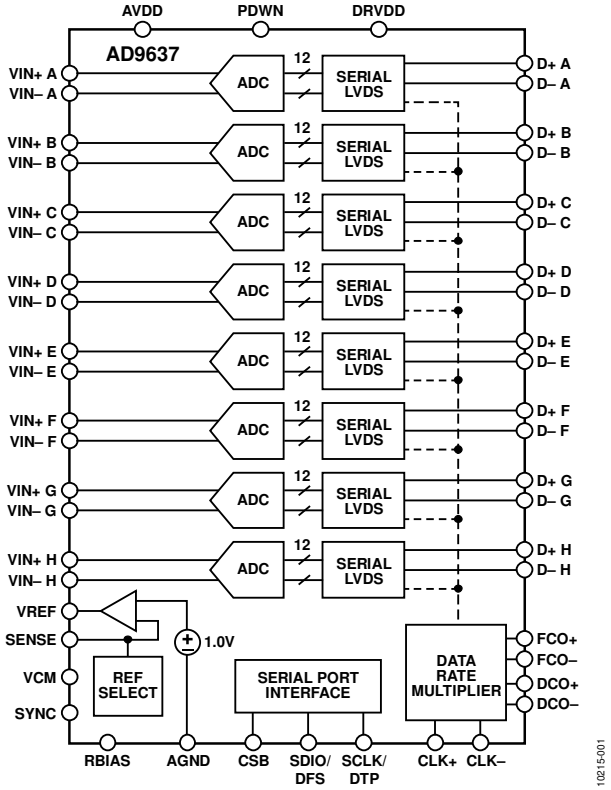

Figure 1.

GENERAL DESCRIPTION

The AD9637 is an octal, 12-bit, 40/80 MSPS analog-to-digital converter (ADC) with an on-chip sample-and-hold circuit designed for low cost, low power, small size, and ease of use. The product operates at a conversion rate of up to 80 MSPS and is optimized for outstanding dynamic performance and low power in applications where a small package size is critical.

The ADC requires a single 1.8 V power supply and LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock output (DCO) for capturing data on the output and a frame clock output (FCO) for signaling a new output byte are provided. Individual channel power-down is supported and typically consumes less than 2 mW when all channels are disabled.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

The AD9637 is available in a RoHS-compliant, 64-lead LFCSP. It is specified over the industrial temperature range of –40°C to +85°C. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Small Footprint. Eight ADCs are contained in a small, space-saving package.
2. Low Power of 60 mW/Channel at 80 MSPS with Scalable Power Options.
3. Ease of Use. A data clock output (DCO) is provided that operates at frequencies of up to 480 MHz and supports double data rate (DDR) operation.
4. User Flexibility. The SPI control offers a wide range of flexible features to meet specific system requirements.
5. Pin Compatible with the AD9257 (14-Bit Octal ADC).

Rev. A Document Feedback

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Technical Support www.analog.com

AD9637* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9637 Evaluation Board

DOCUMENTATION

Application Notes

- AN-501: Aperture Uncertainty and ADC System Performance
- AN-737: How ADIsimADC Models an ADC
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-878: High Speed ADC SPI Control Software
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD9637: Octal, 12-Bit, 40/80 MSPS, Serial LVDS,1.8 V Analog-to-Digital Converter Data Sheet

User Guides

- Evaluating the AD9257/AD9637 Analog to Digital Converters

TOOLS AND SIMULATIONS

- Visual Analog
- AD9637 IBIS Model

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9637 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9637 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

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Submit a technical question or find your regional support number.

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10/11—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, unless otherwise noted.

Table 1.

		AD9637-40			AD9637-80			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		12			12			Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	Full	−0.6	−0.3	+0.1	−0.7	−0.3	+0.1	% FSR
Offset Matching	Full	0.0	0.2	0.6	0.0	0.2	0.6	% FSR
Gain Error	Full	−8.0	−2.1	+2.0	−7.0	−3.2	+1.0	% FSR
Gain Matching	Full	−1.0	+1.7	+5.0	−1.0	+2.3	+6.0	% FSR
Differential Nonlinearity (DNL)	Full	−0.8	±0.3	+0.8	−0.8	±0.4	+0.8	LSB
Integral Nonlinearity (INL)	Full	−1.0	±0.4	+1.0	−1.2	±0.5	+1.2	LSB
TEMPERATURE DRIFT								
Offset Error	Full		±2			±2		ppm/°C
INTERNAL VOLTAGE REFERENCE								
Output Voltage (1 V Mode)	Full	0.98	0.99	1.01	0.98	0.99	1.01	V
Load Regulation at 1.0 mA (V_{REF} = 1 V)	Full		2			2		mV
Input Resistance	Full		7.5			7.5		kΩ
INPUT REFERRED NOISE								
V_{REF} = 1.0 V	25°C		0.36			0.49		LSB rms
ANALOG INPUTS								
Differential Input Voltage (V_{REF} = 1 V)	Full		2			2		V p-p
Common-Mode Voltage	Full		0.9			0.9		V
Common-Mode Range	Full	0.5		1.3	0.5		1.3	V
Differential Input Resistance			5.2			5.2		kΩ
Differential Input Capacitance	Full		3.5			3.5		pF
POWER SUPPLY								
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
I_{AVDD} (Eight Channels)	Full		142	151		221	234	mA
I_{DRVDD} (Eight Channels, ANSI-644 Mode)	Full		51	79		58	85	mA
I_{DRVDD} (Eight Channels, Reduced Range Mode)	25°C		36			43		mA
TOTAL POWER CONSUMPTION								
Total Power Dissipation (Eight Channels, ANSI-644 Mode)	Full		347	414		502	574	mW
Total Power Dissipation (Eight Channels, Reduced Range Mode)	25°C		320			475		mW
Power-Down Dissipation	25°C		1			1		mW
Standby Dissipation[2]	25°C		72			98		mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Can be controlled via the SPI.

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, unless otherwise noted. CLK divider = 8 used for typical characteristics at input frequency ≥ 19.7 MHz.

Table 2.

		AD9637-40			AD9637-80			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE RATIO (SNR)								
f_{IN} = 9.7 MHz	25°C		72.0			71.5		dBFS
f_{IN} = 19.7 MHz	Full	70.0	72.0		71.0	71.5		dBFS
f_{IN} = 30.5 MHz	25°C		71.9			71.5		dBFS
f_{IN} = 63.5 MHz	25°C					71.4		dBFS
f_{IN} = 69.5 MHz	25°C		71.5					dBFS
f_{IN} = 123.5 MHz	25°C					70.5		dBFS
SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)								
f_{IN} = 9.7 MHz	25°C		71.9			71.5		dBFS
f_{IN} = 19.7 MHz	Full	69.0	71.9		70.0	71.5		dBFS
f_{IN} = 30.5 MHz	25°C		71.9			71.5		dBFS
f_{IN} = 63.5 MHz	25°C					71.3		dBFS
f_{IN} = 69.5 MHz	25°C		71.4					dBFS
f_{IN} = 123.5 MHz	25°C					70.4		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)								
f_{IN} = 9.7 MHz	25°C		11.7			11.6		Bits
f_{IN} = 19.7 MHz	Full	11.2	11.7		11.3	11.6		Bits
f_{IN} = 30.5 MHz	25°C		11.7			11.6		Bits
f_{IN} = 63.5 MHz	25°C					11.6		Bits
f_{IN} = 69.5 MHz	25°C		11.6					Bits
f_{IN} = 123.5 MHz	25°C					11.4		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
f_{IN} = 9.7 MHz	25°C		96			93		dBc
f_{IN} = 19.7 MHz	Full	78	96		78	92		dBc
f_{IN} = 30.5 MHz	25°C		96			92		dBc
f_{IN} = 63.5 MHz	25°C					92		dBc
f_{IN} = 69.5 MHz	25°C		89					dBc
f_{IN} = 123.5 MHz	25°C					88		dBc
WORST HARMONIC (SECOND OR THIRD)								
f_{IN} = 9.7 MHz	25°C		−99			−93		dBc
f_{IN} = 19.7 MHz	Full		−96	−78		−92	−78	dBc
f_{IN} = 30.5 MHz	25°C		−98			−92		dBc
f_{IN} = 63.5 MHz	25°C					−92		dBc
f_{IN} = 69.5 MHz	25°C		−89					dBc
f_{IN} = 123.5 MHz	25°C					−88		dBc
WORST OTHER (EXCLUDING SECOND OR THIRD)								
f_{IN} = 9.7 MHz	25°C		−96			−97		dBc
f_{IN} = 19.7 MHz	Full		−98	−86		−97	−86	dBc
f_{IN} = 30.5 MHz	25°C		−96			−97		dBc
f_{IN} = 63.5 MHz	25°C					−96		dBc
f_{IN} = 69.5 MHz	25°C		−97					dBc
f_{IN} = 123.5 MHz	25°C					−92		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)—AIN1 AND AIN2 = −7.0 dBFS								
f_{IN1} = 8 MHz, f_{IN2} = 10 MHz	25°C		93					dBc
f_{IN1} = 30 MHz, f_{IN2} = 32 MHz	25°C					85		dBc

Parameter[1]	Temp	AD9637-40	AD9637-80	Unit
CROSSTALK[2]	25°C	−98	−96	dB
Crosstalk (Overrange Condition)[3]	25°C	−89	−89	dB
ANALOG INPUT BANDWIDTH, FULL POWER	25°C	650	650	MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Crosstalk is measured at 10 MHz with −1.0 dBFS analog input on one channel and no input on the adjacent channel.
[3] Overrange condition is 3 dB above the full-scale input range.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, unless otherwise noted.

Table 3.

Parameter[1]	Temp	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	0.2		3.6	V p-p
Input Voltage Range	Full	AGND − 0.2		AVDD + 0.2	V
Input Common-Mode Voltage	Full		0.9		V
Input Resistance (Differential)	25°C		15		kΩ
Input Capacitance	25°C		4		pF
LOGIC INPUTS (PDWN, SYNC, SCLK)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		2		pF
LOGIC INPUT (CSB)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		2		pF
LOGIC INPUT (SDIO)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		5		pF
LOGIC OUTPUT (SDIO)[3]					
Logic 1 Voltage (I_{OH} = 800 µA)	Full		1.79		V
Logic 0 Voltage (I_{OL} = 50 µA)	Full			0.05	V
DIGITAL OUTPUTS (D± x), ANSI-644					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	247	350	454	mV
Output Offset Voltage (V_{OS})	Full	1.13	1.21	1.38	V
Output Coding (Default)			Twos complement		
DIGITAL OUTPUTS (D± x), LOW POWER, REDUCED SIGNAL OPTION					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	150	200	250	mV
Output Offset Voltage (V_{OS})	Full	1.13	1.21	1.38	V
Output Coding (Default)			Twos complement		

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] This is specified for LVDS and LVPECL only.
[3] This is specified for 13 SDIO/DFS pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, unless otherwise noted.

Table 4.

Parameter[1, 2]	Temp	Min	Typ	Max	Unit
CLOCK[3]					
Input Clock Rate	Full	10		640	MHz
Conversion Rate	Full	10		40/80	MSPS
Clock Pulse Width High (t_{EH})	Full		12.5/6.25		ns
Clock Pulse Width Low (t_{EL})	Full		12.5/6.25		ns
OUTPUT PARAMETERS[3]					
Propagation Delay (t_{PD})	Full	1.5	2.3	3.1	ns
Rise Time (t_R) (20% to 80%)	Full		300		ps
Fall Time (t_F) (20% to 80%)	Full		300		ps
FCO Propagation Delay (t_{FCO})	Full	1.5	2.3	3.1	ns
DCO Propagation Delay (t_{CPD})[4]	Full		t_{FCO} + (t_{SAMPLE}/24)		ns
DCO to Data Delay (t_{DATA})[4]	Full	(t_{SAMPLE}/24) − 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	ps
DCO to FCO Delay (t_{FRAME})[4]	Full	(t_{SAMPLE}/24) − 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	ps
Data to Data Skew ($t_{DATA-MAX}$ − $t_{DATA-MIN}$)	Full		±50	±200	ps
Wake-Up Time (Standby)	25°C		35		µs
Wake-Up Time (Power-Down)[5]	25°C		375		µs
Pipeline Latency	Full		16		Clock cycles
APERTURE					
Aperture Delay (t_A)	25°C		1		ns
Aperture Uncertainty (Jitter)	25°C		0.1		ps rms
Out-of-Range Recovery Time	25°C		1		Clock cycles

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Measured on standard FR-4 material.
[3] Can be adjusted via the SPI.
[4] t_{SAMPLE}/24 is based on the number of bits divided by 2 because the delays are based on half duty cycles. $t_{SAMPLE} = 1/f_S$.
[5] Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Description	Limit	Unit
SYNC TIMING REQUIREMENTS			
t_{SSYNC}	SYNC to rising edge of CLK+ setup time	0.24	ns typ
t_{HSYNC}	SYNC to rising edge of CLK+ hold time	0.40	ns typ
SPI TIMING REQUIREMENTS	See Figure 61		
t_{DS}	Setup time between the data and the rising edge of SCLK	2	ns min
t_{DH}	Hold time between the data and the rising edge of SCLK	2	ns min
t_{CLK}	Period of the SCLK	40	ns min
t_S	Setup time between CSB and SCLK	2	ns min
t_H	Hold time between CSB and SCLK	2	ns min
t_{HIGH}	SCLK pulse width high	10	ns min
t_{LOW}	SCLK pulse width low	10	ns min
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 61)	10	ns min
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 61)	10	ns min

Timing Diagrams

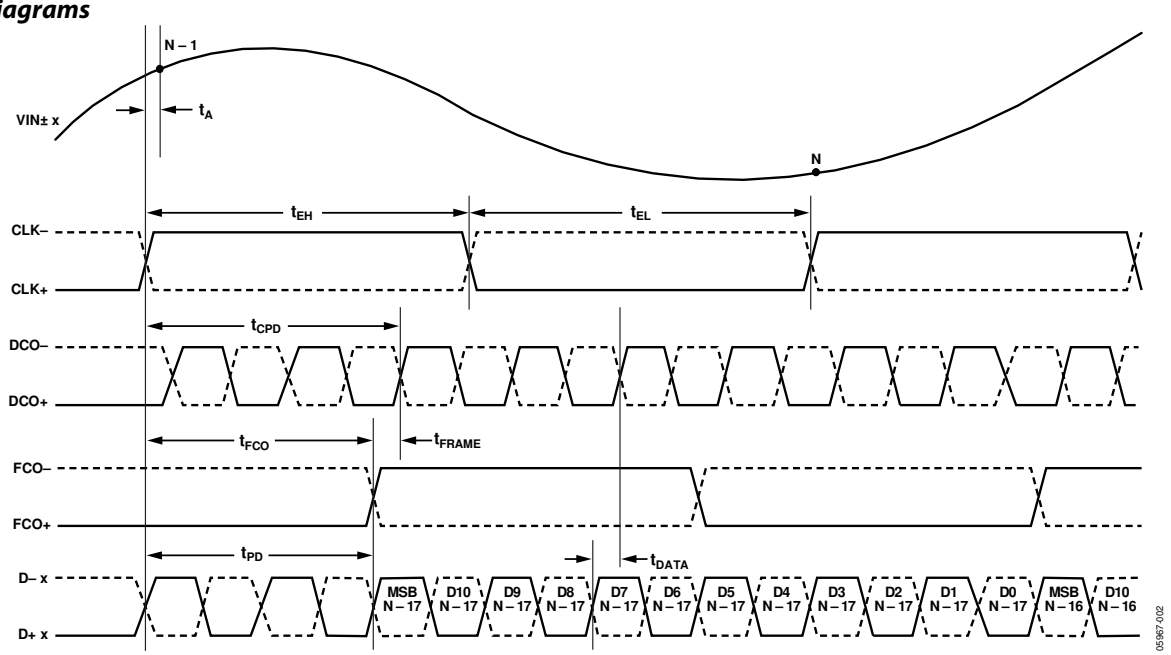


Figure 2. Word-Wise DDR, 1× Frame, 12-Bit Output Mode (Default)

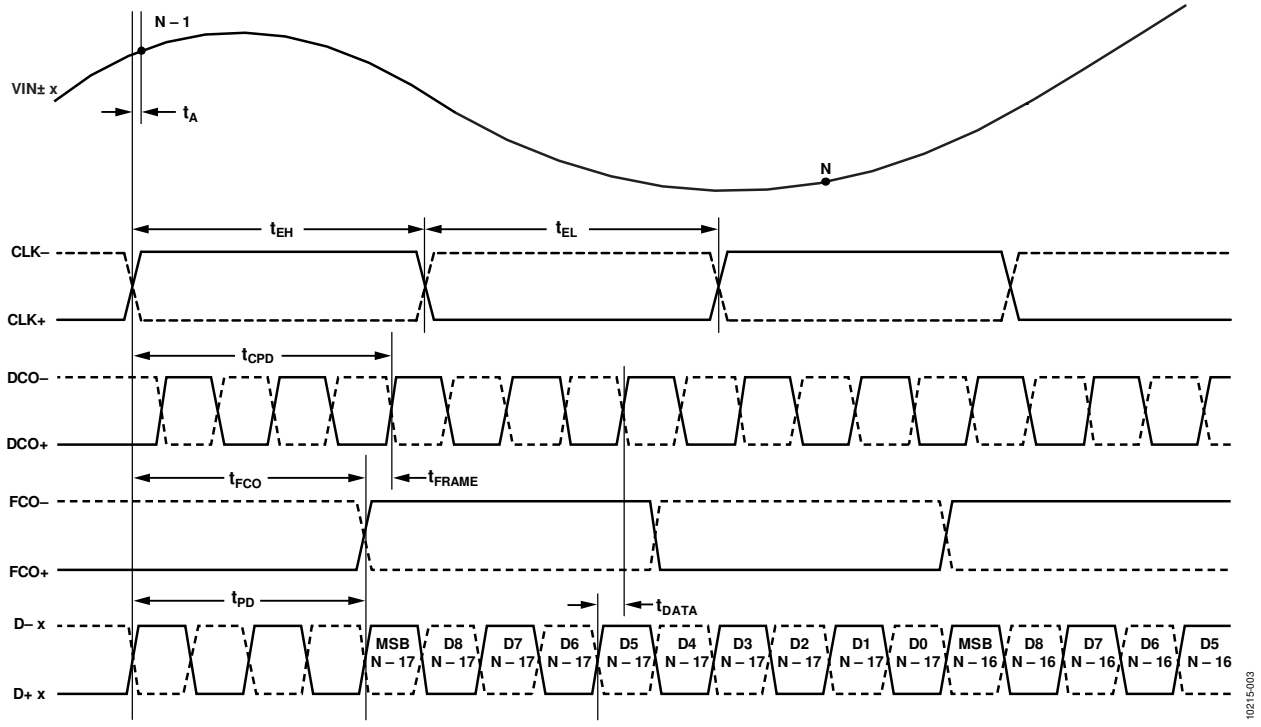


Figure 3. Word-Wise DDR, 1× Frame, 10-Bit Output Mode

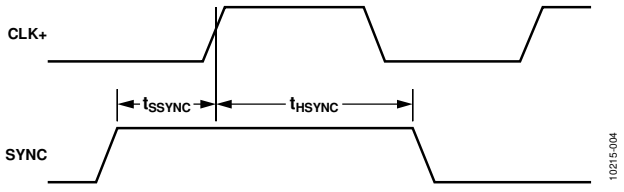


Figure 4. SYNC Input Timing Requirements

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
Digital Outputs (D± x, DCO+, DCO−, FCO+, FCO−) to AGND	−0.3 V to +2.0 V
CLK+, CLK− to AGND	−0.3 V to +2.0 V
VIN+ x, VIN− x to AGND	−0.3 V to +2.0 V
SCLK/DTP, SDIO/DFS, CSB to AGND	−0.3 V to +2.0 V
SYNC, PDWN to AGND	−0.3 V to +2.0 V
RBIAS to AGND	−0.3 V to +2.0 V
VREF, SENSE to AGND	−0.3 V to +2.0 V
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the printed circuit board (PCB) increases the reliability of the solder joints and maximizes the thermal capability of the package.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JC}[1, 3]	θ_{JB}[1, 4]	Ψ_{JT}[1, 2]	Unit
64-Lead LFCSP 9 mm × 9 mm (CP-64-4)	0	22.3	1.4	N/A	0.1	°C/W
	1.0	19.5	N/A	11.8	0.2	°C/W
	2.5	17.5	N/A	N/A	0.2	°C/W

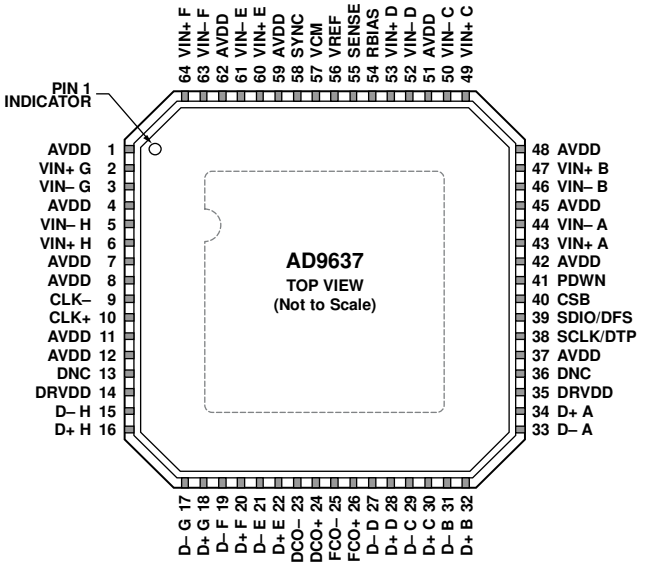
[1] Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. As shown Table 7, airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED PAD MUST BE CONNECTED TO ANALOG GROUND.

10215-005

Figure 5. Pin Configuration, Top View

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
0, EP	AGND, Exposed Pad	Analog Ground, Exposed Pad. The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to analog ground for proper operation.
1, 4, 7, 8, 11, 12, 37, 42, 45, 48, 51, 59, 62	AVDD	1.8 V Analog Supply.
13, 36	DNC	Do Not Connect. Do not connect to this pin.
14, 35	DRVDD	1.8 V Digital Output Driver Supply.
2, 3	VIN+ G, VIN– G	ADC G Analog Input True, ADC G Analog Input Complement.
5, 6	VIN– H, VIN+ H	ADC H Analog Input Complement, ADC H Analog Input True.
9, 10	CLK–, CLK+	Input Clock Complement, Input Clock True.
15, 16	D– H, D+ H	ADC H Digital Output Complement, ADC H Digital Output True.
17, 18	D– G, D+ G	ADC G Digital Output Complement, ADC G Digital Output True.
19, 20	D– F, D+ F	ADC F Digital Output Complement, ADC F Digital Output True.
21, 22	D– E, D+ E	ADC E Digital Output Complement, ADC E Digital Output True.
23, 24	DCO–, DCO+	Data Clock Digital Output Complement, Data Clock Digital Output True.
25, 26	FCO–, FCO+	Frame Clock Digital Output Complement, Frame Clock Digital Output True.
27, 28	D– D, D+ D	ADC D Digital Output Complement, ADC D Digital Output True.
29, 30	D– C, D+ C	ADC C Digital Output Complement, ADC C Digital Output True.
31, 32	D– B, D+ B	ADC B Digital Output Complement, ADC B Digital Output True.
33, 34	D– A, D+ A	ADC A Digital Output Complement, ADC A Digital Output True.
38	SCLK/DTP	Serial Clock (SCLK)/Digital Test Pattern (DTP).
39	SDIO/DFS	Serial Data Input/Output (SDIO)/Data Format Select (DFS).
40	CSB	Chip Select Bar.
41	PDWN	Power-Down.
43, 44	VIN+ A, VIN– A	ADC A Analog Input True, ADC A Analog Input Complement.
46, 47	VIN– B, VIN+ B	ADC B Analog Input Complement, ADC B Analog Input True.
49, 50	VIN+ C, VIN– C	ADC C Analog Input True, ADC C Analog Input Complement.

Pin No.	Mnemonic	Description
52, 53	VIN− D, VIN+ D	ADC D Analog Input Complement, ADC D Analog Input True.
54	RBIAS	Sets analog current bias. Connect to 10 kΩ (1% tolerance) resistor to ground.
55	SENSE	Reference Mode Selection.
56	VREF	Voltage Reference Input/Output.
57	VCM	Analog Output Voltage at Midsupply. Sets common mode of the analog inputs.
58	SYNC	Digital Input. SYNC input to clock divider. 30 kΩ internal pull-down.
60, 61	VIN+ E, VIN− E	ADC E Analog Input True, ADC E Analog Input Complement.
63, 64	VIN− F, VIN+ F	ADC F Analog Input Complement, ADC F Analog Input True.

TYPICAL PERFORMANCE CHARACTERISTICS

AD9637-80

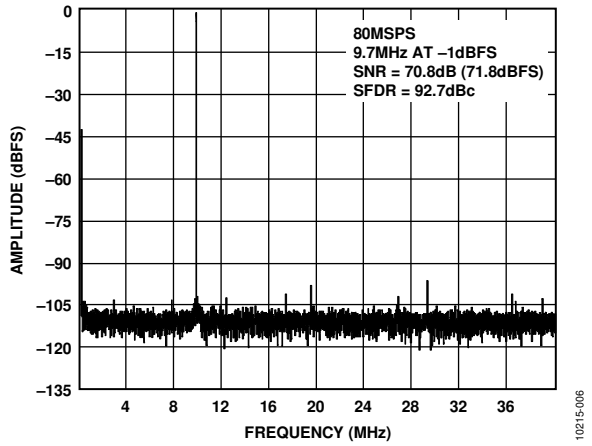


Figure 6. Single-Tone 16k FFT with f_{IN} = 9.7 MHz, f_{SAMPLE} = 80 MSPS

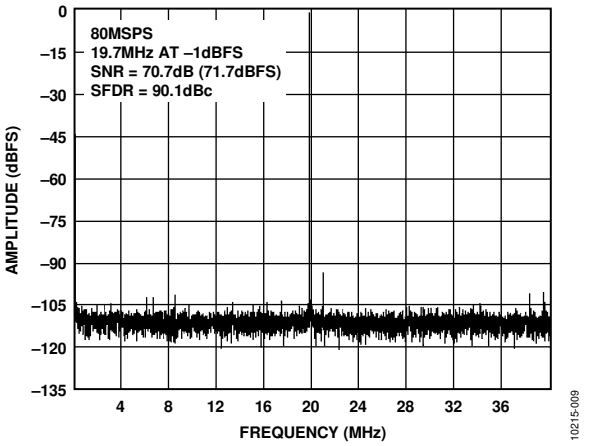


Figure 9. Single-Tone 16k FFT with f_{IN} = 19.7 MHz, f_{SAMPLE} = 80 MSPS, CLK Divider = 8

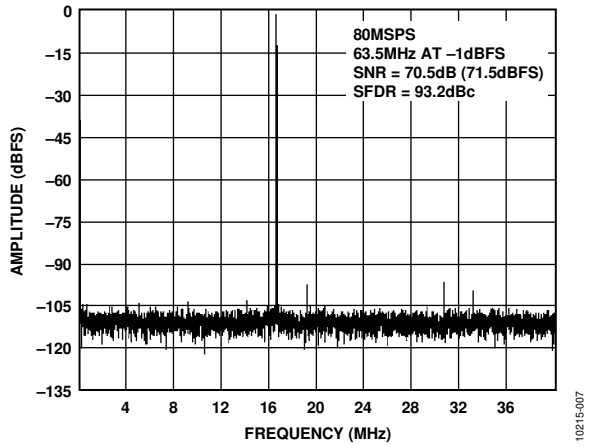


Figure 7. Single-Tone 16k FFT with f_{IN} = 63.5 MHz, f_{SAMPLE} = 80 MSPS, CLK Divider = 8

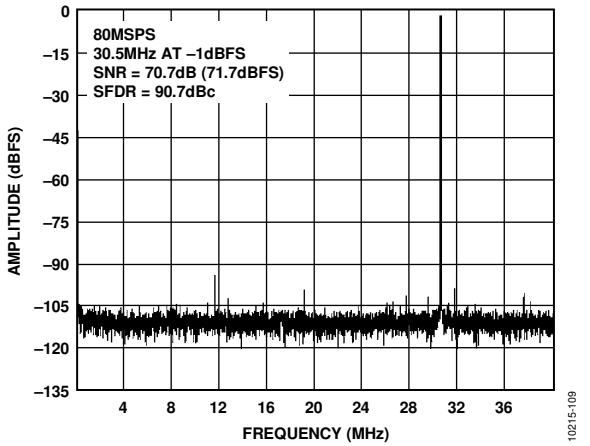


Figure 10. Single-Tone 16k FFT with f_{IN} = 30.5 MHz, f_{SAMPLE} = 80 MSPS, CLK Divider = 8

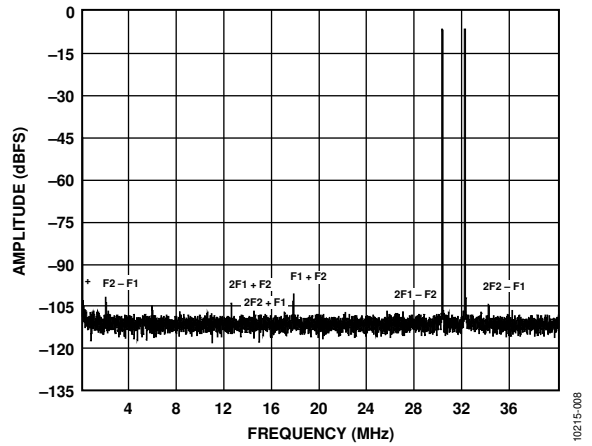


Figure 8. Two-Tone 16k FFT with f_{IN1} = 30 MHz and f_{IN2} = 32 MHz, f_{SAMPLE} = 80 MSPS

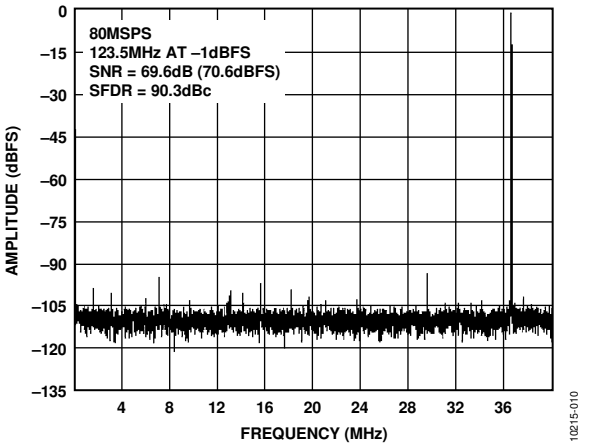


Figure 11. Single-Tone 16k FFT with f_{IN} = 123.5 MHz, f_{SAMPLE} = 80 MSPS, CLK Divider = 8

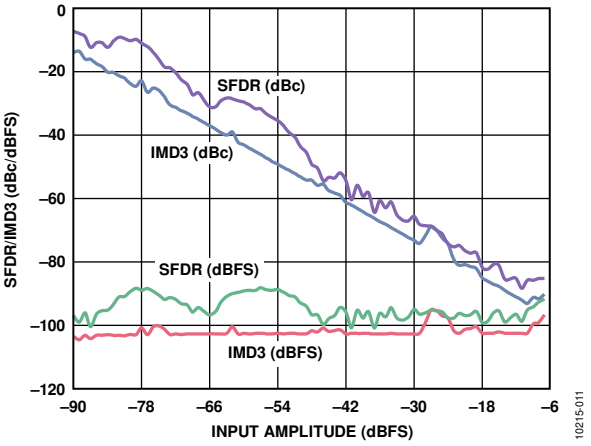


Figure 12. Two-Tone SFDR/IMD3 vs. Input Amplitude (AIN) with f_{IN1} = 30 MHz and f_{IN2} = 32 MHz, f_{SAMPLE} = 80 MSPS

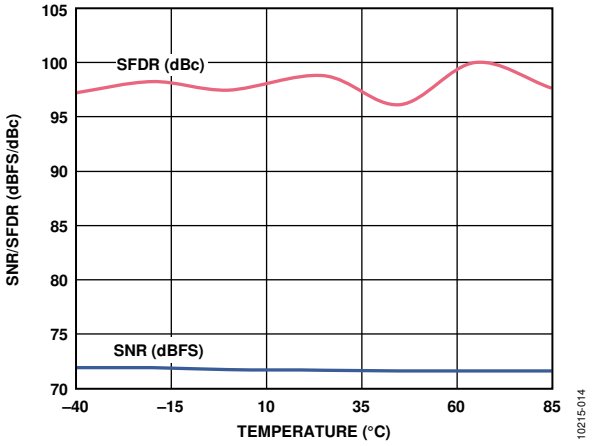


Figure 15. SNR/SFDR vs. Temperature, f_{IN} = 9.7 MHz, f_{SAMPLE} = 80 MSPS

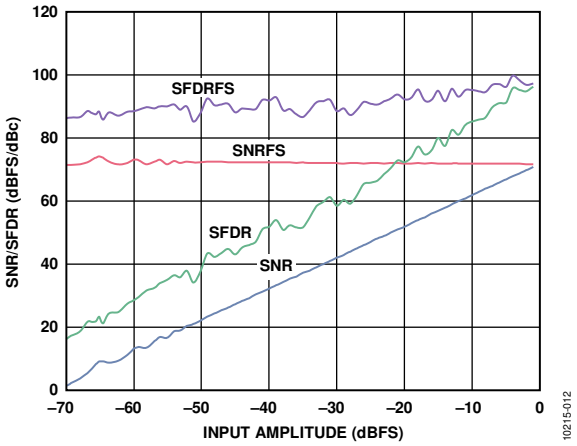


Figure 13. SNR/SFDR vs. Analog Input Level, f_{IN} = 9.7 MHz, f_{SAMPLE} = 80 MSPS

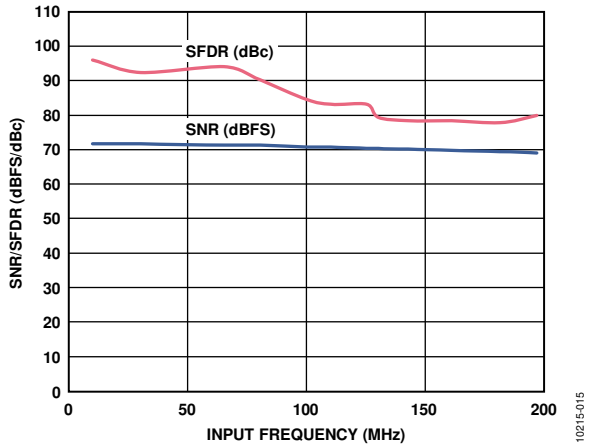


Figure 16. SNR/SFDR vs. f_{IN}, f_{SAMPLE} = 80 MSPS

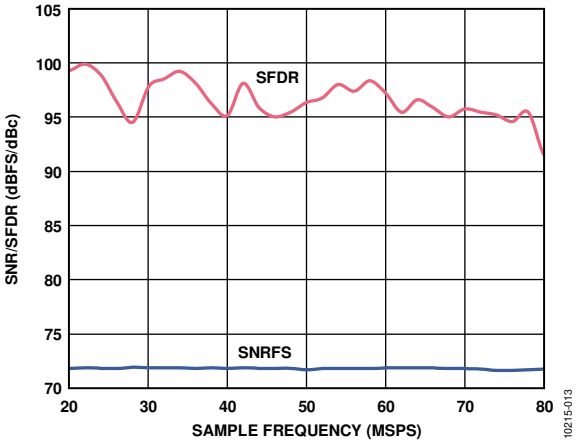


Figure 14. SNR/SFDR vs. Encode, f_{IN} = 19.7 MHz

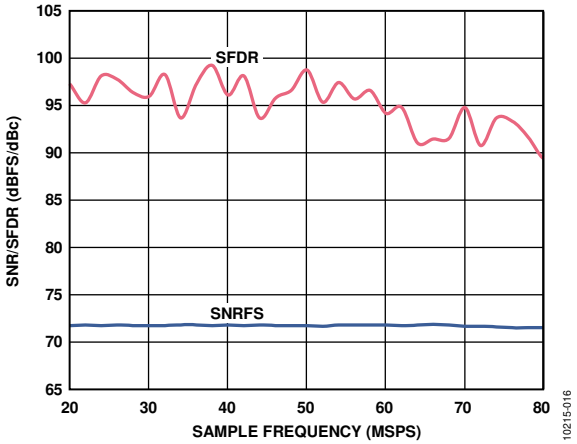


Figure 17. SNR/SFDR vs. Encode, f_{IN} = 30.5 MHz

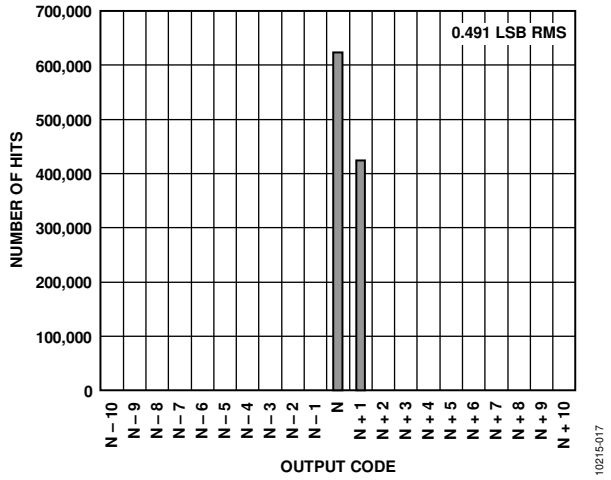


Figure 18. Input Referred Noise Histogram, f_{SAMPLE} = 80 MSPS

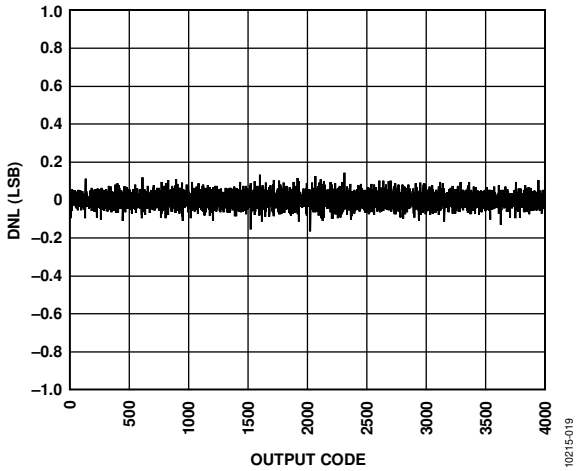


Figure 20. DNL, f_{IN} = 9.7 MHz, f_{SAMPLE} = 80 MSPS

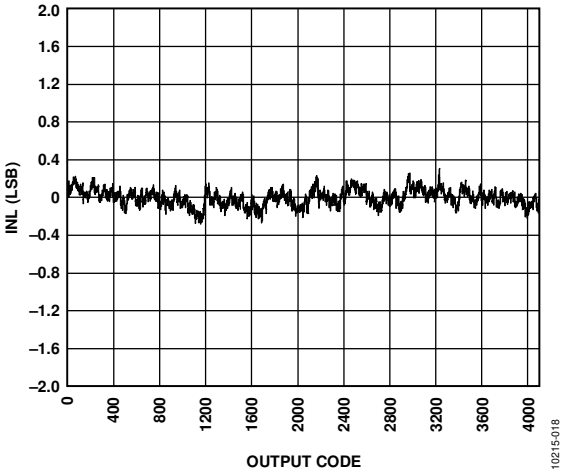


Figure 19. INL, f_{IN} = 9.7 MHz, f_{SAMPLE} = 80 MSPS

AD9637-40

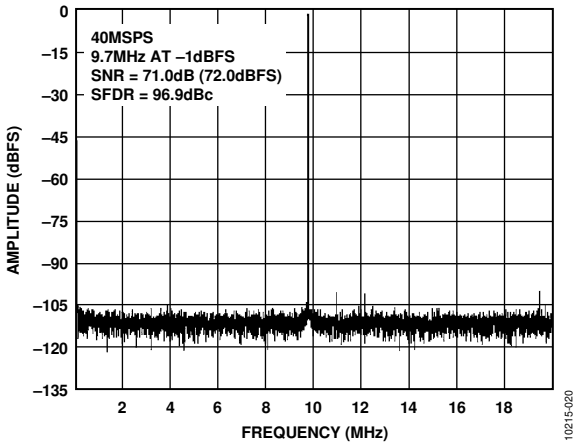


Figure 21. Single-Tone 16k FFT with f_{IN} = 9.7 MHz, f_{SAMPLE} = 40 MSPS

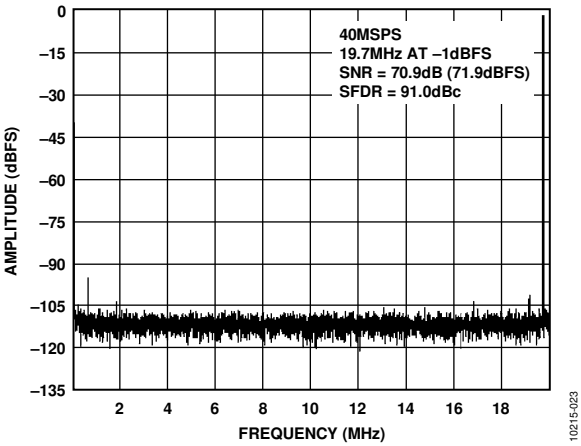


Figure 24. Single-Tone 16k FFT with f_{IN} = 19.7 MHz, f_{SAMPLE} = 40 MSPS, CLK Divider = 8

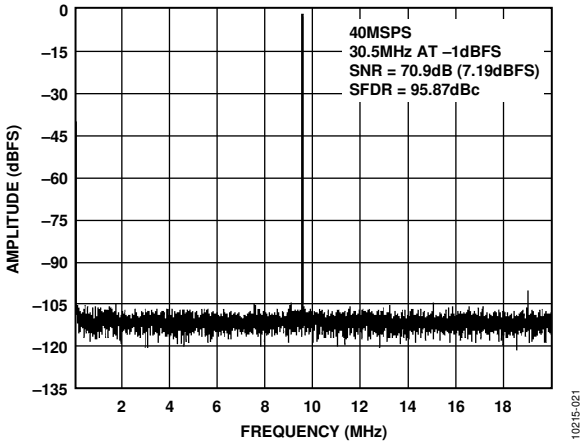


Figure 22. Single-Tone 16k FFT with f_{IN} = 30.5 MHz, f_{SAMPLE} = 40 MSPS , CLK Divider = 8

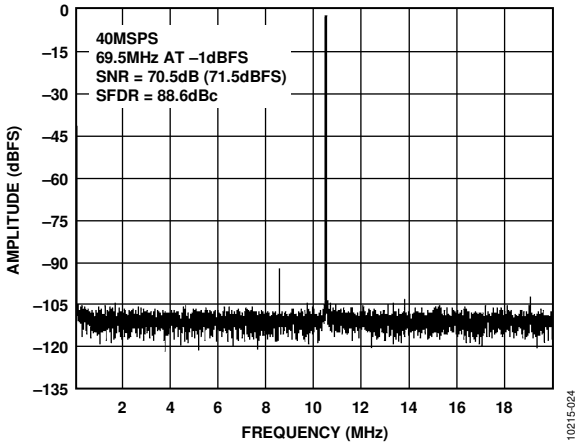


Figure 25. Single-Tone 16k FFT with f_{IN} = 69.5 MHz, f_{SAMPLE} = 40 MSPS, CLK Divider = 8

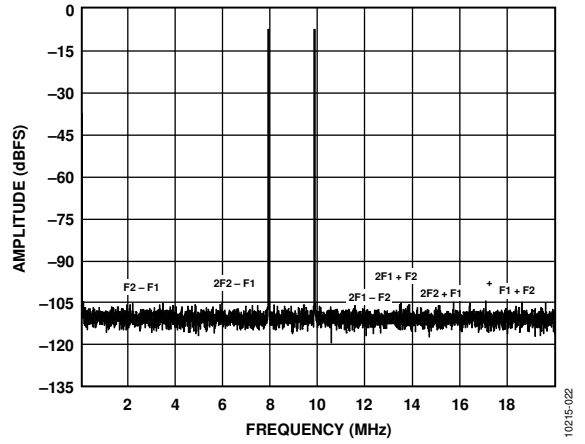


Figure 23. Two-Tone 16k FFT with f_{IN1} = 8 MHz and f_{IN2} = 10 MHz, f_{SAMPLE} = 40 MSPS

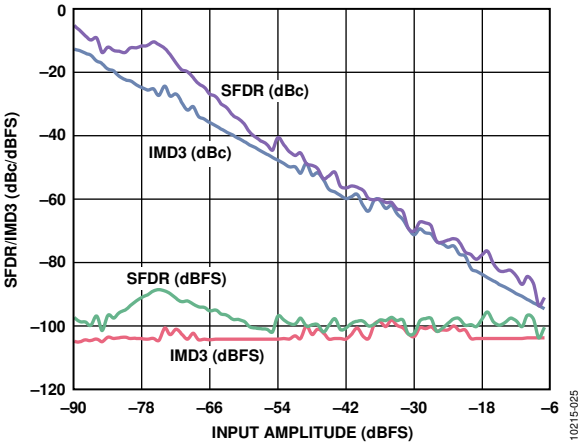


Figure 26. Two-Tone SFDR/IMD3 vs. Input Amplitude (AIN) with f_{IN1} = 30 MHz and f_{IN2} = 32 MHz, f_{SAMPLE} = 40 MSPS

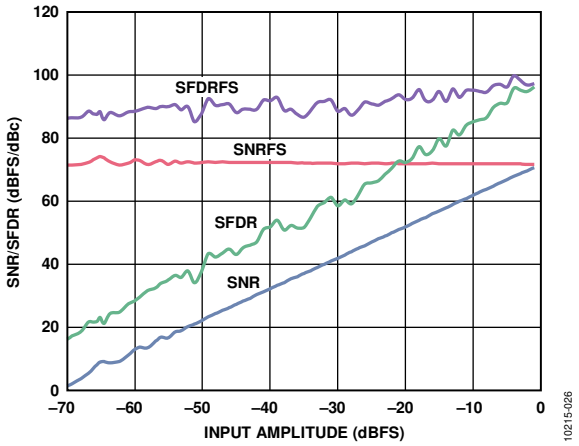


Figure 27. SNR/SFDR vs. Analog Input Level, f_{IN} = 9.7 MHz, f_{SAMPLE} = 40 MSPS

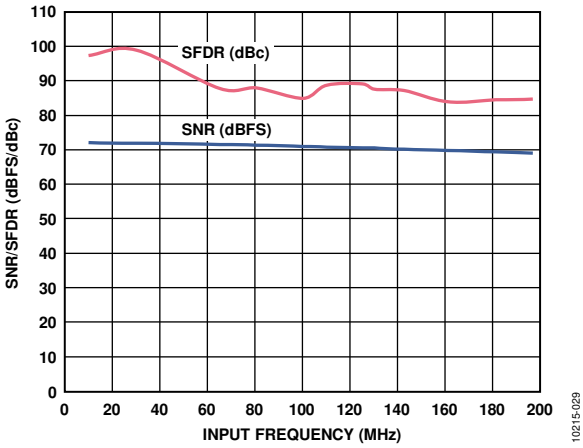


Figure 30. SNR/SFDR vs. f_{IN}, f_{SAMPLE} = 40 MSPS

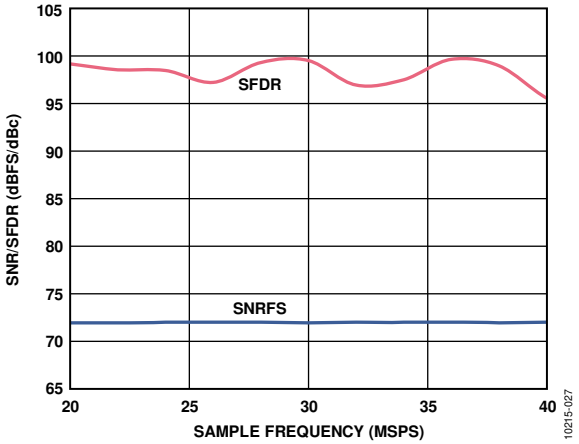


Figure 28. SNR/SFDR vs. Encode, f_{IN} = 19.7 MHz

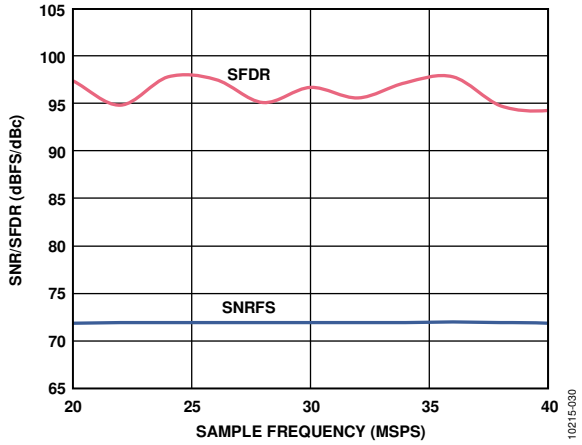


Figure 31. SNR/SFDR vs. Encode, f_{IN} = 30.5 MHz

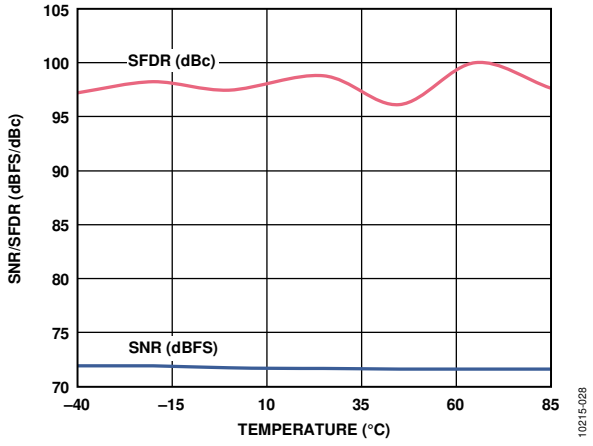


Figure 29. SNR/SFDR vs. Temperature, f_{IN} = 9.7 MHz, f_{SAMPLE} = 40 MSPS

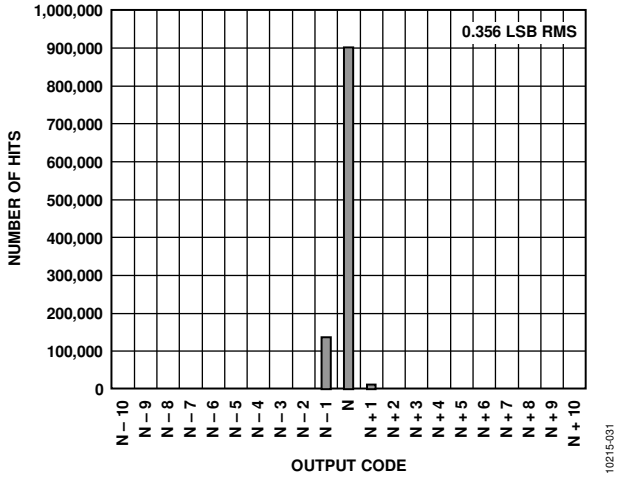


Figure 32. Input-Referred Noise Histogram, f_{SAMPLE} = 40 MSPS

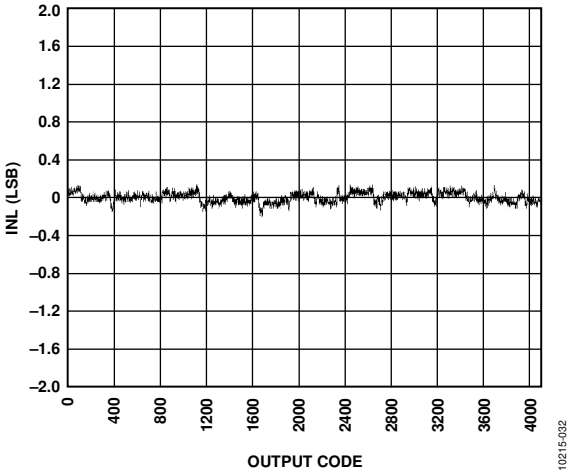


Figure 33. INL, f_{IN} = 9.7 MHz, f_{SAMPLE} = 40 MSPS

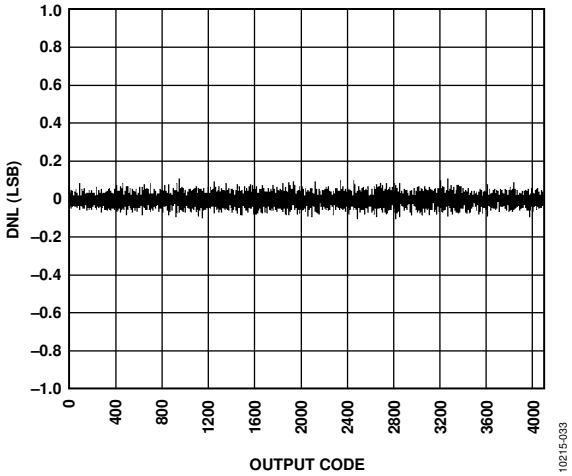


Figure 34. DNL, f_{IN} = 9.7 MHz, f_{SAMPLE} = 40 MSPS

EQUIVALENT CIRCUITS

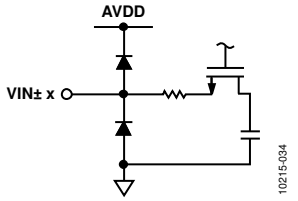


Figure 35. Equivalent Analog Input Circuit

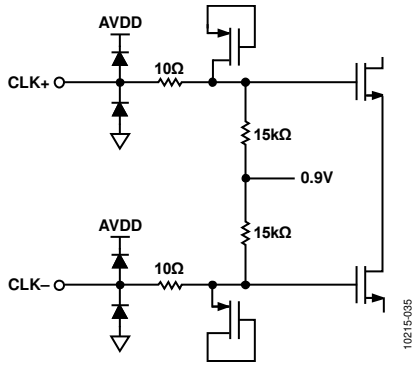


Figure 36. Equivalent Clock Input Circuit

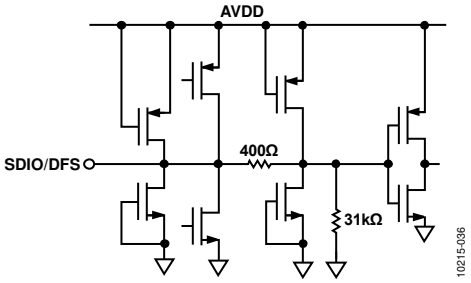


Figure 37. Equivalent SDIO/DFS Input Circuit

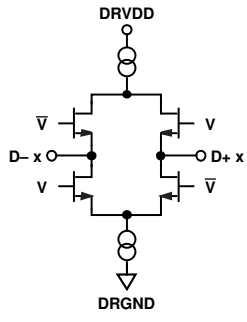


Figure 38. Equivalent Digital Output Circuit

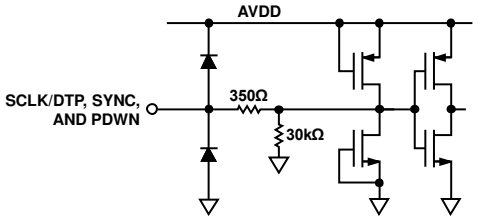


Figure 39. Equivalent SCLK/DTP, SYNC, and PDWN Input Circuit

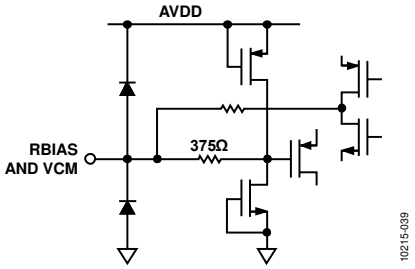


Figure 40. Equivalent RBIAS, VCM Circuit

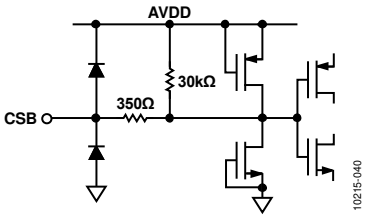


Figure 41. Equivalent CSB Input Circuit

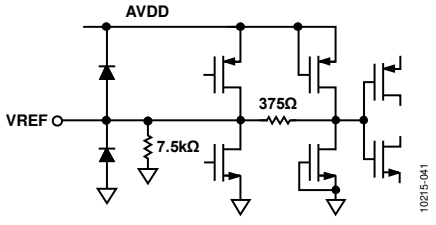


Figure 42. Equivalent VREF Circuit

THEORY OF OPERATION

The AD9637 is a multistage, pipelined ADC. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The serializer transmits this converted data in a 12-bit output. The pipelined architecture permits the first stage to operate with a new input sample, while the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The data is then serialized and aligned to the frame and data clocks.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9637 is a differential, switched capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. By using an input common-mode voltage of midsupply, users can minimize signal-dependent errors and achieve optimum performance.

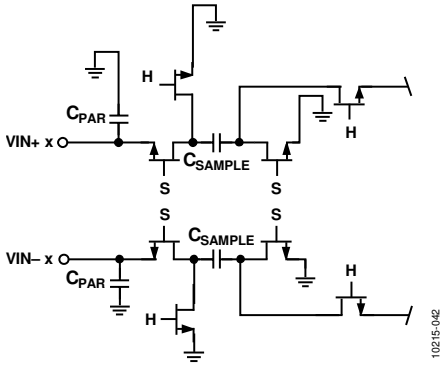


Figure 43. Switched-Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample mode and hold mode (see Figure 43). When the input circuit is switched to sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current injected from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and, therefore, achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Either a differential capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005) for more information. In general, the precise values depend on the application.

Input Common Mode

The analog inputs of the AD9637 are not internally dc-biased. Therefore, in ac-coupled applications, the user must provide this bias externally. Setting the device so that V_{CM} = AVDD/2 is recommended for optimum performance, but the device can function over a wider range with reasonable performance, as shown in Figure 44.

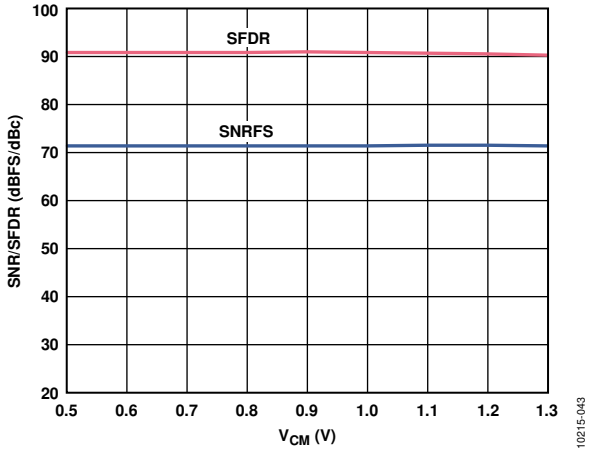


Figure 44. SNR/SFDR vs. Common-Mode Voltage, f_{IN} = 9.7 MHz, f_{SAMPLE} = 80 MSPS

An on-board, common-mode voltage reference is included in the design and is available from the VCM pin. The VCM pin must be decoupled to ground by a 0.1 µF capacitor, as described in the Applications Information section.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9637, the largest input span available is 2 V p-p.

Differential Input Configurations

There are several ways to drive the AD9637 either actively or passively. However, optimum performance is achieved by driving the analog input differentially. Using a differential double balun configuration to drive the AD9637 provides excellent performance and a flexible interface to the ADC (see Figure 46) for baseband applications.

For applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration (see Figure 47), because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9637.

Regardless of the configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

It is not recommended to drive the AD9637 input single-ended.

VOLTAGE REFERENCE

A stable and accurate 1.0 V voltage reference is built into the AD9637. VREF can be configured using either the internal 1.0 V reference or an externally applied 1.0 V reference voltage. The various reference modes are summarized in the sections that follow. The VREF pin should be externally decoupled to ground with a low ESR, 1.0 µF capacitor in parallel with a low ESR, 0.1 µF ceramic capacitor.

Internal Reference Connection

A comparator within the AD9637 detects the potential at the SENSE pin and configures the reference into two possible modes, which are summarized in Table 9. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 45), setting VREF to 1.0 V.

Table 9. Reference Configuration Summary

Selected Mode	SENSE Voltage (V)	Resulting V_{REF} (V)	Resulting Differential Span (V p-p)
Fixed Internal Reference	AGND to 0.2	1.0 internal	2.0
Fixed External Reference	AVDD	1.0 applied to external VREF pin	2.0

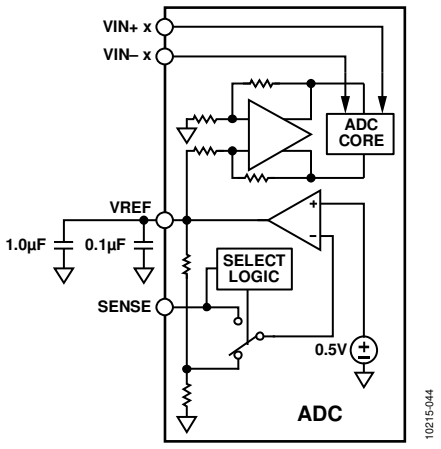


Figure 45. Internal Reference Configuration

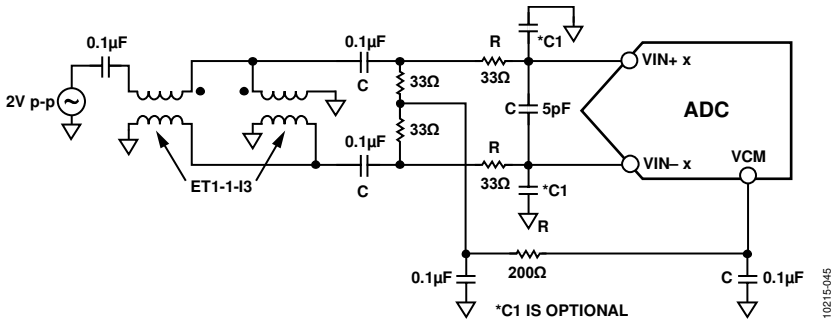


Figure 46. Differential Double Balun Input Configuration for Baseband Applications

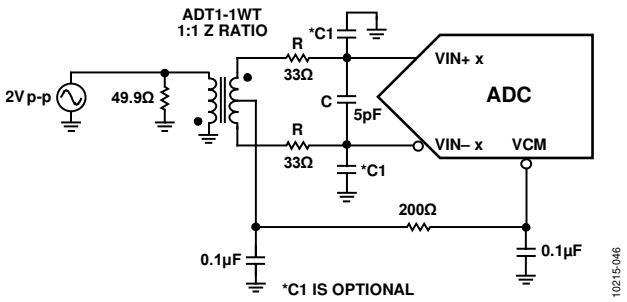


Figure 47. Differential Transformer-Coupled Configuration for Baseband Applications

If the internal reference of the AD9637 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 48 shows how the internal reference voltage is affected by loading.

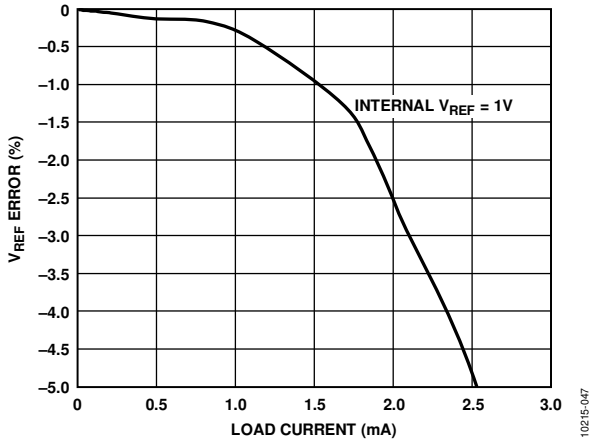


Figure 48. V_{REF} Error vs. Load Current

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 49 shows the typical drift characteristics of the internal reference in 1.0 V mode.

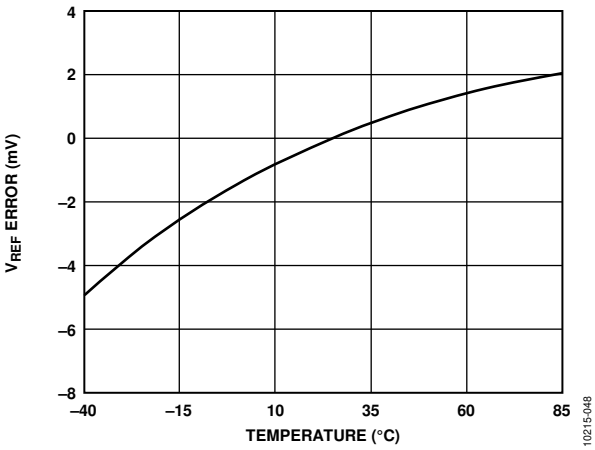


Figure 49. Typical V_{REF} Drift

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7.5 kΩ load (see Figure 42). The internal buffer generates the positive and negative full-scale references for the ADC core. Therefore, the external reference must be limited to a maximum of 1.0 V. It is not recommended to leave the SENSE pin floating.

CLOCK INPUT CONSIDERATIONS

For optimum performance, clock the AD9637 sample clock inputs, CLK+ and CLK–, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK– pins via a transformer or capacitors. These pins are biased internally (see Figure 36) and require no external bias.

Clock Input Options

The AD9637 has a very flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of the utmost concern, as described in the Jitter Considerations section.

Figure 50 and Figure 51 show two preferred methods for clocking the AD9637 (at clock rates of up to 640 MHz prior to the internal CLK divider). A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF transformer or an RF balun.

The RF balun configuration is recommended for clock frequencies between 80 MHz and 640 MHz, and the RF transformer is recommended for clock frequencies from 10 MHz to 200 MHz. The back-to-back Schottky diodes across the transformer/balun secondary winding limit clock excursions into the AD9637 to approximately 0.8 V p-p differential.

This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9637 while preserving the fast rise and fall times of the signal that are critical to a low jitter performance. However, the diode capacitance comes into play at frequencies above 500 MHz. Care must be taken in choosing the appropriate signal limiting diode.

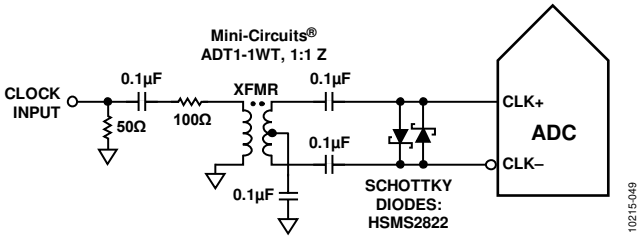


Figure 50. Transformer Coupled Differential Clock (Up to 200 MHz)

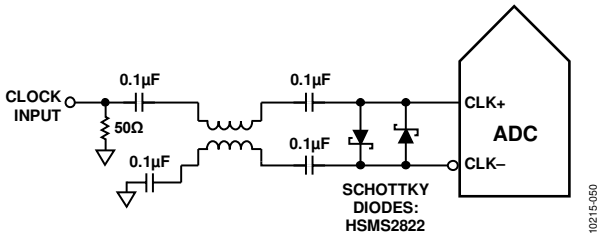


Figure 51. Balun Coupled Differential Clock (80 MHz to 640 MHz)

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 52. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517 clock drivers offer excellent jitter performance.

A third option is to ac couple a differential LVDS signal to the sample clock input pins, as shown in Figure 53. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517 clock drivers offer excellent jitter performance.

In some applications, it may be acceptable to drive the sample clock inputs with a single-ended 1.8 V CMOS signal. In such applications, drive the CLK+ pin directly from a CMOS gate, and bypass the CLK− pin to ground with a 0.1 µF capacitor (see Figure 54).

Input Clock Divider

The AD9637 contains an input clock divider with the ability to divide the input clock by integer values between 1 and 8.

The AD9637 clock divider can be synchronized using the external SYNC input. Bit 0 and Bit 1 of Register 0x109 allow the clock divider to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written. A valid SYNC causes the clock divider to reset to its initial state. This synchronization feature allows multiple parts to have their clock dividers aligned to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9637 contains a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD9637. Noise and distortion performance are nearly flat for a wide range of duty cycles with the DCS turned on.

Jitter in the rising edge of the input is still of concern and is not easily reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates less than 20 MHz, nominally. The loop has a time constant associated with it that must be considered in applications in which the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal.

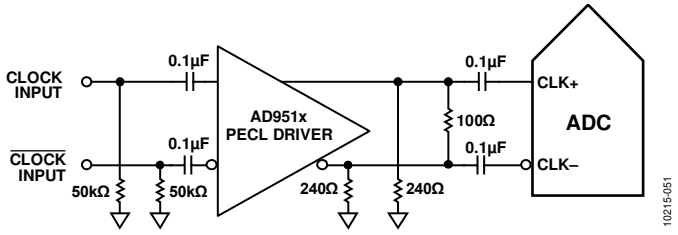


Figure 52. Differential PECL Sample Clock (Up to 640 MHz)

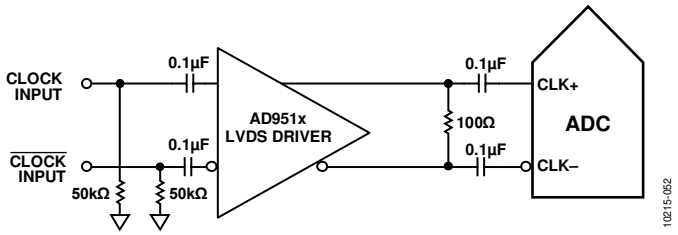


Figure 53. Differential LVDS Sample Clock (Up to 640 MHz)

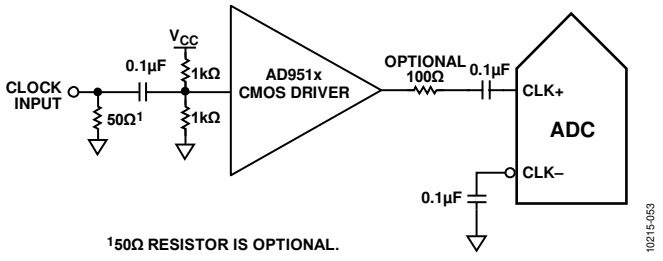


Figure 54. Single-Ended 1.8 V CMOS Input Clock (Up to 200 MHz)

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated by

$$SNR\ Degradation = 20\log_{10}\left(\frac{1}{2\pi \times f_A \times t_J}\right)$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 55).

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9637. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

Refer to the AN-501 Application Note and the AN-756 Application Note for more in-depth information about jitter performance as it relates to ADCs.

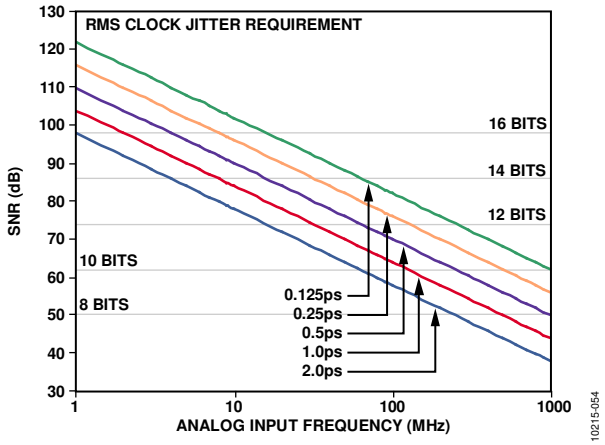


Figure 55. Ideal SNR vs. Input Frequency and Jitter

POWER DISSIPATION AND POWER-DOWN MODE

As shown in Figure 56, the power dissipated by the AD9637 is proportional to its sample rate. The digital power dissipation does not vary significantly because it is determined primarily by the DRVDD supply and bias current of the LVDS output drivers.

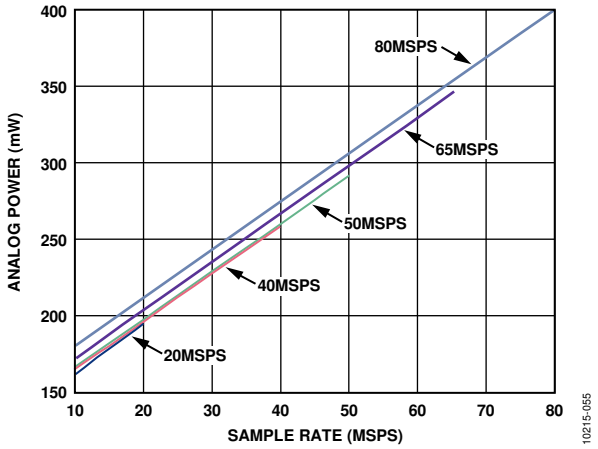


Figure 56. Analog Core Power vs. f_{SAMPLE} for f_{IN} = 9.7 MHz

The AD9637 is placed in power-down mode either by the SPI port or by asserting the PDWN pin high. In this state, the ADC typically dissipates 1 mW. During power-down, the output drivers are placed in a high impedance state. Asserting the PDWN pin low returns the AD9637 to its normal operating mode. Note that PDWN is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when entering power-down mode and then must be recharged when returning to normal operation. As a result, wake-up time is related to the time spent in power-down mode, and shorter power-down cycles result in proportionally shorter wake-up times. When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the Memory Map section for more details on using these features.

DIGITAL OUTPUTS AND TIMING

The AD9637 differential outputs conform to the ANSI-644 LVDS standard on default power-up. This can be changed to a low power, reduced signal option (similar to the IEEE 1596.3 standard) via the SPI. The LVDS driver current is derived on chip and sets the output current at each output equal to a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing (or 700 mV p-p differential) at the receiver.

When operating in reduced range mode, the output current is reduced to 2 mA. This results in a 200 mV swing (or 400 mV p-p differential) across a 100 Ω termination at the receiver.

The AD9637 LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor placed as close to the receiver as possible. If there is no far-end receiver termination or there is poor differential trace routing, timing errors may result. To avoid such timing errors, it is recommended that the trace length be less than 24 inches and that the differential output traces be close together and at equal lengths. An example of the FCO and data stream with proper trace length and position is shown in Figure 57. An example of LVDS output timing in reduced range mode is shown in Figure 58.

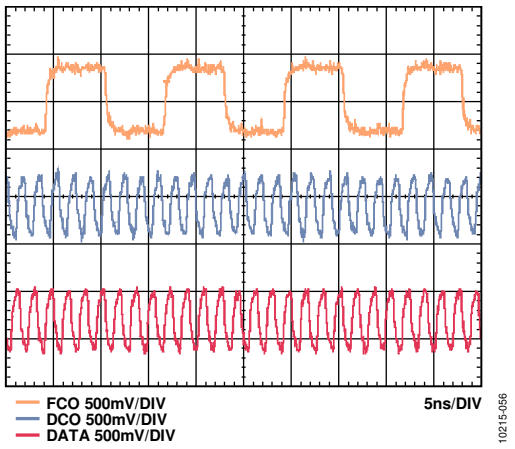


Figure 57. LVDS Output Timing Example in ANSI-644 Mode (Default)

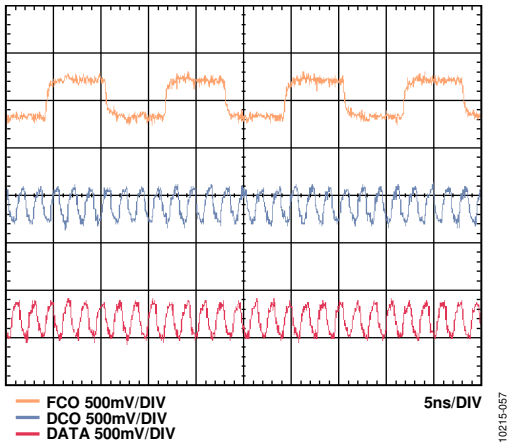


Figure 58. LVDS Output Timing Example in Reduced Range Mode

Figure 59 shows an example of the LVDS output using the ANSI-644 standard (default) data eye and a time interval error (TIE) jitter histogram with trace lengths of less than 24 inches on standard FR-4 material.

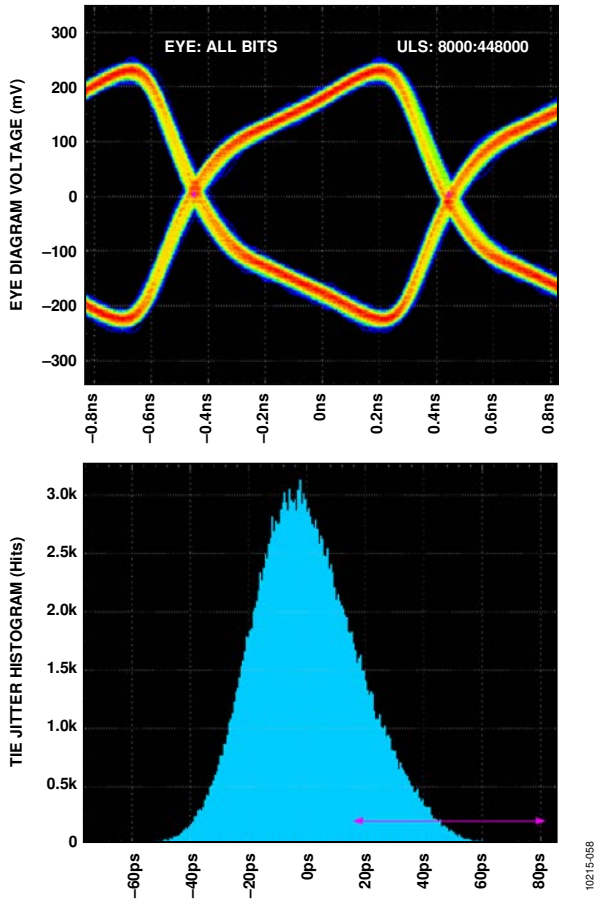


Figure 59. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths of Less Than 24 Inches on Standard FR-4, External 100 Ω Far-End Termination Only

Figure 60 shows an example of trace lengths exceeding 24 inches on standard FR-4 material. Note that the TIE jitter histogram reflects the decrease of the data eye opening as the edge deviates from the ideal position.

It is the responsibility of the user to determine if the waveforms meet the timing budget of the design when the trace lengths exceed 24 inches. Additional SPI options allow the user to further increase the internal termination (increasing the current) of all eight outputs to drive longer trace lengths, which can be achieved by programming Register 0x15. Even though this option produces sharper rise and fall times on the data edges and is less prone to bit errors, it also increases the power dissipation of the DRVDD supply.

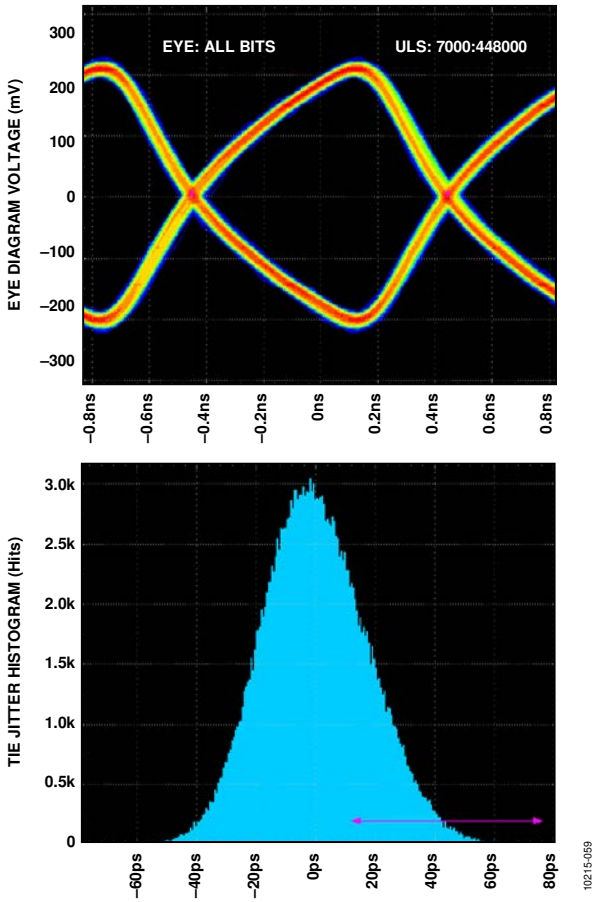


Figure 60. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths Greater Than 24 Inches on Standard FR-4, External 100 Ω Far Termination Only

The default format of the output data is twos complement. Table 10 shows an example of the output coding format. To change the output data format to offset binary, see the Memory Map section.

Data from each ADC is serialized and provided on a separate channel in DDR mode. The data rate for each serial stream is equal to 12 bits times the sample clock rate, with a maximum of 960 Mbps (12 bits × 80 MSPS) = 960 Mbps. The lowest typical conversion rate is 10 MSPS. See the Memory Map section for details on enabling this feature.

Table 10. Digital Output Coding

Input (V)	Condition (V)	Offset Binary Output Mode	Twos Complement Mode
VIN+ – VIN–	< –VREF – 0.5 LSB	0000 0000 0000	1000 0000 0000
VIN+ – VIN–	= –VREF	0000 0000 0000	1000 0000 0000
VIN+ – VIN–	= 0	1000 0000 0000	0000 0000 0000
VIN+ – VIN–	= +VREF – 1.0 LSB	1111 1111 1111	0111 1111 1111
VIN+ – VIN–	> +VREF – 0.5 LSB	1111 1111 1111	0111 1111 1111