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ANALOG DEVICES

Evaluation Board User Guide
UG-294

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Evaluating the AD9644/AD9641 Analog-to-Digital Converters

FEATURES

Full featured evaluation board for the AD9644 or AD9641
SPI interface for setup and control
External clock, on-board oscillator, and AD9524 clocking options
Balun/transformer and amplifier input drive options
LDO regulator and switching power supply options
VisualAnalog® and SPI controller software interfaces

EQUIPMENT NEEDED

Analog signal source and antialiasing filter
Sample clock source (if not using the on-board oscillator)
2 switching power supplies (6.0 V, 2.5 A), CUI EPS060250UH-PHP-SZ, provided
PC running Windows® 98 (2nd ed.), Windows 2000, Windows ME, or Windows XP
USB 2.0 port, recommended (USB 1.1 compatible)
AD9644 or AD9641 evaluation board
FIFO-GX FPGA-based data capture kit

SOFTWARE NEEDED

VisualAnalog
SPI controller

DOCUMENTS NEEDED

AD9644 or AD9641 data sheet
AD9524 data sheet
ADP2114 or ADP2108 data sheet
AD8376 or ADL5562 data sheet
JESD204A specification
AN-905 Application Note, *VisualAnalog Converter Evaluation Tool Version 1.0 User Manual*
AN-878 Application Note, *High Speed ADC SPI Control Software*
AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*
AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*

GENERAL DESCRIPTION

This user guide describes the AD9644 and AD9641 evaluation boards (AD9644-155KITZ, AD9644-80KITZ, AD9641-80KITZ), which provide all of the support circuitry required to operate the AD9644 and AD9641 in the available modes and configurations. The application software used to interface with the device is also described.

The AD9644 and AD9641 data sheets provide additional information and should be consulted when using the evaluation board. For additional information or questions, send an email to highspeed.converters@analog.com.

The JESD204A specification can be downloaded from the JEDEC website. The download is free, but registration is required.

TYPICAL MEASUREMENT SETUP

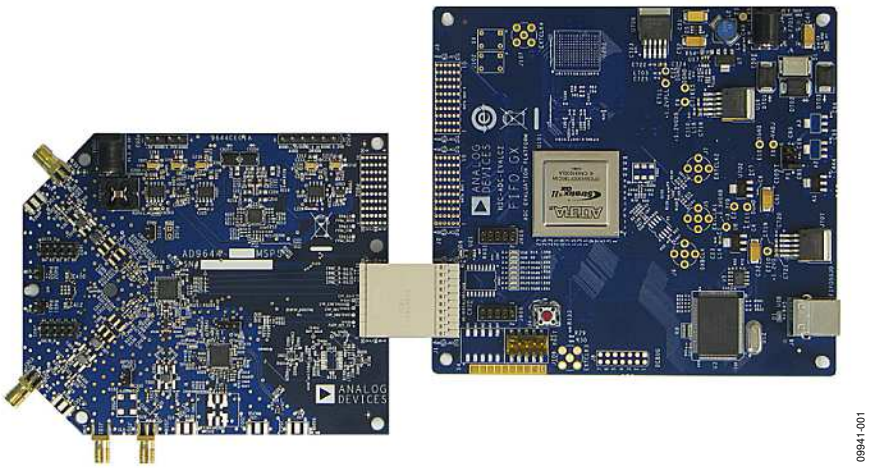

Figure 1. AD9644/AD9641 Evaluation Board and FIFO-GX Data Capture Board

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REVISION HISTORY

3/13—Rev. A to Rev. B

Changed ADA4937 to ADA4937-1 and ADA4938 to ADA4938-1 5
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9/12—Rev. 0 to Rev. A

Removed HSC-ADC-EVALCZ (Throughout) 1

8/11—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The AD9644 and AD9641 evaluation boards provide all of the support circuitry required to operate the parts in various modes and configurations. Figure 2 shows the typical bench characterization setup used to evaluate the ac performance of the AD9644 or AD9641. It is critical that the signal sources used for the analog input and clock have very low phase noise (<1 ps rms jitter) to realize the optimum performance of the signal chain. Proper filtering of the analog input signal to remove harmonics and lower the integrated or broadband noise at the input is necessary to achieve the specified noise performance. The AD9644 evaluation board supports dual-channel operation for the AD9644. The AD9641 evaluation board supports single-channel operation for the AD9641.

See the Evaluation Board Software Quick Start Procedures section to get started, and see Figure 17 to Figure 40 for the complete schematics and layout diagrams. These diagrams demonstrate the routing and grounding techniques that should be applied at the system level when designing application boards using these converters.

POWER SUPPLIES

Each evaluation board is supplied with a wall-mountable switching power supply that provides a 6 V, 2 A maximum output. Connect the supply to an ac wall outlet of 100 V to 240 V at a frequency of 47 Hz to 63 Hz. The output from the supply is provided through a 2.1 mm inner diameter jack that connects to the printed circuit board (PCB) at P201. In the default configuration, the 6 V supply is fused and conditioned on the PCB before connecting to the low dropout linear regulators that supply the proper bias to each of the various sections on the board.

The evaluation board can be powered in a nondefault condition using multiple external bench power supplies to bias each section of the board individually. To do this, remove the E202, E204, E205, and E207 ferrite beads—as well as the E201 ferrite bead for the AD9644—from the evaluation board to disconnect the outputs from the on-board LDOs. Then, use P202 and P203 to connect a different supply for each section. A 1.8 V supply is needed with a 1 A current capability for DUT_AVDD and DRVDD; however, it is recommended that separate supplies be used for the analog domain and the digital domain. An additional supply (DVDD) is also required to supply 1.8 V for digital support circuitry on the board. This supply should also have a 1 A current capability and can be combined with DRVDD without significantly degrading performance.

To operate the evaluation board using the SPI and the alternate clocking options, a separate 3.3 V analog supply is needed in addition to the other supplies. This 3.3 V supply, or 3P3V_ANALOG, should have a 1 A current capability and is used to support the clocking circuitry. On the AD9641 evaluation board, the 3.3 V supply is also used to support the optional input path amplifier (ADL5562). An additional supply (5V_SUPPORT) is used on the AD9644 evaluation board to bias the optional dual input path amplifier (AD8376) on Channel A and Channel B. If used, these supplies should each have a 1 A current capability.

INPUT SIGNALS

When connecting the clock and analog source, use signal generators with low phase noise, such as the Rohde & Schwarz SMA or HP 8644B signal generators, or an equivalent. Use a 1 m, shielded, RG-58, 50 Ω coaxial cable for connecting the signal generators to the evaluation board. Enter the desired frequency and amplitude (see the Specifications section in the data sheet of the respective part). When connecting the analog input source, use of a multi-pole, narrow-band band-pass filter with 50 Ω terminations is recommended. Analog Devices, Inc., uses TTE and K&L Microwave, Inc., band-pass filters. The filters should be connected directly to the evaluation board.

If an external clock source is used, it should also be supplied using a signal generator with low phase noise. Typically, most Analog Devices evaluation boards can accept ~2.8 V p-p or 13 dBm sine wave input for the clock.

OUTPUT SIGNALS

The default setup uses the Analog Devices high speed converter evaluation platform (FIFO-GX FPGA) for data capture. The output signals from Channel A and Channel B are routed through P601 to the FPGA on the data capture board.

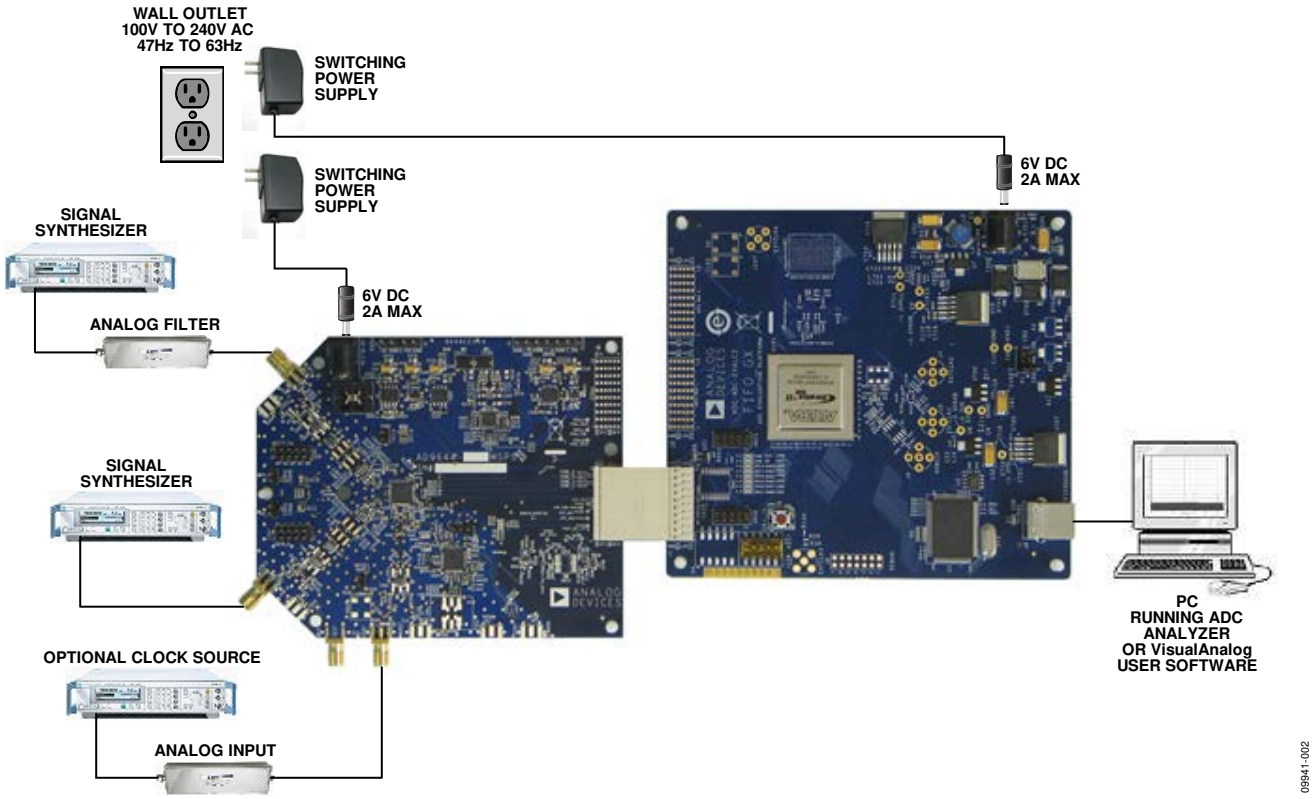

Figure 2. AD9644/AD9641 Evaluation Board Connection

DEFAULT OPERATION AND JUMPER SELECTION SETTINGS

This section explains the default and optional settings and modes available on the AD9644 and AD9641 Rev. A evaluation boards.

Power Circuitry

Connect the switching power supply that is included in the evaluation kit between an ac wall outlet of 100 V to 240 V at 47 Hz to 63 Hz and the P201 jack.

Analog Input

The Channel A and Channel B inputs on the evaluation board are set up for a double balun-coupled analog input with a 50 Ω impedance. This input network is optimized to support a wide frequency band. See the AD9644 data sheet for additional information about the recommended networks for various input frequency ranges. The nominal input drive level is 10 dBm to achieve 2 V p-p full scale into 50 Ω. At higher input frequencies, slightly higher input drive levels are required due to losses in the front-end network.

Optionally, on the AD9644 evaluation board, Channel A and Channel B inputs on the board can be configured to use the AD8376 digitally controlled variable gain amplifier (VGA). The AD8376 is included on the AD9644 evaluation board at U401. However, the path into and out of the AD8376 can be configured in many different ways depending on the application; therefore, the parts in the input and output paths are left unpopulated. Users should see the AD8376 data sheet for additional information about this part and for configuring the inputs and outputs. The AD8376 by default is held in power-down mode but can be enabled by adding a jumper on P401 (Channel A) or P402 (Channel B).

Optionally, on the AD9641 evaluation board, the Channel A input on the board can be configured to use the ADL5562 ultralow distortion RF/IF differential amplifier. The ADL5562 is included on the AD9641 evaluation board at U401. However, the path into and out of the ADL5562 can be configured in many ways depending on the application; therefore, the parts in the input and output paths are left unpopulated. Users should see the ADL5562 data sheet for additional information on this part and for configuring the inputs and outputs. The ADL5562 by default is held in power-down mode but can be enabled by adding a jumper on P401. The ADL5562 can also be substituted with the ADA4937-1 or the ADA4938-1 to allow evaluation of these parts with the analog-to-digital converter (ADC).

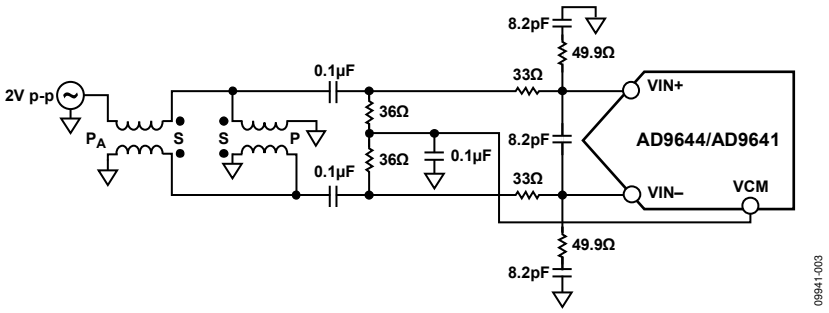

Figure 3. Default Analog Input Configuration of the AD9644/AD9641

Clock Circuitry

The default clock input circuit that is populated on the AD9644 and AD9641 evaluation boards uses a simple transformer-coupled circuit using a high bandwidth 1:1 impedance ratio transformer (T503) that adds a very low amount of jitter to the clock path. The clock input is 50 Ω terminated and ac-coupled to handle single-ended sine wave types of inputs. The transformer converts the single-ended input to a differential signal that is clipped by CR503 before entering the ADC clock inputs.

The board is set by default to use an external clock generator. An external clock source capable of driving a 50 Ω terminated input should be connected to J702.

A differential LVPECL clock driver output can also be used to clock the ADC input using the AD9524 (U501). To place the AD9524 into the clock path, populate R541 and R542 with 0 Ω resistors and remove R522 and R523 to disconnect the default clock path outputs. In addition, populate R533 and R534 with 0 Ω resistors. Next, place Y501, which is the Epson Toyocom voltage controlled oscillator that serves as the VCXO for the AD9524. By completing these connections, OUT2 of the AD9524 is connected to the sampling clock inputs of the AD9644/AD9641. The AD9524 must be configured through the SPI controller software to set up the PLL and other operation modes. Consult the AD9524 data sheet for more information about these and other options.

An additional clocking option is provided on the AD9644 evaluation board. In place of connecting an external source for the clock, Y502 a low jitter Valpey Fisher clock oscillator can be placed and used as the clock source. If using Y502, a jumper must be placed on Header P501.

PDWN

To enable the power-down feature, add a shorting jumper across P101 at Pin 1 and Pin 2 to connect the PDWN pin to AVDD.

Switching Power Supply

The ADC on the AD9644 evaluation board can be configured to use the ADP2114 dual switching power supply to provide power to the DRVDD and AVDD rails of the ADC. To configure the board to operate from the ADP2114, the following changes must be incorporated (see the AD9644 Evaluation Board Schematics and Artwork and Bill of Materials sections for specific recommendations for part values):

1. Install R204 and R221 to enable the ADP2114.
2. Install R216 and R218.
3. Install L201 and L202.
4. Remove JP201 and JP203 and install JP202 and JP204.
5. Remove E205 and E207 and install E208 and E209.

The ADC on the AD9641 evaluation board can be configured to use the ADP2108 switching power supply to provide power to the DRVDD and AVDD rails of the ADC. To configure the board to operate from the ADP2108, the following changes must be incorporated (see the AD9641 Evaluation Board Schematics and Artwork and Bill of Materials sections for specific recommendations for part values):

1. Install R204 to enable the ADP2108.
2. Install L201 and L202.
3. Remove JP201 and JP203 and install JP202 and JP204.
4. Remove E205 and E207 and install E208 and E209.

Making these changes enables the switching converter to power the ADC. Using the switching converter as the ADC power source is more efficient than using the default LDOs.

JESD204A Output Modes

The AD9641 evaluation platform supports one JESD204A output mode (see Table 1), and the AD9644 evaluation platform supports several JESD204A output modes (see Table 2 for typical configurations). Each mode requires a different FPGA configuration to capture data properly. Output Configuration A in Table 2 is the configuration for the default mode for the AD9644, and it consists of two converters, each of which has two links and one output lane.

Table 1. AD9641 JESD204A Configuration

Output Configuration	AD9641 Configuration	JESD204A Link Settings	Comments
A	One converter, One JESD204A link, One lane per link	M = 1; L = 1; S = 1; F = 2; N′ = 16; CF = 0; CS = 0, 1, 2; K = N/A; SCR = 0, 1; HD = 0	Maximum sample rate = 80 MSPS or 155 MSPS

Table 2. AD9644 JESD204A Typical Configurations (Enabled Through SPI Register 0x5E, Bits[2:0])

Output Configuration	AD9644 Configuration	JESD204A Link A Settings	JESD204A Link B Settings	Comments
A	Two converters, two JESD204A links, one lane per link	M = 1; L = 1; S = 1; F = 2; N′ = 16; CF = 0; CS = 0, 1, 2; K = N/A; SCR = 0, 1; HD = 0	M = 1; L = 1; S = 1; F = 2; N′ = 16; CF = 0; CS = 0, 1, 2; K = N/A; SCR = 0, 1; HD = 0	Maximum sample rate = 80 MSPS
B	Two converters, one JESD204A link, two lanes per link	M = 2; L = 2; S = 1; F = 2; N′ = 16; CF = 0; CS = 0, 1, 2; K = see the specifications in the AD9644 data sheet; SCR = 0, 1; HD = 0	Disabled	Maximum sample rate = 80 MSPS This configuration is required for applications needing two aligned samples (that is, I/Q applications)
C	Two converters, one JESD204A link, one lane per link	M = 2; L = 1; S = 1; F = 4; N′ = 16; CF = 0; CS = 0, 1, 2; K = see the specifications in the AD9644 data sheet; SCR = 0, 1; HD = 0	Disabled	Maximum sample rate = 80 MSPS

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

This section provides quick start procedures for using the AD9644 or AD9641 evaluation board. Both the default and optional settings are described.

CONFIGURING THE BOARD

Before using the software for testing, configure the evaluation board as follows:

1. Connect the AD9644 or AD9641 evaluation board to the FIFO-GX data capture board, as shown in Figure 1 and Figure 2.
2. Ensure that a jumper is installed on Header P1 between Pin 1 and Pin 2 on the FIFO-GX evaluation board to set the FPGA I/O voltage to 1.8 V.
3. Connect the AD9644 or AD9641 evaluation board to a 6 V, 2.5 A switching power supply (such as the CUI, Inc., EPS060250UH-PHP-SZ included in the evaluation board package).
4. Connect the FIFO-GX board to a 6 V, 2.5 A switching power supply (such as the CUI EPS060250UH-PHP-SZ included in the evaluation board package).
5. Connect the FIFO-GX board (J6) to a PC with the USB cable.
6. On the ADC evaluation board, confirm that there are no jumpers installed on any of the header pins.
7. Connect a low jitter sample clock to Connector J505 (J506 may be installed on earlier revision boards and can be used for the clock input on these boards). If the AD9644 clock divider is used, provide a clock into J505 (or J506) at the appropriate rate, which is divided to the desired clock rate. The input clock level should be between 10 dBm and 14 dBm.
8. Use a signal generator with low phase noise to provide an input signal to the analog input—Connector J301 (Channel A) and/or Connector J303 (Channel B). Use a 1 m, shielded, RG-58, 50 Ω coaxial cable to connect the signal generator. For best results, use a narrow-band band-pass filter with 50 Ω terminations and an appropriate center frequency. For the testing of these boards, TTE, Allen Avionics, and K&L band-pass filters were used.

USING THE SOFTWARE FOR TESTING

Setting Up the ADC Data Capture

After configuring the board, set up the ADC data capture using the following steps:

1. Open VisualAnalog on the PC that is connected to the evaluation board. The appropriate part type should be listed in the status bar of the **VisualAnalog – New Canvas** window. Select the template that corresponds to the type of testing to be performed (for example, in Figure 4 AD9644 has been selected).

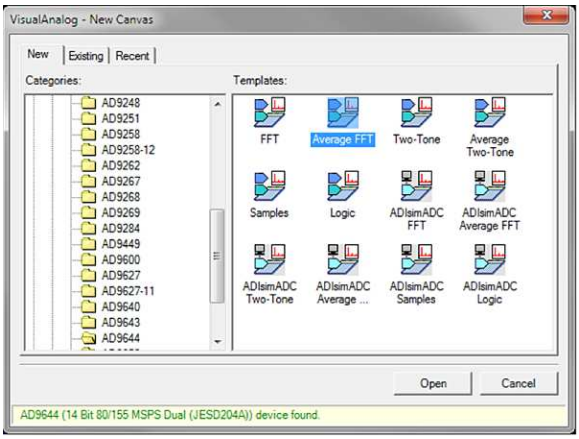

Figure 4. VisualAnalog, New Canvas Window

2. After the template is selected, a message appears asking if the default configuration can be used to program the FPGA (see Figure 5). Click **Yes**, and the window closes.

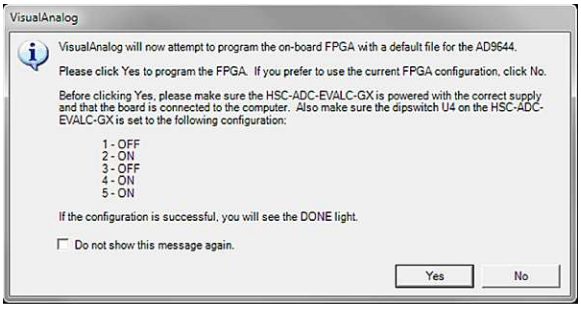

Figure 5. VisualAnalog Default Configuration Message

3. To change features to settings other than the default settings, click the **Expand Display** button (see Figure 6) to view the full window (shown in Figure 7).
   Detailed instructions for changing the features and capture settings can be found in the AN-905 Application Note, *VisualAnalog Converter Evaluation Tool Version 1.0 User Manual*. After the changes are made to the capture settings, click the **Collapse Display** button (see Figure 7) to minimize the window (shown in Figure 6).

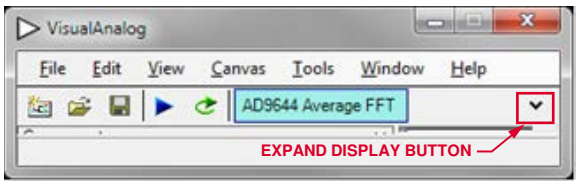

Figure 6. VisualAnalog Window Toolbar, Collapsed Display

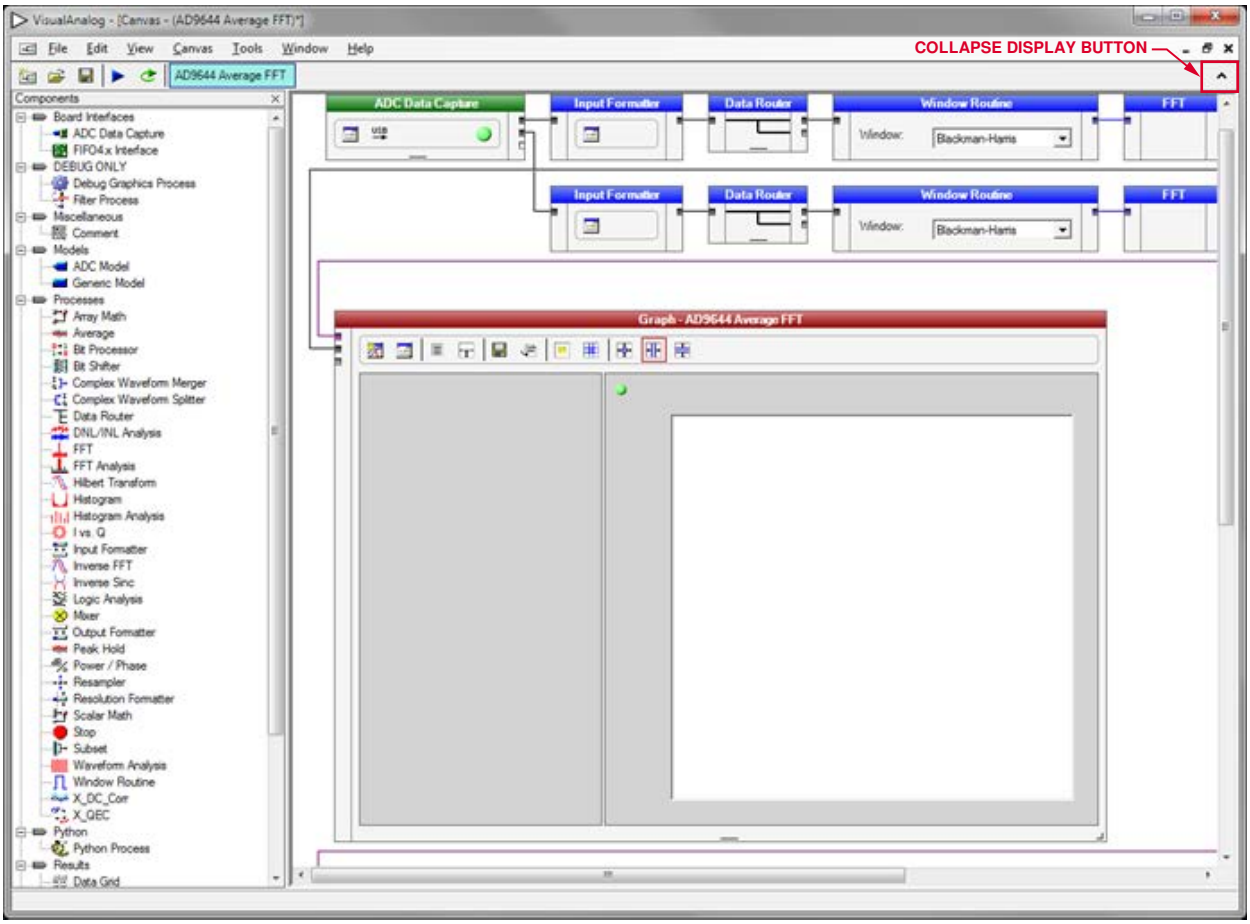

Figure 7. VisualAnalog, Main Window

4. If the input clock divider is used or if testing in Configuration C is desired, a nonstandard FPGA configuration file is required. To program the FPGA with a nonstandard configuration, click **ADC Data Capture**, and the **ADC Data Capture Settings** window appears. Click the **Capture Board** tab. Under the FPGA area, select the appropriate FPGA configuration file from the **Program Files:** box (see Table 2 and Figure 8). The selected FPGA configuration is then downloaded to the hardware using VisualAnalog. Table 2 details the configurations that are available to program the FPGA.

Table 3. AD9644 and AD9641 JESD204A Typical Configurations

Output Configuration			
AD9644	**AD9641**	**Clock Divider**	**FPGA Configuration File Name**
A and B	A	Disabled (Default)	ad9644_41.rbf (default)
A and B	A	Set to Divide by 2	ad9644_41_div2.rbf
A and B	A	Set to Divide by 3	ad9644_41_div3.rbf
A and B	A	Set to Divide by 4	ad9644_41_div4.rbf
A and B	A	Set to Divide by 5	ad9644_41_div5.rbf
A and B	A	Set to Divide by 6	ad9644_41_div6.rbf
A and B	A	Set to Divide by 7	ad9644_41_div7.rbf
A and B	A	Set to Divide by 8	ad9644_41_div8.rbf
C	A	Disabled	ad9644_41_config3.rbf

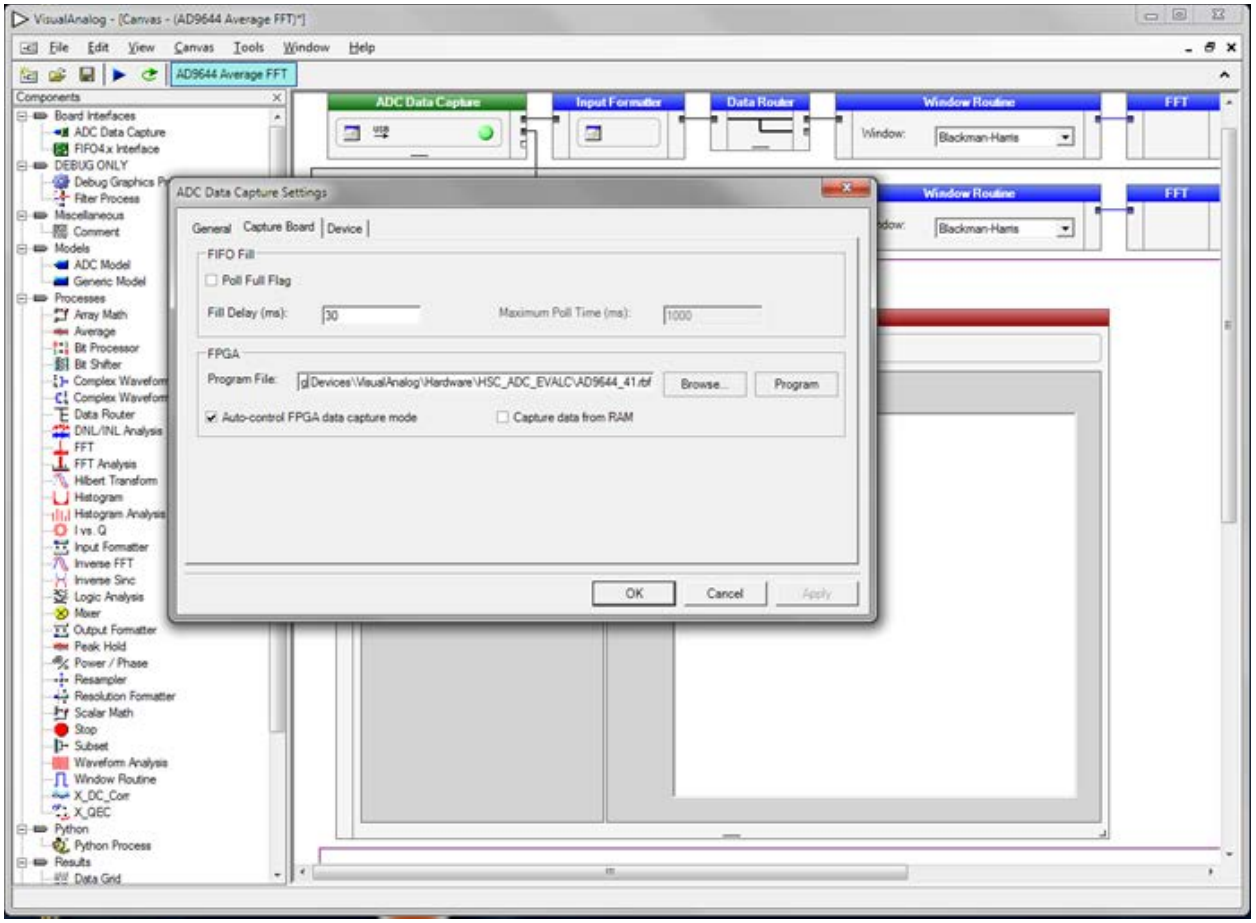

Figure 8. VisualAnalog, Main Window, Data Capture Settings

Setting Up the SPI Controller Software

After the ADC data capture board setup is complete, set up the SPI Controller software using the following procedure:

1. Start the SPI Controller software by selecting the SPI controller software from the **Start** menu or by double-clicking the **SPIController** software desktop icon. If prompted for a configuration file, select the appropriate one. If not, check the title bar of the window to determine which configuration is loaded. If necessary, select **Cfg Open** from the **File** menu and select the appropriate file based on your part type. Note that the **CHIP ID(1)** field should be filled to indicate whether the correct SPI controller configuration file is loaded (see Figure 9).

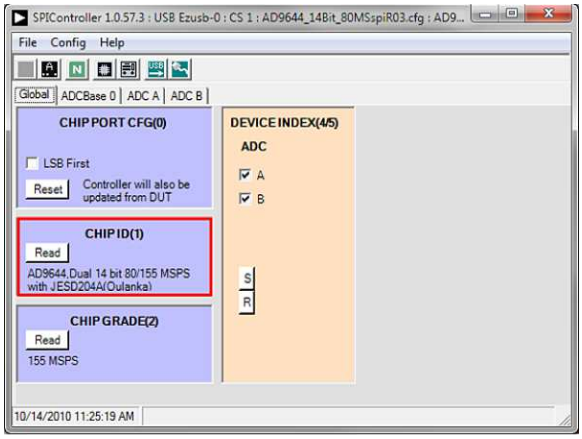

Figure 9. SPI Controller, CHIP ID(1) Box

2. Click the **New DUT** button in the **SPIController** window (see Figure 10).

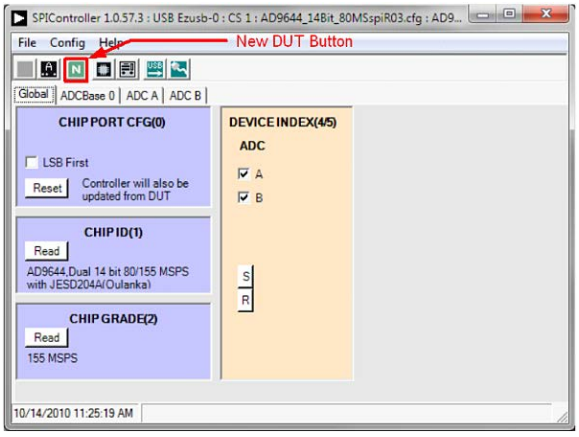

Figure 10. SPI Controller, New DUT Button

3. In the **ADCBase 0** tab of the **SPIController** window, find the **CLKDIV(B)** box (see Figure 11). If using the clock divider, use the drop-down box to select the correct clock divide ratio, if necessary. See the AD9644 or AD9641 data sheet; the AN-878 Application Note, *High Speed ADC SPI Control Software*; and the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, for additional information.

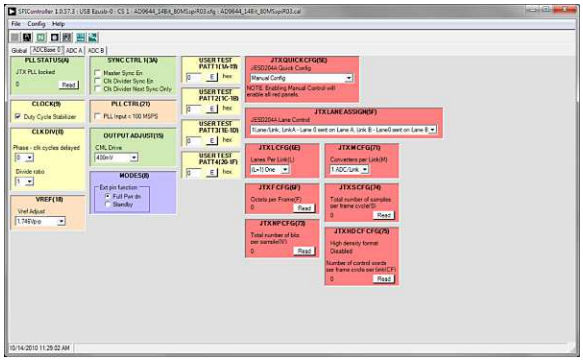

Figure 11. SPI Controller, CLKDIV(B) Box

4. If the ADC sample rate is less than 100 MSPS, click the **PLL Input < 100 MSPS** check box in the **PLL CTRL(21)** box of the **ADCBase0** tab. If you configured the FPGA for a clock divider mode in Step 4 of the Setting Up the ADC Data Capture section, select the appropriate clock divider setting in the **Divide ratio** drop-down box located in the **CLKDIV(B)** box. If you configured the FPGA for Output Configuration C (two converters, one JESD204A link, one lane per link) in Step 4 of the Setting Up the ADC Data Capture section, select this option in the **JTX QUICK CFG** box.
5. Note that other settings can be changed on the **ADCBase 0** tab (see Figure 11) and the **ADC A** and **ADC B** tabs (see Figure 12) to set up the part in the desired mode. The **ADCBase 0** tab settings affect the entire part, whereas the settings on the **ADC A** and **ADC B** tabs affect the selected channel only. Note that for the AD9641, only the **ADCBase0** and **ADC A** tabs are available because the device is a single-channel ADC. See the AD9644 or AD9641 data sheet; the AN-878 Application Note, *High Speed ADC SPI Control Software*; and the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, for additional information on the available settings.
6. Set the single-ended **SYNC** check box in the **JTX LINK CTRL2** box on both the **ADC A** and **ADC B** tabs (or on only the **ADC A** tab for the AD9641) as shown in Figure 12. This sets the JESD input syncs to operate in singled-ended CMOS mode for compatibility with the FPGA configuration.

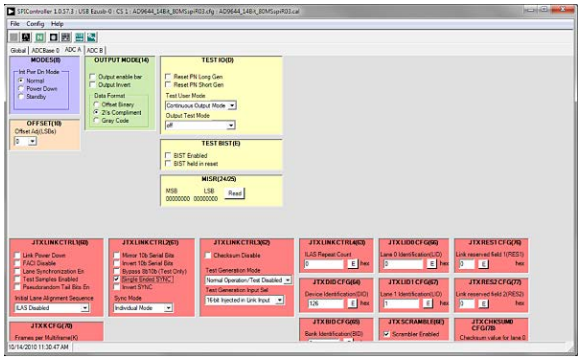

Figure 12. SPI Controller, Example ADC A Tab

7. If Configuration B (two converters, one JESD204A link, two lanes per link) is selected, click the **FACI Disable** check box in the **JTX LINK CTRL1** box (shown in Figure 13) for both Channel A and Channel B (**ADC A** and **ADC B** tabs) for the AD9644, or for only Channel A (**ADC A** tab) for the AD9641. Changing this selection sets the part to match the expected FPGA input configuration.

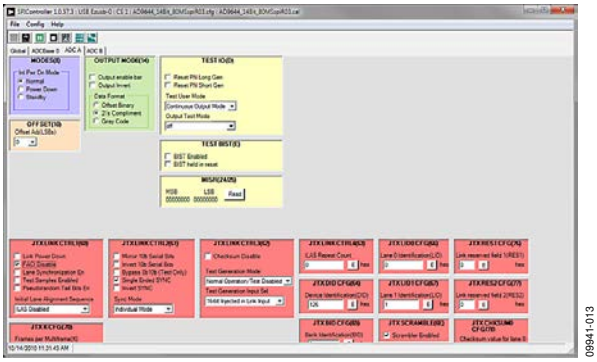

Figure 13. SPI Controller, Example ADC A Tab

8. Click the **Run** button in the **VisualAnalog** toolbar (see Figure 14).

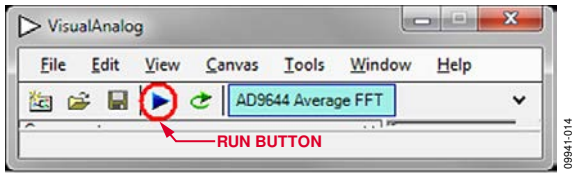

Figure 14. Run Button in VisualAnalog Toolbar, Collapsed Display

Adjusting the Amplitude of the Input Signal

Next, adjust the amplitude of the input signal for each channel as follows:

1. Adjust the amplitude of the input signal for Channel A so that the fundamental is at the desired level. (Examine the **Fund Power** reading in the left panel of the **VisualAnalog Graph – AD9644 Average FFT** window (see Figure 15).)

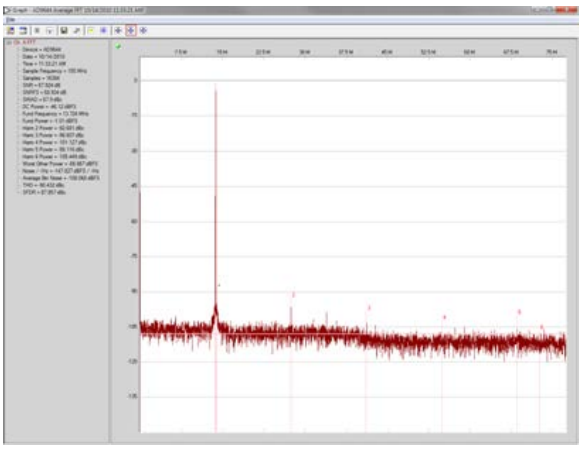

Figure 15. Graph Window of VisualAnalog

2. Repeat Step 1 for Channel B on the AD9644.
3. Click the disk icon within the graph for Channel A to save the performance plot data as a .csv formatted file. See Figure 16 for an example.

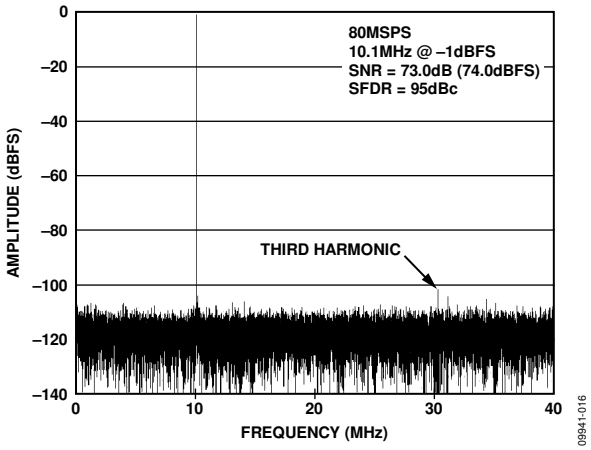

Figure 16. Typical FFT, AD9644

4. Repeat Step 3 for Channel B on the AD9644.

Troubleshooting Tips

If the FFT plot appears abnormal, use the following trouble-shooting tips:

- If you see a normal noise floor when you disconnect the signal generator from the analog input, be sure you are not overdriving the ADC. Reduce the input level, if necessary.
- In the **VisualAnalog** main window, click the **Settings** button in the **Input Formatter** box. Check that **Number Format** is set to the correct encoding (offset binary by default). Repeat this procedure for the other channel.

If the FFT appears normal but the performance is poor, use the following troubleshooting tips:

- Ensure that an appropriate filter is used on the analog input.
- Check that the signal generators for the clock and the analog input have low phase noise.
- Change the analog input frequency slightly if noncoherent sampling is being used.
- Verify that the SPI configuration file matches the product being evaluated.

If the FFT window remains blank after **Run** is clicked, use the following troubleshooting tips:

- Check that the evaluation board is securely connected to the FIFO-GX board.
- Ensure that the FPGA has been programmed by verifying that the **DONE** LED is illuminated on the FIFO-GX board. If this LED is not illuminated, make sure the U4 switch on the board is in the correct position for the USB configuration.
- Verify that the correct FPGA program was installed by clicking the **Settings** button in the **ADC Data Capture** box in VisualAnalog, and then clicking the **FPGA** tab and verifying that the proper FPGA bin file is selected for the part.

If **VisualAnalog** indicates that the FIFO Capture timed out, use the following troubleshooting tips:

- Ensure that all power and USB connections are secure.
- Probe the DCOA signal at RN801 (Pin 2) on the evaluation board and confirm that a clock signal is present at the ADC sampling rate.

EVALUATION BOARD SCHEMATICS AND ARTWORK

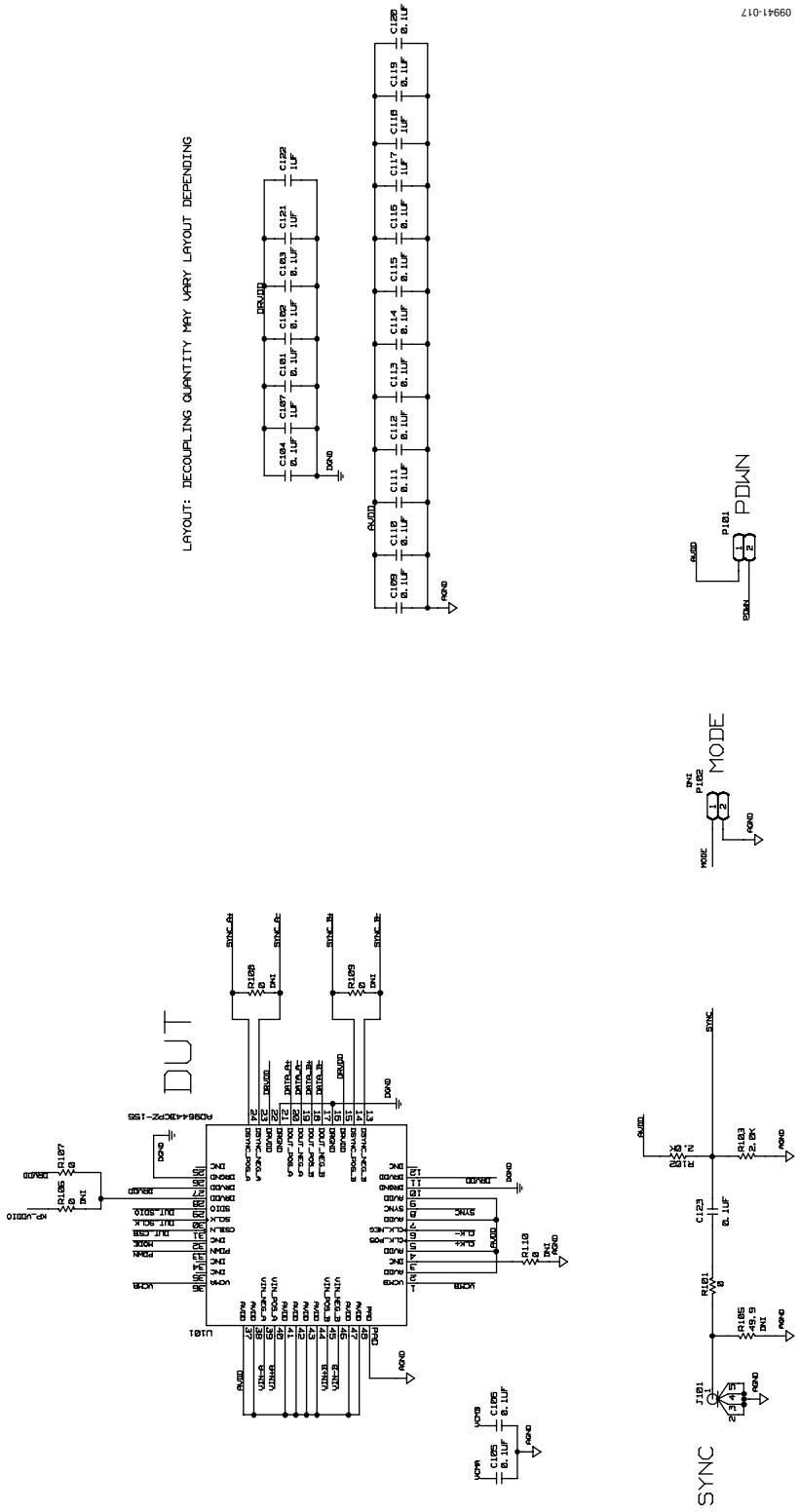

Figure 17. AD9644 DUT and Related Circuits

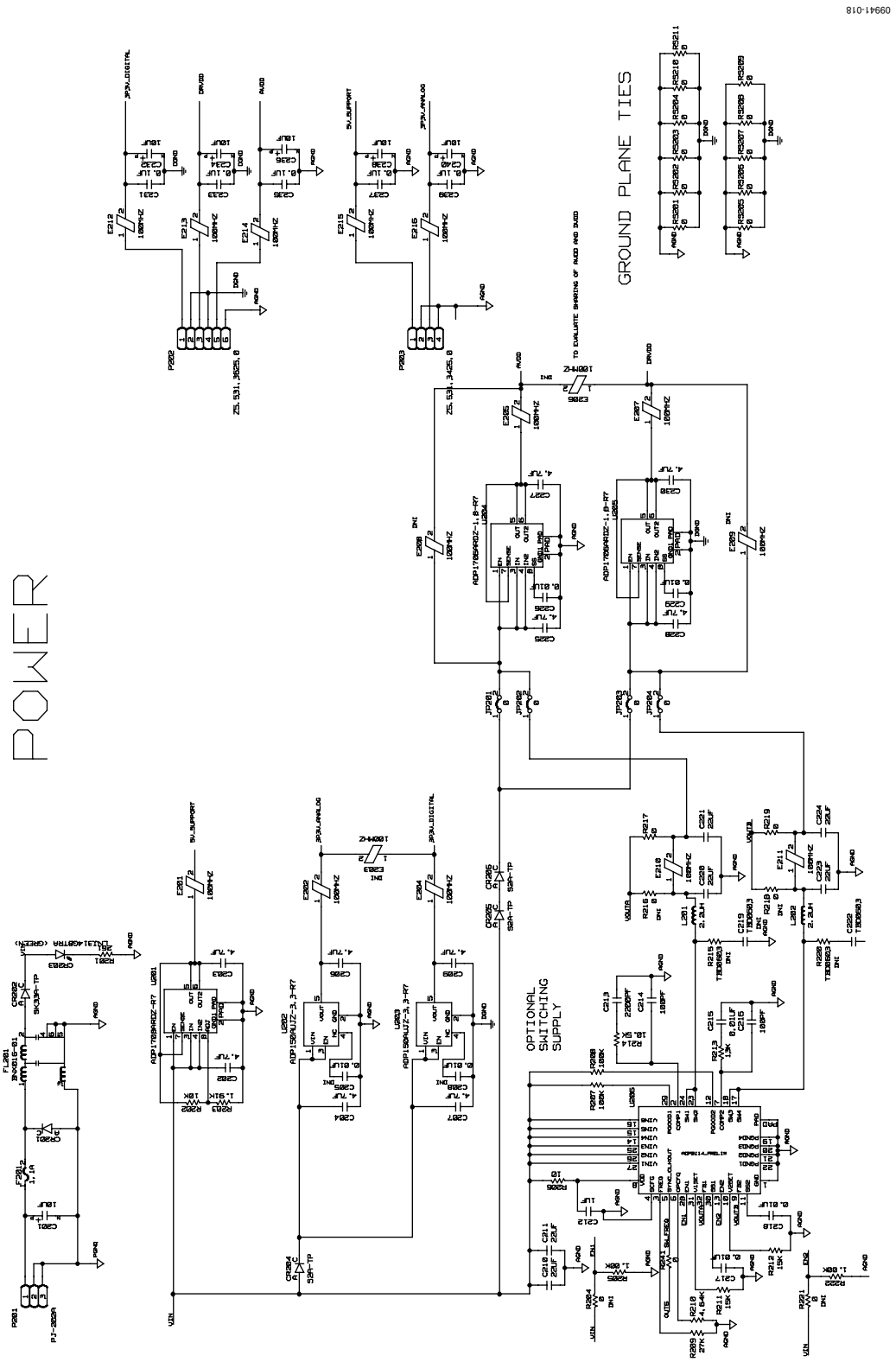

Figure 18. AD9644 Board Power Input and Supply

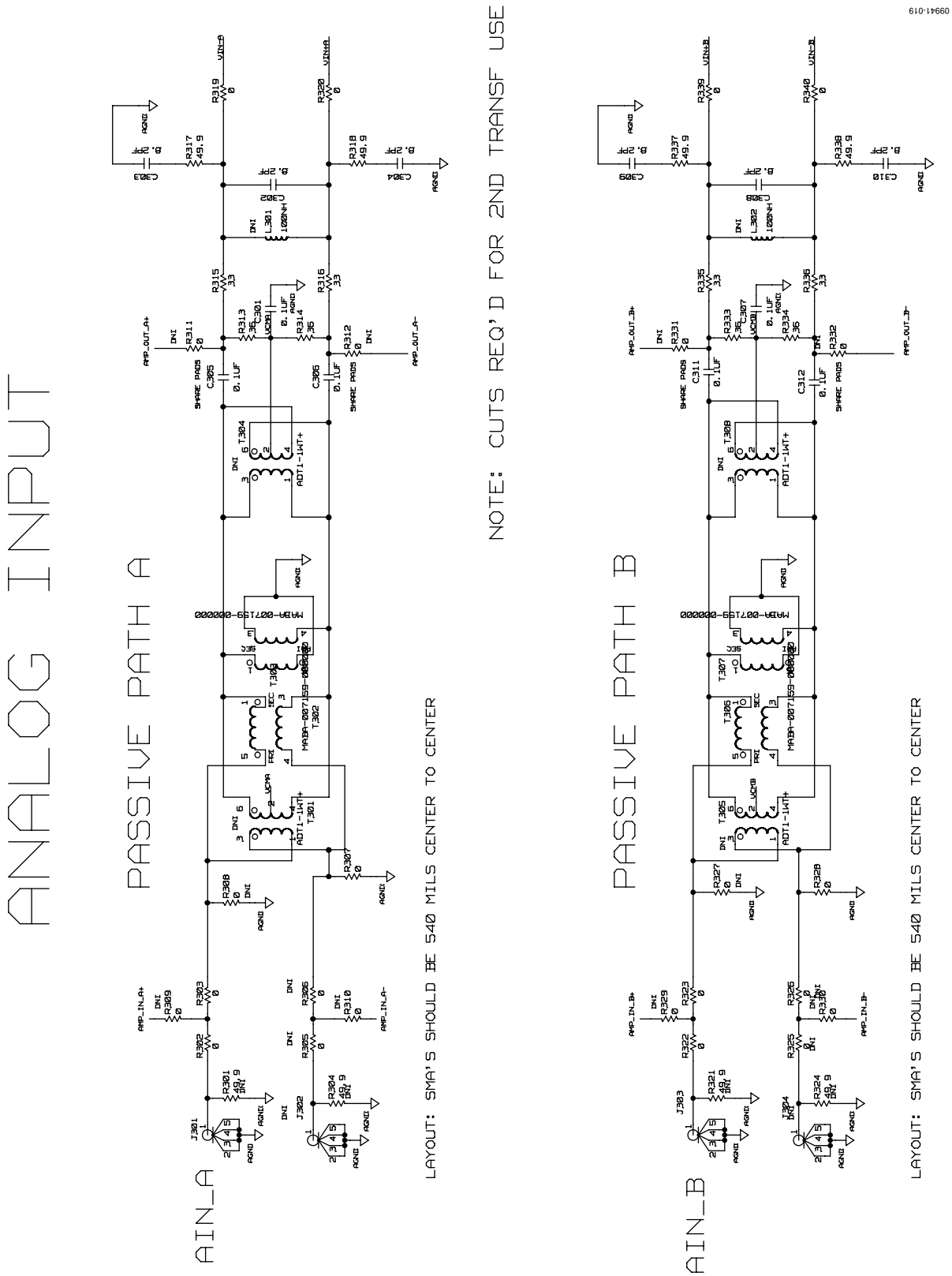

Figure 19. AD9644 Passive Analog Input Circuits

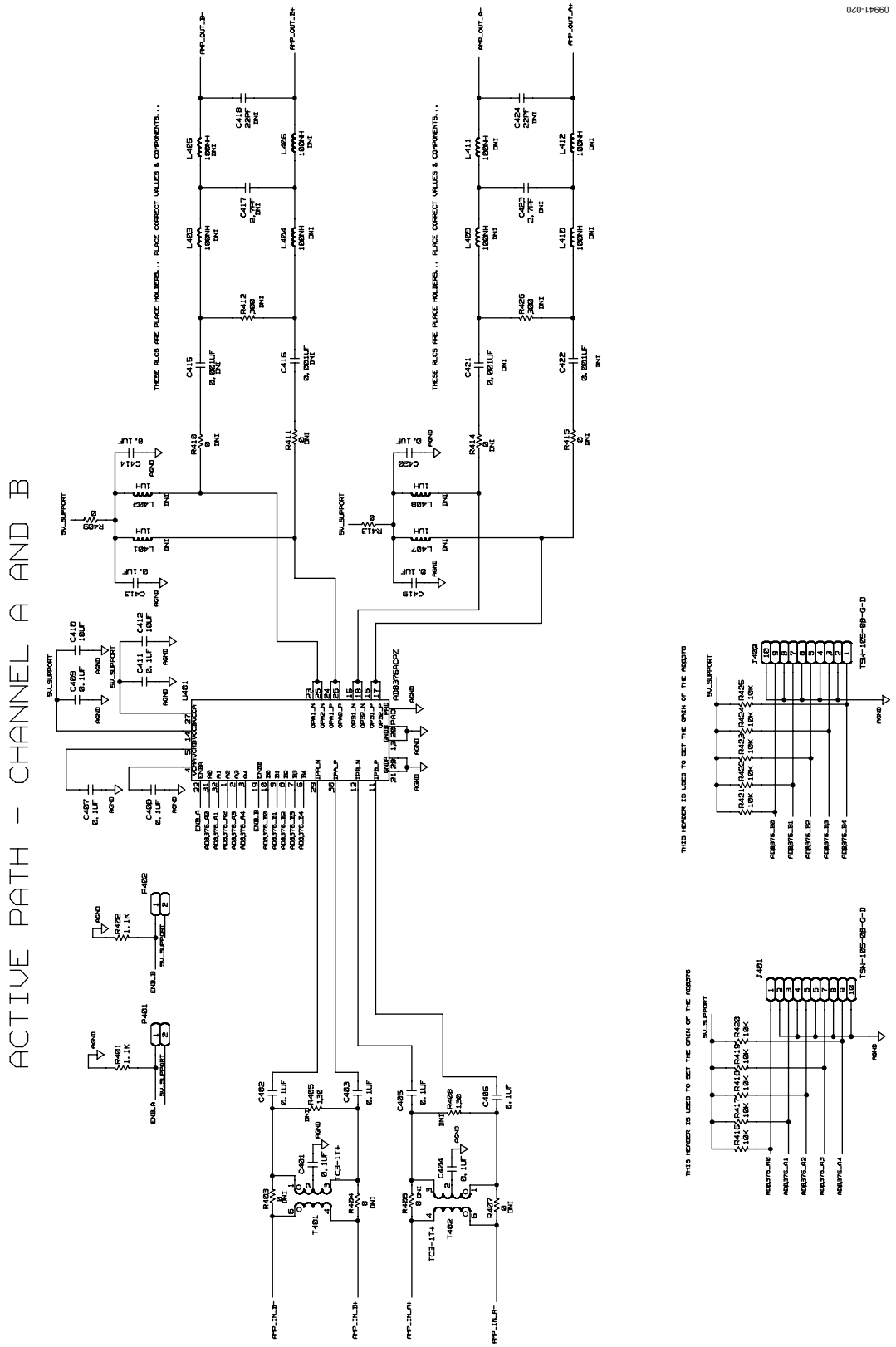

Figure 20. AD9644 Optional Active Input Circuits

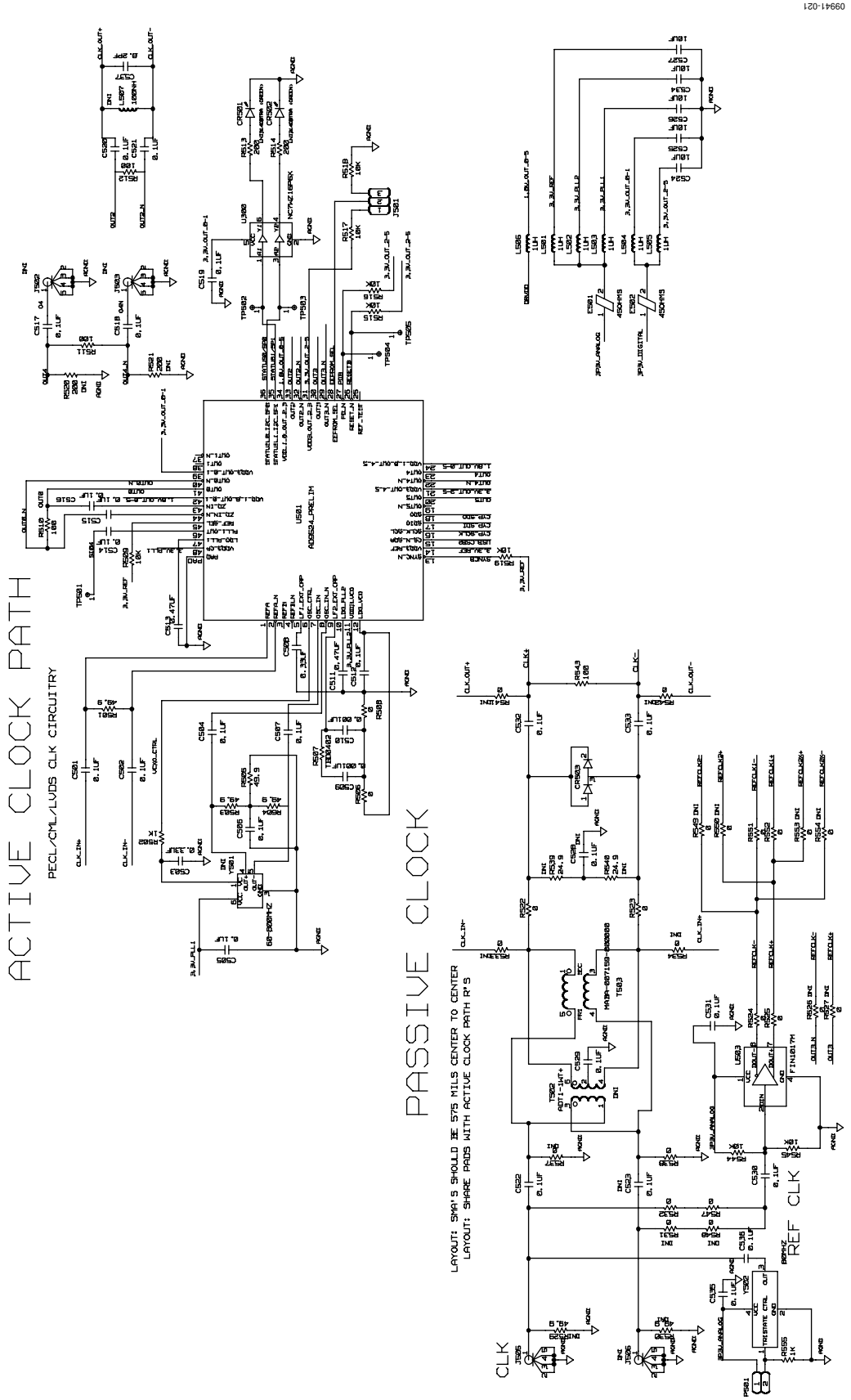

Figure 21. AD9644 Clock Input Circuits

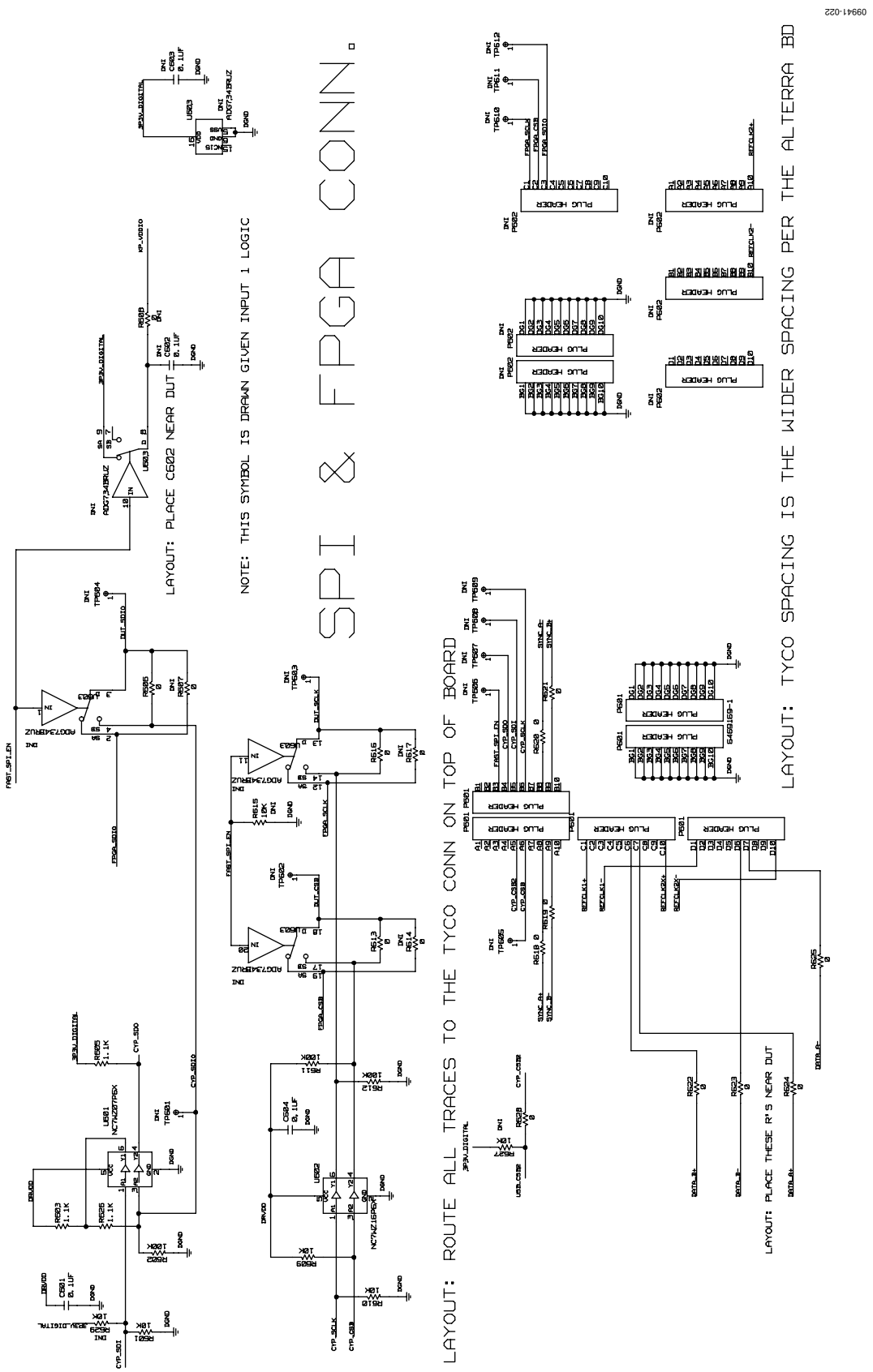

Figure 22. AD9644 SPI Configuration Circuit and FIFO Connections

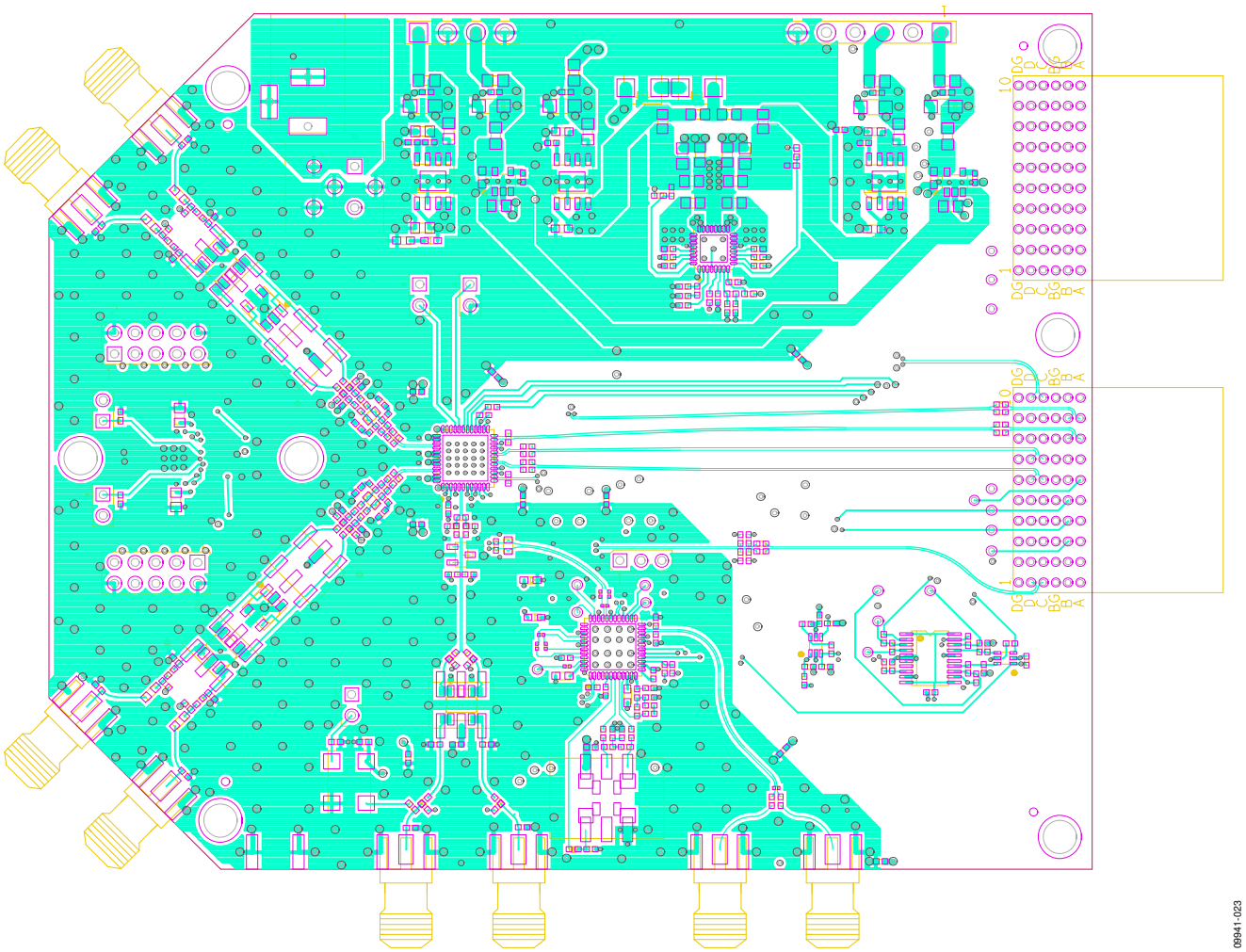

Figure 23. AD9644 Top Side

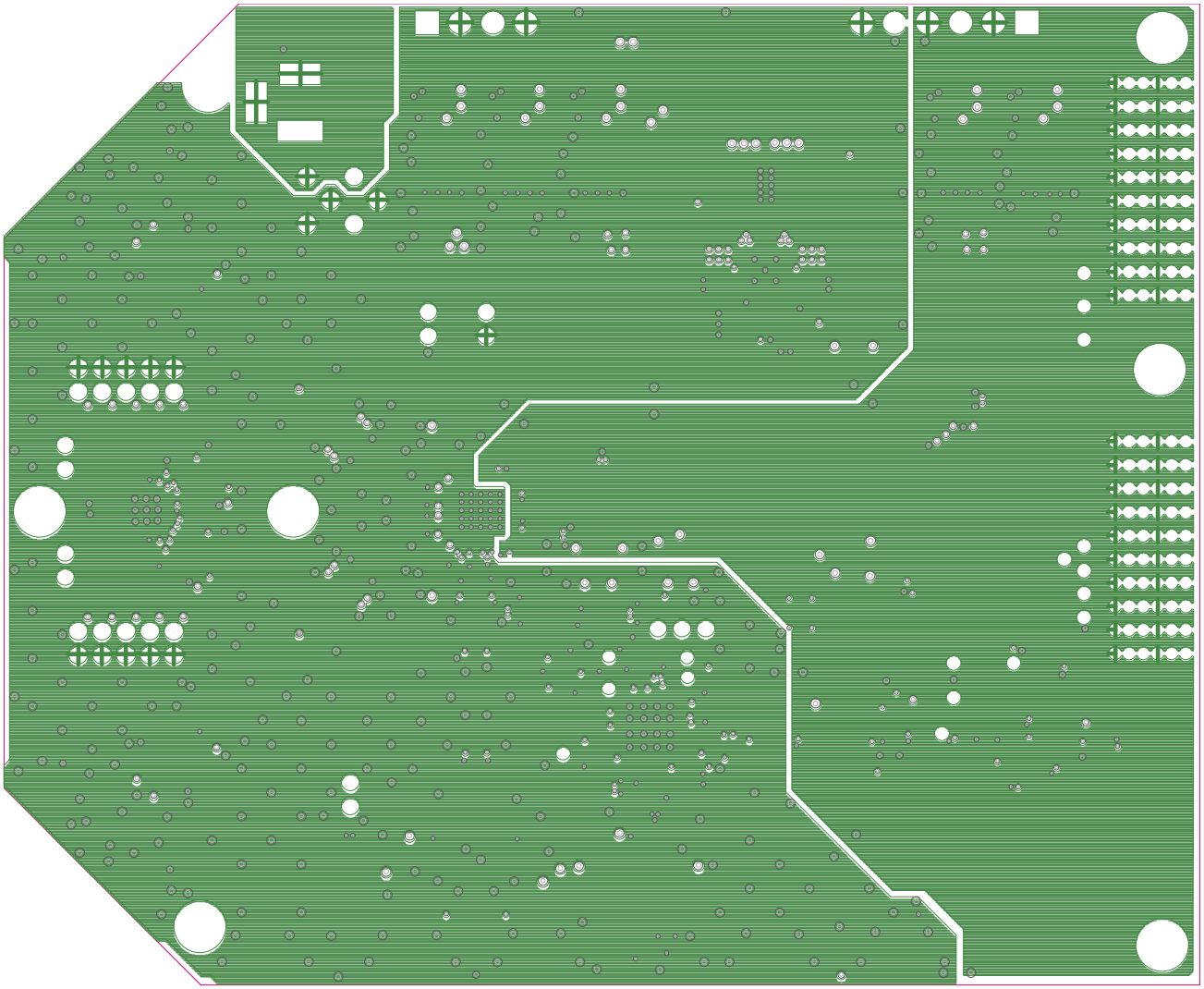

Figure 24. AD9644 Ground Plane (Layer 2)

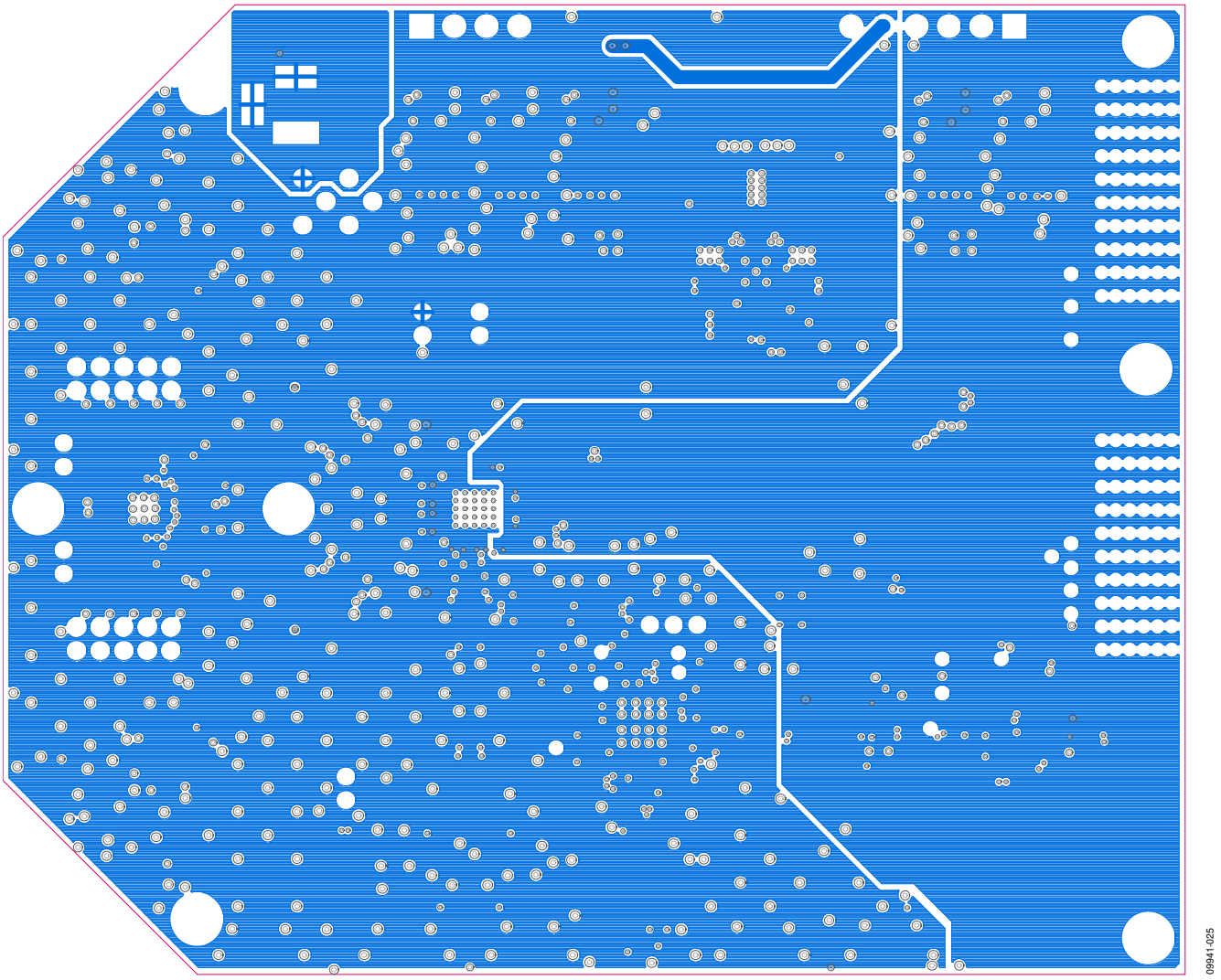

Figure 25. AD9644 Power Plane (Layer 3)

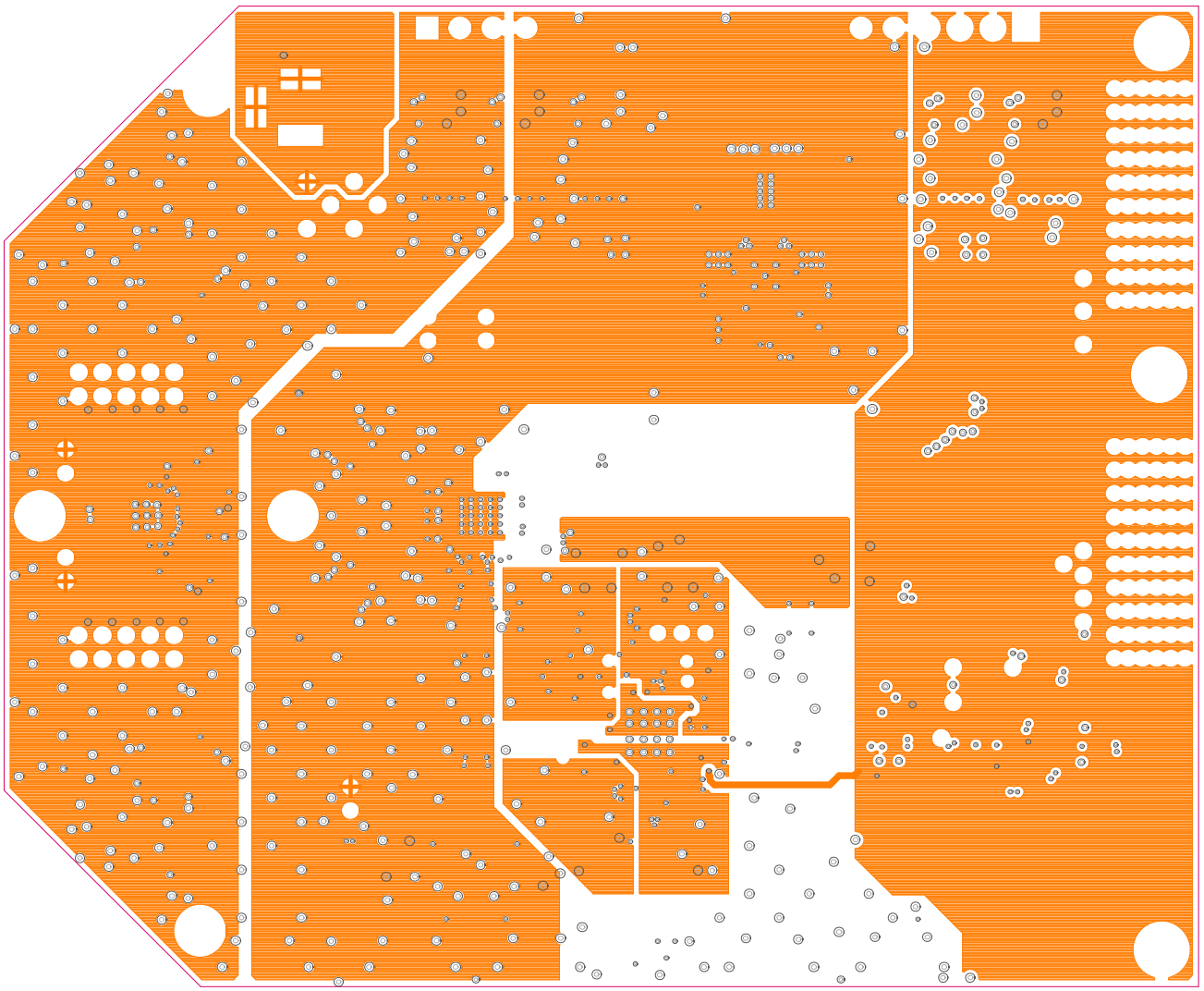

Figure 26. AD9644 Power Plane (Layer 4)

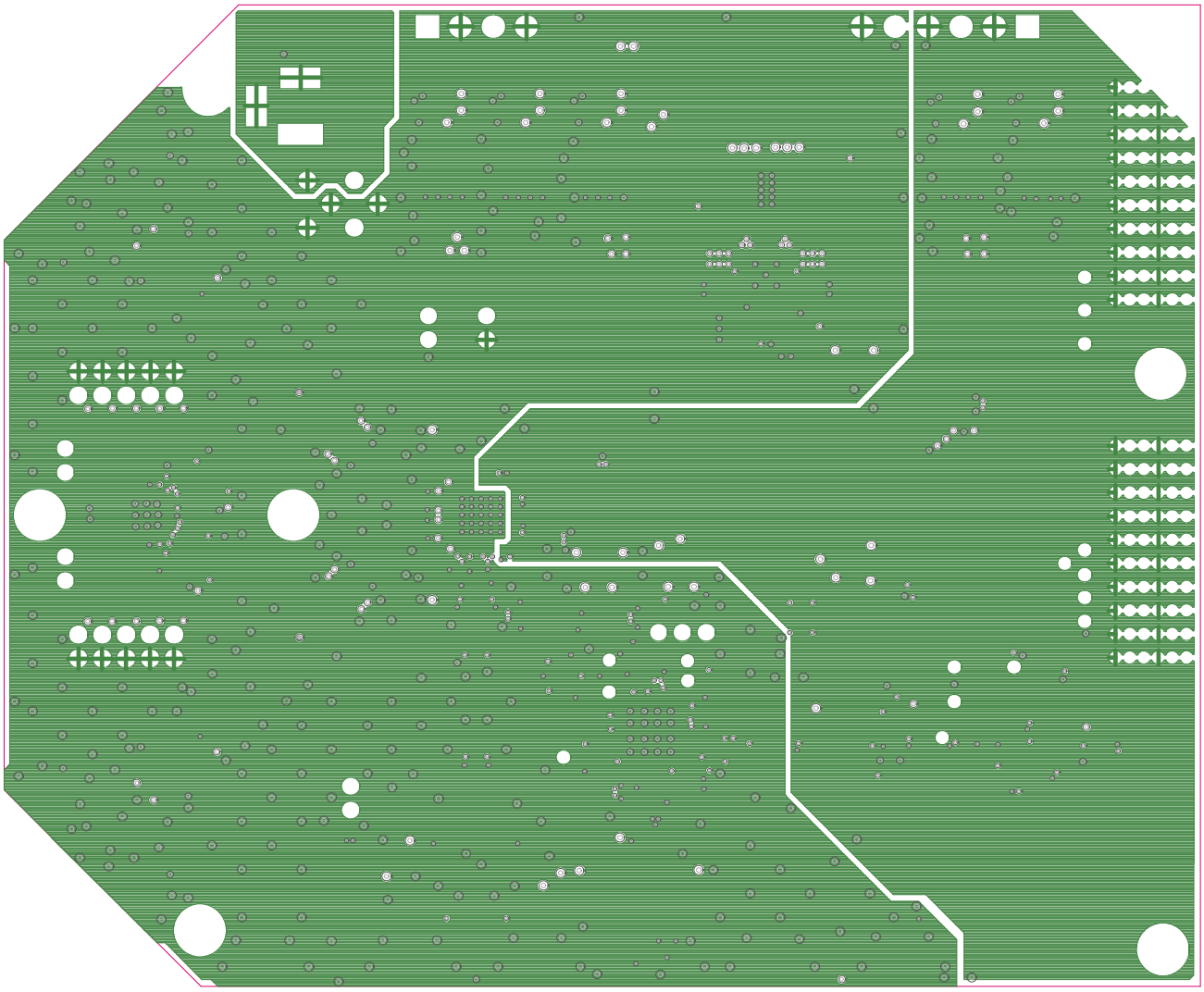

Figure 27. AD9644 Ground Plane (Layer 5)

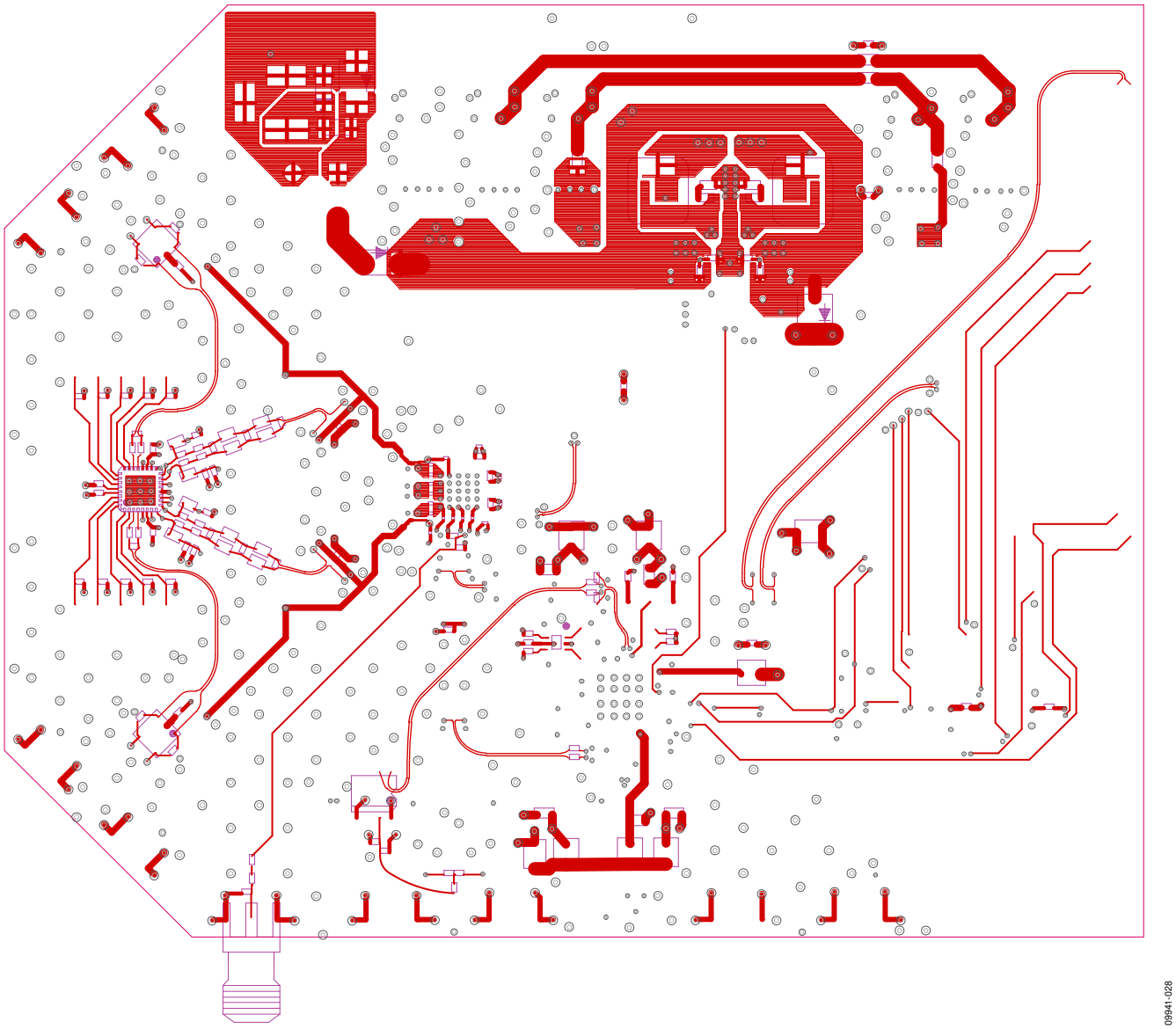

Figure 28. AD9644 Bottom Side