
Chipsmall
深圳市津利帝科技有限公司
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采购部

ANALOG DEVICES

14-Bit, 170 MSPS/210 MSPS/250 MSPS, 1.8 V Analog-to-Digital Converter (ADC)

Data Sheet **AD9642**

FEATURES

- SNR = 71.0 dBFS at 185 MHz A_{IN} and 250 MSPS
- SFDR = 83 dBc at 185 MHz A_{IN} and 250 MSPS
- −152.0 dBFS/Hz input noise at 200 MHz, −1 dBFS A_{IN}, 250 MSPS
- Total power consumption: 390 mW at 250 MSPS
- 1.8 V supply voltages
- LVDS (ANSI-644 levels) outputs
- Integer 1-to-8 input clock divider (625 MHz maximum input)
- Sample rates of up to 250 MSPS
- Internal ADC voltage reference
- Flexible analog input range
  - 1.4 V p-p to 2.0 V p-p (1.75 V p-p nominal)
- ADC clock duty cycle stabilizer
- Serial port control
- Energy saving power-down modes

APPLICATIONS

- Communications
- Diversity radio systems
- Multimode digital receivers (3G)
- TD-SCDMA, WiMAX, WCDMA, CDMA2000, GSM, EDGE, LTE
- I/Q demodulation systems
- Smart antenna systems
- General-purpose software radios
- Ultrasound equipment
- Broadband data applications

FUNCTIONAL BLOCK DIAGRAM

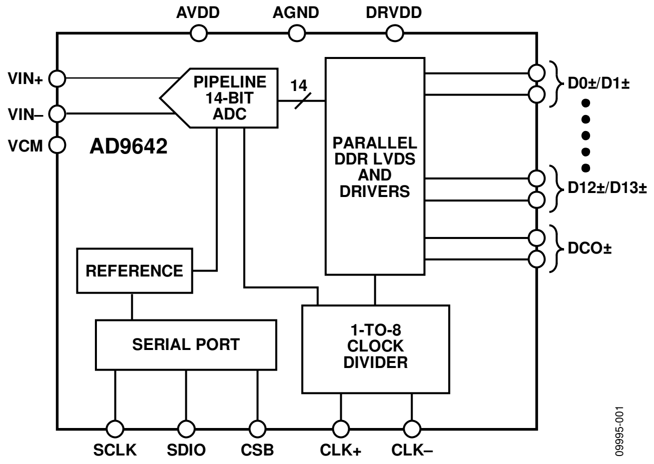

Figure 1.

GENERAL DESCRIPTION

The AD9642 is a 14-bit analog-to-digital converter (ADC) with sampling speeds of up to 250 MSPS. The AD9642 is designed to support communications applications, where low cost, small size, wide bandwidth, and versatility are desired.

The ADC core features a multistage, differential pipelined architecture with integrated output error correction logic. The ADC features wide bandwidth inputs that can support a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. A duty cycle stabilizer (DCS) is provided to compensate for variations in the ADC clock duty cycle, allowing the converter to maintain excellent performance.

The ADC output data is routed directly to the external 14-bit LVDS output port.

Flexible power-down options allow significant power savings, when desired.

Programming for setup and control is accomplished using a 3-wire SPI-compatible serial interface.

The AD9642 is available in a 32-lead LFCSP and is specified over the industrial temperature range of −40°C to +85°C. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Integrated 14-bit, 170 MSPS/210 MSPS/250 MSPS ADC.
2. Operation from a single 1.8 V supply and a separate digital output driver supply accommodating LVDS outputs.
3. Proprietary differential input maintains excellent SNR performance for input frequencies of up to 350 MHz.
4. 3-pin, 1.8 V SPI port for register programming and readback.
5. Pin compatibility with the AD9634, allowing a simple migration from 14 bits to 12 bits, and with the AD6672.

Rev. B **Document Feedback**

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Technical Support **www.analog.com**

AD9642* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9642 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-282: Fundamentals of Sampled Data Systems
- AN-737: How ADIsimADC Models an ADC
- AN-742: Frequency Domain Response of Switched-Capacitor ADCs
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-803: Pin Compatible High Speed ADCs Simplify Design Tasks
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-877: Interfacing to High Speed ADCs via SPI
- AN-878: High Speed ADC SPI Control Software
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD9642: 14-Bit, 170 MSPS/210 MSPS/250 MSPS, 1.8 V Analog-to-Digital Converter (ADC) Data Sheet

Technical Books

- The Data Conversion Handbook, 2005

User Guides

- UG-386: Evaluating the AD9642/AD9634/AD6672 Analog-to-Digital Converters

TOOLS AND SIMULATIONS

- Visual Analog
- AD9642 IBIS Model
- AD9642 LFCSP Analog Input S-Parameter

REFERENCE DESIGNS

- CN0279

REFERENCE MATERIALS

Technical Articles

- MS-1779: Nine Often Overlooked ADC Specifications
- MS-2124: Understanding AC Behaviors of High Speed ADCs
- MS-2210: Designing Power Supplies for High Speed ADC

Tutorials

- MT-002: What the Nyquist Criterion Means to Your Sampled Data System Design
- MT-031: Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"
- MT-075: Differential Drivers for High Speed ADCs Overview

DESIGN RESOURCES

- AD9642 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9642 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

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DOCUMENT FEEDBACK

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7/14—Rev. 0 to Rev. A

Changes to Features Section ... 1
Changes to Full Power Bandwidth Parameter, Table 2 ... 5
Deleted Noise Bandwidth Parameter, Table 2 ... 5

7/11—Revision 0: Initial Version

SPECIFICATIONS

ADC DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, DCS enabled, unless otherwise noted.

Table 1.

		AD9642-170			AD9642-210			AD9642-250			
Parameter	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	14			14			14			Bits
ACCURACY											
No Missing Codes	Full		Guaranteed			Guaranteed			Guaranteed		
Offset Error	Full			±11			±11			±10	mV
Gain Error	Full			+2/−11			+3.5/−8			+3/−7	%FSR
Differential Nonlinearity (DNL)	Full			±0.5			±0.55			±0.6	LSB
	25°C		±0.3			±0.3			±0.32		LSB
Integral Nonlinearity (INL)[1]	Full			±1.3			±2.0			±2.5	LSB
	25°C		±0.6			±0.75			±1.0		LSB
TEMPERATURE DRIFT											
Offset Error	Full		±7			±7			±7		ppm/°C
Gain Error	Full		±52			±105			±75		ppm/°C
INPUT REFERRED NOISE											
VREF = 1.0 V	25°C		0.83			0.85			0.85		LSB rms
ANALOG INPUT											
Input Span	Full		1.75			1.75			1.75		V p-p
Input Capacitance[2]	Full		2.5			2.5			2.5		pF
Input Resistance[3]	Full		20			20			20		kΩ
Input Common-Mode Voltage	Full		0.9			0.9			0.9		V
POWER SUPPLIES											
Supply Voltage											
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
Supply Current											
I_{AVDD}[1]	Full		123	136		129	139		136	146	mA
I_{DRVDD}[1]	Full		50	64		56	67		64	69	mA
POWER CONSUMPTION											
Sine Wave Input (DRVDD = 1.8 V)	Full		311	360		333	371		360	387	mW
Standby Power[4]	Full		50			50			50		mW
Power-Down Power	Full		5			5			5		mW

[1] Measured with a low input frequency, full-scale sine wave.
[2] Input capacitance refers to the effective capacitance between one differential input pin and its complement.
[3] Input resistance refers to the effective resistance between one differential input pin and its complement.
[4] Standby power is measured with a dc input and the CLK pin inactive (that is, set to AVDD or AGND).

ADC AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, unless otherwise noted.

Table 2.

		AD9642-170			AD9642-210			AD9642-250			
Parameter[1]	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE RATIO (SNR)											
f_{IN} = 30 MHz	25°C		72.5			72.4			72.2		dBFS
f_{IN} = 90 MHz	25°C		72.2			72.2			72.0		dBFS
	Full	70.7			70.0						dBFS
f_{IN} = 140 MHz	25°C		71.8			71.6			71.8		dBFS
f_{IN} = 185 MHz	25°C		71.2			71.5			71.4		dBFS
	Full							68.6			dBFS
f_{IN} = 220 MHz	25°C		70.7			71.0			70.9		dBFS
SIGNAL-TO-NOISE AND DISTORTION (SINAD)											
f_{IN} = 30 MHz	25°C		71.5			71.5			71.2		dBFS
f_{IN} = 90 MHz	25°C		71.3			71.3			71.0		dBFS
	Full	69.6			68.7						dBFS
f_{IN} = 140 MHz	25°C		70.8			70.6			70.9		dBFS
f_{IN} = 185 MHz	25°C		70.3			70.5			70.4		dBFS
	Full							67.5			dBFS
f_{IN} = 220 MHz	25°C		69.7			70.1			70.0		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)											
f_{IN} = 30 MHz	25°C		11.6			11.6			11.5		Bits
f_{IN} = 90 MHz	25°C		11.6			11.6			11.5		Bits
f_{IN} = 140 MHz	25°C		11.5			11.4			11.5		Bits
f_{IN} = 185 MHz	25°C		11.4			11.4			11.4		Bits
f_{IN} = 220 MHz	25°C		11.3			11.3			11.3		Bits
WORST SECOND OR THIRD HARMONIC											
f_{IN} = 30 MHz	25°C		−96			−96			−90		dBc
f_{IN} = 90 MHz	25°C		−95			−92			−89		dBc
	Full			−82			−79				dBc
f_{IN} = 140 MHz	25°C		−97			−94			−90		dBc
f_{IN} = 185 MHz	25°C		−86			−95			−86		dBc
	Full									−80	dBc
f_{IN} = 220 MHz	25°C		−84			−84			−86		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)											
f_{IN} = 30 MHz	25°C		96			96			90		dBc
f_{IN} = 90 MHz	25°C		95			92			89		dBc
	Full	82			79						dBc
f_{IN} = 140 MHz	25°C		97			94			90		dBc
f_{IN} = 185 MHz	25°C		86			95			86		dBc
	Full							80			dBc
f_{IN} = 220 MHz	25°C		84			84			86		dBc
WORST OTHER (HARMONIC OR SPUR)											
f_{IN} = 30 MHz	25°C		−99			−98			−95		dBc
f_{IN} = 90 MHz	25°C		−95			−97			−98		dBc
	Full			−87			−81				dBc
f_{IN} = 140 MHz	25°C		−98			−96			−97		dBc
f_{IN} = 185 MHz	25°C		−96			−97			−96		dBc
	Full									−81	dBc
f_{IN} = 220 MHz	25°C		−97			−94			−95		dBc

Parameter[1]	Temperature	AD9642-170			AD9642-210			AD9642-250			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TWO-TONE SFDR											
f_{IN} = 184.1 MHz, 187.1 MHz (−7 dBFS)	25°C		87			88			88		dBc
FULL POWER BANDWIDTH	25°C		1000			1000			1000		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	10		22	µA
Low Level Input Current	Full	−22		−10	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	12	15	18	kΩ
LOGIC INPUT (CSB)[1]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	50		71	µA
Low Level Input Current	Full	−5		+5	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SCLK)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	45		70	µA
Low Level Input Current	Full	−5		+5	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUTS (SDIO)[1]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	45		70	µA
Low Level Input Current	Full	−5		+5	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS					
LVDS Data and OR Outputs (OR+, OR−)					
Differential Output Voltage (V_{OD}), ANSI Mode	Full	250	350	450	mV
Output Offset Voltage (V_{OS}), ANSI Mode	Full	1.15	1.25	1.35	V
Differential Output Voltage (V_{OD}), Reduced Swing Mode	Full	150	200	280	mV
Output Offset Voltage (V_{OS}), Reduced Swing Mode	Full	1.15	1.25	1.35	V

[1] Pull-up.
[2] Pull-down.

SWITCHING SPECIFICATIONS

Table 4.

		AD9642-170			AD9642-210			AD9642-250			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUT PARAMETERS											
Input Clock Rate	Full			625			625			625	MHz
Conversion Rate[1]	Full	40		170	40		210	40		250	MSPS
CLK Period—Divide-by-1 Mode (t_{CLK})	Full	5.8			4.8			4			ns
CLK Pulse Width High (t_{CH})											
Divide-by-1 Mode, DCS Enabled	Full	2.61	2.9	3.19	2.16	2.4	2.64	1.8	2.0	2.2	ns
Divide-by-1 Mode, DCS Disabled	Full	2.76	2.9	3.05	2.28	2.4	2.52	1.9	2.0	2.1	ns
Divide-by-2 Mode Through Divide-by-8 Mode	Full	0.8			0.8			0.8			ns
Aperture Delay (t_A)	Full		1.0			1.0			1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.1			0.1			0.1		ps rms
DATA OUTPUT PARAMETERS											
Data Propagation Delay (t_{PD})	Full	4.1	4.7	5.2	4.1	4.7	5.2	4.1	4.7	5.2	ns
DCO Propagation Delay (t_{DCO})	Full	4.7	5.3	5.8	4.7	5.3	5.8	4.7	5.3	5.8	ns
DCO-to-Data Skew (t_{SKEW})	Full	0.3	0.5	0.7	0.3	0.5	0.7	0.3	0.5	0.7	ns
Pipeline Delay (Latency)	Full		10			10			10		Cycles
Wake-Up Time (from Standby)	Full		10			10			10		µs
Wake-Up Time (from Power-Down)	Full		100			100			100		µs
Out-of-Range Recovery Time	Full		3			3			3		Cycles

[1] Conversion rate is the clock rate after the divider.

Timing Diagram

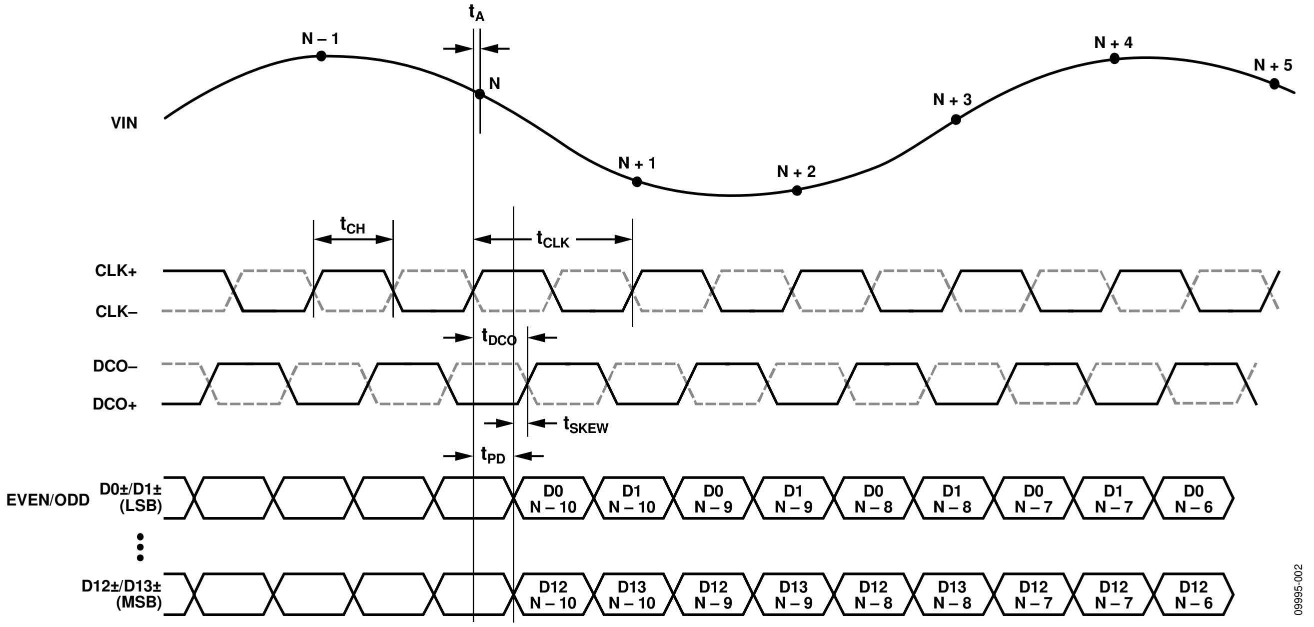


Figure 2. LVDS Data Output Timing

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPI TIMING REQUIREMENTS	See Figure 58 for SPI timing diagram				
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK should be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK should be in a logic low state	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 58)	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 58)	10			ns

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
VIN+, VIN− to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
VCM to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to DRVDD + 0.3 V
SCLK to AGND	−0.3 V to DRVDD + 0.3 V
SDIO to AGND	−0.3 V to DRVDD + 0.3 V
D0−/D1−, D0+/D1+ Through D12−/D13−, D12+/D13+ to AGND	−0.3 V to DRVDD + 0.3 V
DCO+, DCO− to AGND	−0.3 V to DRVDD + 0.3 V
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +125°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the customer board increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JC}[1, 3]	θ_{JB}[1, 4]	Unit
32-Lead LFCSP 5 mm × 5 mm (CP-32-12)	0	37.1	3.1	20.7	°C/W
	1.0	32.4			°C/W
	2.0	29.1			°C/W

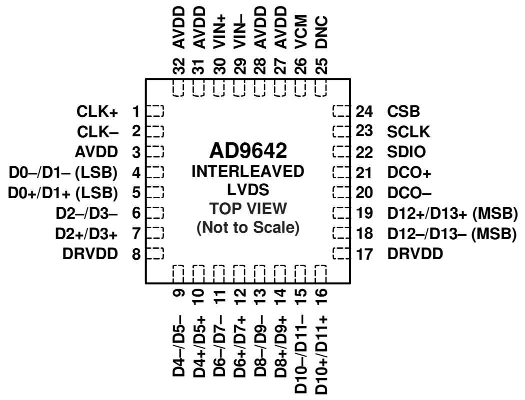
[1] Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. As shown in Table 7, airflow increases heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces—through holes, ground, and power planes—reduces the θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED THERMAL PADDLE ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE PART. THIS EXPOSED PADDLE MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.
2. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

09995-003

Figure 3. LFCSP Pin Configuration (Top View)

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
8, 17	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
3, 27, 28, 31, 32	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
0	AGND, Exposed Paddle	Ground	Analog Ground. The exposed thermal paddle on the bottom of the package provides the analog ground for the part. This exposed paddle must be connected to ground for proper operation.
25	DNC		Do Not Connect. Do not connect to this pin.
ADC Analog			
30	VIN+	Input	Differential Analog Input Pin (+).
29	VIN−	Input	Differential Analog Input Pin (−).
26	VCM	Output	Common-Mode Level Bias Output for Analog Inputs. This pin should be decoupled to ground using a 0.1 µF capacitor.
1	CLK+	Input	ADC Clock Input—True.
2	CLK−	Input	ADC Clock Input—Complement.
Digital Outputs			
5	D0+/D1+ (LSB)	Output	DDR LVDS Output Data 0/1—True.
4	D0−/D1− (LSB)	Output	DDR LVDS Output Data 0/1—Complement.
7	D2+/D3+	Output	DDR LVDS Output Data 2/3—True.
6	D2−/D3−	Output	DDR LVDS Output Data 2/3—Complement.
10	D4+/D5+	Output	DDR LVDS Output Data 4/5—True.
9	D4−/D5−	Output	DDR LVDS Output Data 4/5—Complement.
12	D6+/D7+	Output	DDR LVDS Output Data 6/7—True.
11	D6−/D7−	Output	DDR LVDS Output Data 6/7—Complement.
14	D8+/D9+	Output	DDR LVDS Output Data 8/9—True.
13	D8−/D9−	Output	DDR LVDS Output Data 8/9—Complement.
16	D10+/D11+	Output	DDR LVDS Output Data 10/11—True.
15	D10−/D11−	Output	DDR LVDS Output Data 10/11—Complement.
19	D12+/D13+ (MSB)	Output	DDR LVDS Output Data 12/13—True.
18	D12−/D13− (MSB)	Output	DDR LVDS Output Data 12/13—Complement.
21	DCO+	Output	LVDS Data Clock Output—True.
20	DCO−	Output	LVDS Data Clock Output—Complement.
SPI Control			
23	SCLK	Input	SPI Serial Clock.
22	SDIO	Input/output	SPI Serial Data I/O.
24	CSB	Input	SPI Chip Select (Active Low).

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, sample rate = maximum rate per speed grade, DCS enabled, 1.75 V p-p differential input, VIN = −1.0 dBFS, 32k sample, T_A = 25°C, unless otherwise noted.

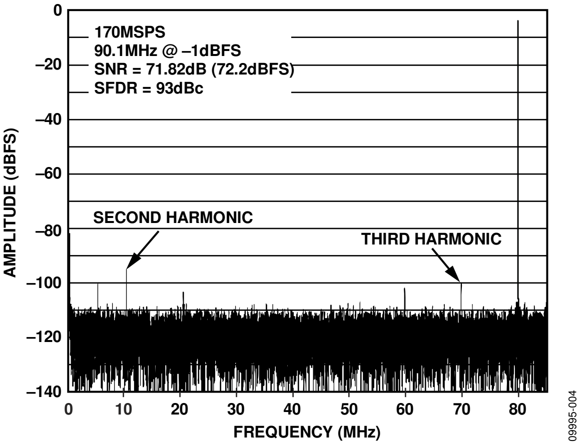


Figure 4. AD9642-170 Single-Tone FFT with f_{IN} = 90.1 MHz

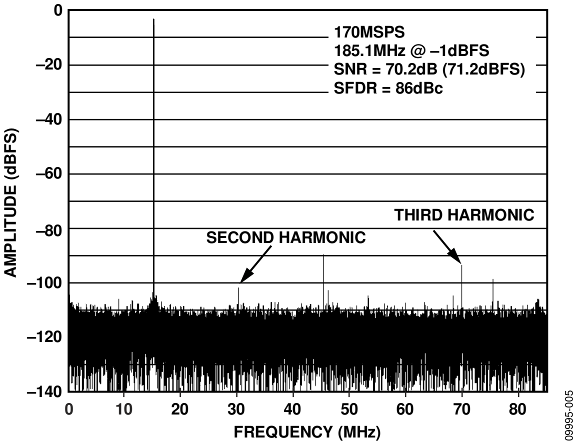


Figure 5. AD9642-170 Single-Tone FFT with f_{IN} = 185.1 MHz

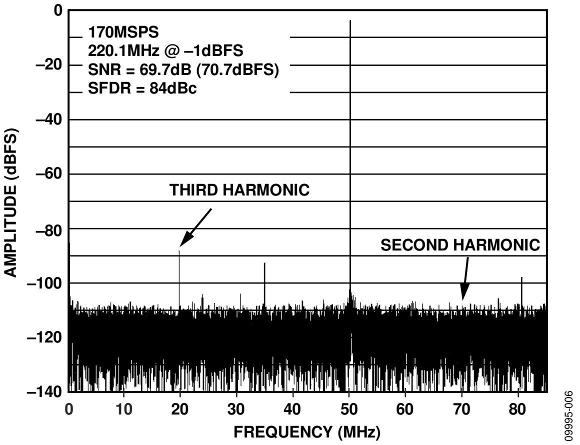


Figure 6. AD9642-170 Single-Tone FFT with f_{IN} = 220.1 MHz

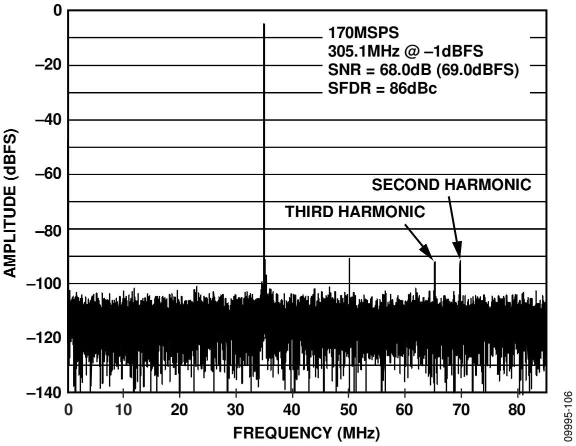


Figure 7. AD9642-170 Single-Tone FFT with f_{IN} = 305.1 MHz

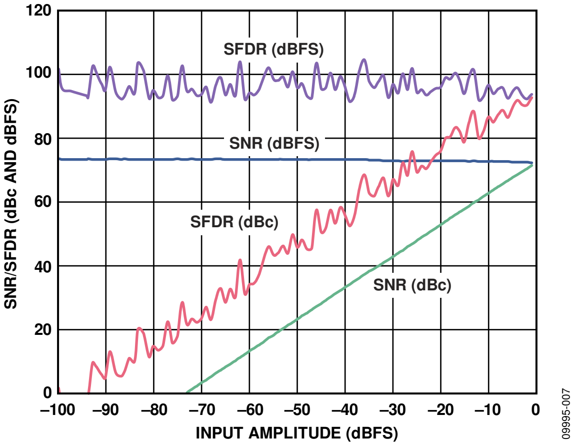


Figure 8. AD9642-170 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 90.1 MHz, f_S = 170 MSPS

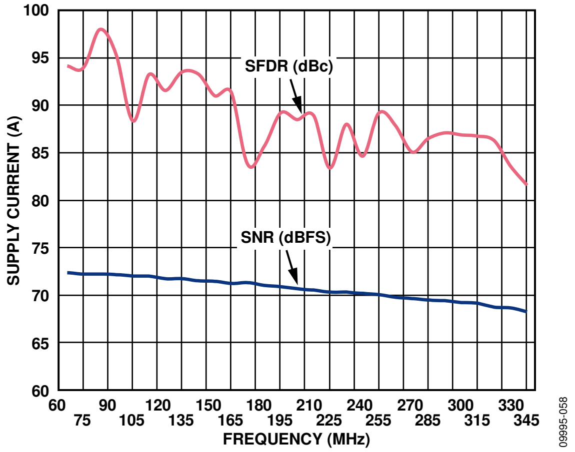


Figure 9. AD9642-170 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}), f_S = 170 MSPS

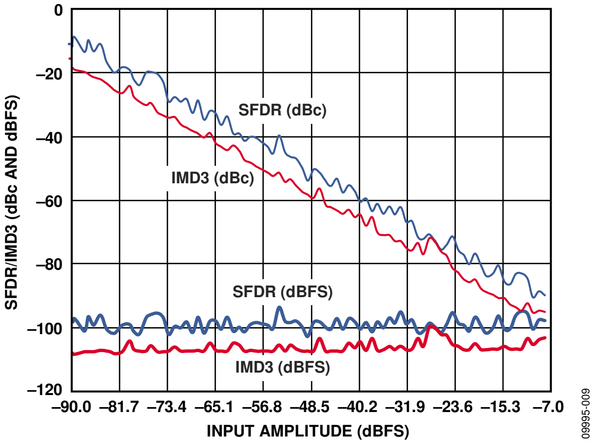


Figure 10. AD9642-170 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz, f_S = 170 MSPS

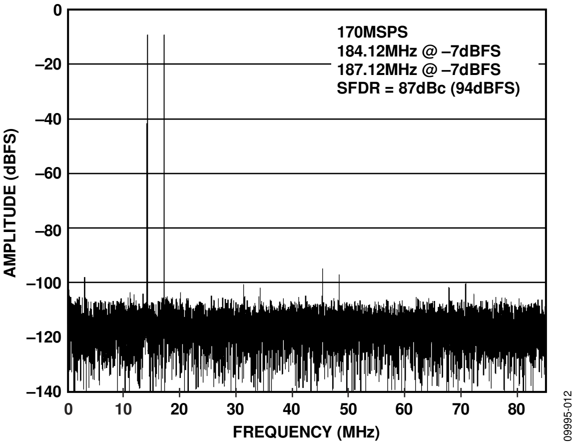


Figure 13. AD9642-170 Two Tone FFT with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz

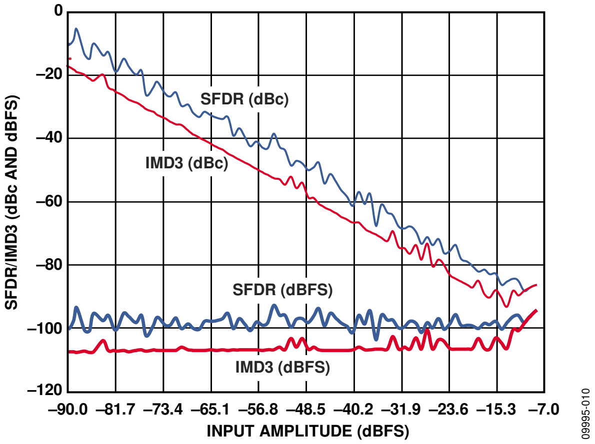


Figure 11. AD9642-170 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz, f_S = 170 MSPS

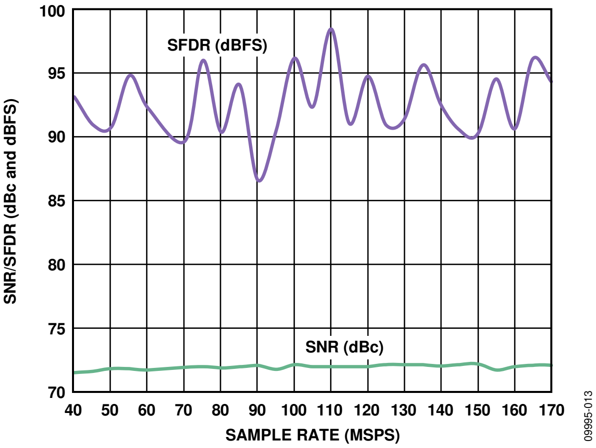


Figure 14. AD9642-170 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 90 MHz

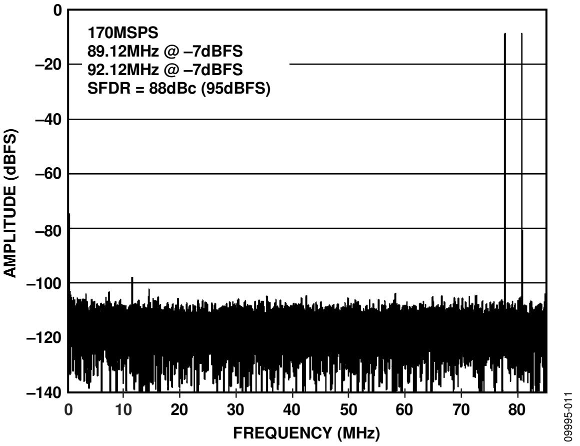


Figure 12. AD9642-170 Two-Tone FFT with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz

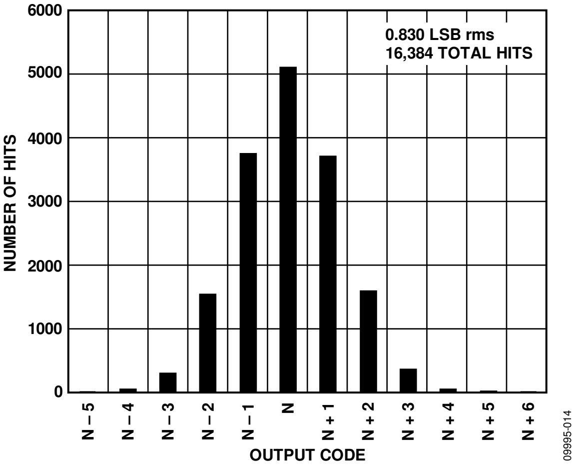


Figure 15. AD9642-170 Grounded Input Histogram, f_S = 170 MSPS

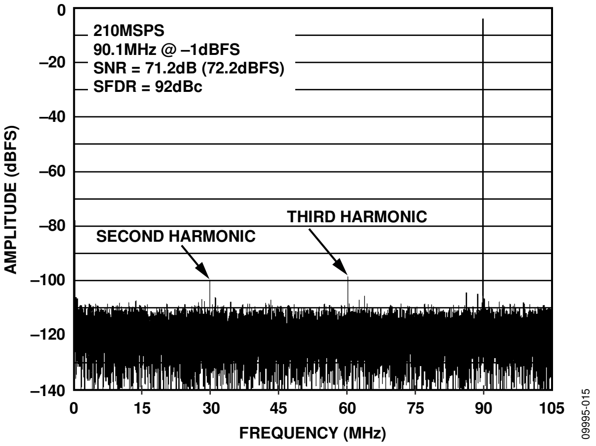


Figure 16. AD9642-210 Single-Tone FFT with f_{IN} = 90.1 MHz

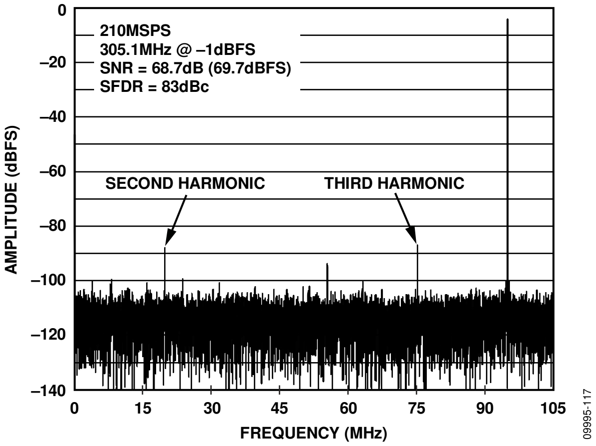


Figure 19. AD9642-210 Single-Tone FFT with f_{IN} = 305.1 MHz

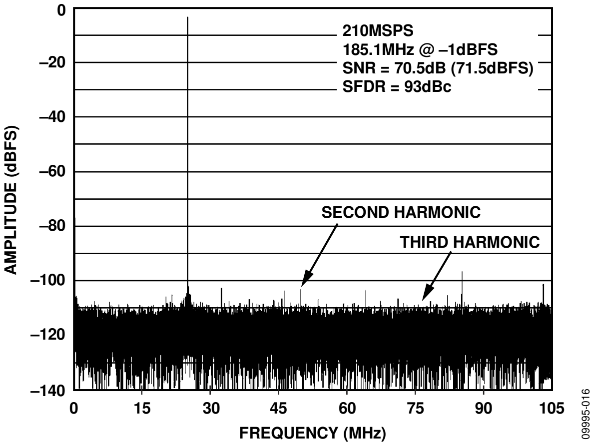


Figure 17. AD9642-210 Single-Tone FFT with f_{IN} = 185.1 MHz

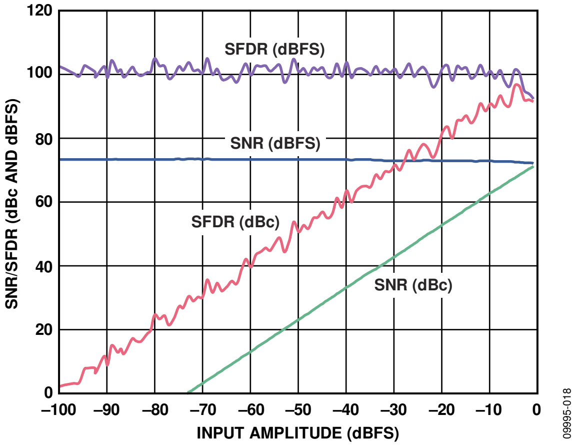


Figure 20. AD9642-210 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 90.1 MHz, f_S = 210 MSPS

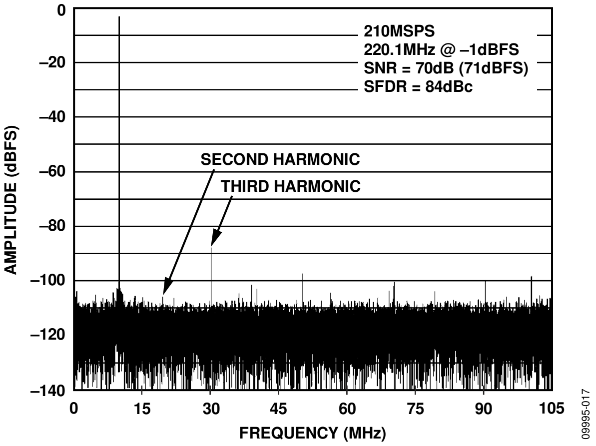


Figure 18. AD9642-210 Single-Tone FFT with f_{IN} = 220.1 MHz

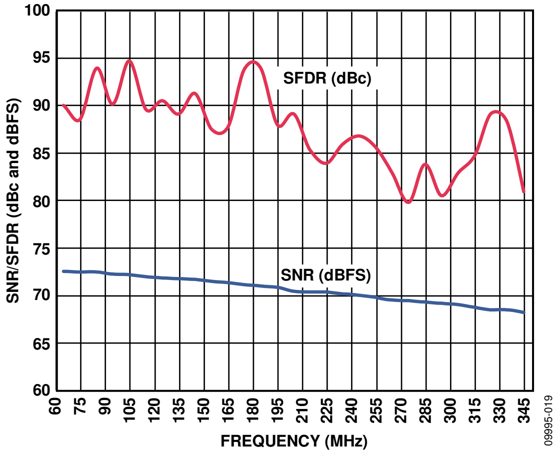


Figure 21. AD9642-210 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}), f_S = 210 MSPS

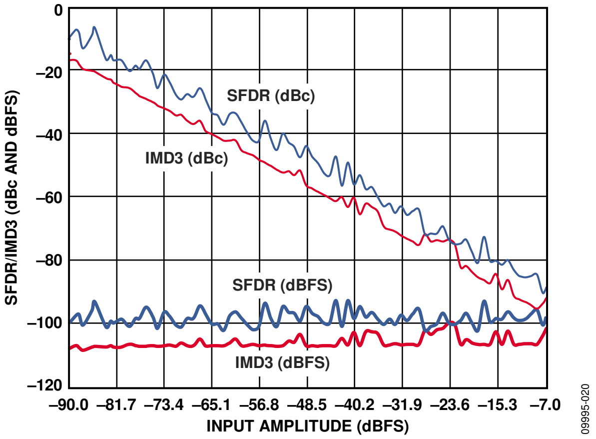


Figure 22. AD9642-210 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz, f_S = 210 MSPS

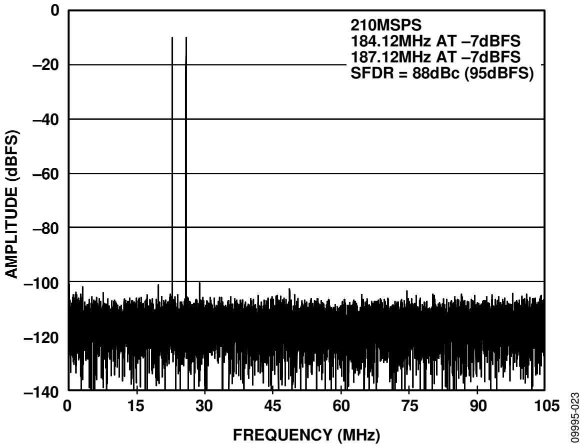


Figure 25. AD9642-210 Two-Tone FFT with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz

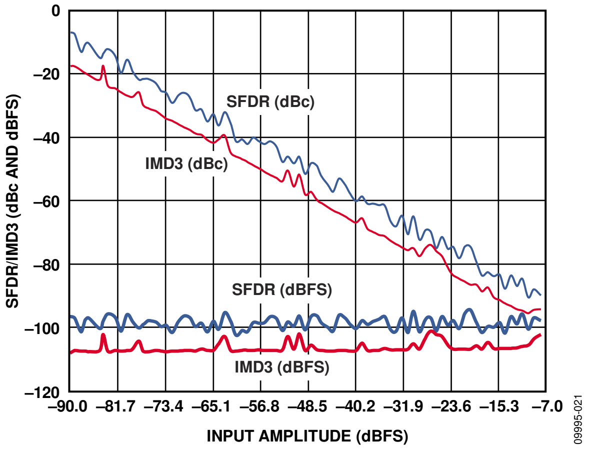


Figure 23. AD9642-210 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz, f_S = 210 MSPS

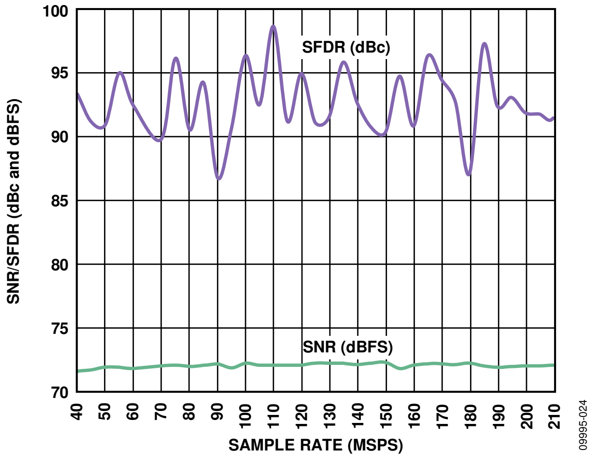


Figure 26. AD9642-210 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 90 MHz

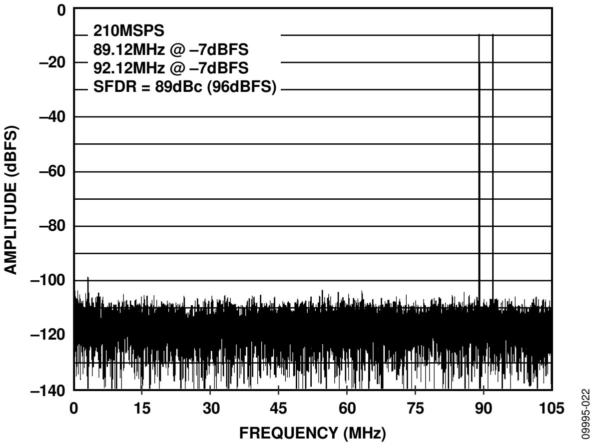


Figure 24. AD9642-210 Two-Tone FFT with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz

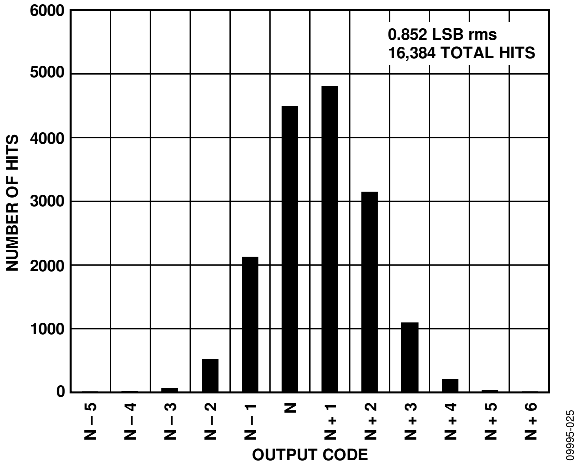


Figure 27. AD9642-210 Grounded Input Histogram, f_S = 210 MSPS

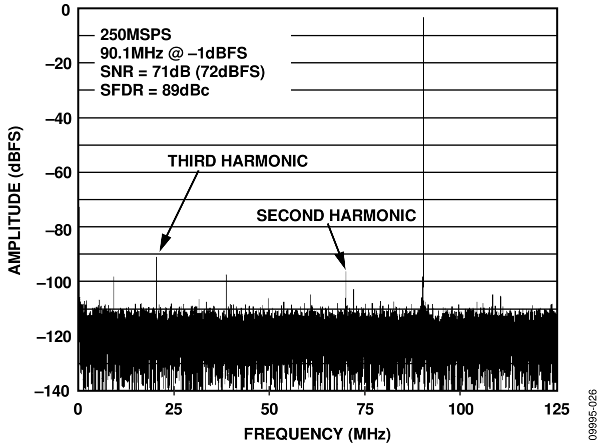


Figure 28. AD9642-250 Single-Tone FFT with f_{IN} = 90.1 MHz

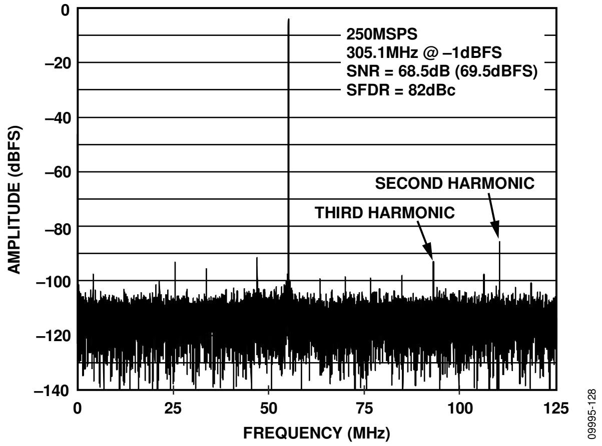


Figure 31. AD9642-250 Single-Tone FFT with f_{IN} = 305.1 MHz

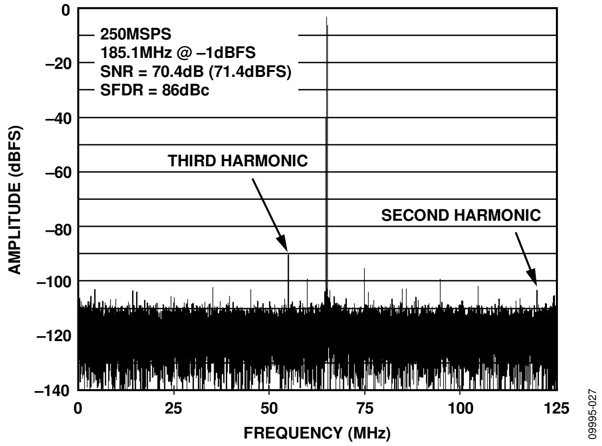


Figure 29. AD9642-250 Single-Tone FFT with f_{IN} = 185.1 MHz

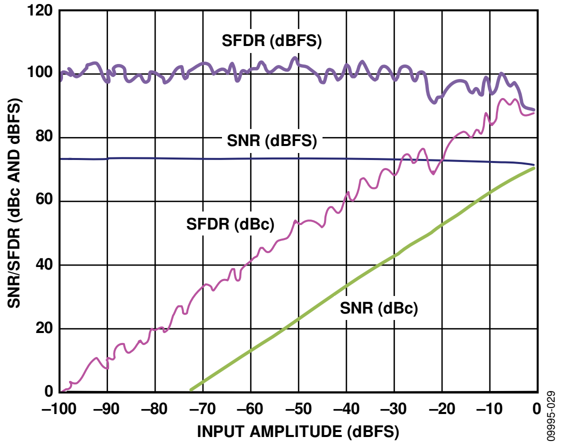


Figure 32. AD9642-250 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 90.1 MHz, f_S = 250 MSPS

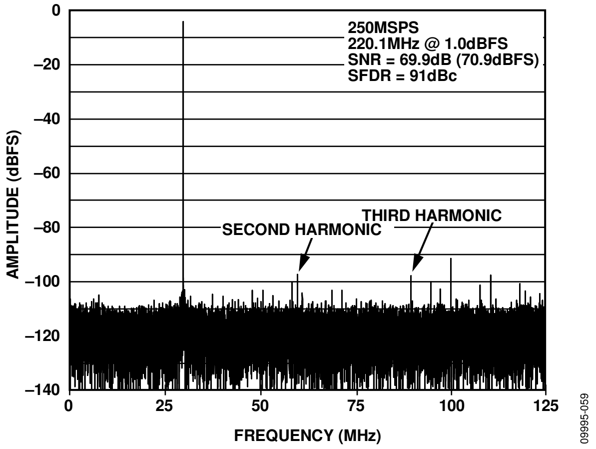


Figure 30. AD9642-250 Single-Tone FFT with f_{IN} = 220.1 MHz

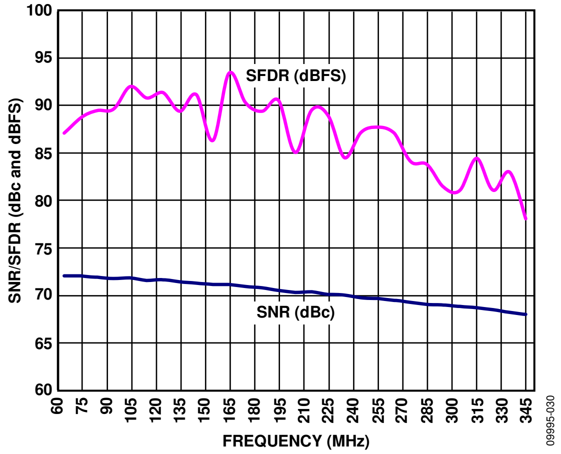


Figure 33. AD9642-250 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}), f_S = 250 MSPS

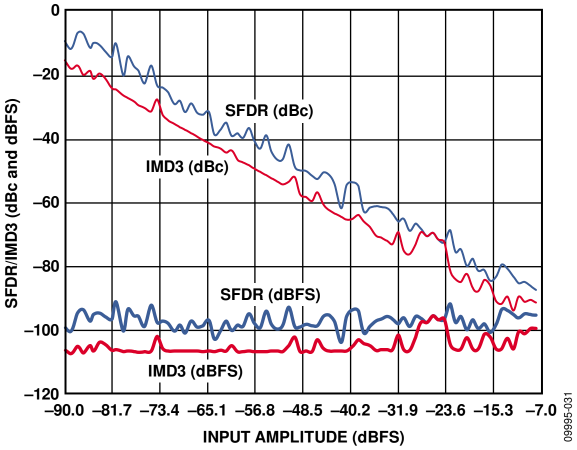


Figure 34. AD9642-250 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz, f_S = 250 MSPS

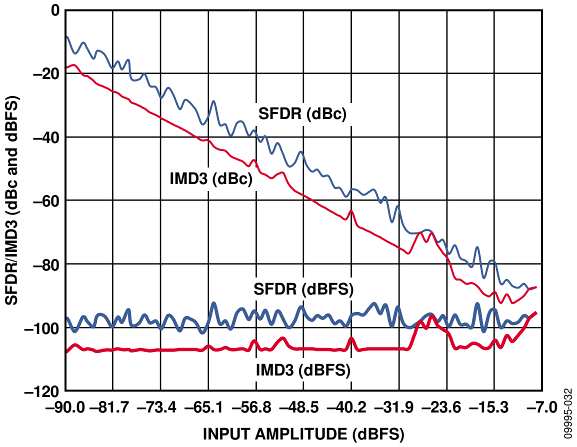


Figure 35. AD9642-250 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz, f_S = 250 MSPS

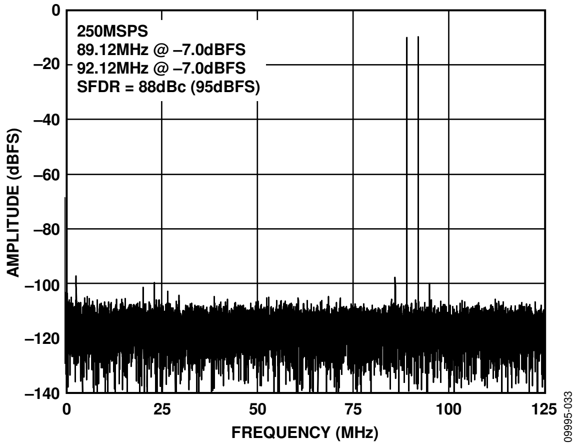


Figure 36. AD9642-250 Two-Tone FFT with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz

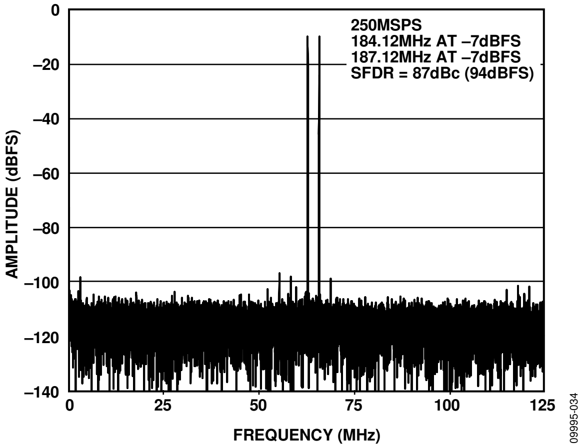


Figure 37. AD9642-250 Two Tone FFT with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz

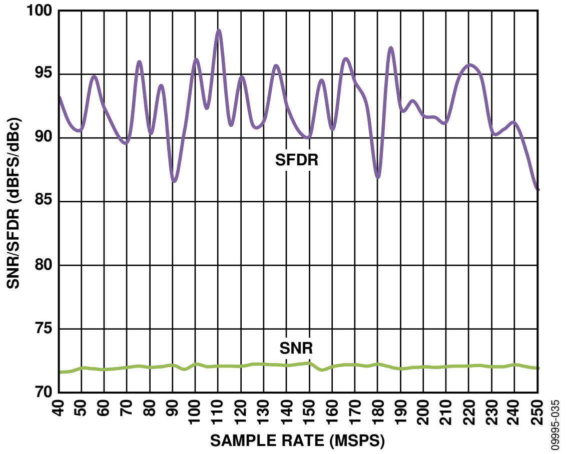


Figure 38. AD9642-250 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 90 MHz

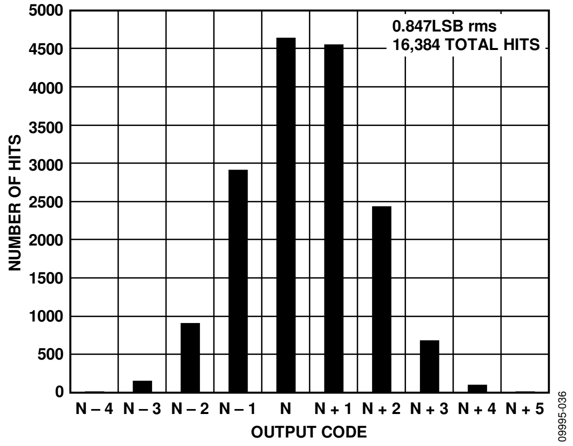


Figure 39. AD9642-250 Grounded Input Histogram, f_S = 250 MSPS

EQUIVALENT CIRCUITS

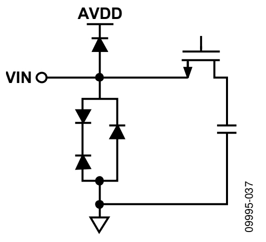


Figure 40. Equivalent Analog Input Circuit

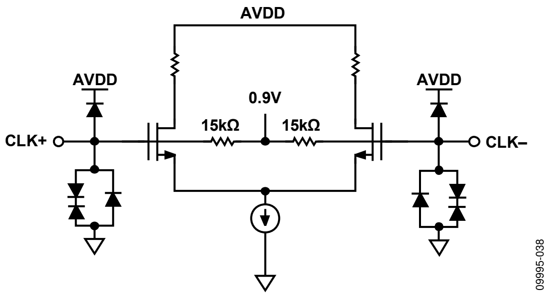


Figure 41. Equivalent Clock Input Circuit

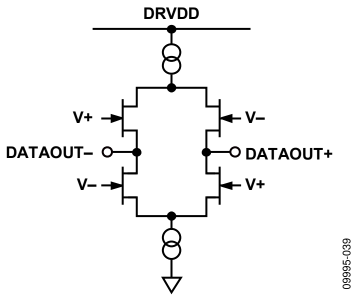


Figure 42. Equivalent LVDS Output Circuit

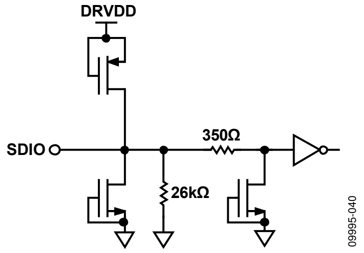


Figure 43. Equivalent SDIO Circuit

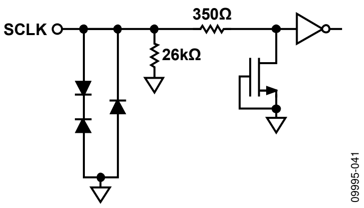


Figure 44. Equivalent SCLK Input Circuit

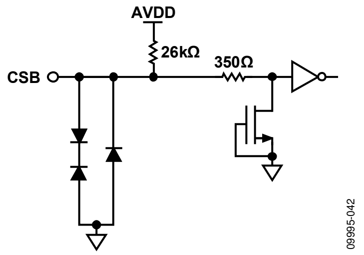


Figure 45. Equivalent CSB Input Circuit

THEORY OF OPERATION

The AD9642 can sample any $f_S/2$ frequency segment from dc to 250 MHz using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in ADC performance.

Programming and control of the AD9642 are accomplished using a 3-pin, SPI-compatible serial interface.

ADC ARCHITECTURE

The AD9642 architecture consists of a front-end sample-and-hold circuit, followed by a pipelined switched-capacitor ADC. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample and the remaining stages to operate on the preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor digital-to-analog converter (DAC) and an interstage residue amplifier (MDAC). The MDAC magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage of the AD9642 contains a differential sampling circuit that can be ac- or dc-coupled in differential or single-ended modes. The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing digital output noise to be separated from the analog core. During power-down, the output buffers go into a high impedance state.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9642 is a differential switched-capacitor circuit that has been designed to attain optimum performance when processing a differential input signal.

The clock signal alternatively switches the input between sample mode and hold mode (see the configuration shown in Figure 46). When the input is switched into sample mode, the signal source must be capable of charging the sampling capacitors and settling within 1/2 clock cycle.

A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. A shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC input; therefore, the precise values are dependent on the application.

In intermediate frequency (IF) undersampling applications, the shunt capacitors should be reduced. In combination with the driving source impedance, the shunt capacitors limit the input bandwidth. Refer to the AN-742 Application Note, *Frequency Domain Response of Switched-Capacitor ADCs*; the AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*; and the *Analog Dialogue* article, "Transformer-Coupled Front-End for Wideband A/D Converters," for more information on this subject.

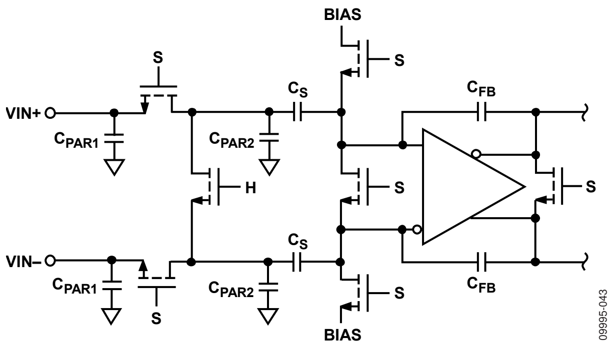


Figure 46. Switched-Capacitor Input

For best dynamic performance, match the source impedances driving VIN+ and VIN− and differentially balance the inputs.

Input Common Mode

The analog inputs of the AD9642 are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. Setting the device so that $V_{CM} = 0.5 \times \text{AVDD}$ (or 0.9 V) is recommended for optimum performance. An on-board common-mode voltage reference is included in the design and is available from the VCM pin. Using the VCM output to set the input common mode is recommended. Optimum performance is achieved when the common-mode voltage of the analog input is set by the VCM pin voltage (typically 0.5 × AVDD). The VCM pin must be decoupled to ground by a 0.1 µF capacitor, as described in the Applications Information section. Place this decoupling capacitor close to the pin to minimize the series resistance and inductance between the part and this capacitor.

Differential Input Configurations

Optimum performance can be achieved when driving the AD9642 in a differential input configuration. For baseband applications, the AD8138, ADA4937-1, and ADA4930-1 differential drivers provide excellent performance and a flexible interface to the ADC.

The output common-mode voltage of the ADA4930-1 is easily set with the VCM pin of the AD9642 (see Figure 47), and the driver can be configured in a Sallen-Key filter topology to provide band-limiting of the input signal.

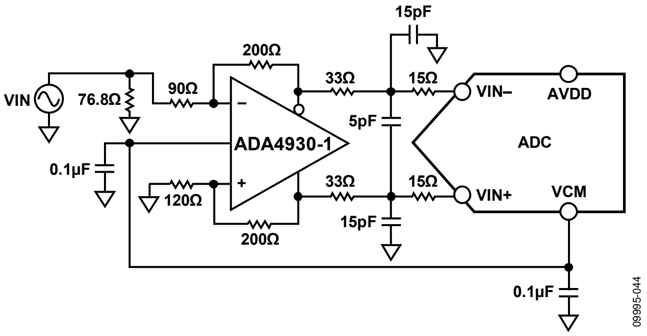


Figure 47. Differential Input Configuration Using the ADA4930-1

For baseband applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 48. To bias the analog input, connect the VCM voltage to the center tap of the secondary winding of the transformer.

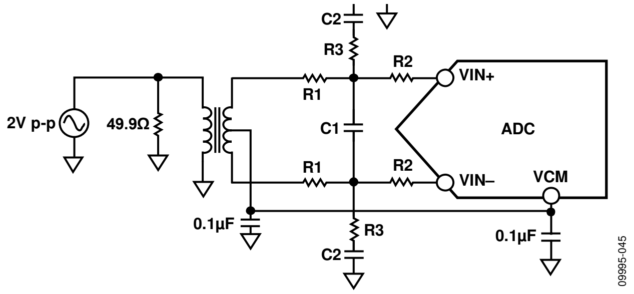


Figure 48. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz. Excessive signal power can also cause core saturation, which leads to distortion.

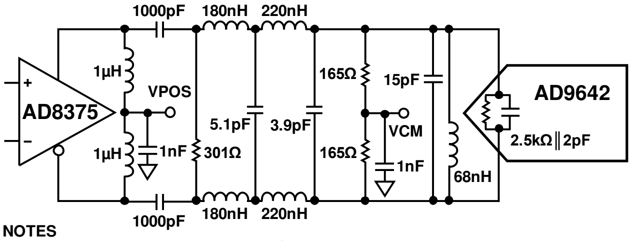
At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD9642. For applications where SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 50). In this configuration, the input is ac-coupled and the VCM voltage is provided to each input through a 33 Ω resistor. This resistor compensates for losses in the input baluns to provide a 50 Ω impedance to the driver.

In the double balun and transformer configurations, the value of the input capacitors and resistors is dependent on the input frequency and source impedance. Based on these parameters, the value of the input resistors and capacitors may need to be adjusted or some components may need to be removed. Table 9 displays recommended values to set the RC network for different input frequency ranges. However, these values are dependent on the input signal and bandwidth and should be used only as a starting guide. Note that the values given in Table 9 are for each R1, R2, C2, and R3 component shown in Figure 48 and Figure 50.

Table 9. Example RC Network

Frequency Range (MHz)	R1 Series (Ω)	C1 Differential (pF)	R2 Series (Ω)	C2 Shunt (pF)	R3 Shunt (Ω)
0 to 100	33	8.2	0	15	49.9
100 to 300	15	3.9	0	8.2	49.9

An alternative to using a transformer-coupled input at frequencies in the second Nyquist zone is to use an amplifier with variable gain. The AD8375 digital variable gain amplifier (DVGA) provides good performance for driving the AD9642. Figure 49 shows an example of the AD8375 driving the AD9642 through a band-pass antialiasing filter.



NOTES
1. ALL INDUCTORS ARE COILCRAFT® 0603CS COMPONENTS WITH THE EXCEPTION OF THE 1µH CHOKE INDUCTORS (COIL CRAFT 0603LS).
2. FILTER VALUES SHOWN ARE FOR A 20MHz BANDWIDTH FILTER CENTERED AT 140MHz.

Figure 49. Differential Input Configuration Using the AD8375

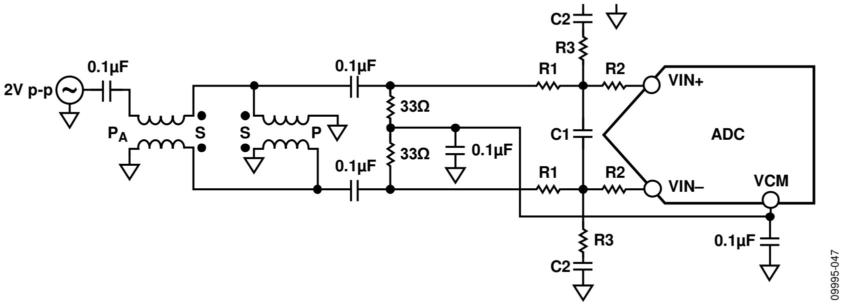


Figure 50. Differential Double Balun Input Configuration

VOLTAGE REFERENCE

A stable and accurate voltage reference is built into the AD9642. The full-scale input range can be adjusted by varying the reference voltage via SPI. The input span of the ADC tracks reference voltage changes linearly.

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9642 sample clock inputs, CLK+ and CLK−, should be clocked with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK− pins via a transformer or via capacitors. These pins are biased internally (see Figure 51) and require no external bias. If the inputs are floated, the CLK− pin is pulled low to prevent spurious clocking.

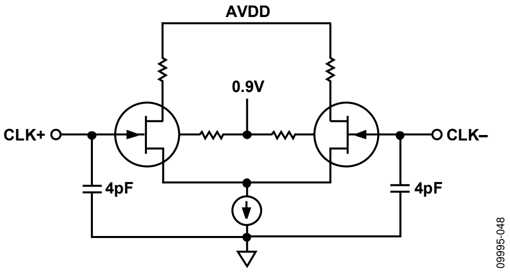


Figure 51. Simplified Equivalent Clock Input Circuit

Clock Input Options

The AD9642 has a very flexible clock input structure. Clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of the most concern, as described in the Jitter Considerations section.

Figure 52 and Figure 53 show two preferable methods for clocking the AD9642 (at clock rates of up to 625 MHz). A low jitter clock source is converted from a single-ended signal to a differential signal using an RF balun or RF transformer.

The RF balun configuration is recommended for clock frequencies between 125 MHz and 625 MHz, and the RF transformer is recommended for clock frequencies from 10 MHz to 200 MHz. The back-to-back Schottky diodes across the secondary winding of the transformer limit clock excursions into the AD9642 to approximately 0.8 V p-p differential. This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9642 while preserving the fast rise and fall times of the signal, which are critical for low jitter performance.

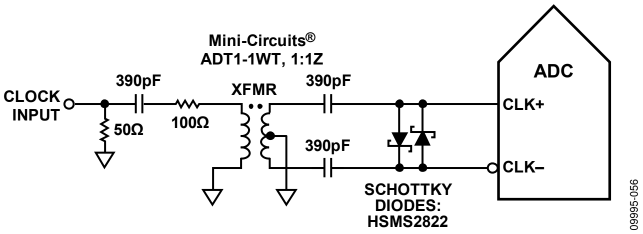


Figure 52. Transformer-Coupled Differential Clock (Up to 200 MHz)

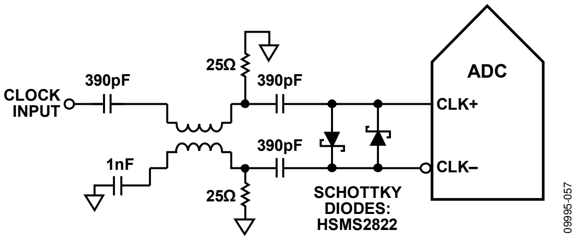


Figure 53. Balun-Coupled Differential Clock (Up to 625 MHz)

If a low jitter clock source is not available, another option is to ac-couple a differential PECL signal to the sample clock input pins as shown in Figure 54. The AD9510, AD9511, AD9512, AD9513, AD9514, AD9515, AD9516, AD9517, AD9518, AD9520, AD9522, AD9523, AD9524, and ADCLK905/ADCLK907/ ADCLK925 clock drivers offer excellent jitter performance.

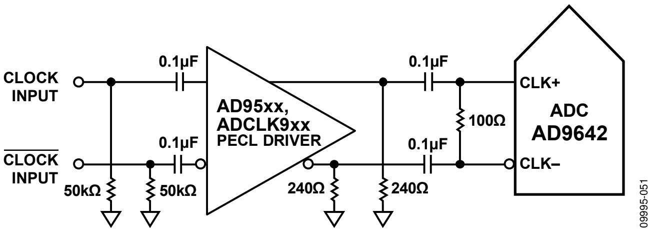


Figure 54. Differential PECL Sample Clock (Up to 625 MHz)

A third option is to ac-couple a differential LVDS signal to the sample clock input pins, as shown in Figure 55. The AD9510, AD9511, AD9512, AD9513, AD9514, AD9515, AD9516, AD9517, AD9518, AD9520, AD9522, AD9523, and AD9524 clock drivers offer excellent jitter performance.

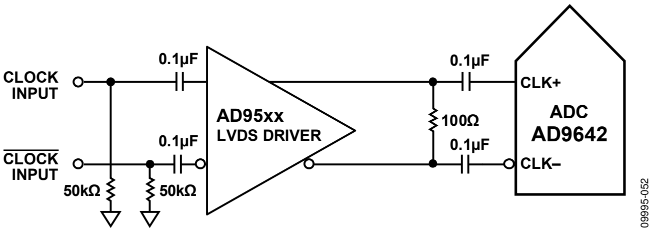


Figure 55. Differential LVDS Sample Clock (Up to 625 MHz)

Input Clock Divider

The AD9642 contains an input clock divider with the ability to divide the input clock by integer values between 1 and 8. The duty cycle stabilizer (DCS) is enabled by default on power-up.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9642 contains a DCS that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD9642.

Jitter on the rising edge of the input clock is still of paramount concern and is not reduced by the duty cycle stabilizer. The duty cycle control loop does not function for clock rates less than 40 MHz nominally. The loop has a time constant associated with it that must be considered when the clock rate may change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal. During the time that the loop is not locked, the DCS loop is bypassed, and internal device timing is dependent on the duty cycle of the input clock signal. In such applications, it may be appropriate to disable the duty cycle stabilizer. In all other applications, enabling the DCS circuit is recommended to maximize ac performance.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_{IN}) due to jitter (t_J) can be calculated by

$$SNR_{HF} = -10 \log[(2\pi \times f_{IN} \times t_{JRMS})^2 + 10^{(-SNR_{LF}/10)}]$$

In the equation, the rms aperture jitter represents the root-mean-square of all jitter sources, which include the clock input, the analog input signal, and the ADC aperture jitter specification. IF undersampling applications are particularly sensitive to jitter, as shown in Figure 56.

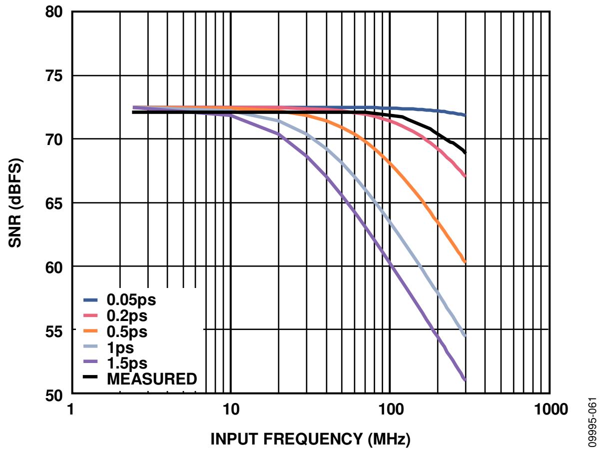


Figure 56. AD9642-250 SNR vs. Input Frequency and Jitter

In cases where aperture jitter may affect the dynamic range of the AD9642, treat the clock input as an analog signal. In addition, use separate power supplies for the clock drivers and the ADC output driver to avoid modulating the clock signal with digital noise. Low jitter, crystal controlled oscillators provide the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), it should be retimed by the original clock during the last step.

Refer to the AN-501 Application Note, *Aperture Uncertainty and ADC System Performance*, and the AN-756 Application Note, *Sampled Systems and the Effects of Clock Phase Noise and Jitter*, for more information about jitter performance as it relates to ADCs.

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 57, the power dissipated by the AD9642 is proportional to its sample rate. The data in Figure 57 was taken using the same operating conditions as those used for the Typical Performance Characteristics section.

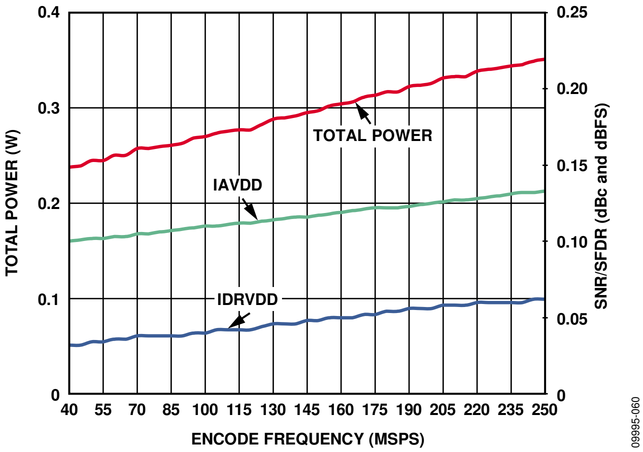


Figure 57. AD9642-250 Power and Current vs. Sample Rate

By setting the internal power-down mode bits (Bits[1:0]) in the power modes register (Address 0x08) to 01, the AD9642 is placed in power-down mode. In this state, the ADC typically dissipates 2.5 mW. During power-down, the output drivers are placed in a high impedance state.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when entering power-down mode and then must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in power-down mode, and shorter power-down cycles result in proportionally shorter wake-up times.

When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. To put the part into standby mode, set the internal power-down mode bits (Bits[1:0]) in the power modes register (Address 0x08) to 10. See the Memory Map section and the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, for additional details.

DIGITAL OUTPUTS

The AD9642 output drivers can be configured for either ANSI LVDS or reduced swing LVDS using a 1.8 V DRVDD supply.

As detailed in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, the data format can be selected for offset binary, twos complement, or gray code when using the SPI control.

Digital Output Enable Function (OEB)

The AD9642 has a flexible three-state ability for the digital output pins. The three-state mode is enabled using the SPI interface. The data outputs can be three-stated by using the output enable bar bit (Bit 4) in Register 0x14. This OEB function is not intended for rapid access to the data bus.

Timing

The AD9642 provides latched data with a pipeline delay of 10 input sample clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal.

Minimize the length of the output data lines as well as the loads placed on these lines to reduce transients within the AD9642. These transients may degrade converter dynamic performance.

The lowest typical conversion rate of the AD9642 is 40 MSPS. At clock rates below 40 MSPS, dynamic performance may degrade.

Data Clock Output (DCO)

The AD9642 also provides the data clock output (DCO) intended for capturing the data in an external register. Figure 2 shows a timing diagram of the AD9642 output modes.

Table 10. Output Data Format

Input (V)	VIN+ − VIN−, Input Span = 1.75 V p-p (V)	Offset Binary Output Mode	Twos Complement Mode (Default)
VIN+ − VIN−	<−0.875	00 0000 0000 0000	10 0000 0000 0000
VIN+ − VIN−	−0.875	00 0000 0000 0000	10 0000 0000 0000
VIN+ − VIN−	0	10 0000 0000 0000	00 0000 0000 0000
VIN+ − VIN−	+0.875	11 1111 1111 1111	01 1111 1111 1111
VIN+ − VIN−	>+0.875	11 1111 1111 1111	01 1111 1111 1111

SERIAL PORT INTERFACE (SPI)

The AD9642 serial port interface (SPI) allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI offers added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section. For detailed operational information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin, and the CSB pin (see Table 11). The SCLK (serial clock) pin is used to synchronize the read and write data presented from and to the ADC. The SDIO (serial data input/output) pin is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) pin is an active low control that enables or disables the read and write cycles.

Table 11. Serial Port Interface Pins

Pin	Function
SCLK	Serial clock. The serial shift clock input, which is used to synchronize serial interface reads and writes.
SDIO	Serial data input/output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip select bar. An active low control that gates the read and write cycles.

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 58 and Table 5.

Other modes involving the CSB are available. The CSB can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB can stall high between bytes to allow for additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

During an instruction phase, a 16-bit instruction is transmitted. Data follows the instruction phase, and its length is determined by the W0 and W1 bits.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued. This allows the serial data input/output (SDIO) pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or in LSB first mode. MSB first mode is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

HARDWARE INTERFACE

The pins described in Table 11 comprise the physical interface between the user programming device and the serial port of the AD9642. The SCLK pin and the CSB pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9642 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

SPI ACCESSIBLE FEATURES

Table 12 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Table 12. Features Accessible Using the SPI

Feature Name	Description
Mode	Allows the user to set either power-down mode or standby mode
Clock	Allows the user to access the DCS via the SPI
Offset	Allows the user to digitally adjust the converter offset
Test I/O	Allows the user to set test modes to have known data on output bits
Output Mode	Allows the user to set up outputs
Output Phase	Allows the user to set the output clock polarity
Output Delay	Allows the user to vary the DCO delay
VREF	Allows the user to set the reference voltage
Digital Processing	Allows the user to enable the synchronization features

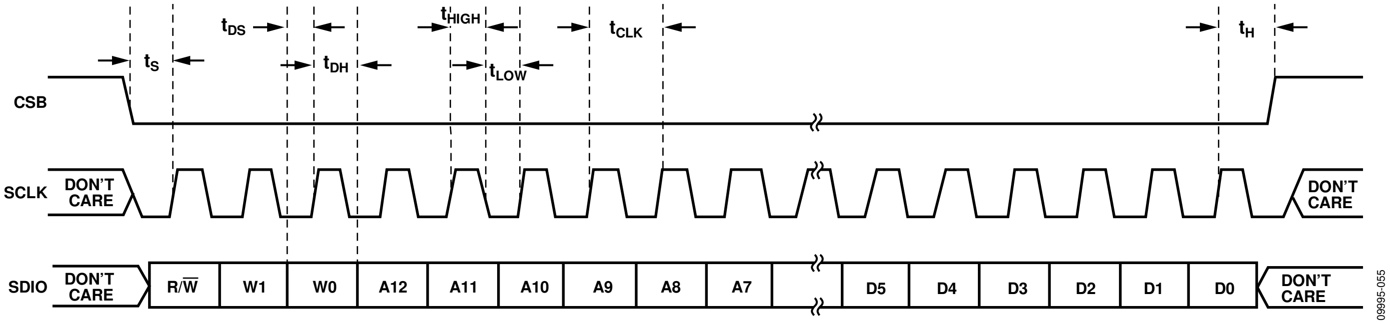


Figure 58. Serial Port Interface Timing Diagram

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is roughly divided into three sections: the chip configuration registers (Address 0x00 to Address 0x02); the transfer register (Address 0xFF); and the ADC functions registers, including setup, control, and test (Address 0x08 to Address 0x20).

The memory map register table (Table 13) documents the default hexadecimal value for each hexadecimal address shown. The Bit 7 (MSB) column is the start of the default hexadecimal value given. For example, Address 0x14, the output mode register, has a hexadecimal default value of 0x01. This means that Bit 0 = 1 and the remaining bits are 0s. This setting is the default output format value, which is twos complement. For more information on this function and others, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. This document details the functions controlled by Register 0x00 to Register 0x20.

Open Locations

All address and bit locations that are not included in Table 13 are not currently supported for this device. Write 0s to unused bits of a valid address location. Writing to these locations is required only when part of an address location is open (for example, Address 0x18). If the entire address location is open (for example, Address 0x13), this address location should not be written.

Default Values

After the AD9642 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table (Table 13).

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

Transfer Register Map

Address 0x08 to Address 0x20 are shadowed. Writes to these addresses do not affect part operation until a transfer command is issued by writing 0x01 to Address 0xFF, setting the transfer bit. This allows these registers to be updated internally and simultaneously when the transfer bit is set. The internal update takes place when the transfer bit is set, and then the bit autoclears.