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Evaluation Board User Guide
UG-293

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Evaluating the AD9643/AD9613/AD6649/AD6643 Analog-to-Digital Converters

FEATURES

Full featured evaluation board for the AD9643/AD9613/AD6649/AD6643
SPI interface for setup and control
External or AD9523 clocking option
Balun/transformer or amplifier input drive options
LDO regulator power supply
VisualAnalog and SPI controller software interfaces

EQUIPMENT NEEDED

Analog signal source and antialiasing filter
Sample clock source (if not using the on-board oscillator)
2 switching power supplies (6.0 V, 2.5 A), CUI EPS060250UH-PHP-SZ, provided
PC running Windows® 98 (2nd ed.), Windows 2000, Windows ME, or Windows XP
USB 2.0 port recommended (USB 1.1 compatible)
AD9643, AD9613, AD6649, or AD6643 evaluation board
HSC-ADC-EVALCZ FPGA-based data capture kit

SOFTWARE NEEDED

VisualAnalog
SPI controller

DOCUMENTS NEEDED

AD9643, AD9613, AD6649, or AD6643 data sheet
HSC-ADC-EVALCZ data sheet
AN-905 Application Note, *VisualAnalog Converter Evaluation Tool Version 1.0 User Manual*
AN-878 Application Note, *High Speed ADC SPI Control Software*
AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*
AN-835 Application Note, *Understanding ADC Testing and Evaluation*

GENERAL DESCRIPTION

This user guide describes the AD9643, AD9613, AD6649, and AD6643 evaluation board, which provides all of the support circuitry required to operate the AD9643, AD9613, AD6649, and AD6643 in their various modes and configurations. The application software used to interface with the devices is also described.

The AD9643, AD9613, AD6649, and AD6643 data sheets provide additional information and should be consulted when using the evaluation board. All documents and software tools are available at http://www.analog.com/fifo. For additional information or questions, send an email to highspeed.converters@analog.com.

TYPICAL MEASUREMENT SETUP

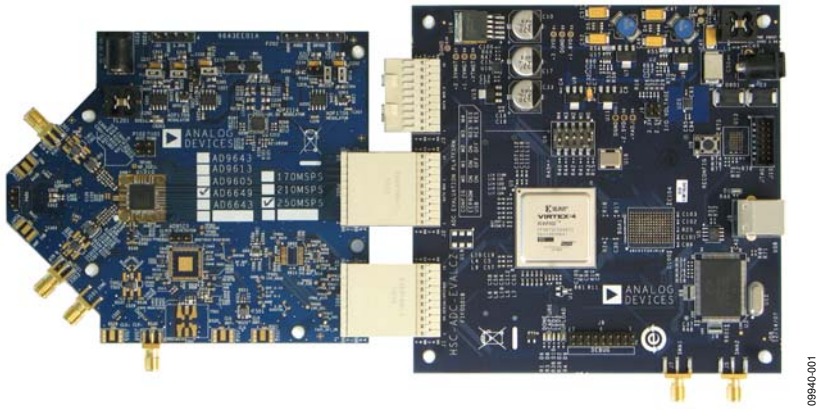


Figure 1. AD9643, AD9613, AD6649, or AD6643 Family Evaluation Board and HSC-ADC-EVALCZ Data Capture Board

TABLE OF CONTENTS

REVISION HISTORY

11/11—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The AD9643, AD9613, AD6649, or AD6643 evaluation board provides all of the support circuitry required to operate these parts in their various modes and configurations. Figure 2 shows the typical bench characterization setup used to evaluate the ac performance of the AD9643, AD9613, AD6649, or AD6643. It is critical that the signal sources used for the analog input and the clock have very low phase noise (<1 ps rms jitter) to realize the optimum performance of the signal chain. Proper filtering of the analog input signal to remove harmonics and lower the integrated or broadband noise at the input is necessary to achieve the specified noise performance.

See the Evaluation Board Software Quick Start Procedures section to get started, and see Figure 23 to Figure 34 for the complete schematics and layout diagrams. These diagrams demonstrate the routing and grounding techniques that should be applied at the system level when designing application boards using these converters.

POWER SUPPLIES

This evaluation board comes with a wall-mountable switching power supply that provides a 6 V, 2 A maximum output. Connect the supply to a rated 100 V ac to 240 V ac wall outlet at 47 Hz to 63 Hz. The output from the supply is provided through a 2.1 mm inner diameter jack that connects to the printed circuit board (PCB) at P201. The 6 V supply is fused and conditioned on the PCB before connecting to the low dropout linear regulators (default configuration) that supply the proper bias to each of the various sections on the board.

The evaluation board can be powered in a nondefault condition using external bench power supplies. To do this, remove the jumpers on the P103, P104, P107, P108, and P105 header pins to disconnect the outputs from the on-board LDOs. This enables the user to bias each section of the board individually. Use P202 and P203 to connect a different supply for each section. A 1.8 V supply is needed with a 1 A current capability for DUT_AVDD and DRVDD; however, it is recommended that separate supplies be used for both analog and digital domains. An additional supply is also required to supply 1.8 V for digital support circuitry on the board, DVDD. This should also have a 1 A current capability and can be combined with DRVDD with little or no degradation in performance. To operate the evaluation board using the SPI and alternate clock options, a separate 3.3 V analog supply is needed in addition to the other supplies. This 3.3 V supply, or 3P3V_ANALOG, should have a 1 A current capability. This 3.3 V supply is also used to support the optional input path amplifier (ADL5202) on Channel A and Channel B.

INPUT SIGNALS

When connecting the clock and analog source, use clean signal generators with low phase noise, such as the Rohde & Schwarz SMA or HP 8644B signal generators or an equivalent. Use a 1 m shielded, RG-58, 50 Ω coaxial cable for connecting to the evaluation board. Enter the desired frequency and amplitude (see the Specifications section in the data sheet of the respective part).

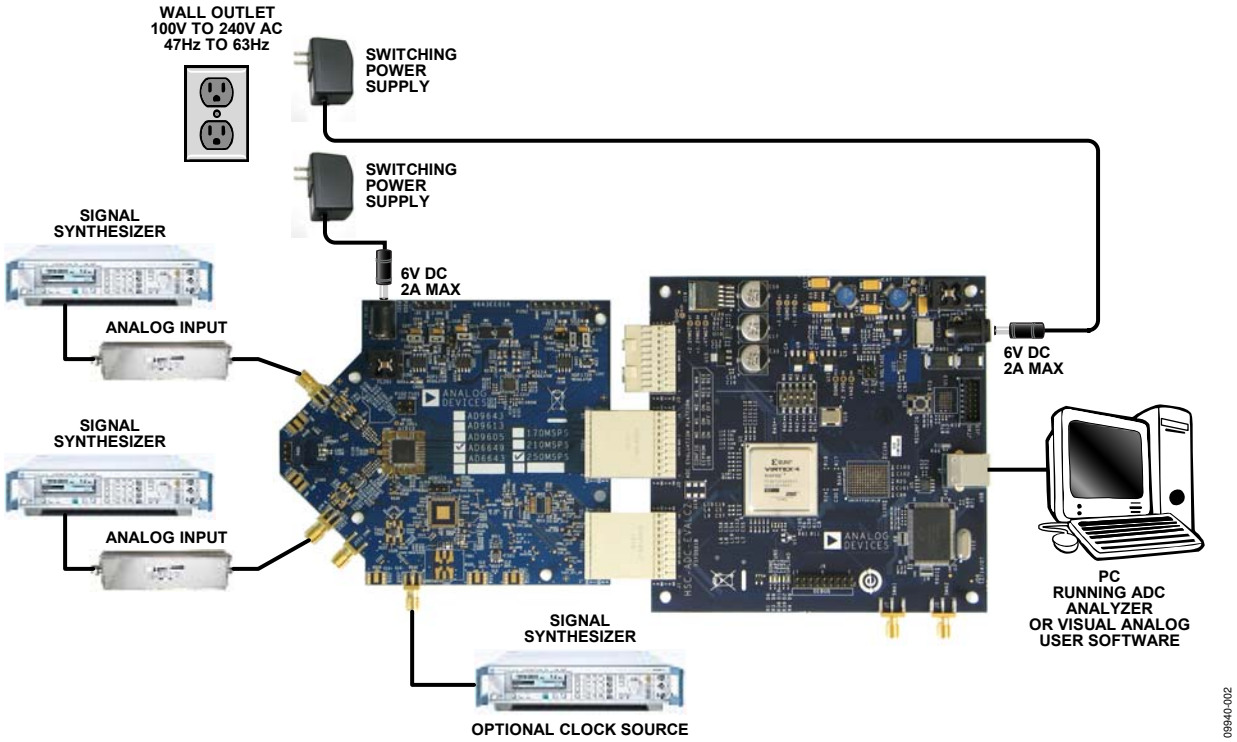


Figure 2. Evaluation Board Connection

When connecting the analog input source, use of a multipole, narrow-band, band-pass filter with 50 Ω terminations is recommended. Analog Devices, Inc., uses TTE and K&L Microwave, Inc., band-pass filters. The filters should be connected directly to the evaluation board.

If an external clock source is used, it should also be supplied with a clean signal generator as previously specified. Typically, most Analog Devices evaluation boards can accept ~2.8 V p-p or 13 dBm sine wave input for the clock.

OUTPUT SIGNALS

The default setup uses the Analog Devices high speed converter evaluation platform (HSC-ADC-EVALCZ) for data capture. The output signals from Channel A and Channel B for the AD9643, AD9613, AD6649, and AD6643 are routed through P601 and P602, respectively, to the FPGA on the data capture board.

DEFAULT OPERATION AND JUMPER SELECTION SETTINGS

This section explains the default and optional settings or modes allowed on the AD9643/AD9613/AD6649/AD6643 evaluation board.

Power Circuitry

Connect the switching power supply that is supplied in the evaluation kit between a rated 100 V ac to 240 V ac wall outlet at 47 Hz to 63 Hz and P201.

Analog Input

The A and B channel inputs on the evaluation board are set up for a double balun-coupled analog input with a 50 Ω impedance. This input network is optimized to support a wide frequency band. See the AD9643, AD9613, AD6649, and AD6643 data sheets for additional information on the recommended networks for different input frequency ranges. The nominal input drive level is 10 dBm to achieve 2 V p-p full scale into 50 Ω. At higher input frequencies, slightly higher input drive levels are required due to losses in the front-end network.

Optionally, Channel A and Channel B inputs on the board can be configured to use the ADL5202 digitally controlled, variable gain wide bandwidth amplifier. The ADL5202 component is included on the evaluation board at U401. However, the path into and out of the ADL5202 can be configured in many different ways depending on the application; therefore, the parts in the input and output path are left unpopulated. Users should see the ADL5202 data sheet for additional information on this part and for configuring the inputs and outputs. The ADL5202, by default, is held in power-down mode but can be enabled by adding 1 kΩ resistors at R427 and R428 to enable Channel A and Channel B, respectively.

Clock Circuitry

The default clock input circuit that is populated on the AD9643/AD9613/AD6649/AD6643 evaluation board uses a simple transformer-coupled circuit with a high bandwidth 1:1 impedance ratio transformer (T503) that adds a very low amount of jitter to the clock path. The clock input is 50 Ω terminated and ac-coupled to handle single-ended sine wave types of inputs. The transformer converts the single-ended input to a differential signal that is clipped by CR503 before entering the ADC clock inputs.

The board is set by default to use an external clock generator. An external clock source capable of driving a 50 Ω terminated input should be connected to J506.

A differential LVPECL clock driver output can also be used to clock the ADC input using the AD9523 (U501). To place the AD9523 into the clock path, populate R541 and R542 with 0 Ω resistors and remove C532 and C533 to disconnect the default clock path inputs. In addition, populate R533 and R534 with 0 Ω resistors, remove R522 and R523 to disconnect the default clock path outputs, and insert AD9523 LVPECL Output 2. The AD9523 must be configured through the SPI controller software to set up the PLL and other operation modes. Consult the AD9523 data sheet for more information about these and other options.

PDWN

To enable the power-down feature, add a shorting jumper across P101 at Pin 1 and Pin 2 to connect the PDWN pin to AVDD.

OEB

To disable the digital output pins and place them in a high impedance state, add a shorting jumper across P102 at Pin 1 and Pin 2 to connect the OEB pin to AVDD.

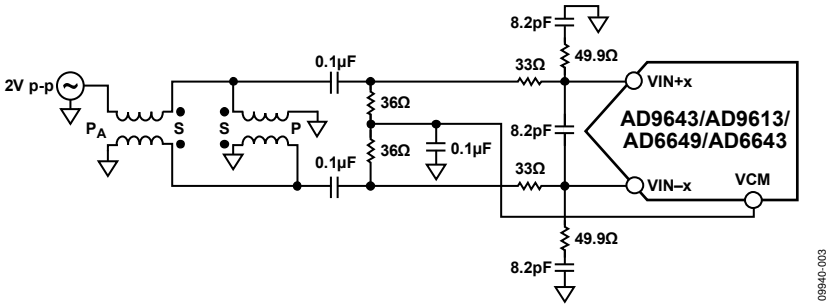


Figure 3. Default Analog Input Configuration of the AD9643/AD9613/AD6649/AD6643

Switching Power Supply

Optionally, the ADC on the board can be configured to use the ADP2114 dual switching power supply to provide power to the DRVDD and AVDD rails of the ADC. To configure the board to operate from the ADP2114, the following changes must be incorporated (see the Evaluation Board Schematics and Artwork and the Bill of Materials sections for specific recommendations for part values):

1. Install R204 and R221 to enable the ADP2114.
2. Install R216 and R218.
3. Install L201 and L202.
4. Remove JP201 and JP203.
5. Remove jumpers from across Pin 1 and Pin 2 on P107 and P108, respectively.
6. Place jumpers across Pin 1 and Pin 2 of P106 and P109, respectively.

Making these changes enables the switching converter to power the ADC. Using the switching converter as the ADC power source is more efficient than using the default LDOs.

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

This section provides quick start procedures for using the AD9643/AD9613/AD6649/AD6643 evaluation board. Both the default and optional settings are described.

CONFIGURING THE BOARD

Before using the software for testing, configure the evaluation board as follows:

1. Connect the evaluation board to the data capture board, as shown in Figure 1 and Figure 2.
2. Connect one 6 V, 2.5 A switching power supply (such as the CUI, Inc., EPS060250UH-PHP-SZ that is supplied) to the AD9643/AD9613/AD6649/AD6643 board.
3. Connect another 6 V, 2.5 A switching power supply (such as the CUI EPS060250UH-PHP-SZ that is supplied) to the HSC-ADC-EVALCZ board.
4. Connect the HSC-ADC-EVALCZ board (J6) to the PC with a USB cable.
5. On the ADC evaluation board, confirm that jumpers are installed on the P105, P108, P104, P107, P110, and P103 headers.
6. Connect a low jitter sample clock to Connector J506.
7. Use a clean signal generator with low phase noise to provide an input signal to the desired channel(s) at Connector J301 (Channel A) and/or Connector J303 (Channel B). Use a 1 m, shielded, RG-58, 50 Ω coaxial cable to connect the signal generator. For best results, use a narrow-band band-pass filter with 50 Ω terminations and an appropriate center frequency. (Analog Devices uses TTE, Allen Avionics, and K&L band-pass filters.)

USING THE SOFTWARE FOR TESTING

Setting Up the ADC Data Capture

After configuring the board, set up the ADC data capture using the following steps:

1. Open VisualAnalog® on the connected PC. The appropriate part type should be listed in the status bar of the **VisualAnalog – New Canvas** window. Select the template that corresponds to the type of testing to be performed (see Figure 4 where the AD9643 is shown as an example). The AD9643 is given as an example in this user guide. Similar settings are used for the AD9613. For the AD6649 and AD6643, the differences are noted where necessary in the steps that follow.

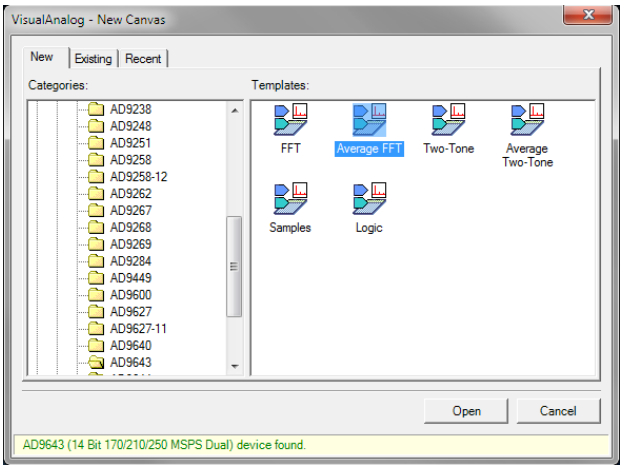


Figure 4. VisualAnalog, New Canvas Window

2. After the template is selected, a message appears asking if the default configuration can be used to program the FPGA (see Figure 5). Click **Yes**, and the window closes.

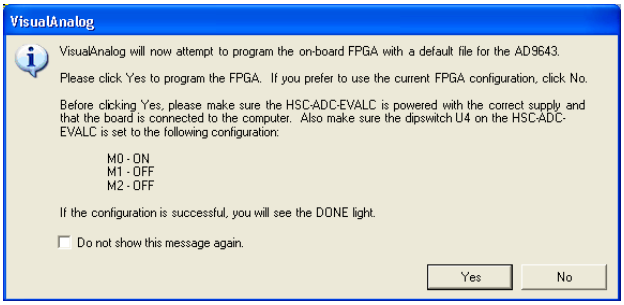


Figure 5. VisualAnalog Default Configuration Message

3. To change features to settings other than the default settings, click the **Expand Display** button, located on the bottom right corner of the window, to see what is shown in Figure 7. Detailed instructions for changing the features and capture settings can be found in the AN-905 Application Note, *VisualAnalog™ Converter Evaluation Tool Version 1.0 User Manual*. After the changes are made to the capture settings, click the **Collapse Display** button (see Figure 6).

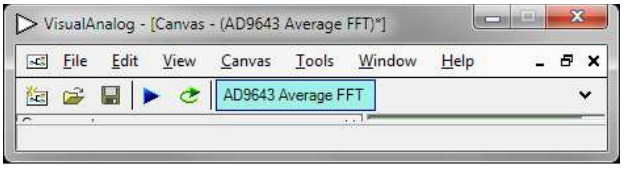


Figure 6. VisualAnalog Window Toolbar, Collapsed Display

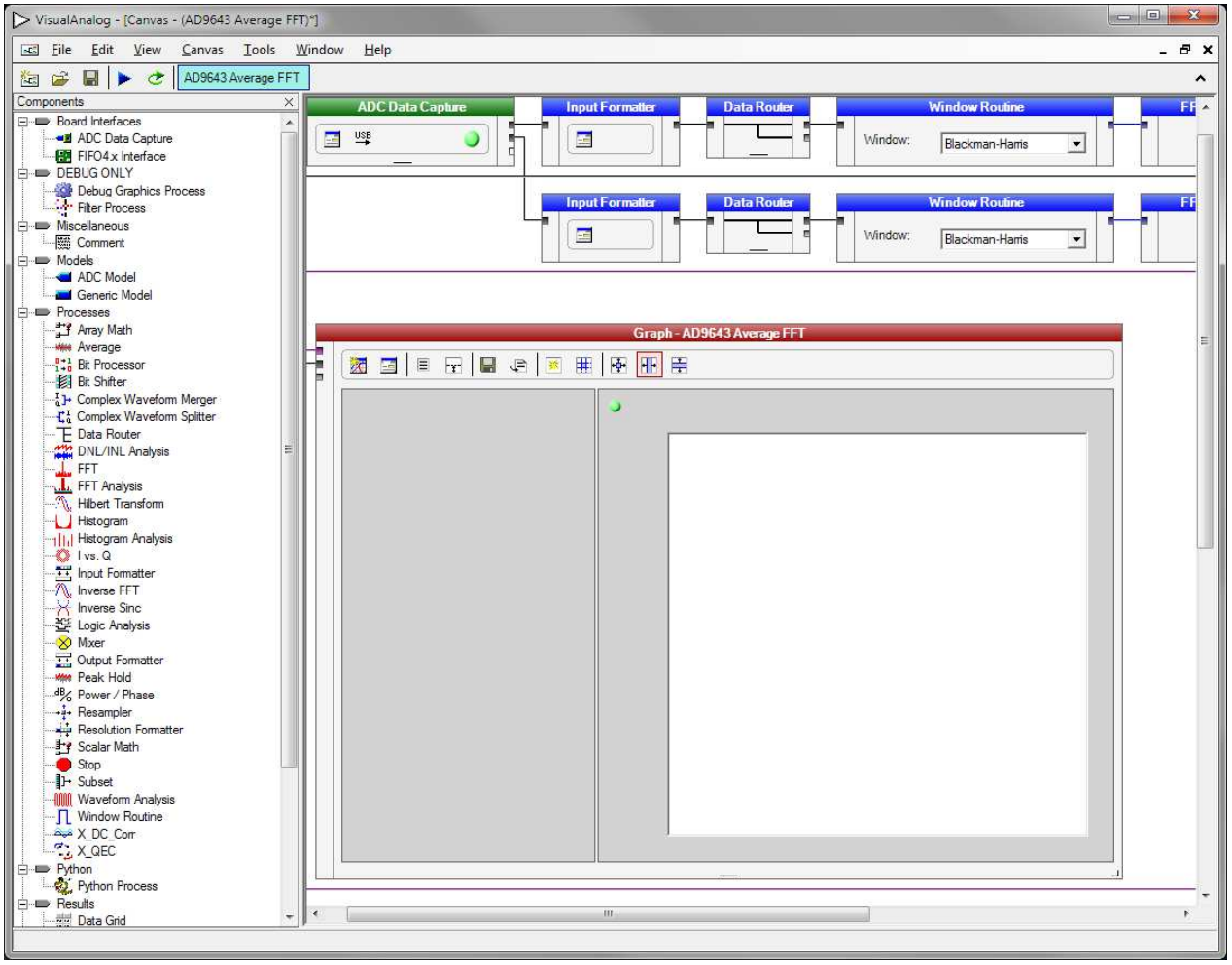


Figure 7. VisualAnalog, Main Window

Setting Up the SPI Controller Software

After the ADC data capture board setup is complete, set up the SPI controller software using the following procedure:

1. Open the SPI controller software by going to the **Start** menu or by double-clicking the **SPIController** software desktop icon. If prompted for a configuration file, select the appropriate one. If not, check the title bar of the window to determine which configuration is loaded. If necessary, choose **Cfg Open** from the **File** menu and select the appropriate file based on your part type. Note that the **CHIP ID(1)** field should be filled to indicate whether the correct SPI controller configuration file is loaded (see Figure 8).

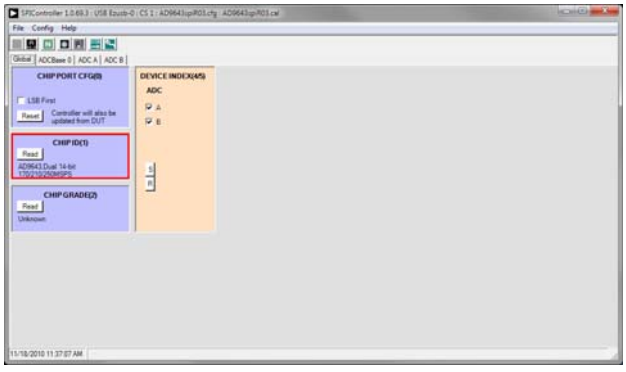


Figure 8. SPI Controller, CHIP ID(1) Section

2. Click the **New DUT** button in the **SPIController** window (see Figure 9).

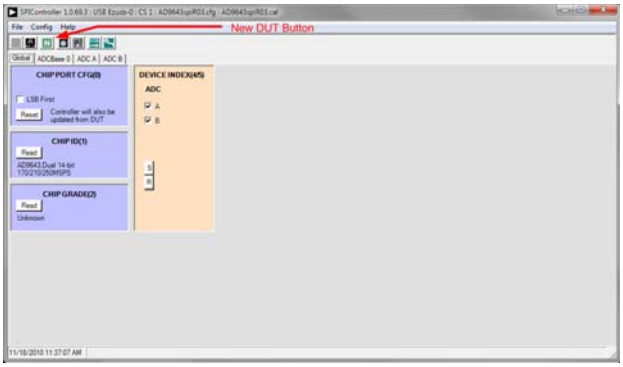


Figure 9. SPI Controller, New DUT Button

3. In the **ADCBase 0** tab of the **SPIController** window, find the **CLK DIV(B)** section (see Figure 11). If using the clock divider, use the drop-down box to select the correct clock divide ratio, if necessary. See the appropriate part data sheet; the AN-878 Application Note, *High Speed ADC SPI Control Software*; and the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, for additional information.
4. In the **ADCBase 0** tab of the **SPIController** window, find the **FLEX OUTPUT DELAY(17)** box. Select the **DCO Clk Delay Enable** checkbox to enable this feature. In the drop-down box, select **600 ps additional delay on DCO pin**. These settings align the output timing with the input timing on the capture FPGA.
5. Note that other settings can be changed on the **ADCBase 0** tab (see Figure 11) and the **ADC A** and **ADC B** tabs (see Figure 10) to set up the part in the desired mode. The settings on the **ADCBase 0** tab affect the entire part, whereas the settings on the **ADC A** and **ADC** pages affect the selected channel only. See the appropriate part data sheet; the AN-878 Application Note, *High Speed ADC SPI Control Software*; and the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, for additional information on the available settings.

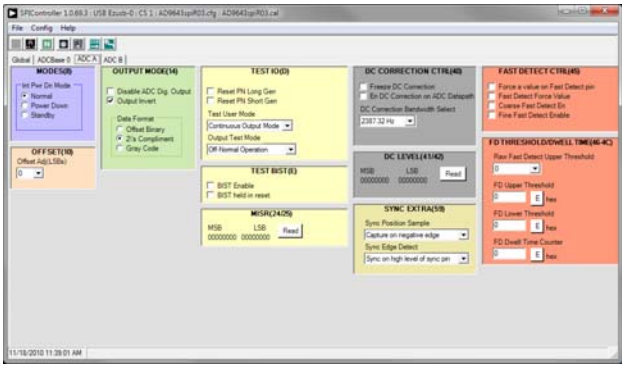


Figure 10. SPI Controller, Example ADC A Tab

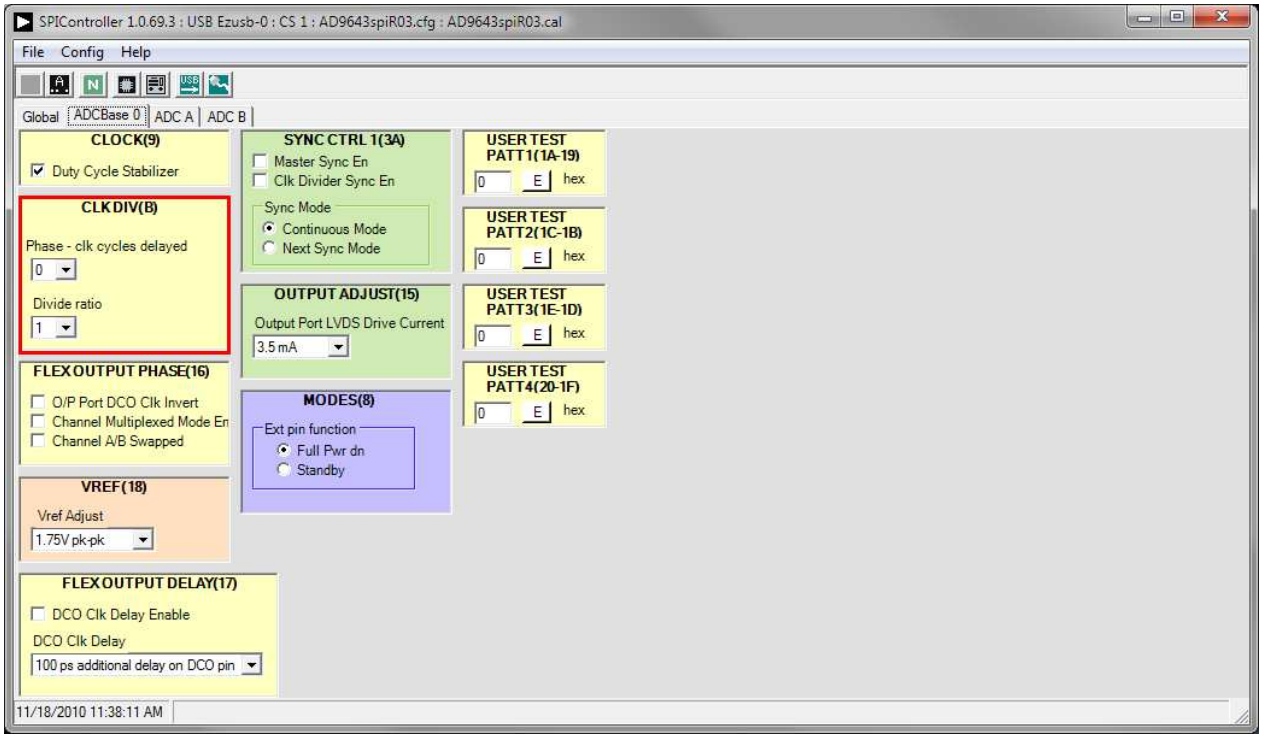


Figure 11. SPI Controller, CLK DIV(B) Section

6. If using the AD6649, the device can be configured into two different modes. The default mode utilizes a 95 MHz FIR filter and fixed-frequency NCO. The SPI controller settings for this mode are shown in Figure 12. Under the **MAIN(50)** section, the **Fir Low Latency Mode En** checkbox must be selected and the **Low Latency NCO (Fs/4 Only)** option must be clicked under the **MISC EXTRA(5A)** section. The second mode uses a 100 MHz FIR filter and a tunable-frequency NCO (see Figure 13). In this mode, the **High Latency NCO** option under **MISC EXTRA(5A)** must be clicked and the **Fir Low Latency Mode En** checkbox must be cleared under the **MAIN(50)** section.

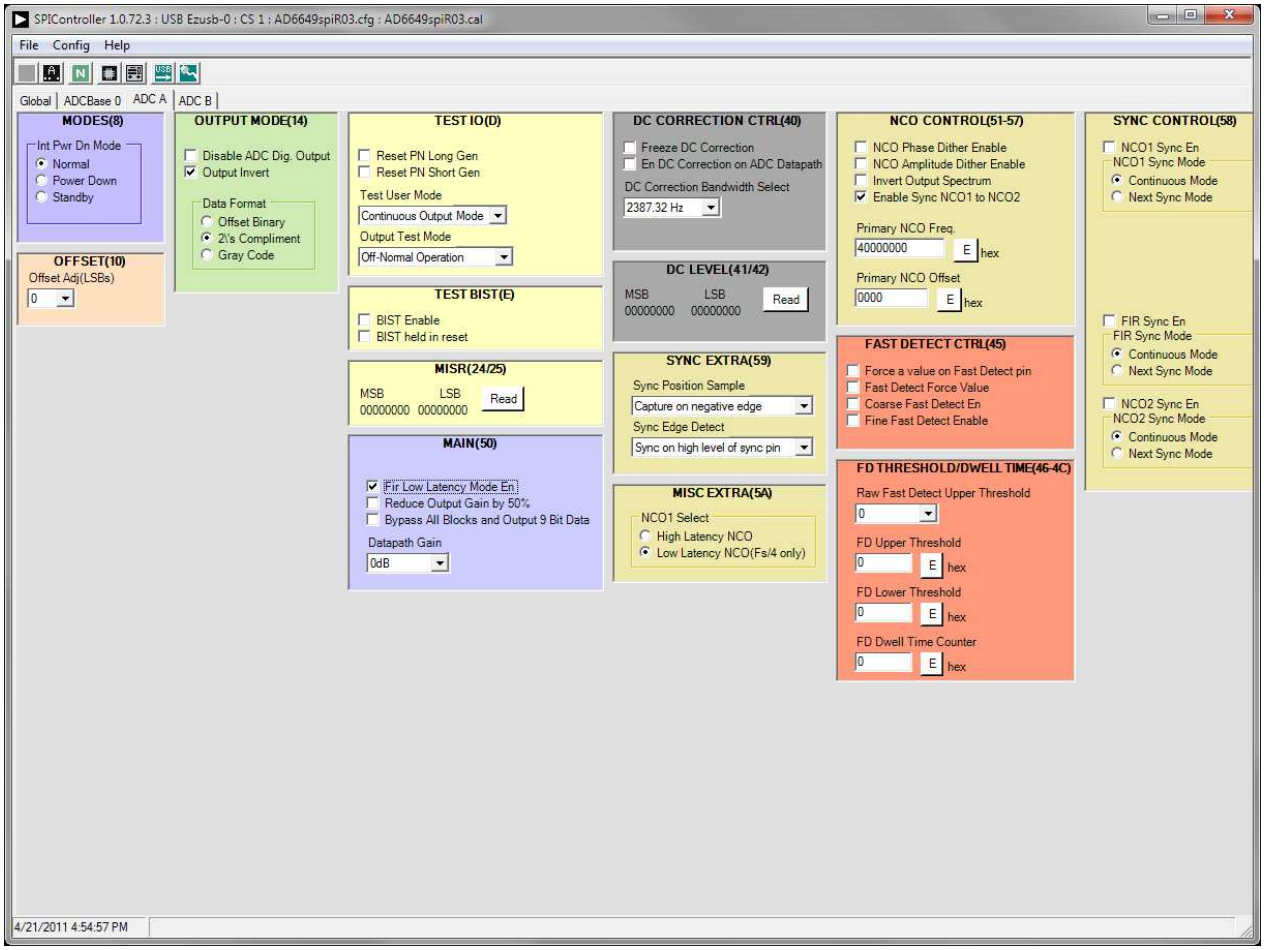


Figure 12. SPI Controller, AD6649 ADC A Tab—95 MHz FIR Filter and Fixed-Frequency NCO Mode

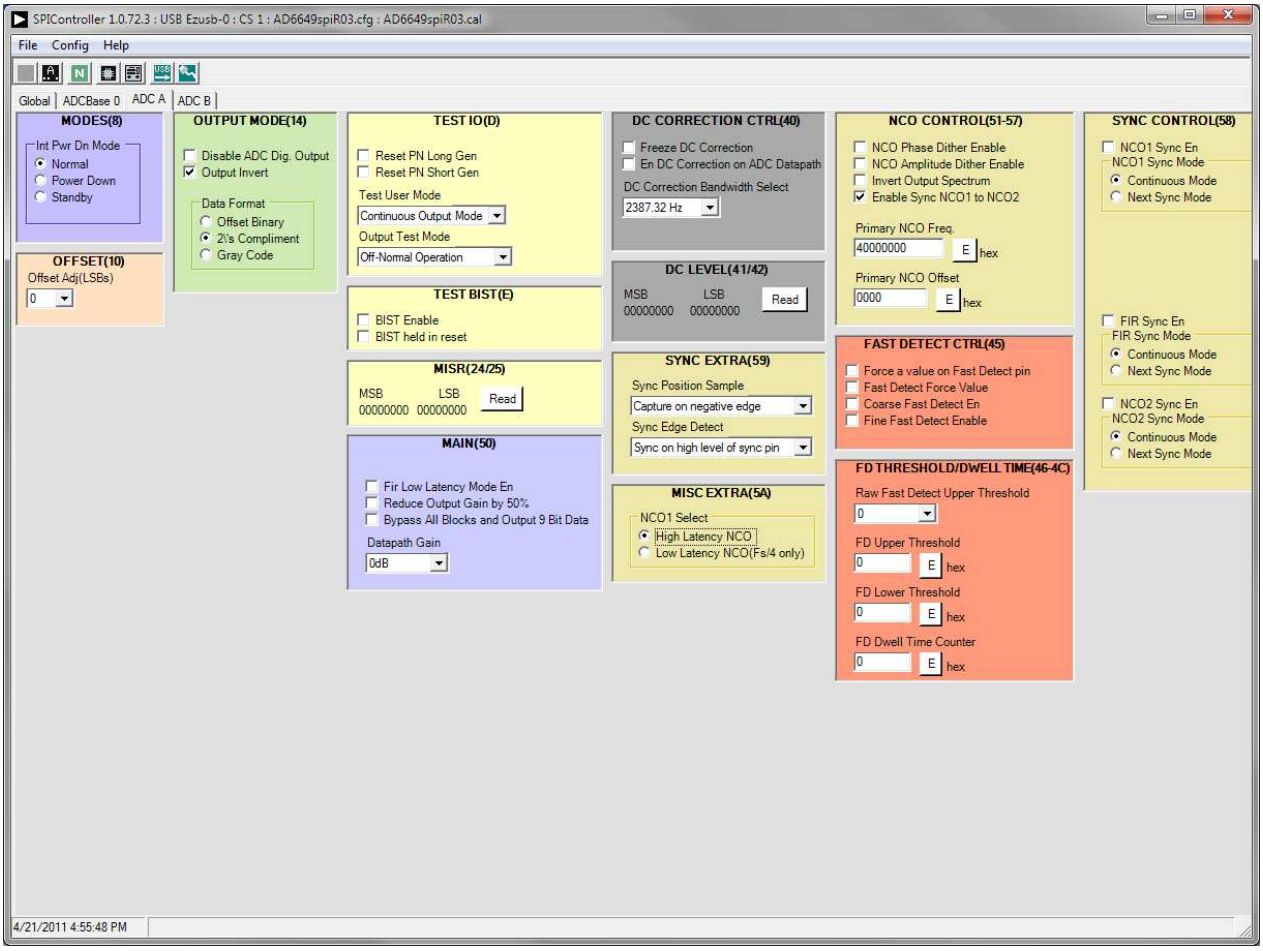


Figure 13. SPI Controller, AD6649 ADC A Tab—95 MHz FIR Filter and Fixed-Frequency NCO Mode

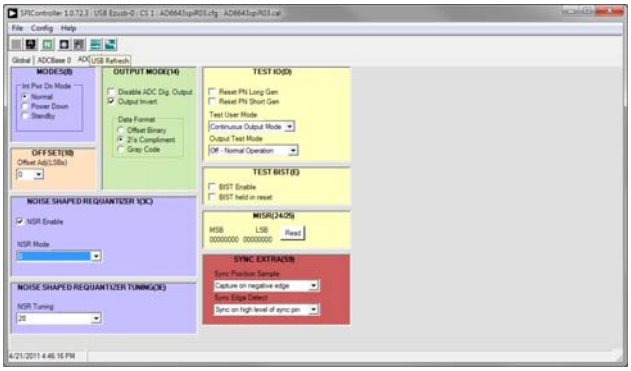


Figure 14. SPI Controller, Example ADC A Tab—NSR Settings for the AD6643

7. If using the Noise Shaping Requantizer (NSR) feature of the AD6643, the settings in the **ADC A** and/or **ADC B** pages must be changed (see Figure 14). The **NSR Enable** checkbox must be selected under the **NOISE SHAPED REQUANTIZER 1(3C)** section. This enables the circuitry in the AD6643. To select the bandwidth mode, select 0 for 22% and 1 for 33% under the **NSR Mode** drop-down menu in the **NOISE SHAPED REQUANTIZER 1(3C)** section. Upon selecting the bandwidth mode, select the desired tuning word in the **NSR Tuning** drop-down menu under the **NOISE SHAPED REQUANTIZER TUNING(3E)** section.
8. Click the **Run** button in the **VisualAnalog** toolbar (see Figure 15).

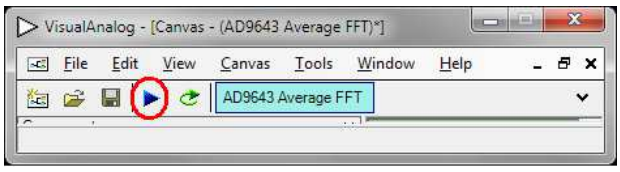


Figure 15. Run Button (Encircled in Red) in VisualAnalog Toolbar, Collapsed Display

Adjusting the Amplitude of the Input Signal

The next step is to adjust the amplitude of the input signal for each channel as follows:

1. Adjust the amplitude of the input signal so that the fundamental is at the desired level. (Examine the **Fund Power** reading in the left panel of the VisualAnalog **Graph** window.) See Figure 17.
2. Repeat this procedure for Channel B if desired.
3. Click the **Save** disk icon within the **Graph** window to save the performance plot data as a .csv formatted file. See Figure 16 for an example.

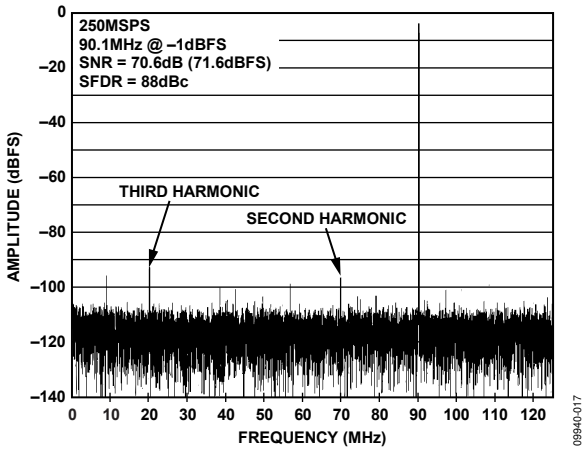


Figure 16. Typical FFT, AD9643

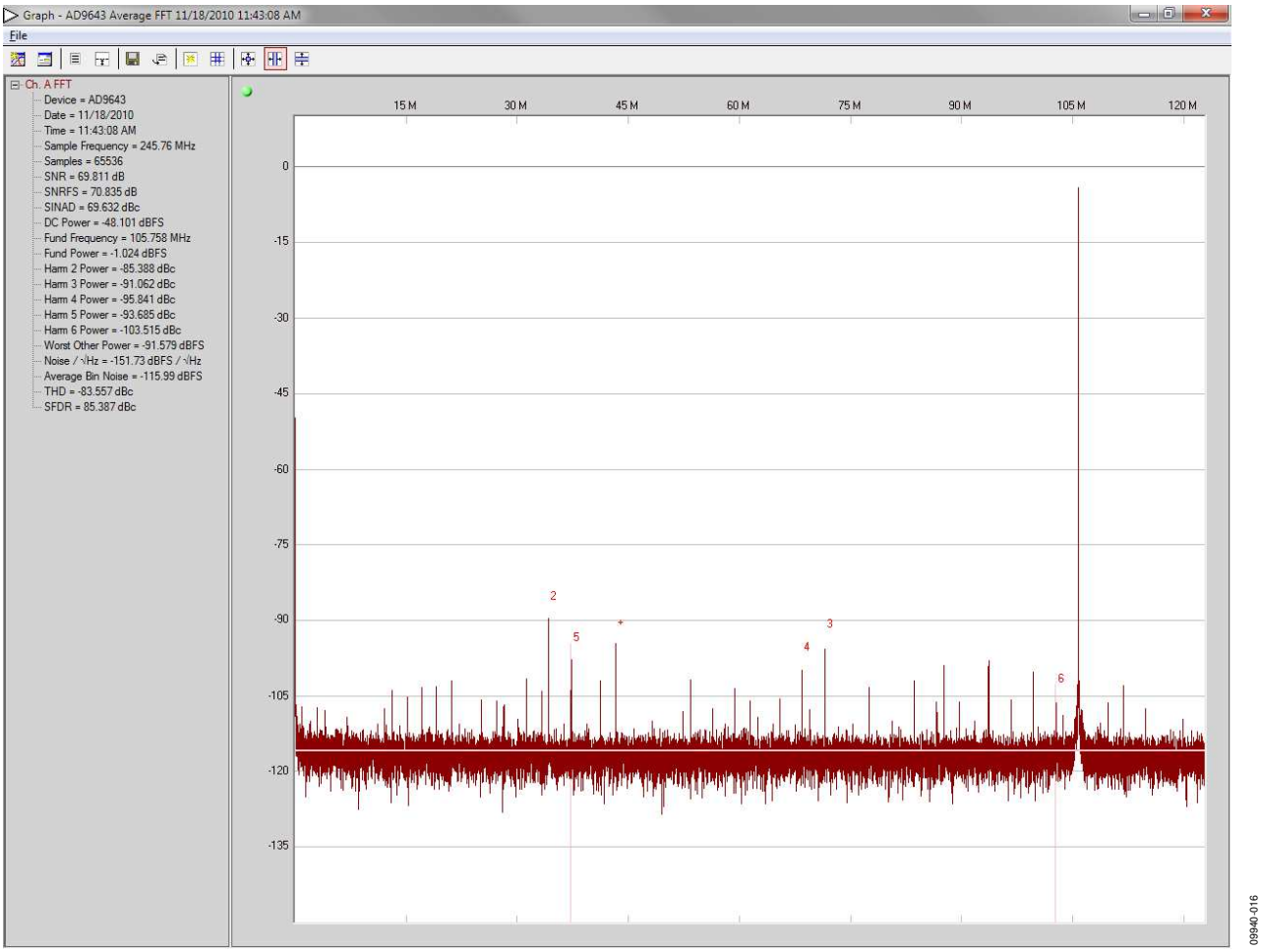


Figure 17. Graph Window of VisualAnalog (AD9643)

4. If operating the AD6649 in the mode using the 95 MHz FIR filter and fixed-frequency NCO, the amplitude displayed is −2.5 dBFS for a −1.0 dBFS input signal (see Figure 18) to the desired settings. If operating the AD6649 in the mode utilizing the 100 MHz FIR filter and tunable-frequency NCO, the amplitude displayed is −1.3 dBFS for a −1.0 dBFS input signal (see Figure 19).

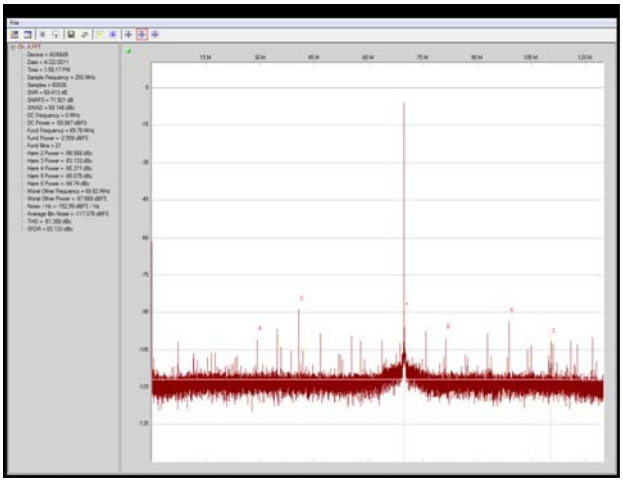


Figure 18. Visual Graph Window of VisualAnalog (AD6649)—95 MHz FIR Filter and Fixed-Frequency NCO Mode

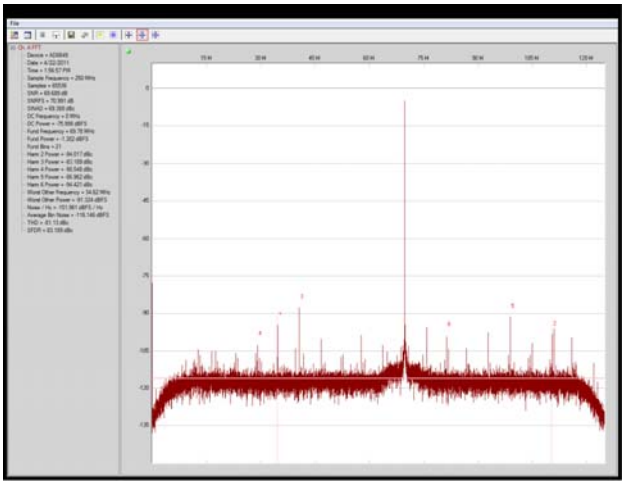


Figure 19. Visual Graph Window of VisualAnalog (AD6649)—100 MHz FIR Filter and Tunable-Frequency NCO Mode

5. Repeat Step 3 to save the graph in a .csv file format.
6. If operating the AD6643 with NSR enabled, certain options in VisualAnalog must be enabled. Click the button circled in the **FFT Analysis** box (see Figure 20) in VisualAnalog to bring up the options for setting the NSR.

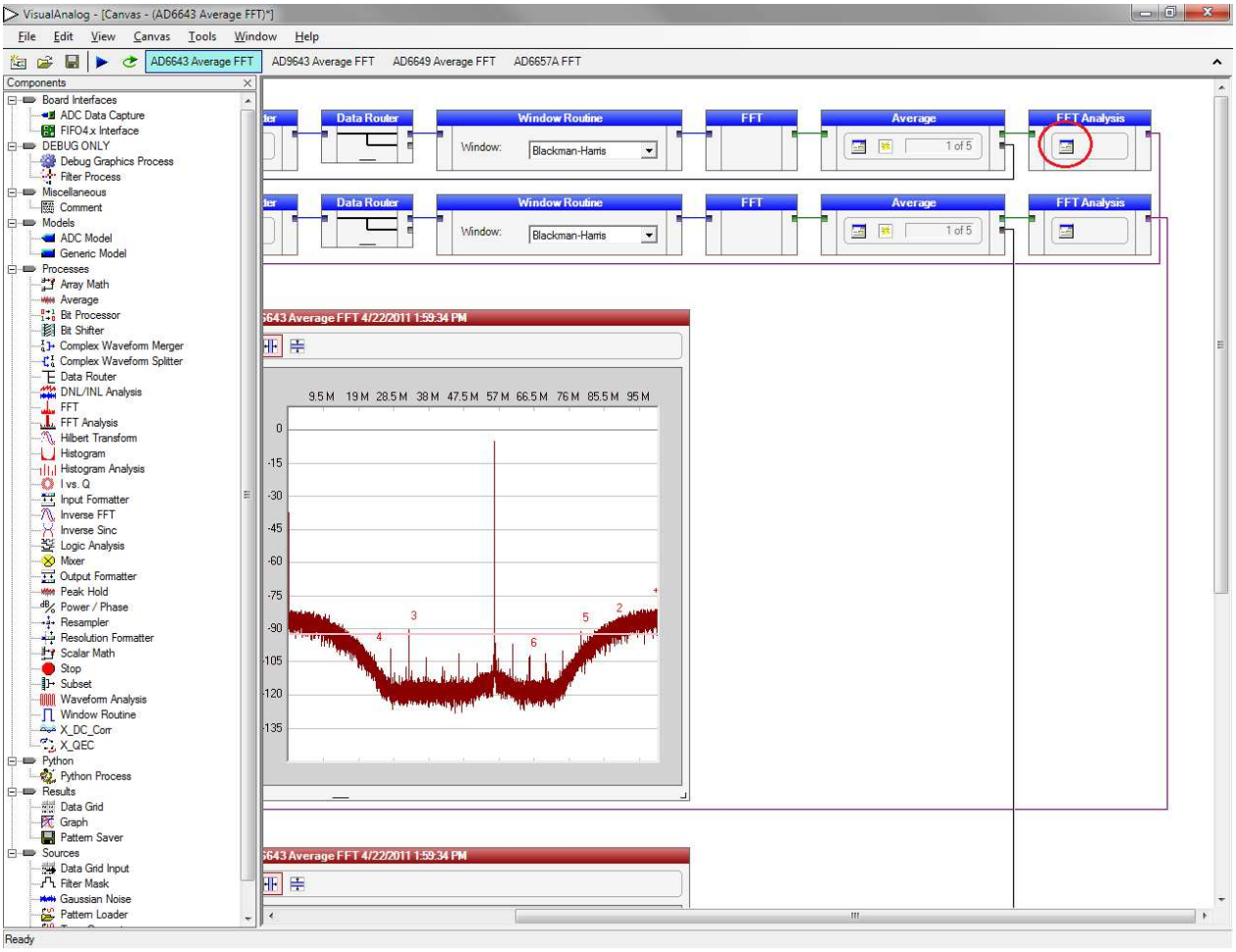
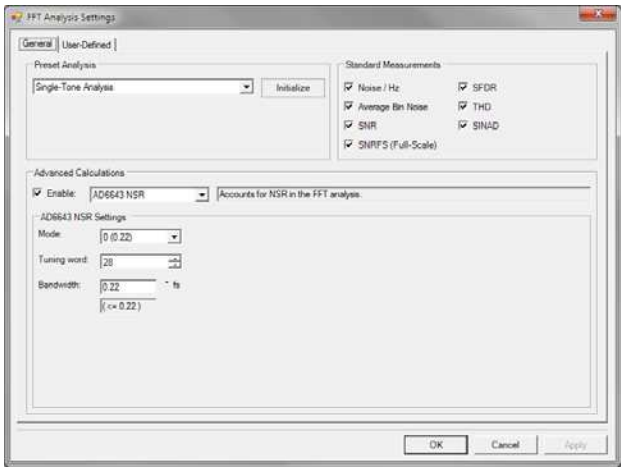


Figure 20. VisualAnalog, Main Window—Showing FFT Analysis for AD6643

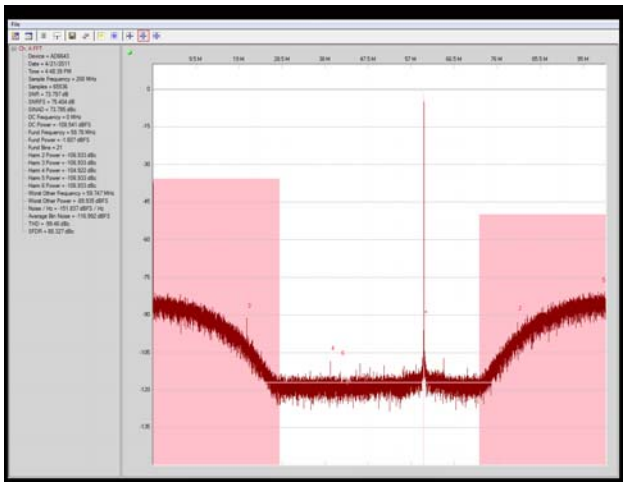
7. Configure the settings in the FFT analysis to match the settings selected for the NSR in the SPI controller (see Figure 21).



09940-021

Figure 21. VisualAnalog, FFT Analysis Settings for AD6643

8. The result should show an FFT plot that looks similar to Figure 22.



09940-022

Figure 22. Graph Window of VisualAnalog, NSR Enabled, AD6643

9. The amplitude shows approximately 0.6 dB lower than when the NSR is disabled. The NSR circuitry introduces this loss. An amplitude of −1.6 dBFS with NSR enabled is analogous to an amplitude of −1.0 dBFS with NSR disabled.
10. Repeat Step 3 to save the graph in a .csv file format.

Troubleshooting Tips

If the FFT plot appears abnormal, do the following:

- If you see a normal noise floor when you disconnect the signal generator from the analog input, be sure you are not overdriving the ADC. Reduce the input level, if necessary.
- In VisualAnalog, click the **Settings** button in the **Input Formatter** block (see Figure 7). Check that **Number Format** in the settings of the **Input Formatter** block is set to the correct encoding (offset binary by default). Repeat for the other channel.

If the FFT appears normal but the performance is poor, check the following:

- Make sure an appropriate filter is used on the analog input.
- Make sure the signal generators for the clock and the analog input are clean (low phase noise).
- Change the analog input frequency slightly if noncoherent sampling is being used.
- Make sure the SPI configuration file matches the product being evaluated.

If the FFT window remains blank after **Run** is clicked, do the following:

- Make sure the evaluation board is securely connected to the HSC-ADC-EVALCZ board.
- Make sure the FPGA has been programmed by verifying that the **DONE** LED is illuminated on the HSC-ADC-EVALCZ board. If this LED is not illuminated, make sure the U4 switch on the board is in the correct position for USB CONFIG.
- Make sure the correct FPGA program was installed by clicking the **Settings** button in the **ADC Data Capture** block in **VisualAnalog**. Then select the **FPGA** tab and verify that the proper FPGA bin file is selected for the part.

If VisualAnalog indicates that the data capture timed out, do the following:

- Make sure that all power and USB connections are secure.
- Probe the DCO signal at the ADC on the evaluation board and confirm that a clock signal is present at the ADC sampling rate.

EVALUATION BOARD SCHEMATICS AND ARTWORK

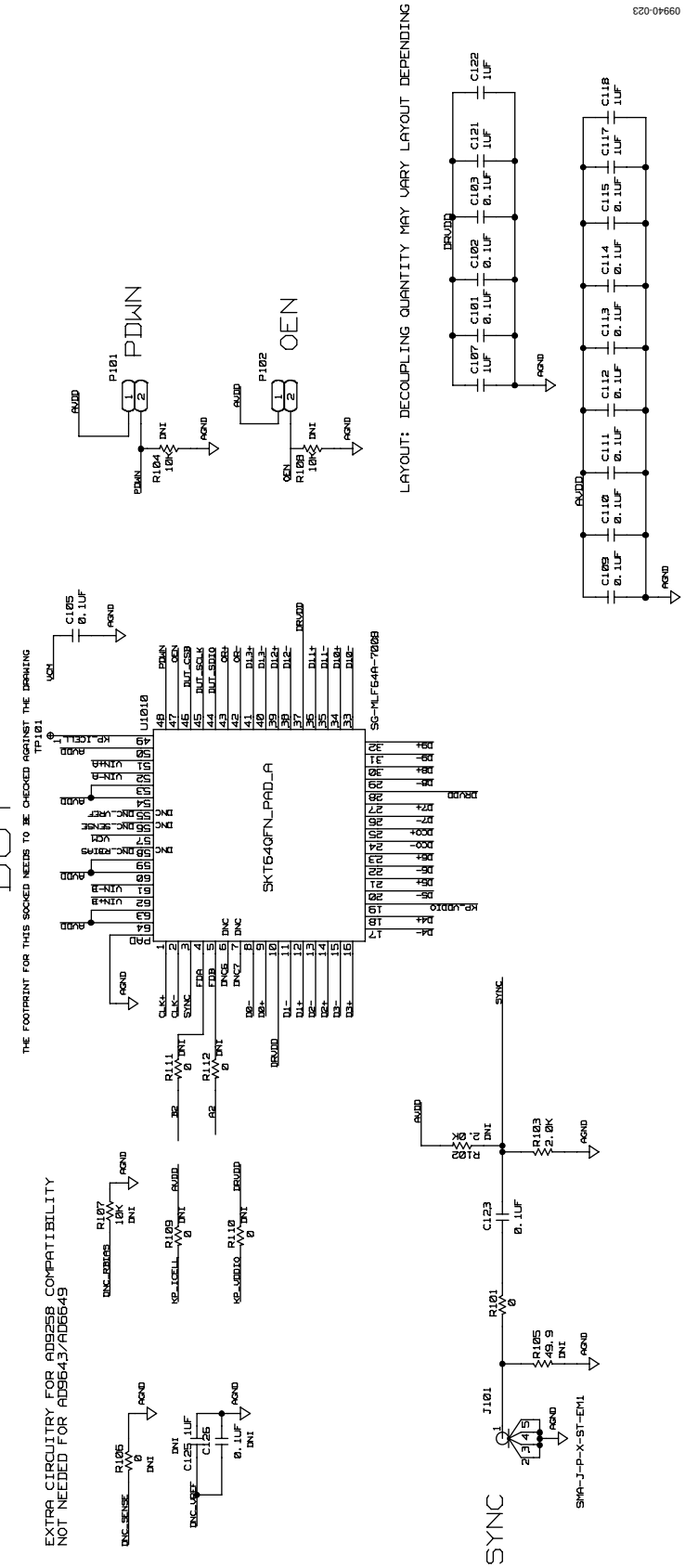


Figure 23. DUT and Related Circuits

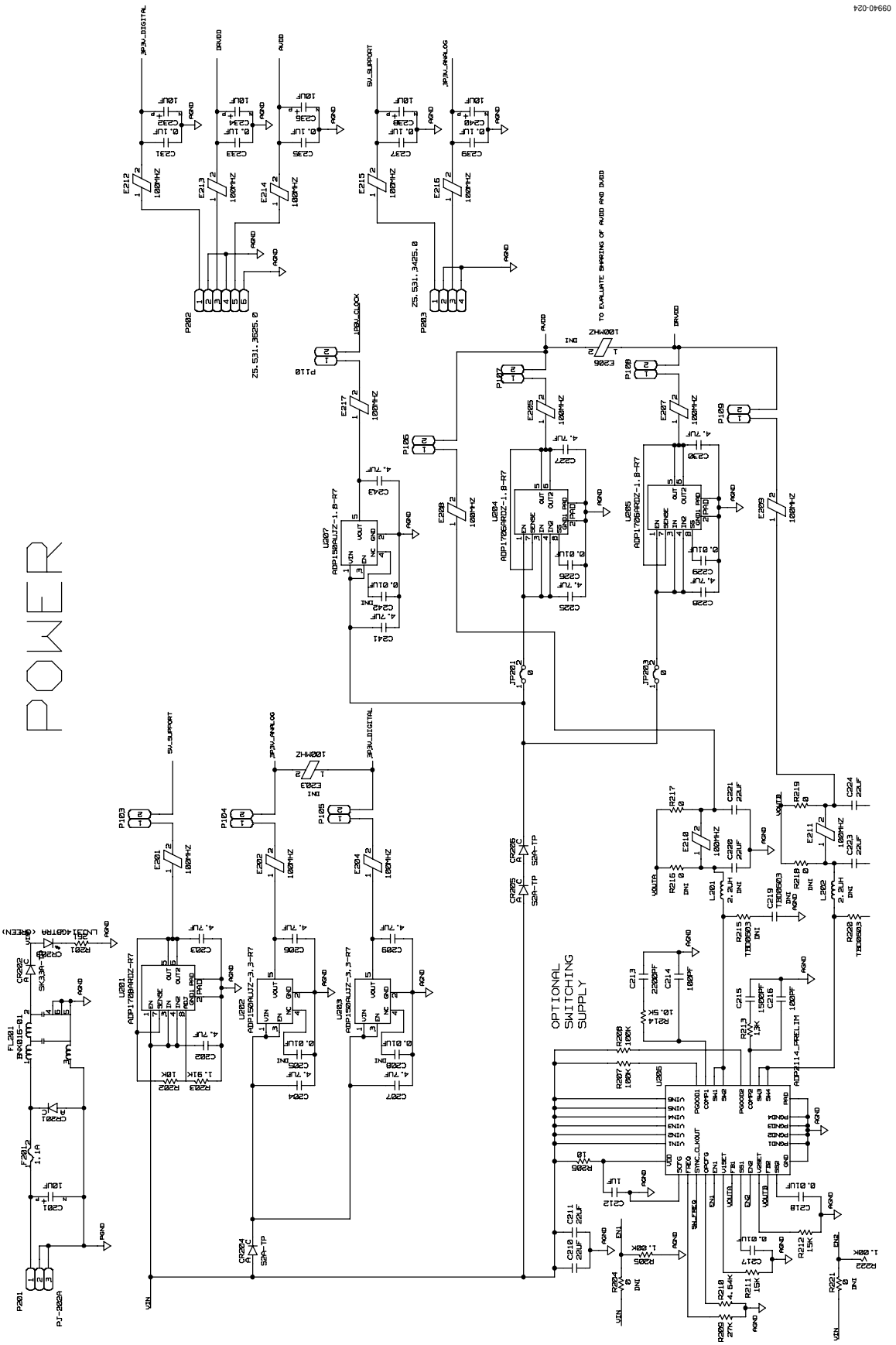


Figure 24. Board Power Input and Supply

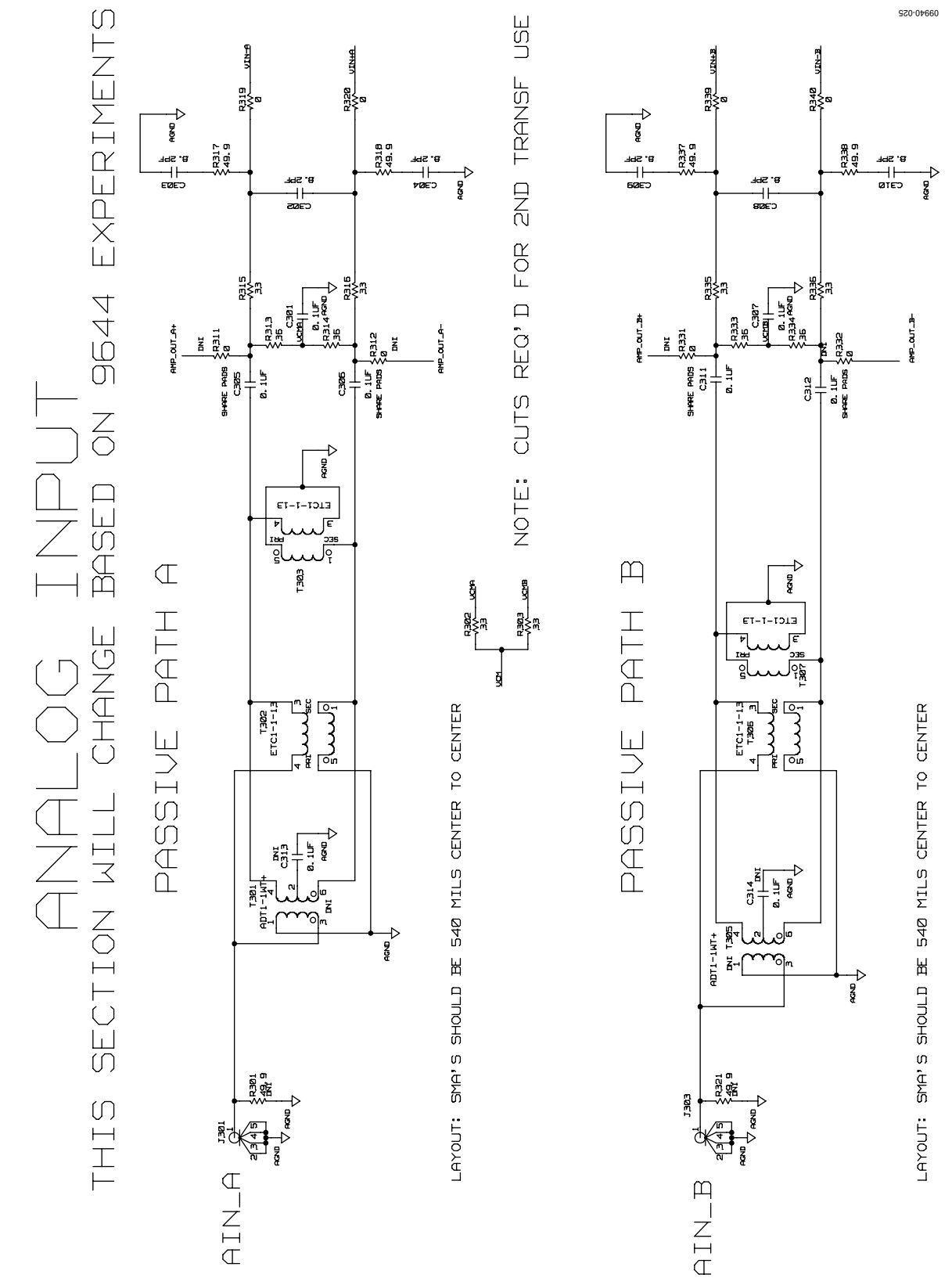


Figure 25. Passive Analog Input Circuits

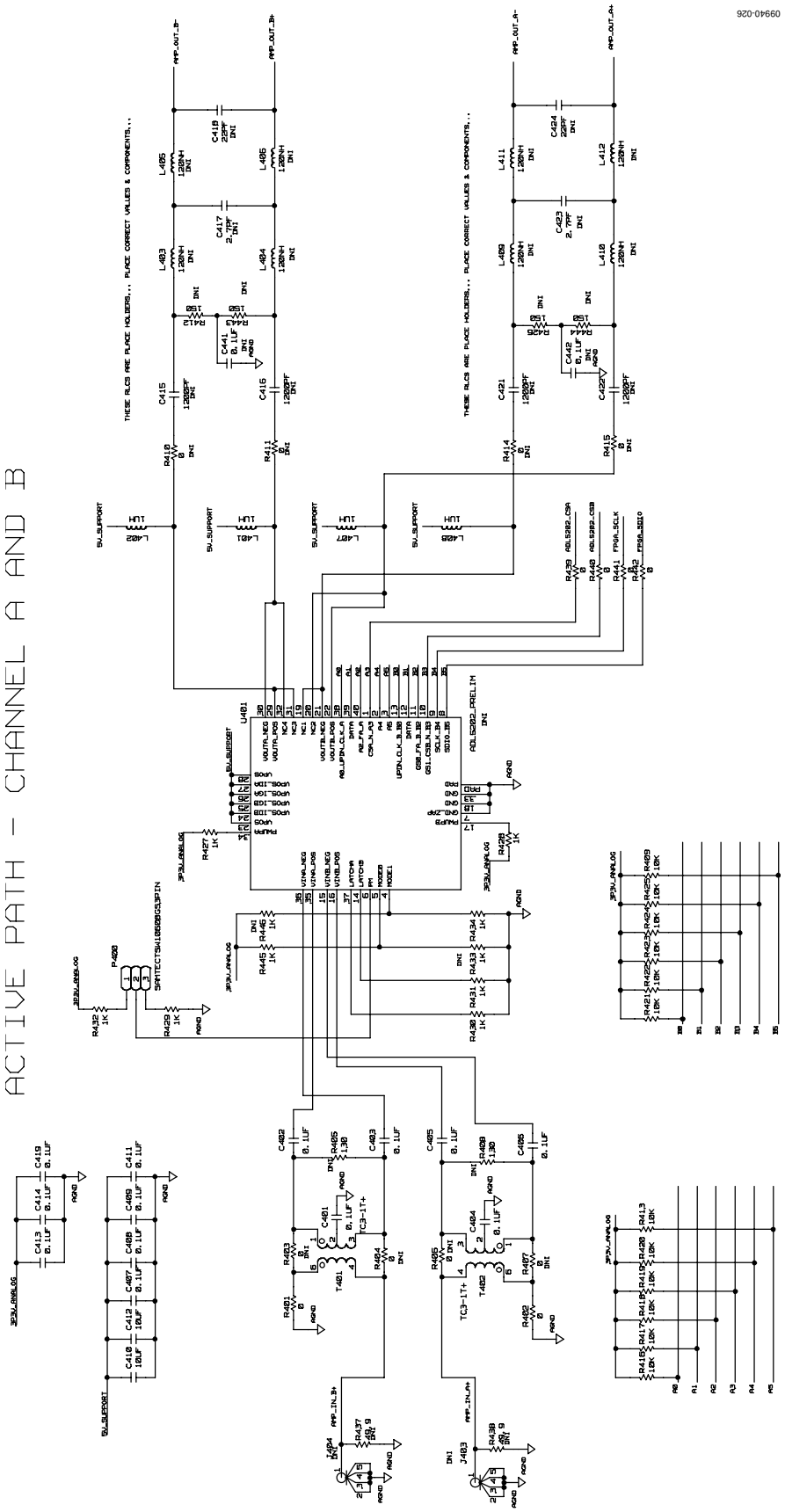


Figure 26. Optional Active Input Circuits

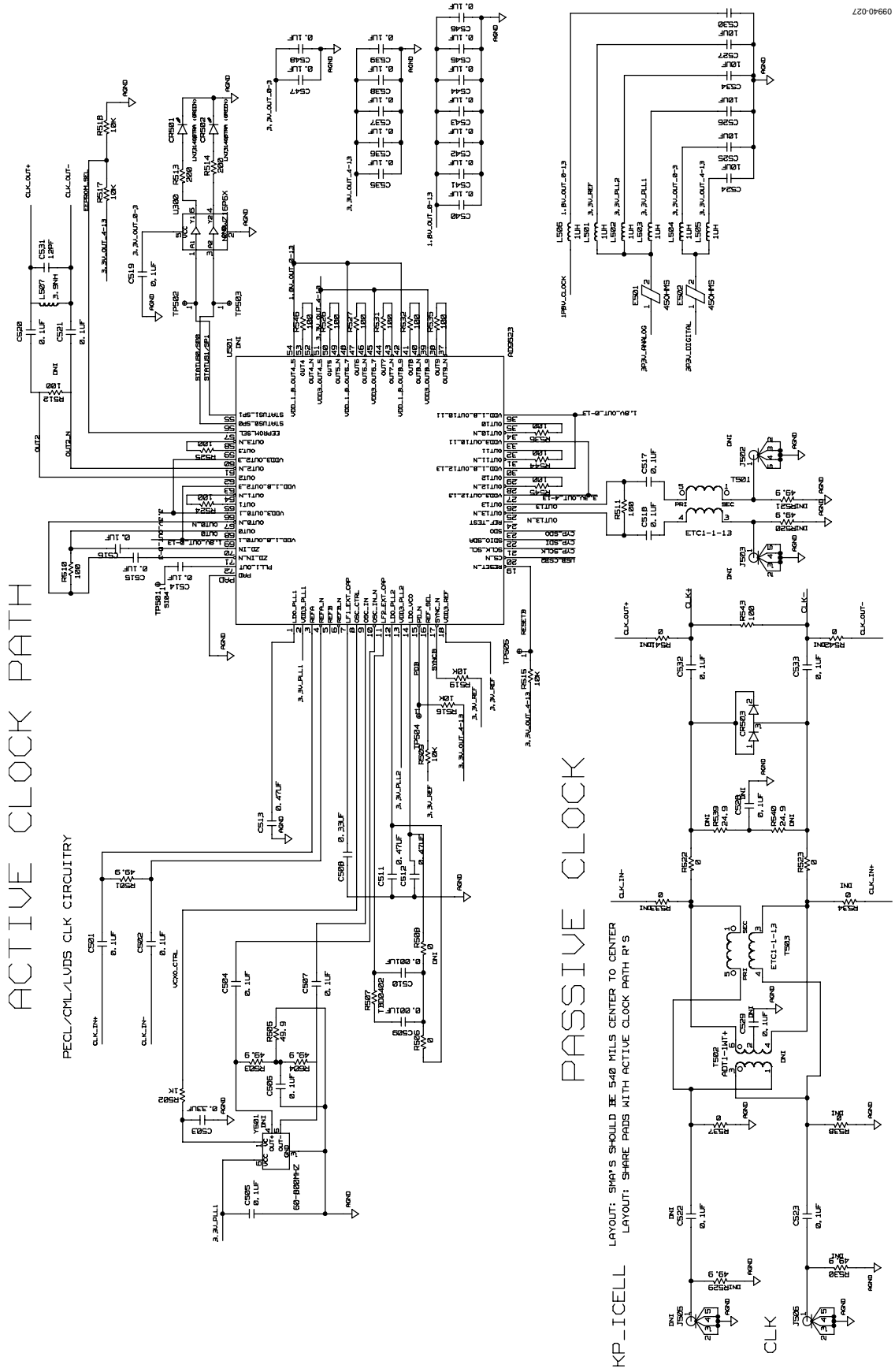


Figure 27. Default and Optional Clock Input Circuits

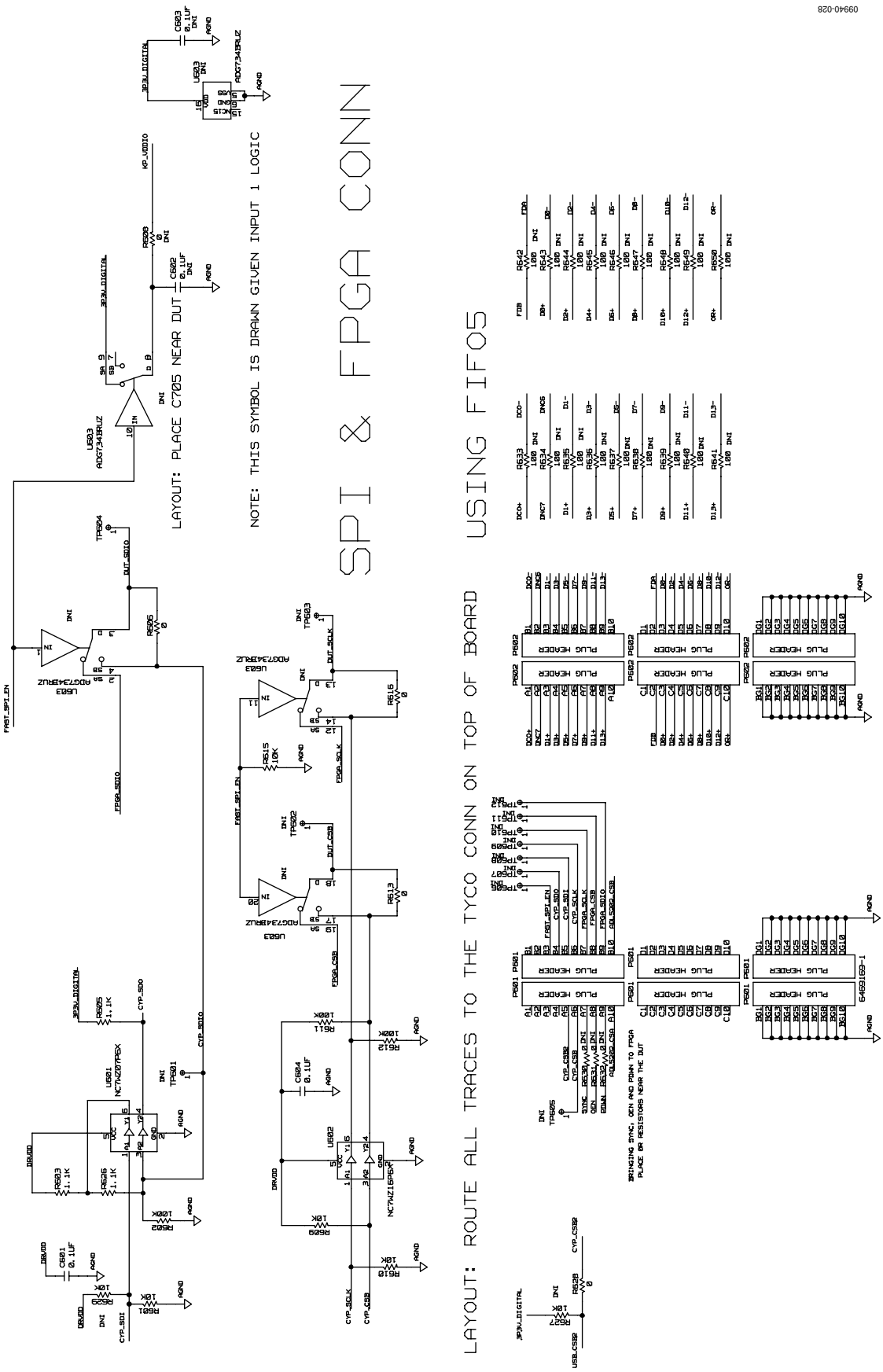


Figure 28. SPI Configuration Circuit and FIFO Board Connector Circuit

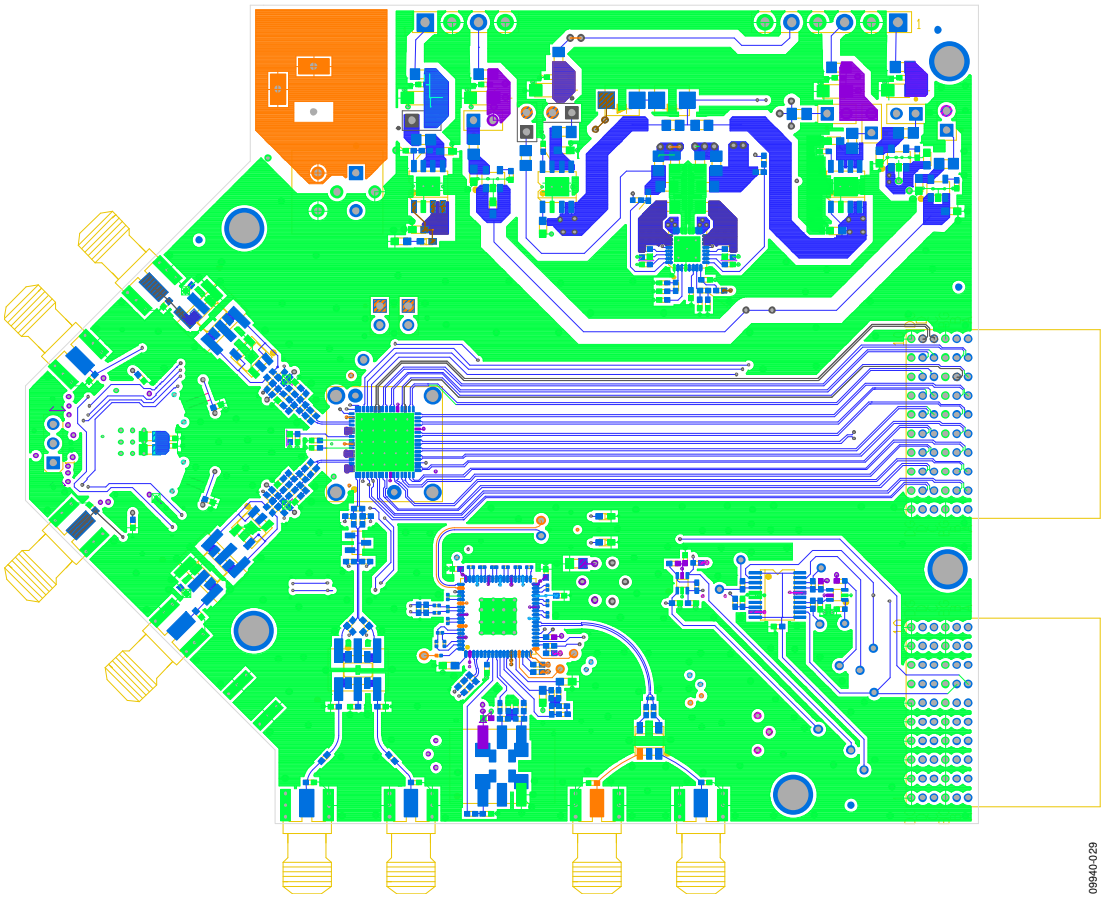


Figure 29. Top Side

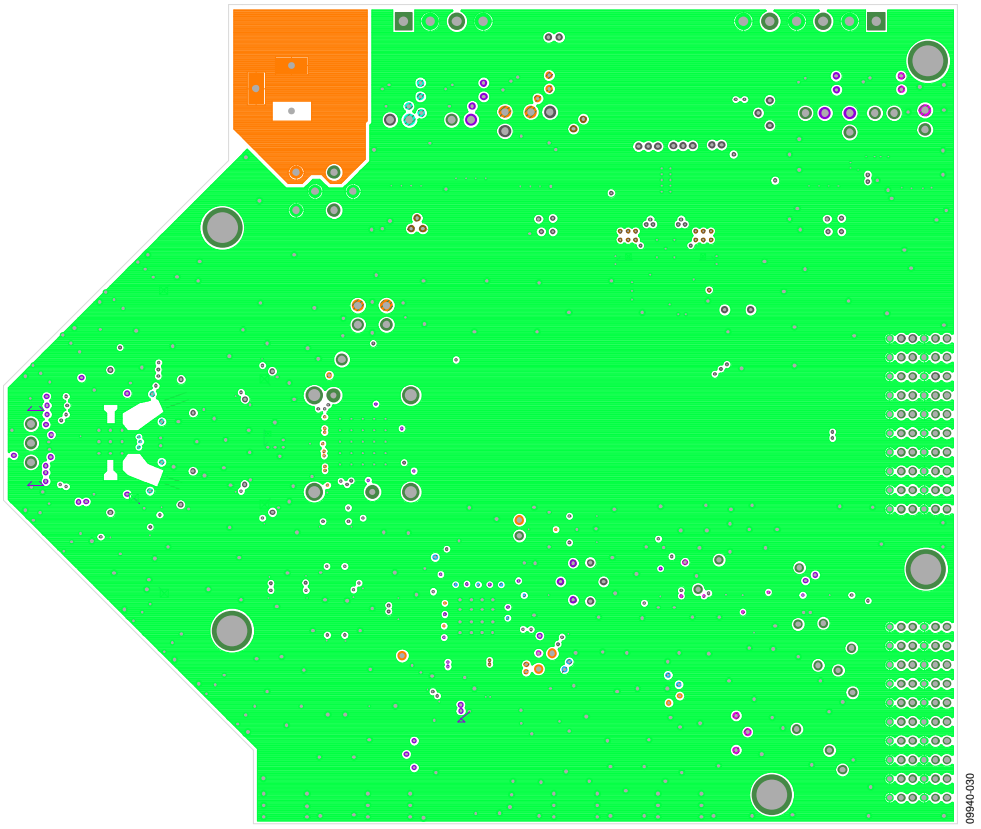


Figure 30. Ground Plane (Layer 2)

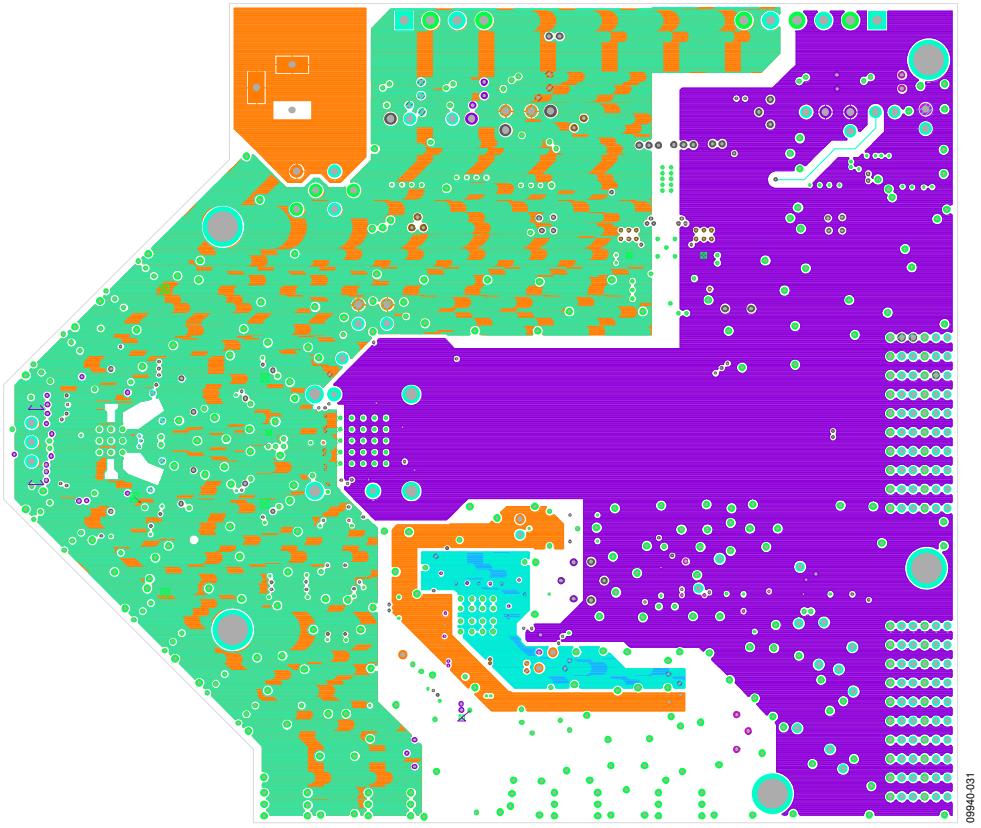


Figure 31. Power Plane (Layer 3)

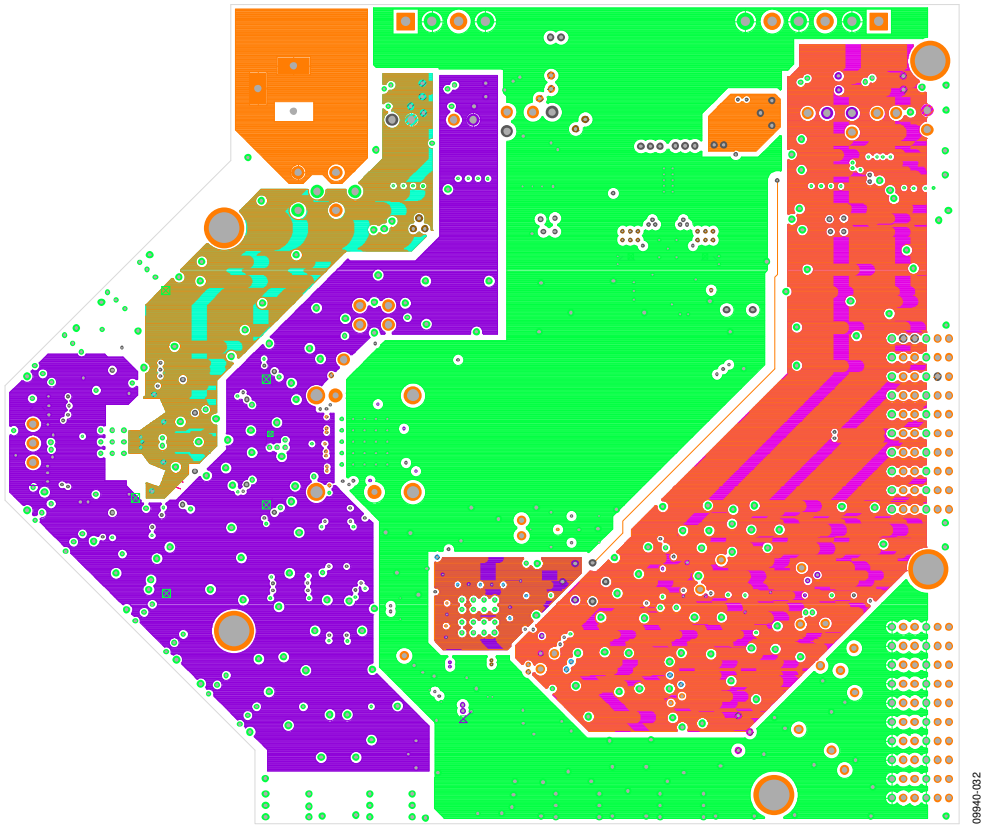


Figure 32. Power Plane (Layer 4)

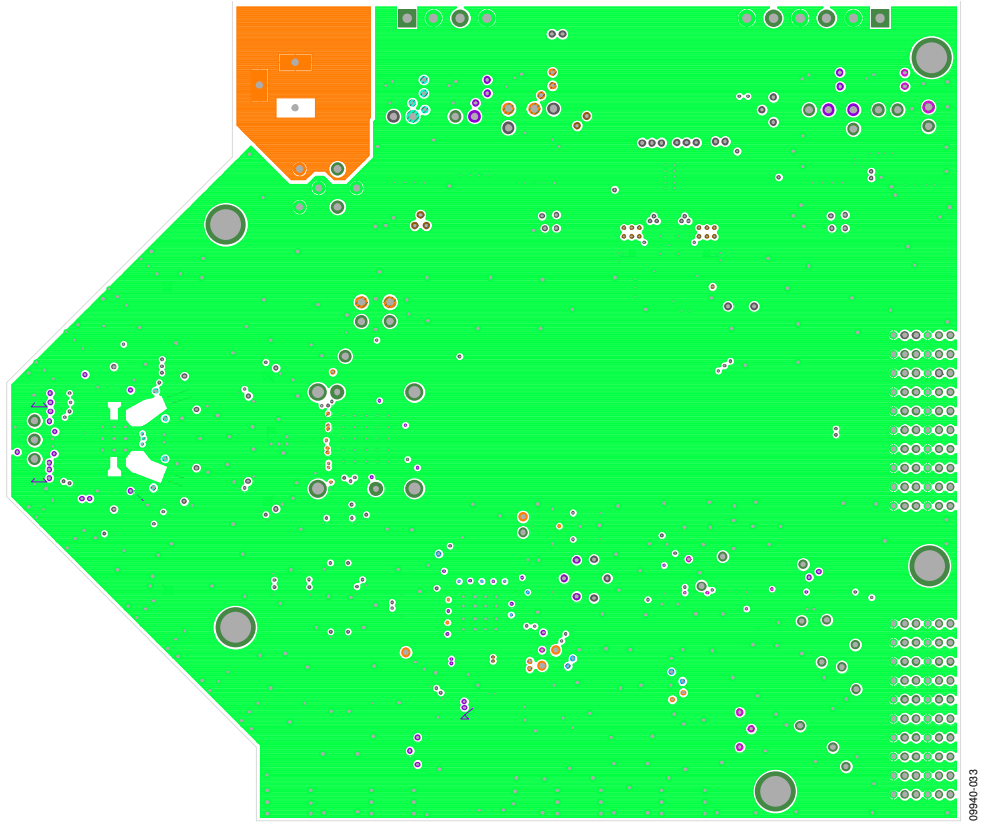


Figure 33. Ground Plane (Layer 5)

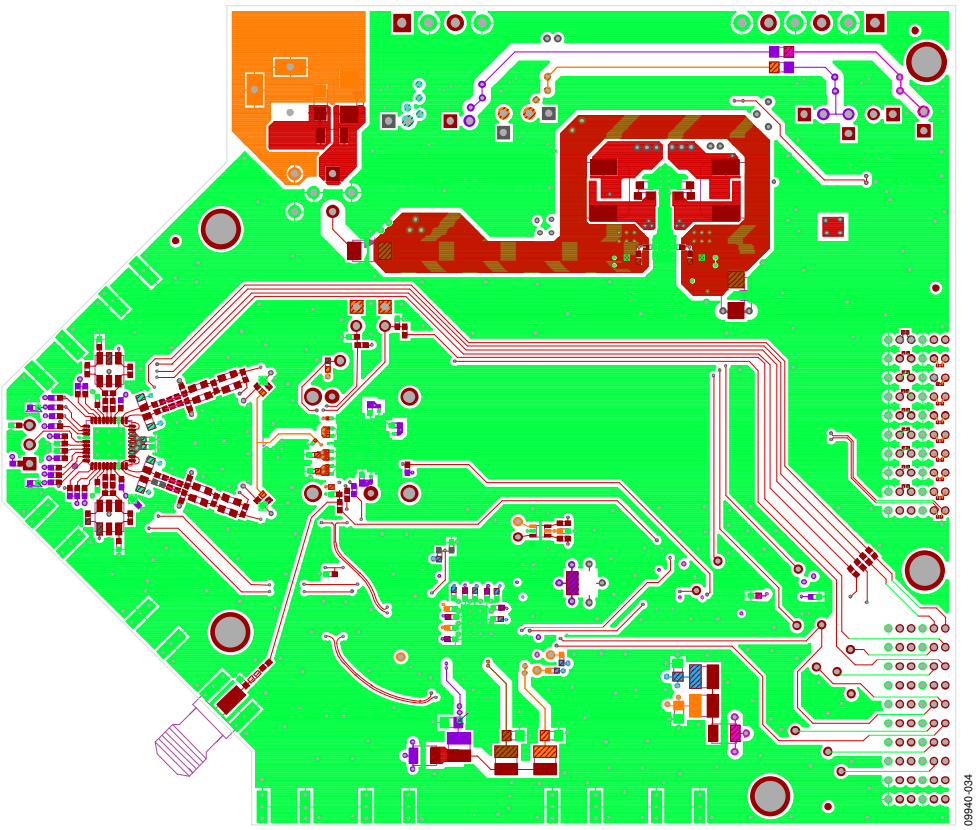


Figure 34. Bottom Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 1. AD9643/AD9613/AD6649/AD6643 Bill of Materials

Item	Qty	Reference Designator	Description	Manufacturer/Part No.
1	1	N/A	Printed circuit board, AD9643 engineering board	9643EE01
2	16	C101, C102, C103, C105, C109, C110, C111, C112, C113, C114, C115, C514, C515, C516, C520, C521	0.1 µF capacitor ceramic X5R 0201	Murata GRM033R60J104KE19D
3	6	C107, C117, C118, C121, C122, C212	1 µF capacitor monolithic ceramic 0402	Murata GRM155R60J105KE19D
4	50	C123, C231, C233, C235, C237, C239, C301, C305, C306, C307, C311, C312, C401, C402, C403, C404, C405, C406, C407, C408, C409, C411, C413, C414, C419, C501, C502, C504, C505, C506, C507, C517, C518, C519, C535, C536, C537, C538, C539, C540, C541, C542, C543, C544, C545, C546, C547, C548, C601, C604	0.1 µF capacitor ceramic X7R 0402	Murata GRM155R71C104KA88D
5	6	C201, C232, C234, C236, C238, C240	10 µF capacitor tantalum	AVX TAJA106K010RNJ
6	12	C202, C203, C204, C206, C207, C209, C225, C227, C228, C230, C241, C243	4.7 µF capacitor monolithic ceramic X5R	Murata GRM188R60J475KE19
7	6	C210, C211, C220, C221, C223, C224	22 µF capacitor ceramic chip	Murata GRM21BR60J226ME39L
8	1	C213	2200 pF capacitor ceramic X7R 0402	Phycomp (Yageo) CC0402KRX7R9BB222
9	2	C214, C216	100 pF capacitor chip mono ceramic C0G 0402	Murata GRM1555C1H101JD01D
10	1	C215	1500 pF capacitor ceramic X7R 0402	Murata GRM155R71H152KA01D
11	4	C217, C218, C226, C229	0.01 µF capacitor ceramic X7R 0402	Murata GRM155R71H103KA01D
12	2	C302, C308	3.9 pF capacitor ceramic NP0 0402	Murata GRM1555C1H3R9CZ01D
13	4	C303, C304, C309, C310	8.2 pF capacitor ceramic NP0 0402	YAGEO 0402CG829D9B200
14	8	C410, C412, C524, C525, C526, C527, C530, C534	10 µF capacitor ceramic monolithic	Murata GRM21BR61C106KE15L
15	2	C503, C508	0.33 µF capacitor ceramic X5R	Murata GRM155R61A334KE15D
16	1	C510	0.001 µF capacitor ceramic monolithic	Murata GRM155R71H102KA01D
17	3	C511, C512, C513	0.47 µF capacitor chip ceramic X7R 0603	Murata GCM188R71C474KA55D
18	3	C523, C532, C533	390 pF capacitor chip monolithic ceramic C0G 0402	Murata GRM1555C1H391JA01D
19	1	CR201	Diode rectifier GPP SMD	Diode, Inc. S1AB-13
20	1	CR202	Diode Schottky 3-amp rectifier	MCC SK33A-TP
21	3	CR203, CR501, CR502	LED green surface-mount	Panasonic LNJ314G8TRA
22	3	CR204, CR205, CR206	Diode recovery rectifier	Micro Commercial Components CORP S2A-TP
23	1	CR503	Diode Schottky dual series	Avago HSMS-2812BLK
24	15	E201, E202, E204, E205, E207, E208, E209, E210, E211, E212, E213, E214, E215, E216, E217	100 MHZ inductor ferrite bead	Panasonic EXC-ML20A390U
25	2	E501, E502	45 Ω chip bead core	Panasonic EXCCL3225U1
26	1	F201	1.1 A fuse poly-switch PTC device 1812	Tyco Electronics NANOSMDC110F-2
27	1	FL201	Filter noise suppression LC combined type	Murata BNX016-01
28	4	J101, J301, J303, J506	Connector-PCB SMA ST edge mount	Samtec SMA-J-P-X-ST-EM1
29	2	JP201, JP203	0 Ω resistor jumper SMD 0805 (SHRT)	Panasonic ERJ-6GEYJ0.0
30	4	L401, L402, L407, L408	1 µH inductor SM	Coilcraft 0603LS-102XGLB
31	6	L501, L502, L503, L504, L505, L506	1 µH inductor SMT power	Coilcraft ME3220-102MLB
32	10	P101, P102, P103, P104, P105, P106, P107, P108, P109, P110	Connector-PCB header 2-position	Samtec TSW-102-08-G-S

Item	Qty	Reference Designator	Description	Manufacturer/Part No.
33	1	P201	Connector-PCB DC power jack SM	CUI, Inc. PJ-202A
34	1	P202	Connector-PCB header 6-position	Wieland Z5.531.3625.0
35	1	P203	Connector-PCB, pluggable header	Wieland Z5.531.3425.0
36	1	P400	Connector-PCB BERG header ST male 3-pin	Samtec TSW-103-08-G-S
37	2	P601, P602	Connector-PCB 60-pin RA connector	Tyco 6469169-1
38	18	C528, R101, R217, R219, R401, R402, R439, R440, R441, R442, R506, R522, R523, R537, R606, R613, R616, R628	0 Ω resistor film SMD 0402	Panasonic ERJ-2GE0R00X
39	1	R201	261 Ω resistor film chip thick	NIC Components Corp NRC06F2610TRF
40	22	R202, R409, R413, R416, R417, R418, R419, R420, R421, R422, R423, R424, R425, R509, R515, R516, R518, R519, R601, R609, R610, R615	10 kΩ resistor PREC thick film chip R0402	Panasonic ERJ-2RKF1002X
41	2	R103, R203	1.91 kΩ resistor PREC thick film chip R0402	Panasonic ERJ-2RKF1911X
42	14	R205, R222, R427, R428, R429, R430, R431, R432, R434, R445, R502, R603, R605, R626	1.00 kΩ resistor PREC thick film chip R0402	Panasonic ERJ-2RKF1001X
43	5	R206, R319, R320, R339, R340	10 Ω resistor PREC thick film chip R0402	Panasonic ERJ-2RKF10R0X
44	5	R207, R208, R602, R611, R612	100 kΩ resistor PREC thick film chip R0402	Panasonic ERJ-2RKF1003X
	1	R209	27 kΩ resistor CHIP SMD 0402	Panasonic ERJ-2RKF2702X
46	1	R210	4.64 kΩ resistor PREC thick film chip R0402	Panasonic ERJ-2RKF4641X
47	2	R211, R212	15 kΩ resistor chip SMD 0402	Panasonic ERJ-2RKF1502X
48	1	R213	13 kΩ resistor film SMD 0402	Yageo 9C04021A1302FLHF3
49	1	R214	10.5 kΩ resistor PREC thick film chip R0402	Panasonic ERJ-2RKF1052X
50	4	R302, R303, R539, R540	33 Ω resistor film SMD 0402	Panasonic ERJ-2GEJ330X
51	4	R313, R314, R333, R334	36 Ω resistor film SMD 0402	Panasonic ERJ-2GEJ360X
52	4	R315, R316, R335, R336	15.0 Ω resistor film SMD 0402	Panasonic ERJ-2RFK15R0X
53	8	R317, R318, R337, R338, R501, R503, R505, R604	49.9 Ω resistor PREC thick film chip R0402	Panasonic ERJ-2RKF49R9X
54	13	R510, R511, R524, R525, R526, R527, R531, R532, R535, R536, R544, R545, R546	100 Ω resistor PREC thick film chip R0201	Panasonic ERJ-1GEF1000C
55	2	R513, R514	200 Ω resistor PREC thick film chip R0402	Panasonic ERJ-2RKF2000X
56	6	T302, T303, T306, T307, T501, T503	XFMR RF 1:1	M/A-COM ETC1-1-13
57	1	U1010	SKT 64-pin LFCSP	Analog Devices AD6649BCPZ or AD9643BCPZ
58	1	U201	IC Analog Devices low dropout CMOS linear regulator	Analog Devices ADP1708ARDZ-R7
59	2	U202, U203	IC 150 mA ultralow noise, CMOS linear regulator	Analog Devices ADP150AUJZ-3.3-R7
60	2	U204, U205	IC Analog Devices low dropout CMOS linear regulator	Analog Devices ADP1706ARDZ-1.8-R7
61	1	U206	IC Analog Devices dual configurable synchronous PWM step-down regulator	Analog Devices ADP2114ACPZ
62	1	U207	IC 150 mA ultralow noise, CMOS linear regulator	Analog Devices ADP150AUJZ-1.8-R7
63	2	U300, U602	IC tiny logic UHS dual buffer	Fairchild NC7WZ16P6X
64	1	U601	IC tiny logic UHS dual buffer	Fairchild NC7WZ07P6X
65[1]		C125	1 µF capacitor monolithic ceramic 0402	Murata GRM155R60J105KE19D
66[1]		C126, C313, C314, C441, C442, C522, C529, C602, C603	0.1 µF capacitor ceramic X7R 0402	Murata GRM155R71C104KA88D
67[1]		C205, C208, C242	0.01 µF capacitor ceramic X7R 0402	Murata GRM155R71H103KA01D