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14-Bit, 80 MSPS/155 MSPS, 1.8 V Dual Serial Output Analog-to-Digital Converter (ADC)

Data Sheet **AD9644**

FEATURES

- JESD204A coded serial digital outputs
- SNR = 73.7 dBFS at 70 MHz and 80 MSPS
- SNR = 71.7 dBFS at 70 MHz and 155 MSPS
- SFDR = 92 dBc at 70 MHz and 80 MSPS
- SFDR = 92 dBc at 70 MHz and 155 MSPS
- Low power: 423 mW at 80 MSPS, 567 mW at 155 MSPS
- 1.8 V supply operation
- Integer 1-to-8 input clock divider
- IF sampling frequencies to 250 MHz
- −148.6 dBFS/Hz input noise at 180 MHz and 80 MSPS
- −150.3 dBFS/Hz input noise at 180 MHz and 155 MSPS
- Programmable internal ADC voltage reference
- Flexible analog input range: 1.4 V p-p to 2.1 V p-p
- ADC clock duty cycle stabilizer
- Serial port control
- User-configurable, built-in self-test (BIST) capability
- Energy-saving power-down modes

APPLICATIONS

- Communications
- Diversity radio systems
- Multimode digital receivers (3G and 4G)
  - GSM, EDGE, W-CDMA, LTE,
  - CDMA2000, WiMAX, TD-SCDMA
- I/Q demodulation systems
- Smart antenna systems
- General-purpose software radios
- Broadband data applications
- Ultrasound equipment

FUNCTIONAL BLOCK DIAGRAM

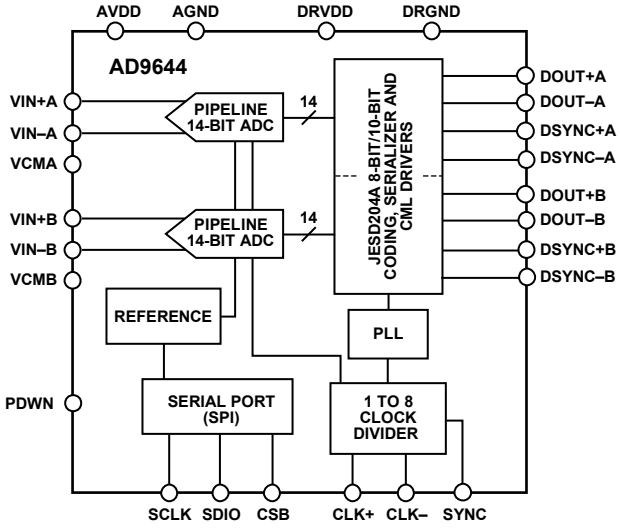

Figure 1. 48-Lead 7 mm × 7 mm LFCSP

PRODUCT HIGHLIGHTS

1. An on-chip PLL allows users to provide a single ADC sampling clock; the PLL multiplies the ADC sampling clock to produce the corresponding JESD204A data rate clock.
2. The configurable JESD204A output block supports up to 1.6 Gbps per channel data rate when using a dedicated data link per ADC or 3.2 Gbps data rate when using a single shared data link for both ADCs.
3. Proprietary differential input that maintains excellent SNR performance for input frequencies up to 250 MHz.
4. Operation from a single 1.8 V power supply.
5. Standard serial port interface (SPI) that supports various product features and functions, such as data formatting (offset binary, twos complement, or gray coding), controlling the clock DCS, power-down, test modes, voltage reference mode, and serial output configuration.

Rev. C

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AD9644* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9644 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-586: LVDS Outputs for High Speed A/D Converters
- AN-742: Frequency Domain Response of Switched-Capacitor ADCs
- AN-807: Multicarrier WCDMA Feasibility
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-812: MicroController-Based Serial Port Interface (SPI) Boot Circuit
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-878: High Speed ADC SPI Control Software
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD9644: 14-Bit, 80 MSPS/155 MSPS, 1.8 V Dual Serial Output Analog-to-Digital Converter (ADC) Data Sheet

User Guides

- UG-294: Evaluating the AD9644/AD9641 Analog-to-Digital Converters

TOOLS AND SIMULATIONS

- Visual Analog
- AD9644 IBIS Model
- AD9641/AD9644-155 S-Parameter Data
- AD9641/AD9644-80 S-Parameter Data

REFERENCE MATERIALS

Informational

- JESD204 Serial Interface

Technical Articles

- Improve The Design Of Your Passive Wideband ADC Front-End Network
- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9644 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9644 EngineerZone Discussions.

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6/10—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9644 is a dual, 14-bit, analog-to-digital converter (ADC) with a high speed serial output interface and sampling speeds of either 80 MSPS or 155 MSPS.

The AD9644 is designed to support communications applications where high performance, combined with low cost, small size, and versatility, is desired. The JESD204A high speed serial interface reduces board routing requirements and lowers pin count requirements for the receiving device.

The dual ADC core features a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth differential sample-and-hold analog input amplifiers that support a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

By default, the ADC output data is routed directly to the two external JESD204A serial output ports. These outputs are at CML voltage levels. Two modes are supported such that output coded data is either sent through one data link or two. (L = 1; F = 4 or L = 2; F = 2). Independent synchronization inputs (DSYNC) are provided for each channel.

Flexible power-down options allow significant power savings, when desired.

Programming for setup and control is accomplished using a 3-wire SPI-compatible serial interface.

The AD9644 is available in a 48-lead LFCSP and is specified over the industrial temperature range of −40°C to +85°C.

This product is protected by a U.S. patent.

SPECIFICATIONS

ADC DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, 1.75 V p-p differential input, VIN = −1.0 dBFS differential input, DCS enabled, unless otherwise noted.

Table 1.

		AD9644-80			AD9644-155			
Parameter	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	14			14			Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	Full		±2	±10		±2.2	±11	mV
Gain Error	Full	−7	−2.5	+1	−6	−1.5	+4	% FSR
Differential Nonlinearity (DNL)[1]	Full			±0.55			±0.55	LSB
	25°C		±0.3			±0.3		LSB
Integral Nonlinearity (INL)[1]	Full			±1.1			±1.25	LSB
	25°C		±0.5			±0.55		LSB
MATCHING CHARACTERISTIC								
Offset Error	Full	−7	+1.5	+10	−6	+1.5	+9	mV
Gain Error	Full	−1.5	+0.6	+2.75	−3.1	+0.75	+5	% FSR
TEMPERATURE DRIFT								
Offset Error	Full		±2			±2		ppm/°C
Gain Error	Full		±35			±144		ppm/°C
INPUT REFERRED NOISE	25°C		0.7			0.7		LSB rms
ANALOG INPUT								
Input Span	Full	1.383	1.75	2.087	1.383	1.75	2.087	V p-p
Input Capacitance[2]	Full		7			5		pF
Input Resistance	Full		20			20		kΩ
VCM OUTPUT LEVEL	Full	0.88	0.9	0.92	0.87	0.9	0.93	V
POWER SUPPLIES								
Supply Voltage								
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
Supply Current								
IAVDD[1]	Full		175	190		226	242	mA
IDRVDD[1]	Full		60	67		89	97	mA
POWER CONSUMPTION								
Sine Wave Input1	Full		423	460		567	610	mW
Standby Power[3]	Full		85			168		mW
Power-Down Power	Full		15	27		18	27	mW

[1] Measured with a low input frequency, full-scale sine wave.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND.
[3] Standby power is measured with a dc input and with the CLK pins inactive (set to AVDD or AGND).

ADC AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, 1.75 V p-p differential input, VIN = −1.0 dBFS differential input, DCS enabled, unless otherwise noted.

Table 2.

		AD9644-80			AD9644-155			
Parameter[1]	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE-RATIO (SNR)								
f_{IN} = 10 MHz	25°C		73.8			71.9		dBFS
f_{IN} = 70 MHz	25°C		73.7			71.7		dBFS
f_{IN} = 180 MHz	25°C		72.6			71.4		dBFS
AD9644BCPZ-80	Full	71.8						dBFS
AD9644CCPZ-80	Full	70.0						dBFS
AD9644BCPZ-155	Full				69.8			dBFS
f_{IN} = 220 MHz	25°C		72.0			71.0		dBFS
SIGNAL-TO-NOISE AND DISTORTION (SINAD)								
f_{IN} = 10 MHz	25°C		72.7			70.8		dBFS
f_{IN} = 70 MHz	25°C		72.6			70.7		dBFS
f_{IN} = 180 MHz	25°C		71.5			70.3		dBFS
AD9644BCPZ-80	Full	70.4						dBFS
AD9644CCPZ-80	Full	68.6						dBFS
AD9644BCPZ-155	Full				68.7			dBFS
f_{IN} = 220 MHz	25°C		71.1			69.9		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)								
f_{IN} = 10 MHz	25°C		11.8			11.5		Bits
f_{IN} = 70 MHz	25°C		11.8			11.5		Bits
f_{IN} = 180 MHz	25°C		11.6			11.4		Bits
f_{IN} = 220 MHz	25°C		11.5			11.3		Bits
WORST SECOND OR THIRD HARMONIC								
f_{IN} = 10 MHz	25°C		−94			−94		dBc
f_{IN} = 70 MHz	25°C		−92			−92		dBc
f_{IN} = 180 MHz	25°C		−87			−92		dBc
AD9644BCPZ-80	Full			−80				dBc
AD9644CCPZ-80	Full			−73				dBc
AD9644BCPZ-155	Full						−80	dBc
f_{IN} = 220 MHz	25°C		−85			−90		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
f_{IN} = 10 MHz	25°C		94			94		dBc
f_{IN} = 70 MHz	25°C		92			92		dBc
f_{IN} = 180 MHz	25°C		87			92		dBc
AD9644BCPZ-80	Full	80						dBc
AD9644CCPZ-80	Full	73						dBc
AD9644BCPZ-155	Full				80			dBc
f_{IN} = 220 MHz	25°C		85			90		dBc
WORST OTHER (HARMONIC OR SPUR)								
f_{IN} = 10 MHz	25°C		−98			−97		dBc
f_{IN} = 70 MHz	25°C		−98			−97		dBc
f_{IN} = 180 MHz	25°C		−96			−95		dBc
AD9644BCPZ-80	Full			−90				dBc
AD9644CCPZ-80	Full			−87				dBc
AD9644BCPZ-155	Full						−89	dBc
f_{IN} = 220 MHz	25°C		−95			−94		dBc

Parameter[1]	Temperature	AD9644-80 Min	AD9644-80 Typ	AD9644-80 Max	AD9644-155 Min	AD9644-155 Typ	AD9644-155 Max	Unit
TWO-TONE SFDR								
f_{IN} = +30 MHz (−7 dBFS), +33 MHz (−7 dBFS)	25°C		93			90		dBc
f_{IN} = +169 MHz (−7 dBFS), +172 MHz (−7 dBFS)	25°C		89			89		dBc
CROSSTALK[2]	Full		−105			−105		dB
ANALOG INPUT BANDWIDTH[3]	25°C		780			780		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Crosstalk is measured at 100 MHz with −1.0 dBFS on one channel and no input on the alternate channel.
[3] Analog input bandwidth specifies the −3 dB input BW of the AD9644 input. The usable full-scale BW of the part with good performance is 250 MHz.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, 1.75 V p-p differential input, VIN = −1.0 dBFS differential input, and DCS enabled, unless otherwise noted.

Table 3.

Parameter	Temperature	AD9644-80/AD9644-155 Min	AD9644-80/AD9644-155 Typ	AD9644-80/AD9644-155 Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	−100		+100	µA
Low Level Input Current	Full	−100		+100	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
SYNC INPUT					
Logic Compliance			CMOS		
Internal Bias	Full		0.9		V
Input Voltage Range	Full	AGND		AVDD	V
High Level Input Voltage	Full	1.2		AVDD	V
Low Level Input Voltage	Full	AGND		0.6	V
High Level Input Current	Full	−100		+100	µA
Low Level Input Current	Full	−100		+100	µA
Input Capacitance	Full		1		pF
Input Resistance	Full	12	16	20	kΩ
DSYNC INPUT					
Logic Compliance			CMOS/LVDS		
Internal Bias	Full		0.9		V
Input Voltage Range	Full	AGND		AVDD	V
High Level Input Voltage	Full	1.2		AVDD	V
Low Level Input Voltage	Full	AGND		0.6	V
High Level Input Current	Full	−100		+100	µA
Low Level Input Current	Full	−100		+100	µA
Input Capacitance	Full		1		pF
Input Resistance	Full	12	16	20	kΩ

Parameter	Temperature	AD9644-80/AD9644-155 Min	Typ	Max	Unit
LOGIC INPUT (CSB)[1]					
Logic Compliance			CMOS		
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	40		132	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SCLK, PDWN)[2]					
Logic Compliance			CMOS		
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current (VIN = 1.8 V)	Full	−92		−135	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT/OUTPUT (SDIO)[1]					
Logic Compliance			CMOS		
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	38		128	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS					
Logic Compliance	Full		CML		
Differential Output Voltage (V_{OD})	Full	0.6	0.8	1.1	V
Output Offset Voltage (V_{OS})	Full	0.75	DRVDD/2	1.05	V

[1] Pull up.
[2] Pull down.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, 1.75 V p-p differential input, VIN = −1.0 dBFS differential input, and DCS enabled, unless otherwise noted.

Table 4.

		AD9644-80			AD9644-155			
Parameter	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUT PARAMETERS								
Input Clock Rate	Full			640			640	MHz
Conversion Rate[1]	Full	40		80	40		155	MSPS
CLK Period—Divide-by-1 Mode (t_{CLK})	Full	12.5			6.45			ns
CLK Pulse Width High (t_{CH})								
Divide-by-1 Mode, DCS Enabled	Full	3.75	6.25	8.75	1.935	3.225	4.515	ns
Divide-by-1 Mode, DCS Disabled	Full	5.95	6.25	6.55	3.065	3.225	3.385	ns
Divide-by-2 Mode Through Divide-by-8 Mode	Full	0.8			0.8			ns
Aperture Delay (t_A)	Full		0.78			0.78		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.125			0.125		ps rms
DATA OUTPUT PARAMETERS								
Data Output Period or UI (Unit Interval)	Full		$1/(20 \times f_{CLK})$			$1/(20 \times f_{CLK})$		Seconds
Data Output Duty Cycle	25°C		50			50		%
Data Valid Time	25°C		0.78			0.74		UI
PLL Lock Time (t_{LOCK})	25°C		4			4		µs
Wake Up Time (Standby)	25°C		5			5		µs
Wake Up Time (Power-Down)[2]	25°C		2.5			2.5		ms
Pipeline Delay (Latency)	Full	23		24	23		24	CLK cycles
Data Rate per Channel (NRZ)	25°C		1.6			3.1		Gbps
Deterministic Jitter	25°C		40			40		ps
Random Jitter at 1.6 Gbps	25°C		9.5					ps rms
Random Jitter at 3.2 Gbps	25°C		5.2			5.2		ps rms
Output Rise/Fall Time	25°C		50			50		ps
TERMINATION CHARACTERISTICS								
Differential Termination Resistance	25°C		100			100		Ω
OUT-OF-RANGE RECOVERY TIME	25°C		2			2		CLK cycles

[1] Conversion rate is the clock rate after the divider.
[2] Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Conditions	Limit
SYNC TIMING REQUIREMENTS		
t_{SSYNC}	SYNC to rising edge of CLK+ setup time	0.30 ns typ
t_{HSYNC}	SYNC to rising edge of CLK+ hold time	0.30 ns typ
SPI TIMING REQUIREMENTS		
t_{DS}	Setup time between the data and the rising edge of SCLK	2 ns min
t_{DH}	Hold time between the data and the rising edge of SCLK	2 ns min
t_{CLK}	Period of the SCLK	40 ns min
t_S	Setup time between CSB and SCLK	2 ns min
t_H	Hold time between CSB and SCLK	2 ns min
t_{HIGH}	SCLK pulse width high	10 ns min
t_{LOW}	SCLK pulse width low	10 ns min
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10 ns min
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10 ns min

Timing Diagrams

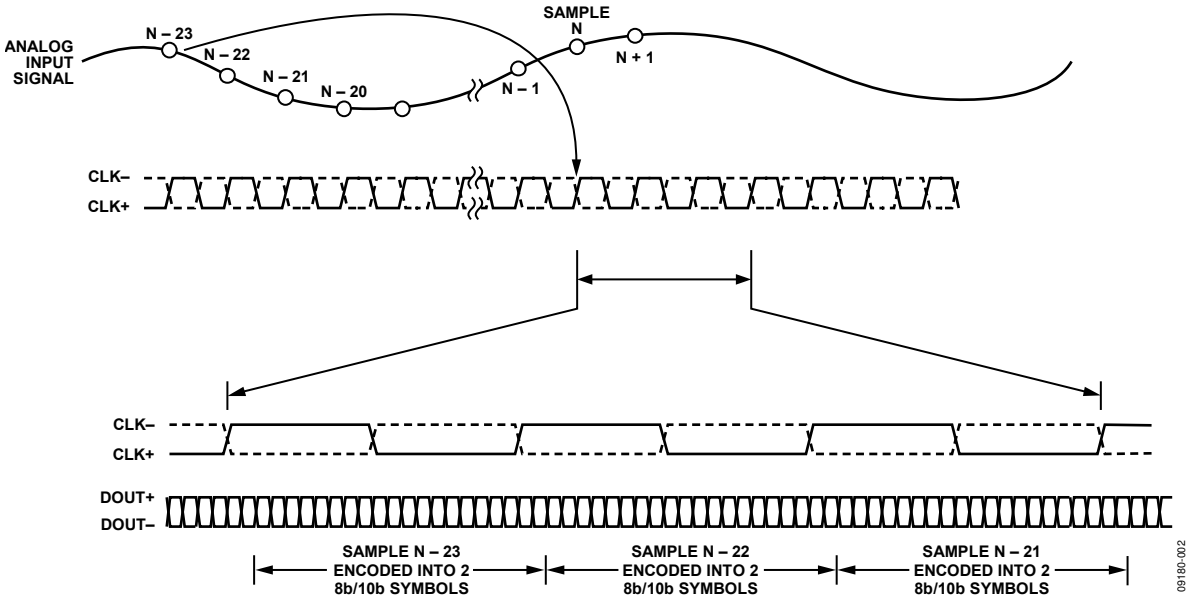


Figure 2. Data Output Timing

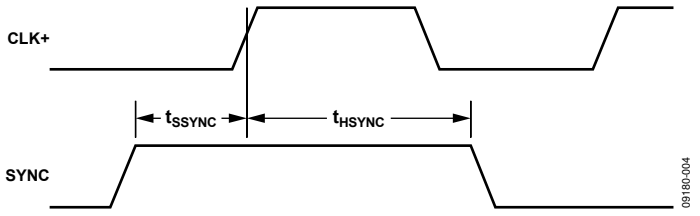


Figure 3. SYNC Input Timing Requirements

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
ELECTRICAL	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0V
VIN+A/VIN+B, VIN−A/VIN−B to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
SYNC to AGND	−0.3 V to AVDD + 0.2 V
VCMA, VCMB to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to DRVDD + 0.2 V
SCLK to AGND	−0.3 V to DRVDD + 0.2 V
SDIO to AGND	−0.3 V to DRVDD + 0.2 V
PDWN to AGND	−0.3 V to DRVDD + 0.2 V
DOUT+A, DOUT0−A, DOUT0+B, DOUT−B to AGND	−0.3 V to DRVDD + 0.2 V
DSYNC+A, DSYNC−A, DSYNC+B, DSYNC−B to AGND	−0.3 V to DRVDD + 0.2 V
ENVIRONMENTAL	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the PCB increases the reliability of the solder joints and maximizes the thermal capability of the package.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1,2]	θ_{JC}[1,3]	θ_{JB}[1,4]	Unit
48-Lead LFCSP 7 mm × 7 mm (CP-48-8)	0	25	2	14	°C/W
	1.0	22			°C/W
	2.5	20			°C/W

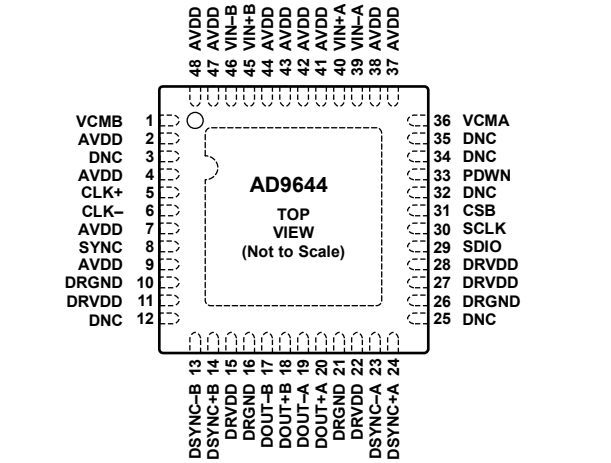
[1] Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-STD 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. As shown Table 7, airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes, reduces θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. DNC = DO NOT CONNECT.
2. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE PART. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

09180-104

Figure 4. LFCSP Pin Configuration (Top View)

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
11, 15, 22, 27, 28	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
2, 4, 7, 9, 37, 38, 41, 42, 43, 44, 47, 48	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
3, 12, 25, 32, 34, 35	DNC		Do Not Connect.
10, 16, 21, 26	DRGND	Driver Ground	Digital Driver Supply Ground.
0	AGND, Exposed Pad	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
ADC Analog			
40	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
39	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
45	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
46	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
36	VCMA	Output	Common-Mode Level Bias Output for Channel A Analog Input.
1	VCMB	Output	Common-Mode Level Bias Output for Channel B Analog Input.
5	CLK+	Input	ADC Clock Input—True.
6	CLK−	Input	ADC Clock Input—Complement.
Digital Input			
8	SYNC	Input	Input Clock Divider Synchronization Pin.
24	DSYNC+A	Input	Active Low JESD204A LVDS Channel A SYNC Input—True/JESD204A CMOS Channel A SYNC Input.
23	DSYNC−A	Input	Active Low JESD204A LVDS Channel A SYNC Input—Complement.
14	DSYNC+B	Input	Active Low JESD204A LVDS Channel B SYNC Input—True/JESD204A CMOS Channel A SYNC Input.
13	DSYNC−B	Input	Active Low JESD204A LVDS Channel B SYNC Input—Complement.

Pin No.	Mnemonic	Type	Description
Digital Outputs			
20	DOUT+A	Output	Channel A CML Output Data—True.
19	DOUT−A	Output	Channel A CML Output Data—Complement.
18	DOUT+B	Output	Channel B CML Output Data—True.
17	DOUT−B	Output	Channel B CML Output Data—Complement.
SPI Control			
30	SCLK	Input	SPI Serial Clock.
29	SDIO	Input/Output	SPI Serial Data Input/Output.
31	CSB	Input	SPI Chip Select (Active Low).
ADC Configuration			
33	PDWN	Input	Power-Down Input. Using the SPI interface, this input can be configured as power-down or standby.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, DCS enabled, 1.75 V p-p differential input, VIN = −1.0 dBFS, and 32k sample, T_A = 25°C, unless otherwise noted.

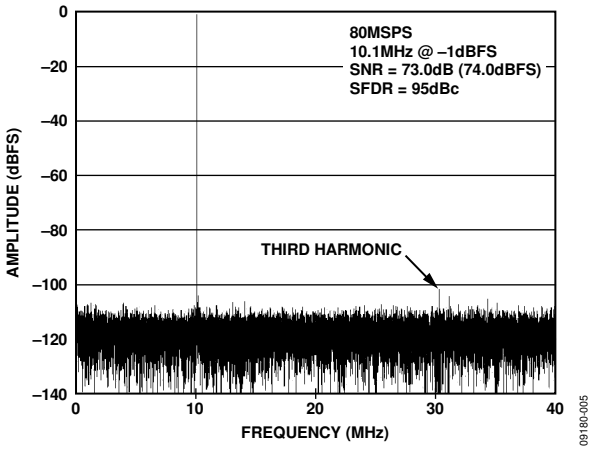


Figure 5. AD9644-80 Single-Tone FFT with f_{IN} = 10.1 MHz

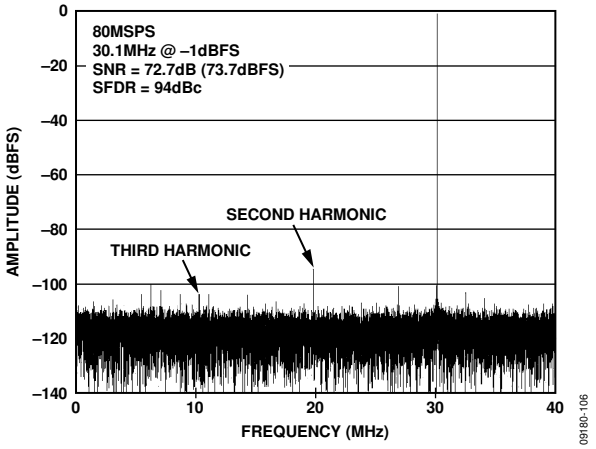


Figure 6. AD9644-80 Single-Tone FFT with f_{IN} = 30.1 MHz

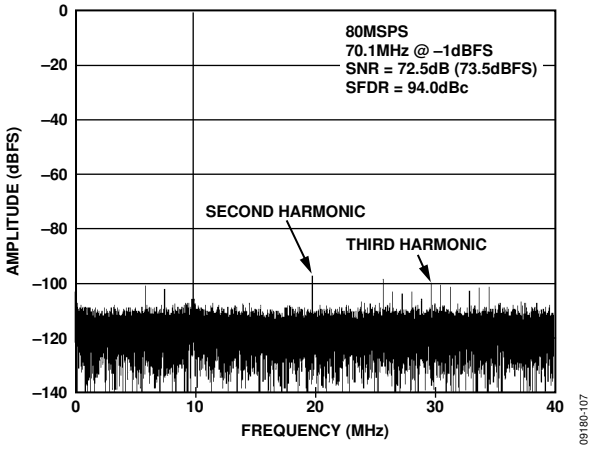


Figure 7. AD9644-80 Single-Tone FFT with f_{IN} = 70.1 MHz

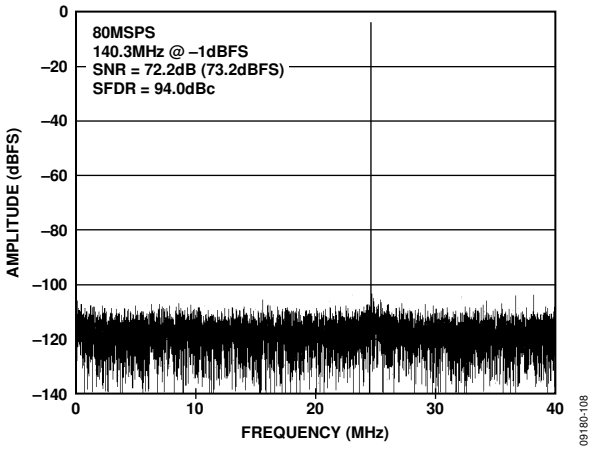


Figure 8. AD9644-80 Single-Tone FFT with f_{IN} = 140.1 MHz

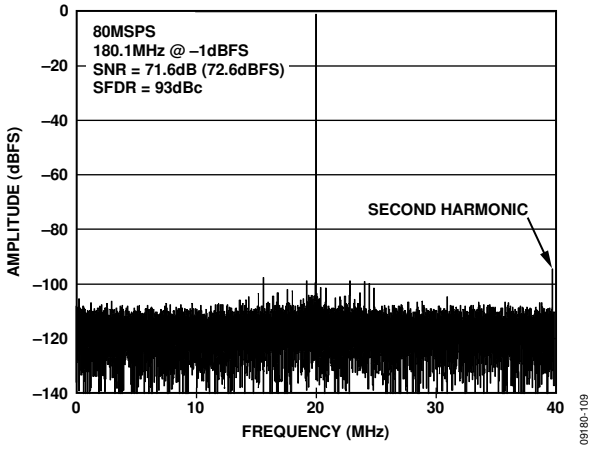


Figure 9. AD9644-80 Single-Tone FFT with f_{IN} = 180.1 MHz

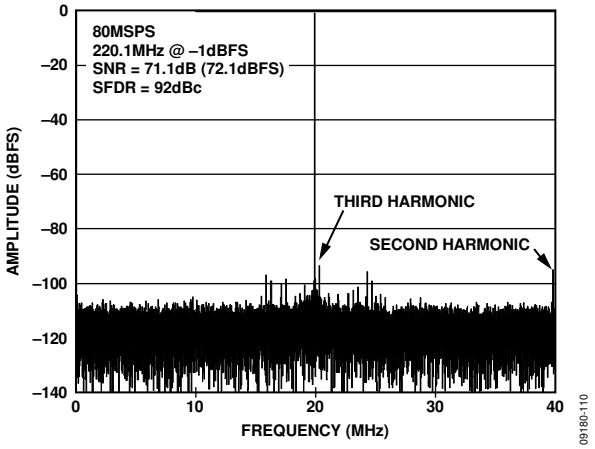


Figure 10. AD9644-80 Single-Tone FFT with f_{IN} = 220.1 MHz

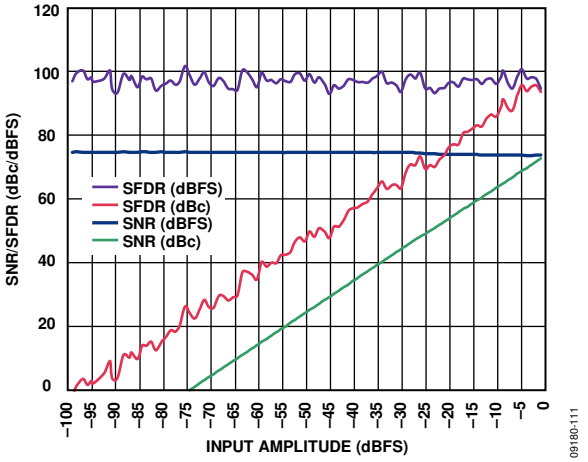


Figure 11. AD9644-80 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 10.1 MHz, f_S = 80 MSPS

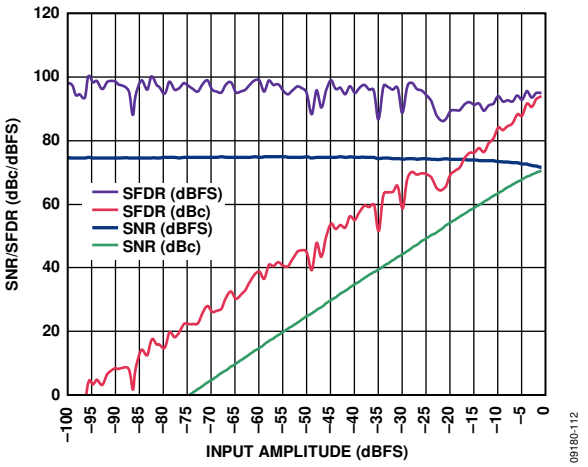


Figure 12. AD9644-80 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 180 MHz, f_S = 80 MSPS

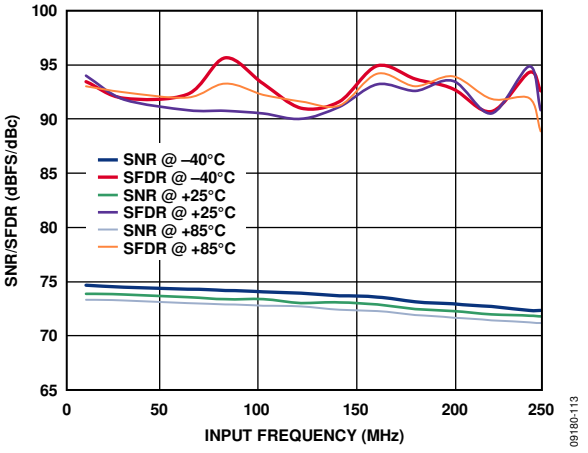


Figure 13. AD9644-80 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 1.75 V p-p Full-Scale, f_S = 80 MSPS

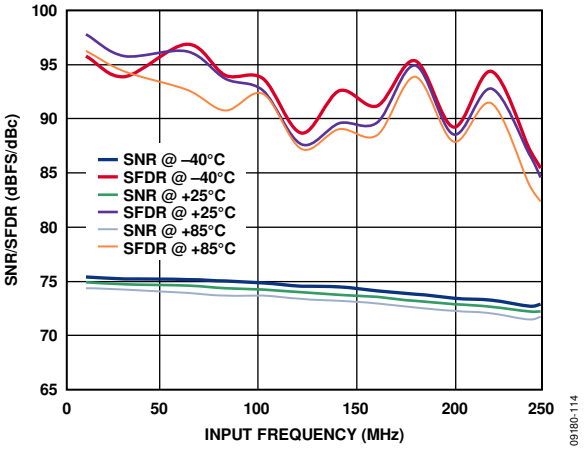


Figure 14. AD9644-80 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 2.0 V p-p Full-Scale, f_S = 80 MSPS

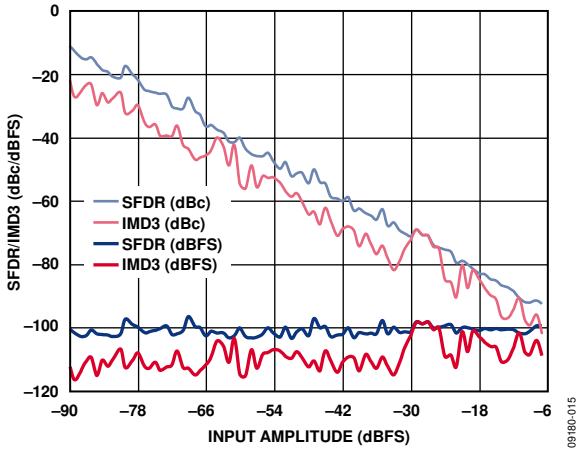


Figure 15. AD9644-80 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 29.9 MHz, f_{IN2} = 32.9 MHz, f_S = 80 MSPS

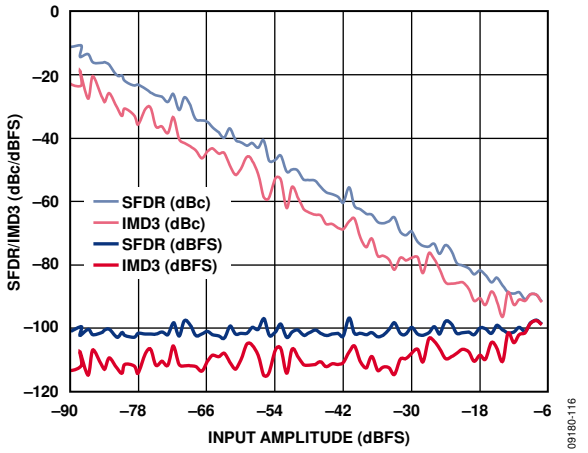


Figure 16. AD9644-80 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 169.1 MHz, f_{IN2} = 172.1 MHz, f_S = 80 MSPS

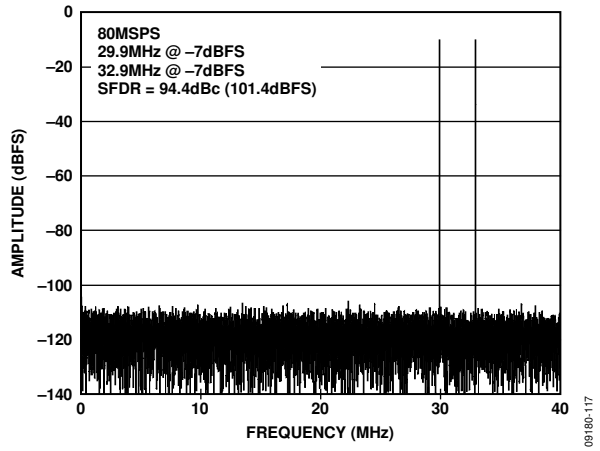


Figure 17. AD9644-80 Two-Tone FFT with f_{IN1} = 29.9 MHz and f_{IN2} = 32.9 MHz

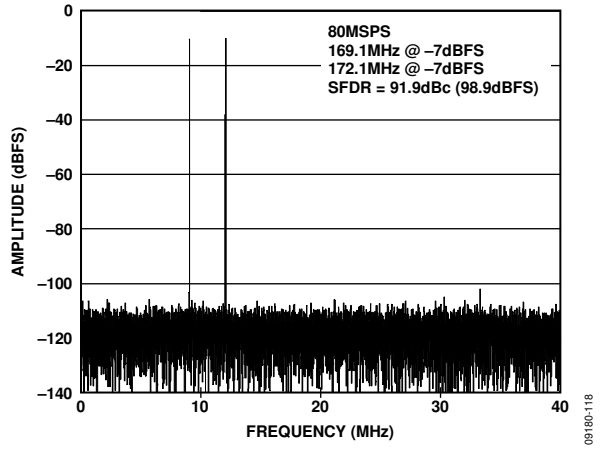


Figure 18. AD9644-80 Two-Tone FFT with f_{IN1} = 169.1 MHz and f_{IN2} = 172.1 MHz

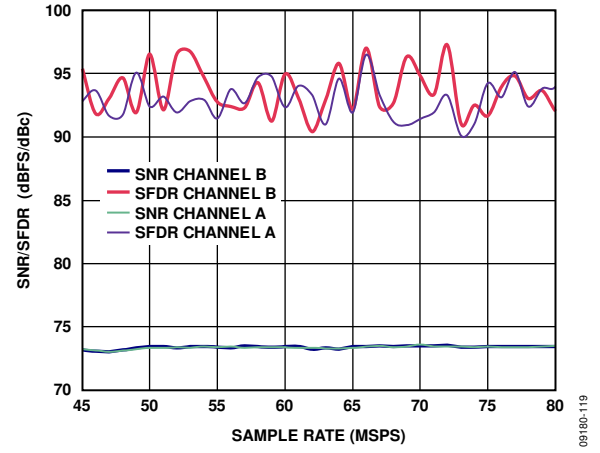


Figure 19. AD9644-80 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 70. MHz

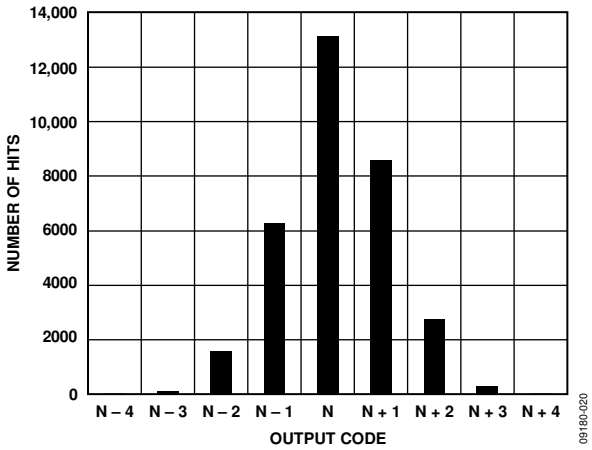


Figure 20. AD9644-80 Grounded Input Histogram

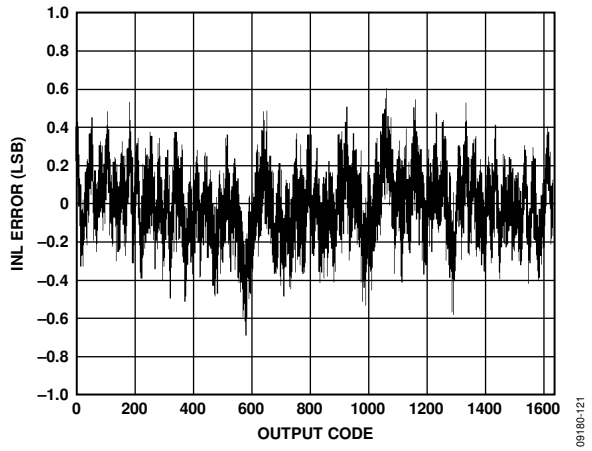


Figure 21. AD9644-80 INL with f_{IN} = 30.3 MHz

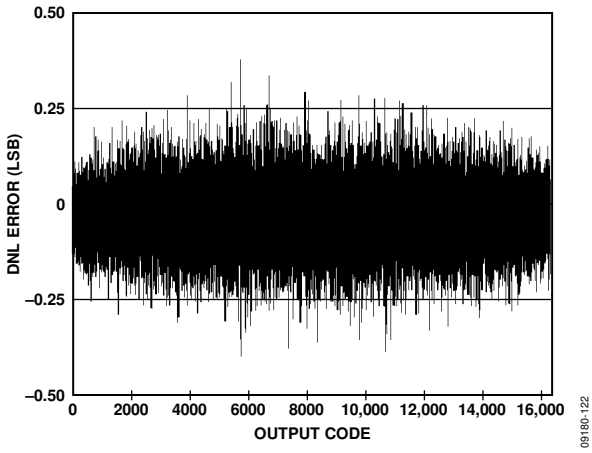


Figure 22. AD9644-80 DNL with f_{IN} = 30.3 MHz

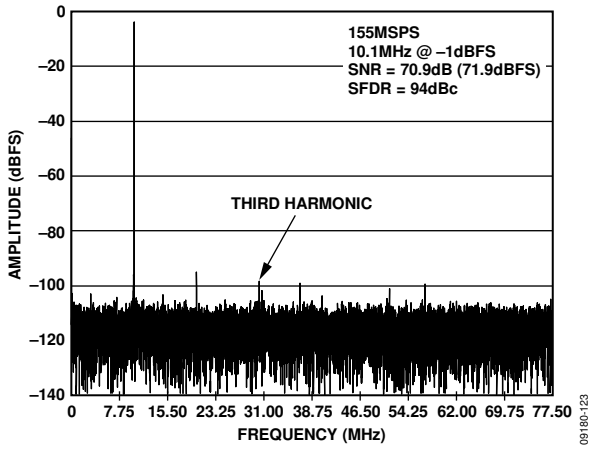


Figure 23. AD9644-155 Single-Tone FFT with f_{IN} = 10.1 MHz

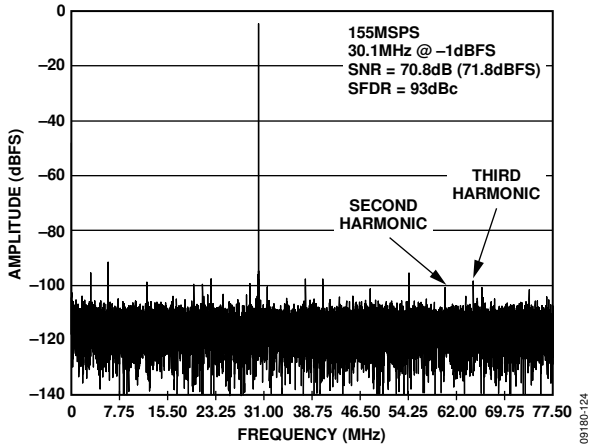


Figure 24. AD9644-155 Single-Tone FFT with f_{IN} = 30.1 MHz

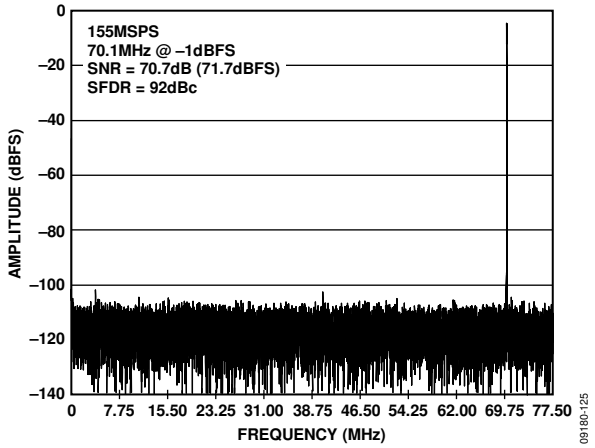


Figure 25. AD9644-155 Single-Tone FFT with f_{IN} = 70.1 MHz

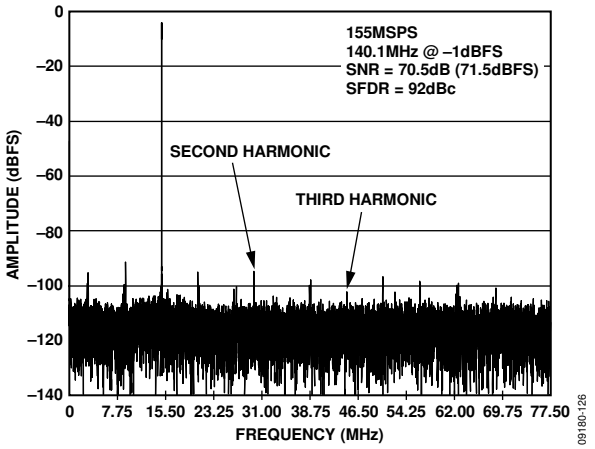


Figure 26. AD9644-155 Single-Tone FFT with f_{IN} = 140.1 MHz

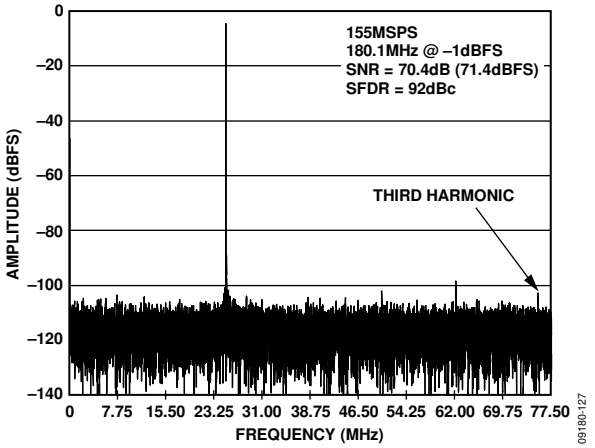


Figure 27. AD9644-155 Single-Tone FFT with f_{IN} = 180.1 MHz

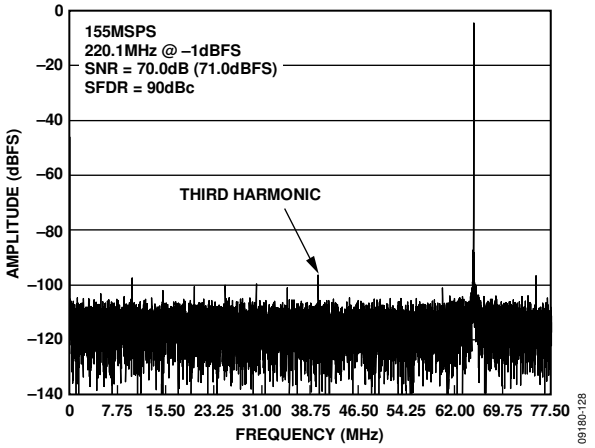


Figure 28. AD9644-155 Single-Tone FFT with f_{IN} = 220.1 MHz

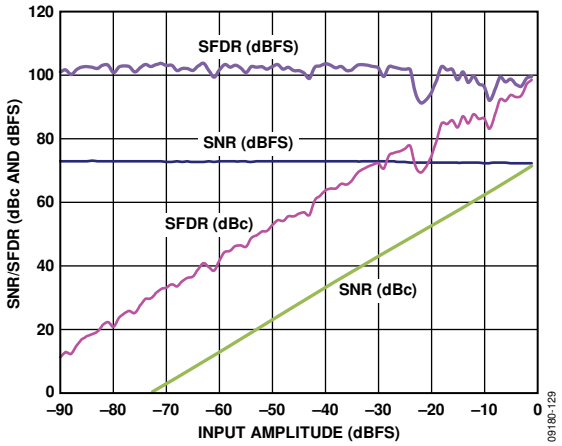


Figure 29. AD9644-155 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 10.1 MHz, f_S = 80 MSPS

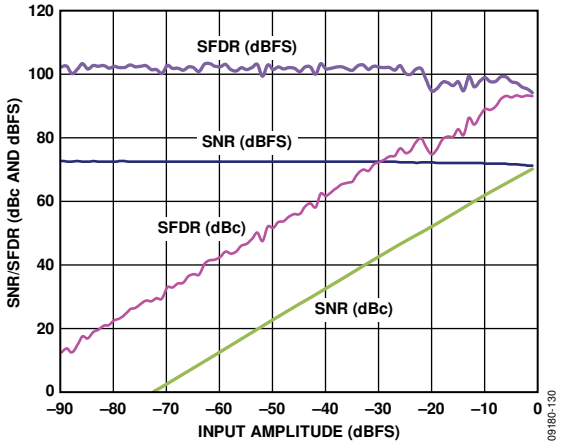


Figure 30. AD9644-155 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 180 MHz, f_S = 80 MSPS

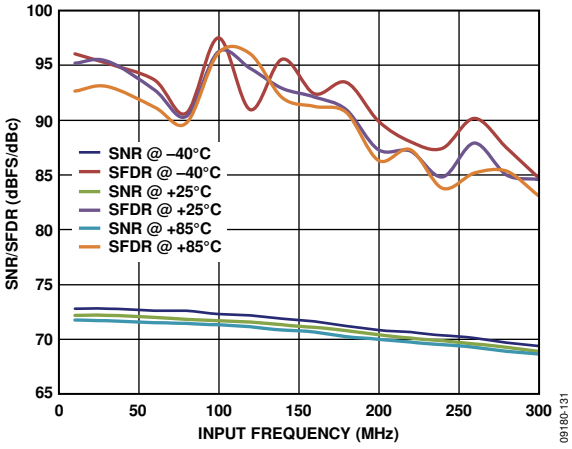


Figure 31. AD9644-155 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 1.75 V p-p Full-Scale, f_S = 80 MSPS

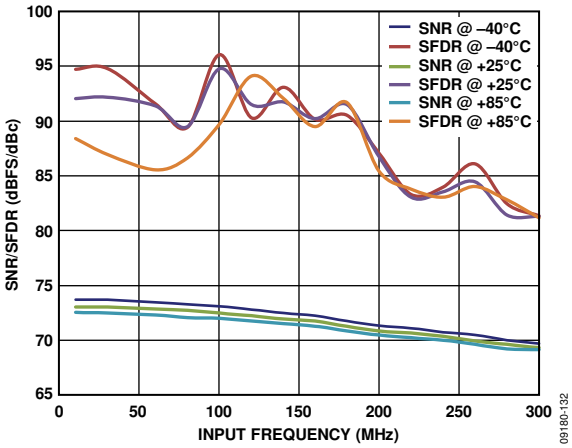


Figure 32. AD9644-155 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 2.0 V p-p Full-Scale, f_S = 80 MSPS

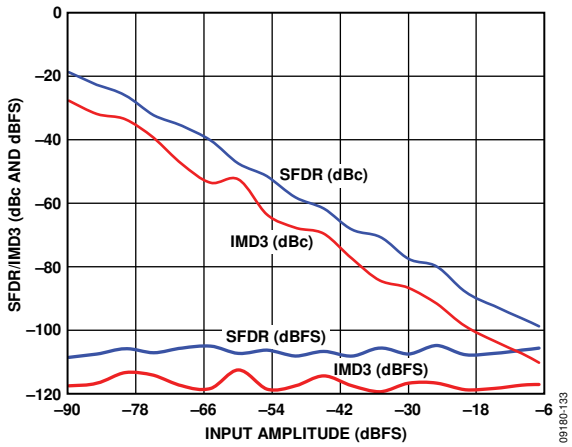


Figure 33. AD9644-155 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 29.9 MHz, f_{IN2} = 32.9 MHz, f_S = 80 MSPS

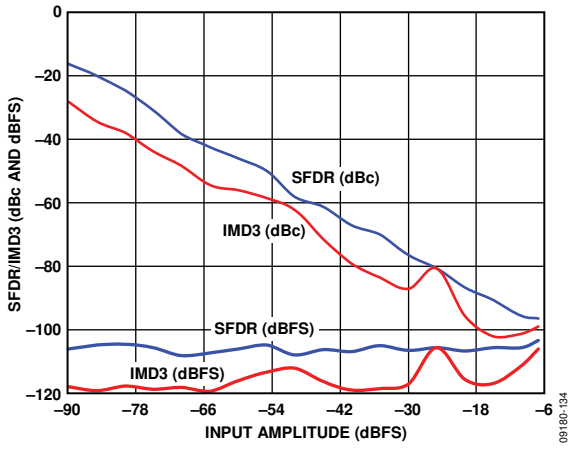


Figure 34. AD9644-155 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 169.1 MHz, f_{IN2} = 172.1 MHz, f_S = 80 MSPS

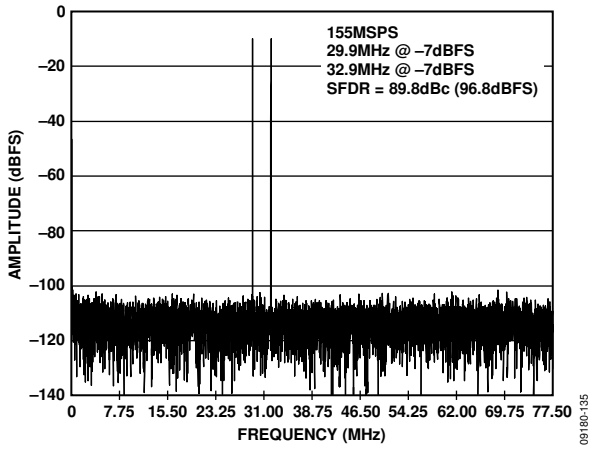


Figure 35. AD9644-155 Two-Tone FFT with f_{IN1} = 29.9 MHz and f_{IN2} = 32.9 MHz

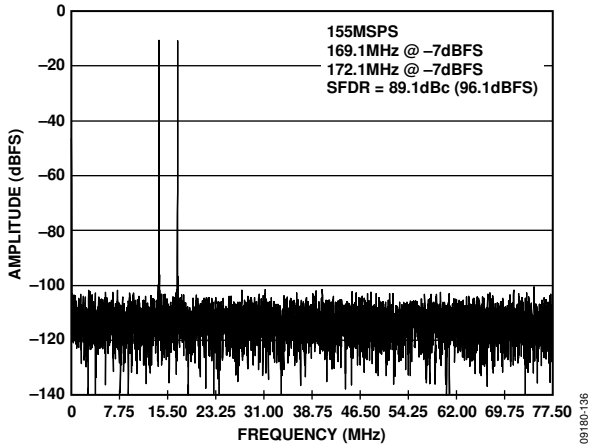


Figure 36. AD9644-155 Two-Tone FFT with f_{IN1} = 169.1 MHz and f_{IN2} = 172.1 MHz

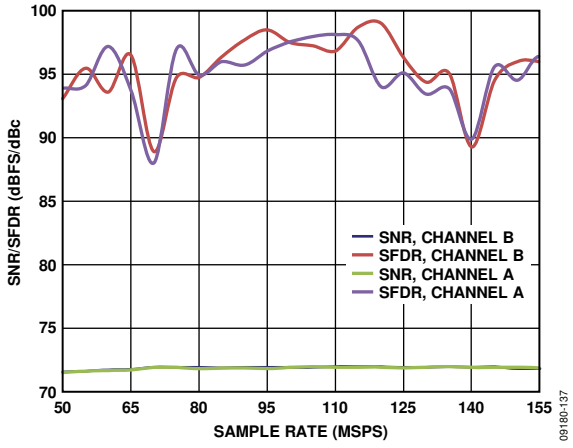


Figure 37. AD9644-155 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 70. MHz

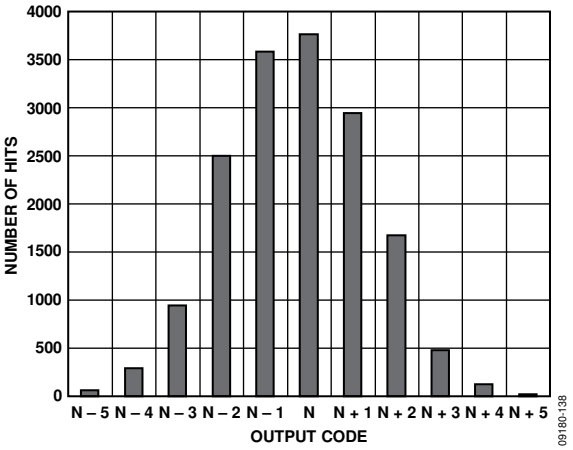


Figure 38. AD9644-155 Grounded Input Histogram

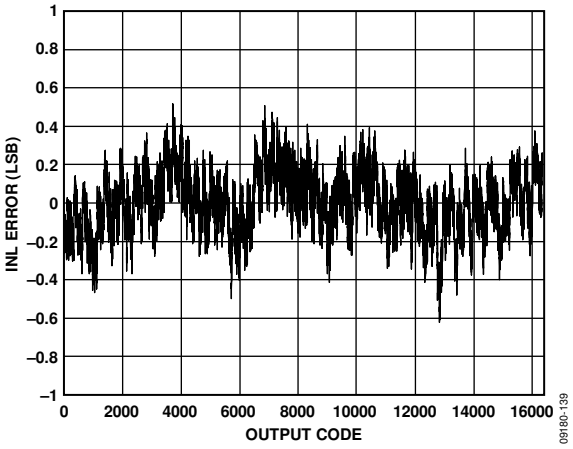


Figure 39. AD9644-155 INL with f_{IN} = 30.3 MHz

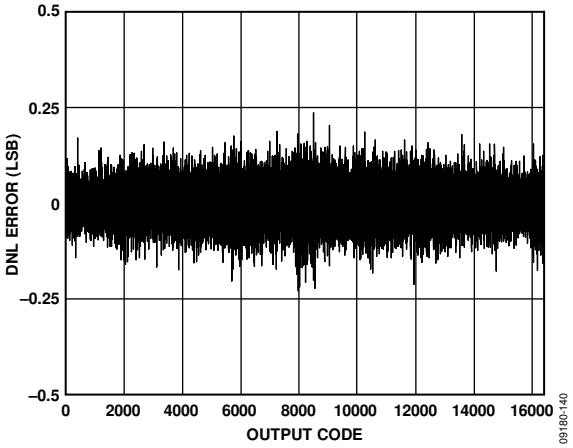


Figure 40. AD9644-155 DNL with f_{IN} = 30.3 MHz

EQUIVALENT CIRCUITS

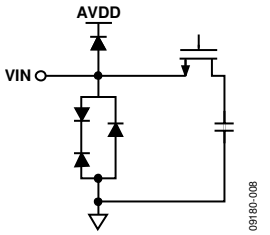


Figure 41. Equivalent Analog Input Circuit

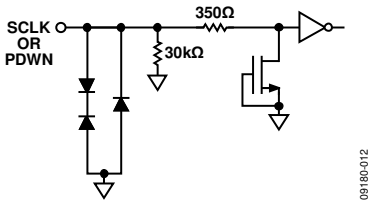


Figure 45. Equivalent SCLK or PDWN Input Circuit

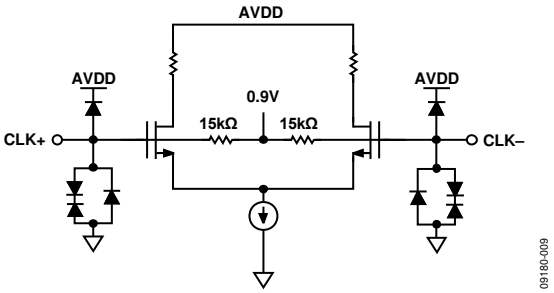


Figure 42. Equivalent Clock Input Circuit

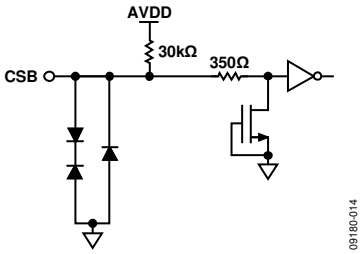


Figure 46. Equivalent CSB Input Circuit

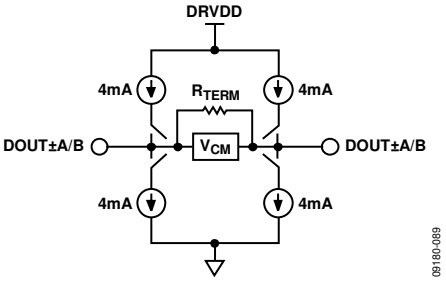


Figure 43. Digital CML Output

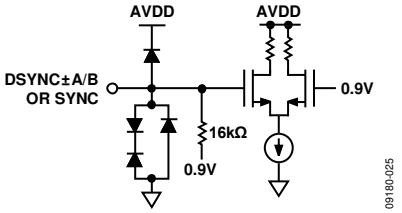


Figure 47. Equivalent SYNC and DSYNC Input Circuit

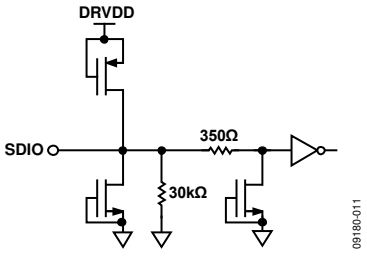


Figure 44. Equivalent SDIO Circuit

THEORY OF OPERATION

The AD9644 dual-core analog-to-digital converter (ADC) can be used for diversity reception of signals, in which the ADCs are operating identically on the same carrier but from two separate antennae. The ADCs can also be operated with independent analog inputs. The user can sample any $f_S/2$ frequency segment from dc to 250 MHz, using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in ADC performance.

In nondiversity applications, the AD9644 can be used as a baseband or direct downconversion receiver, in which one ADC is used for I input data, and the other is used for Q input data.

Synchronization capability is provided to allow synchronized timing between multiple devices.

Programming and control of the AD9644 are accomplished using a 3-wire SPI-compatible serial interface.

ADC ARCHITECTURE

The AD9644 architecture consists of a dual front-end sample-and-hold circuit, followed by a pipelined, switched-capacitor ADC. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample and the remaining stages to operate on the preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor digital-to-analog converter (DAC) and an interstage residue amplifier (MDAC). The MDAC magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage of each channel contains a differential sampling circuit that can be ac- or dc-coupled in differential or single-ended modes. The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing digital output noise to be separated from the analog core. During power-down, the output buffers go into a high impedance state.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9644 is a differential switched-capacitor circuit that has been designed for optimum performance while processing a differential input signal.

The clock signal alternatively switches the input between sample mode and hold mode (see Figure 48). When the input is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within ½ of a clock cycle.

A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. A shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC input; therefore, the precise values are dependent on the application.

In intermediate frequency (IF) undersampling applications, any shunt capacitors or series resistors should be reduced since the input sample capacitor is unbuffered. In combination with the driving source impedance, the shunt capacitors limit the input bandwidth. Refer to the AN-742 Application Note, *Frequency Domain Response of Switched-Capacitor ADCs*; the AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*; and the *Analog Dialog* article, "Transformer-Coupled Front-End for Wideband A/D Converters," for more information on this subject (refer to www.analog.com).

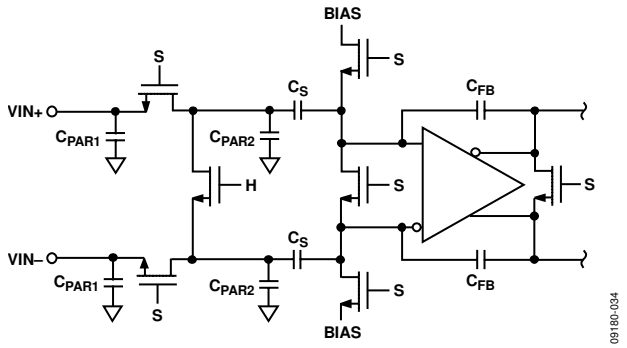


Figure 48. Switched-Capacitor Input

For best dynamic performance, the source impedances driving VIN+ and VIN− should be matched, and the inputs should be differentially balanced.

Input Common Mode

The analog inputs of the AD9644 are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. Setting the device so that VCM = 0.5 × AVDD (or 0.9 V) is recommended for optimum performance. An on-board common-mode voltage reference is included in the design and is available from the VCMA and VCMB pins. Using the VCMA and VCMB outputs to set the input common mode is recommended. Optimum performance is achieved when the common-mode voltage of the analog input is set by the VCMA and VCMB pin voltages (typically 0.5 × AVDD). The VCMA and VCMB pins must be decoupled to ground by a 0.1 µF capacitor. This decoupling capacitor should be placed close to the pin to minimize the series resistance and inductance between the part and this capacitor.

Differential Input Configurations

Optimum performance is achieved while driving the AD9644 in a differential input configuration. For baseband applications, the AD8138, ADA4937-2, and ADA4938-2 differential drivers provide excellent performance and a flexible interface to the ADC.

The output common-mode voltage of the ADA4938-2 is easily set with the VCM pin of the AD9644 (see Figure 49), and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

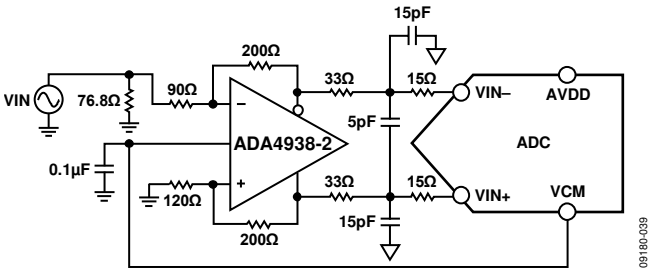


Figure 49. Differential Input Configuration Using the ADA4938-2

For baseband applications in which SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 50. To bias the analog input, the VCM voltage can be connected to the center tap of the secondary winding of the transformer.

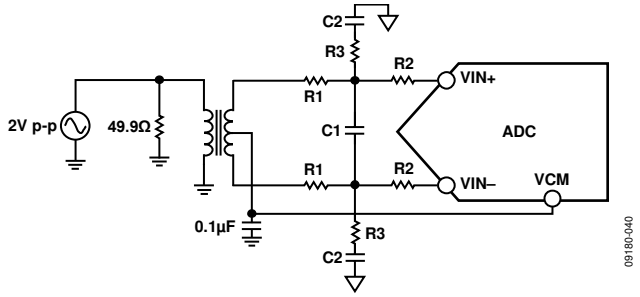


Figure 50. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz (MHz). Excessive signal power can also cause core saturation, which leads to distortion.

At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD9644. For applications in which SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 51). In this configuration, the input is ac-coupled and the VCM is provided to each input through a 33 Ω resistor. These resistors compensate for losses in the input baluns to provide a 50 Ω impedance to the driver.

In the double balun and transformer configurations, the value of the input capacitors and resistors is dependent on the input frequency and source impedance. Based on these parameters the value of the input resistors and capacitors may need to be adjusted or some components may need to be removed. Table 9 displays recommended values to set the RC network for different input frequency ranges. However, these values are dependent on the input signal and bandwidth and should be used only as a starting guide. Note that the values given in Table 9 are for each R1, R2, C2, and R3 component shown in Figure 50 and Figure 51.

Table 9. Example RC Network

Frequency Range (MHz)	R1 Series (Ω)	C1 Differential (pF)	R2 Series (Ω)	C2 Shunt (pF)	R3 Shunt (Ω)
0 to 100	33	8.2	0	8.2	49.9
100 to 250	15	3.9	0	Open	Open

An alternative to using a transformer-coupled input at frequencies in the second Nyquist zone is to use the AD8376 variable gain amplifier. An example drive circuit including a band-pass filter is shown in Figure 52. See the AD8376 data sheet for more information.

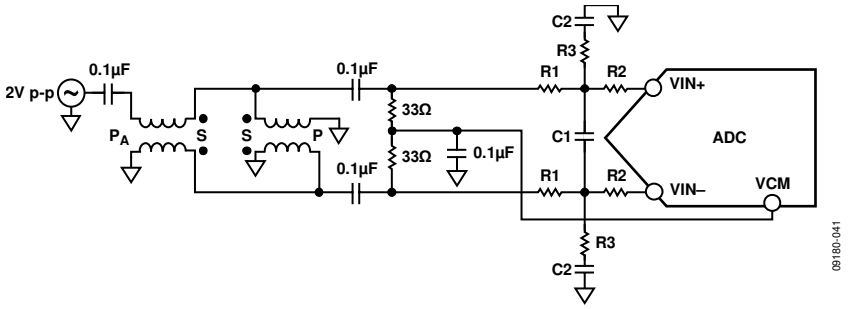


Figure 51. Differential Double Balun Input Configuration

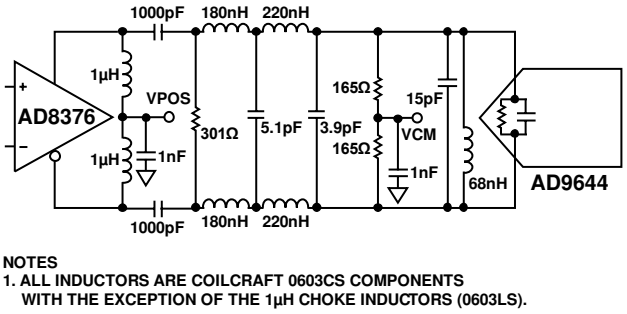


Figure 52. Differential Input Configuration Using the AD8376 (Filter Values Shown Are for a 20 MHz Bandwidth Filter Centered at 140 MHz)

VOLTAGE REFERENCE

A stable and accurate voltage reference is built into the AD9644. The input full scale range can be adjusted through the SPI port by adjusting Bit 0 through Bit 4 of Register 0x18. These bits can be used to change the full scale between 1.383 V p-p and 2.087 V p-p in 0.022 V steps, as shown in Table 17.

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9644 sample clock inputs, CLK+ and CLK–, should be clocked with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK– pins by means of a transformer or a passive component configuration. These pins are biased internally (see Figure 53) and require no external bias. If the inputs are floated, the CLK– pin is pulled low to prevent inadvertent clocking.

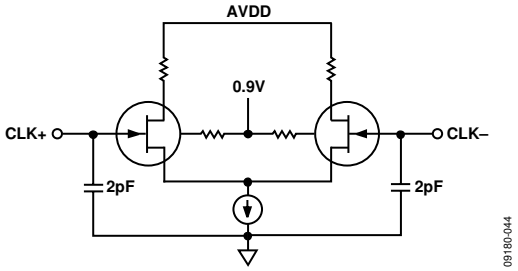


Figure 53. Equivalent Clock Input Circuit

Clock Input Options

The AD9644 has a very flexible clock input structure. Clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of the most concern, as described in the Jitter Considerations section. The minimum conversion rate of the AD9644 is 40 MSPS. At clock rates below 40 MSPS, dynamic performance of the AD9644 can degrade.

Figure 54 and Figure 55 show two preferred methods for clocking the AD9644 (at clock rates up to 640 MHz). A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF balun or an RF transformer.

The RF balun configuration is recommended for clock frequencies between 125 MHz and 640 MHz, and the RF transformer is recommended for clock frequencies from 40 MHz to 200 MHz. The back-to-back Schottky diodes across the transformer/balun secondary limit clock excursions into the AD9644 to approximately 0.8 V p-p differential.

This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9644 while preserving the fast rise and fall times of the signal that are critical to a low jitter performance.

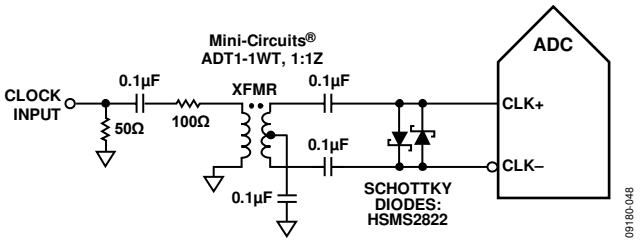


Figure 54. Transformer-Coupled Differential Clock (Up to 200 MHz)

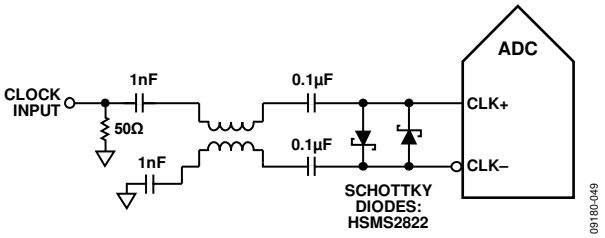


Figure 55. Balun-Coupled Differential Clock (Up to 640 MHz)

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 56. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517/AD9518/AD9520/AD9522 clock drivers offer excellent jitter performance.

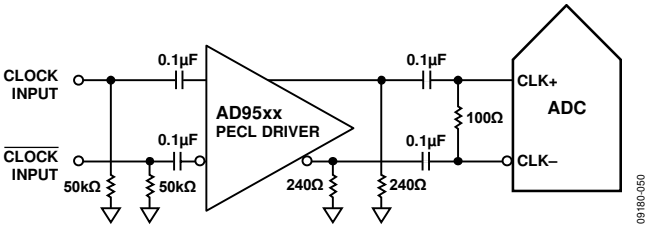


Figure 56. Differential PECL Sample Clock (Up to 640 MHz)

A third option is to ac-couple a differential LVDS signal to the sample clock input pins, as shown in Figure 57. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517/AD9518/AD9520/AD9522 clock drivers offer excellent jitter performance.

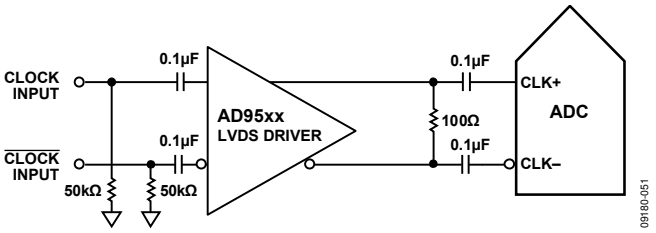


Figure 57. Differential LVDS Sample Clock (Up to 640 MHz)

In some applications, it may be acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, the CLK+ pin should be driven directly from a CMOS gate, and the CLK– pin should be bypassed to ground with a 0.1 µF capacitor (see Figure 58).

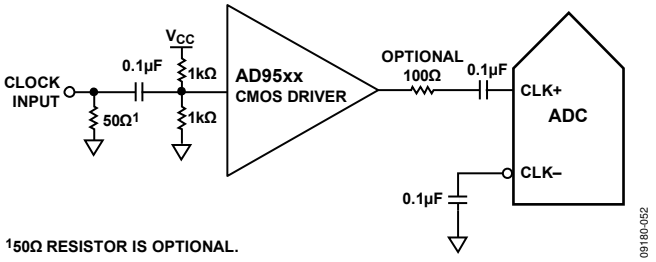


Figure 58. Single-Ended 1.8 V CMOS Input Clock (Up to 200 MHz)

Input Clock Divider

The AD9644 contains an input clock divider with the ability to divide the input clock by integer values between 1 and 8. For divide ratios other than 1 the duty cycle stabilizer is automatically enabled.

The AD9644 clock divider can be synchronized using the external SYNC input. Bit 1 and Bit 2 of Register 0x3A allow the clock divider to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written. A valid SYNC causes the clock divider to reset to its initial state. This synchronization feature allows multiple parts to have their clock dividers aligned to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. The AD9644 requires a tight tolerance on the clock duty cycle to maintain dynamic performance characteristics.

The AD9644 contains a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD9644. Noise and distortion performance are nearly flat for a wide range of duty cycles with the DCS enabled.

Jitter in the rising edge of the input is still of paramount concern and is not easily reduced by the internal stabilization circuit. The loop has a time constant associated with it that must be considered in applications in which the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal. During the time period that the loop is not locked, the DCS loop is bypassed, and internal device timing is dependent on the duty cycle of the input clock signal. In such applications, it may be appropriate to disable the duty cycle stabilizer. In all other applications, enabling the DCS circuit is recommended to maximize ac performance.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. For inputs near full scale, the degradation in SNR from the low frequency SNR (SNR_{LF}) at a given input frequency (f_{INPUT}) due to jitter (t_{JRMS}) can be calculated by

$$SNR_{HF} = -10 \log[(2\pi \times f_{INPUT} \times t_{JRMS})^2 + 10^{(-SNR_{LF}/10)}]$$

In the equation, the rms aperture jitter represents the clock input jitter specification. IF undersampling applications are particularly sensitive to jitter, as illustrated in Figure 59. The measured curve in Figure 59 was taken using an ADC clock source with approximately 65 fs of jitter, which combines with the 125 fs of jitter inherent in the AD9644 to produce the result shown.

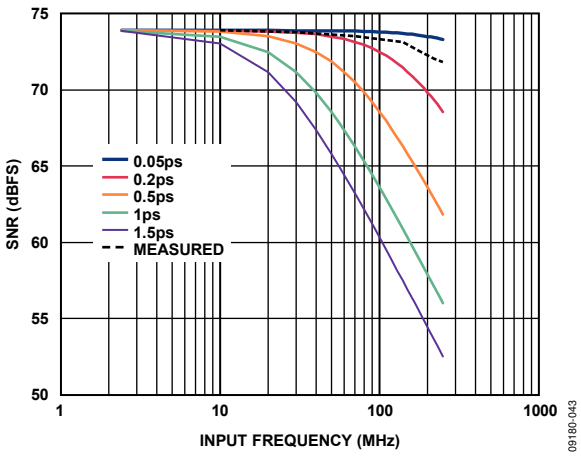


Figure 59. SNR vs. Input Frequency and Jitter

The clock input should be treated as an analog signal in cases in which aperture jitter may affect the dynamic range of the AD9644. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), it should be retimed by the original clock at the last step.

Refer to the AN-501 Application Note and the AN-756 Application Note (visit www.analog.com) for more information about jitter performance as it relates to ADCs.

CHANNEL/CHIP SYNCHRONIZATION

The AD9644 has a SYNC input that offers the user flexible synchronization options for synchronizing the clock divider. The clock divider sync feature is useful for guaranteeing synchronized sample clocks across multiple ADCs. The input clock divider can be enabled to synchronize on a single occurrence of the SYNC signal or on every occurrence.

The SYNC input is internally synchronized to the sample clock; however, to ensure that there is no timing uncertainty between multiple parts, the SYNC input signal should be externally synchronized to the input clock signal, meeting the setup and hold times shown in Table 5. The SYNC input should be driven using a single-ended CMOS-type signal.

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 60 and Figure 61, the power dissipated by the AD9644 varies with its sample rate (AD9644-80 shown).

The data in Figure 60 and Figure 61 was taken in JESD204A serial output mode, using the same operating conditions as those used for the Typical Performance Characteristics.

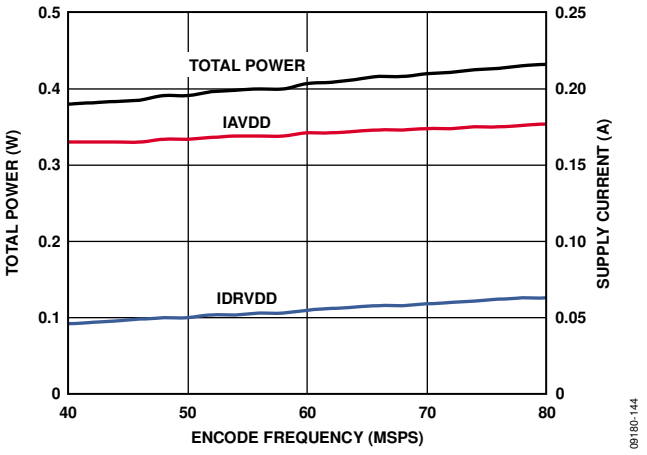


Figure 60. AD9644-80 Power and Current vs. Encode Frequency with f_{IN} = 10.1 MHz

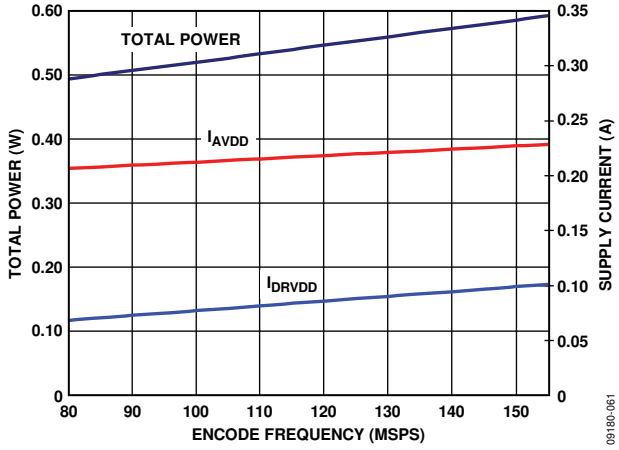


Figure 61. AD9644-155 Power and Current vs. Encode Frequency with f_{IN} = 10.1 MHz

By asserting PDWN (either through the SPI port or by asserting the PDWN pin high), the AD9644 is placed in power-down mode. In this state, the ADC typically dissipates 15 mW. During power-down, the output drivers are placed in a high impedance state. Asserting the PDWN pin low returns the AD9644 to its normal operating mode.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, clock, and JESD204A outputs . Internal capacitors are discharged when entering power-down mode and then must be recharged when returning to normal operation.

When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered and the JESD204A outputs running when faster wake-up times are required.

DIGITAL OUTPUTS

JESD204A Transmit Top Level Description

The AD9644 digital output complies with the JEDEC Standard No. 204A (JESD204A), which describes a serial interface for data converters. JESD204A uses 8B/10B encoding as well as optional scrambling. K28.5 and K28.7 comma symbols are used for frame synchronization and the K28.3 control symbol is used for lane synchronization. The receiver is required to lock onto the serial data stream and recover the clock with the use of a PLL. For details on the output interface, users are encouraged to refer to the JESD204A standard.

The JESD204A transmit block is used to multiplex data from the two analog-to-digital converters onto two independent JESD204A Links. Each JESD204A Link is considered a separate instance of the JESD204A specification, has an independent DSYNC signal, and contains one or more lanes. Note that the JESD204 specification only allows one lane per link, while the JESD204A specification adds multilane support through an alignment procedure.

Each JESD204A Link is described according to the following nomenclature:

- S = samples transmitted/single converter/frame cycle
- M = number of converters/converter device (link)
- L = number of lanes/converter device (link)
- N = converter resolution
- N' = total number of bits per sample
- CF = number of control words/frame clock cycle/converter device (link)
- CS = number of control bits/conversion sample
- K = number of frames per multiframe
- HD = high density mode
- F = octets/frame
- C = control bit (overrange, overflow, underflow)
- T = tail bit
- SCR = scrambler enable/disable
- FCHK = checksum