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14-Bit, 125 MSPS/105 MSPS, 1.8 V Dual Analog-to-Digital Converter

Data Sheet **AD9648**

FEATURES

- 1.8 V analog supply operation
- 1.8 V CMOS or LVDS outputs
- SNR = 74.5 dBFS @ 70 MHz
- SFDR = 91 dBc @ 70 MHz
- Low power: 106 mW/channel @ 125 MSPS
- Differential analog input with 650 MHz bandwidth
- IF sampling frequencies to 200 MHz
- On-chip voltage reference and sample-and-hold circuit
- 2 V p-p differential analog input
- DNL = ±0.5 LSB
- Serial port control options
  - Offset binary, gray code, or twos complement data format
  - Optional clock duty cycle stabilizer
  - Integer 1-to-8 input clock divider
  - Data output multiplex option
  - Built-in selectable digital test pattern generation
  - Energy-saving power-down modes
  - Data clock out with programmable clock and data alignment

APPLICATIONS

- Communications
- Diversity radio systems
- Multimode digital receivers
  - GSM, EDGE, W-CDMA, LTE, CDMA2000, WiMAX, TD-SCDMA
- I/Q demodulation systems
- Smart antenna systems
- Broadband data applications
- Battery-powered instruments
- Hand held scope meters
- Portable medical imaging
- Ultrasound
- Radar/LIDAR

FUNCTIONAL BLOCK DIAGRAM

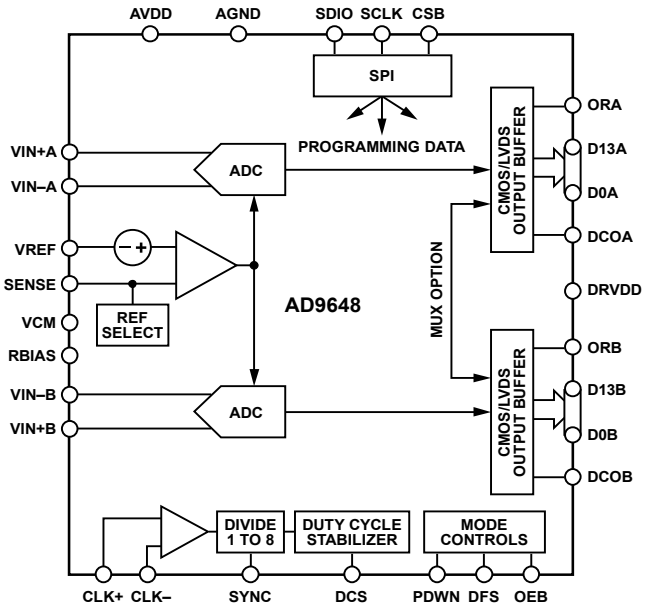

Figure 1.

PRODUCT HIGHLIGHTS

1. The AD9648 operates from a single 1.8 V analog power supply and features a separate digital output driver supply to accommodate 1.8 V CMOS or LVDS logic families.
2. The patented sample-and-hold circuit maintains excellent performance for input frequencies up to 200 MHz and is designed for low cost, low power, and ease of use.
3. A standard serial port interface supports various product features and functions, such as data output formatting, internal clock divider, power-down, DCO/data timing and offset adjustments.
4. The AD9648 is packaged in a 64-lead RoHS compliant LFCSP that is pin compatible with the AD9650/AD9269/AD9268 16-bit ADC, the AD9258 14-bit ADC, the AD9628/AD9231 12-bit ADCs, and the AD9608/AD9204 10-bit ADCs, enabling a simple migration path between 10-bit and 16-bit converters sampling from 20 MSPS to 125 MSPS.

Rev. C
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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9648 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-282: Fundamentals of Sampled Data Systems
- AN-737: How ADIsimADC Models an ADC
- AN-742: Frequency Domain Response of Switched-Capacitor ADCs
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-803: Pin Compatible High Speed ADCs Simplify Design Tasks
- AN-807: Multicarrier WCDMA Feasibility
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-878: High Speed ADC SPI Control Software
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD9648-EP: Enhanced Product Data Sheet
- AD9648: 14-Bit, 125 MSPS/105 MSPS, 1.8 V Dual Analog-to-Digital Converter Data Sheet
- AD9648: Military Data Sheet

User Guides

- UG-003: Evaluating the AD9650/AD9268/AD9258/AD9251/AD9231/AD9204 Analog-to-Digital Converters

TOOLS AND SIMULATIONS

- Visual Analog
- AD9648 IBIS Model
- AD9648/AD9628/AD9608 S-Parameters

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9648 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9648 EngineerZone Discussions.

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7/11—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9648 is a monolithic, dual-channel, 1.8 V supply, 14-bit, 105 MSPS/125 MSPS analog-to-digital converter (ADC). It features a high performance sample-and-hold circuit and on-chip voltage reference.

The product uses multistage differential pipeline architecture with output error correction logic to provide 14-bit accuracy at 125 MSPS data rates and to guarantee no missing codes over the full operating temperature range.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

A differential clock input controls all internal conversion cycles. An optional duty cycle stabilizer (DCS) compensates for wide variations in the clock duty cycle while maintaining excellent overall ADC performance.

The digital output data is presented in offset binary, Gray code, or twos complement format. A data output clock (DCO) is provided for each ADC channel to ensure proper latch timing with receiving logic. Output logic levels of 1.8 V CMOS or LVDS are supported. Output data can also be multiplexed onto a single output bus.

The AD9648 is available in a 64-lead RoHS compliant LFCSP and is specified over the industrial temperature range (−40°C to +85°C).

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, unless otherwise noted.

Table 1.

		AD9648-105			AD9648-125			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	14			14			Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	Full	−0.8	−0.3	+0.2	−0.8	−0.3	+0.2	% FSR
Gain Error	Full	−4.20	±1.3	+4.2	−5.1	±1.3	+5.1	% FSR
Differential Nonlinearity (DNL)[1]	Full	−0.5		+1.2	−0.5		+1.2	LSB
	25°C		±0.5			±0.5		LSB
Integral Nonlinearity (INL)[1]	Full	−2.3		+2.3	−2.3		+2.3	LSB
	25°C		±1.0			±1.0		LSB
MATCHING CHARACTERISTIC								
Offset Error	Full		±0.01	±0.58		±0.01	±0.58	% FSR
Gain Error	Full		±0.5	±4.0		±0.5	±4.0	% FSR
TEMPERATURE DRIFT								
Offset Error	Full		±2			±2		ppm/°C
Gain Error	Full		±50			±50		ppm/°C
INTERNAL VOLTAGE REFERENCE								
Output Voltage (1 V Mode)	Full	0.98	1.00	1.02	0.98	1.00	1.02	V
Load Regulation Error at 1.0 mA	Full		2			2		mV
INPUT REFERRED NOISE								
VREF = 1.0 V	25°C		0.98			0.98		LSB rms
ANALOG INPUT								
Input Span, VREF = 1.0 V	Full		2			2		V p-p
Input Capacitance[2]	Full		5			5		pF
Input Resistance (Differential)	Full		7.5			7.5		kΩ
Input Common-Mode Voltage	Full		0.9			0.9		V
Input Common-Mode Range	Full	0.5		1.3	0.5		1.3	V
POWER SUPPLIES								
Supply Voltage								
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
Supply Current								
I_{AVDD}[1]	Full		81	86		95	100	mA
I_{DRVDD} (1.8 V CMOS)[1]	Full		19.2			22.5		mA
I_{DRVDD}(1.8 V LVDS)[1]	Full		63.5			65.0		mA

Parameter	Temp	AD9648-105 Min	AD9648-105 Typ	AD9648-105 Max	AD9648-125 Min	AD9648-125 Typ	AD9648-125 Max	Unit
POWER CONSUMPTION								
DC Input	Full		135.4			155.5		mW
Sine Wave Input (DRVDD = 1.8 V CMOS Output Mode)	Full		180.4	189.4		211.5	220.5	mW
Sine Wave Input (DRVDD = 1.8 V LVDS Output Mode)	Full		260			288		mW
Standby Power[3]	Full		108			120		mW
Power-Down Power	Full		2.0			2.0		mW

[1] Measure with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND.
[3] Standby power is measured with a dc input and with the CLK± pins active (1.8 V CMOS mode).

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, unless otherwise noted.

Table 2.

Parameter[1]	Temp	AD9648-105 Min	AD9648-105 Typ	AD9648-105 Max	AD9648-125 Min	AD9648-125 Typ	AD9648-125 Max	Unit
SIGNAL-TO-NOISE-RATIO (SNR)								
f_{IN} = 9.7 MHz	25°C		75.4			75.0		dBFS
f_{IN} = 30.5 MHz	25°C		75.2			74.7		dBFS
f_{IN} = 70 MHz	25°C		74.8			74.5		dBFS
	Full	73.8			73.0			dBFS
f_{IN} = 100 MHz	25°C		73.8			73.9		dBFS
f_{IN} = 200 MHz	25°C		71.0			71.5		dBFS
SIGNAL-TO-NOISE AND DISTORTION (SINAD)								
f_{IN} = 9.7 MHz	25°C		74.3			73.9		dBFS
f_{IN} = 30.5 MHz	25°C		74.0			73.4		dBFS
f_{IN} = 70 MHz	25°C		73.4			73.3		dBFS
	Full	73.0			72.8			dBFS
f_{IN} = 100 MHz	25°C		72.8			72.8		dBFS
f_{IN} = 200 MHz	25°C		69.6			70.3		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)								
f_{IN} = 9.7 MHz	25°C		12.0			11.9		Bits
f_{IN} = 30.5 MHz	25°C		12.0			11.9		Bits
f_{IN} = 70 MHz	25°C		11.8			11.8		Bits
f_{IN} = 100 MHz	25°C		11.8			11.8		Bits
f_{IN} = 200 MHz	25°C		11.3			11.4		Bits
WORST SECOND OR THIRD HARMONIC								
f_{IN} = 9.7 MHz	25°C		−98			−96		dBc
f_{IN} = 30.5 MHz	25°C		−90			−90		dBc
f_{IN} = 70 MHz	25°C		−93			−91		dBc
	Full			−86			−82	dBc
f_{IN} = 100 MHz	25°C		−92			−90		dBc
f_{IN} = 200 MHz	25°C		−81			−84		dBc

Parameter[1]	Temp	AD9648-105 Min	AD9648-105 Typ	AD9648-105 Max	AD9648-125 Min	AD9648-125 Typ	AD9648-125 Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
f_{IN} = 9.7 MHz	25°C		98			96		dBc
f_{IN} = 30.5 MHz	25°C		90			90		dBc
f_{IN} = 70 MHz	25°C		93			91		dBc
	Full	86			82			dBc
f_{IN} = 100 MHz	25°C		92			90		dBc
f_{IN} = 200 MHz	25°C		81			84		dBc
WORST OTHER (HARMONIC OR SPUR)								
f_{IN} = 9.7 MHz	25°C		−98			−97		dBc
f_{IN} = 30.5 MHz	25°C		−96			−97		dBc
f_{IN} = 70 MHz	25°C		−96			−97		dBc
	Full			−91			−90	dBc
f_{IN} = 100 MHz	25°C		−92			−92		dBc
f_{IN} = 200 MHz	25°C		−90			−90		dBc
TWO-TONE SFDR								
f_{IN} = 29 MHz (−7 dBFS), 32 MHz (−7 dBFS)	25°C		84			84		dBc
CROSSTALK[2]	Full		−95			−95		dB
ANALOG INPUT BANDWIDTH	25°C		650			650		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Crosstalk is measured at 100 MHz with −1.0 dBFS on one channel and no input on the alternate channel.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, and DCS enabled, unless otherwise noted.

Table 3.

Parameter	Temp	AD9648-105/AD9648-125 Min	AD9648-105/AD9648-125 Typ	AD9648-105/AD9648-125 Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND - 0.3		AVDD + 0.2	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	−10		+10	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
LOGIC INPUT (CSB)[1]					
High Level Input Voltage	Full	1.22		DRVDD + 0.2	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	40		132	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF

Parameter	Temp	AD9648-105/AD9648-125 Min	Typ	Max	Unit
LOGIC INPUT (SCLK/DFS/SYNC)[2]					
High Level Input Voltage	Full	1.22		DRVDD + 0.2	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current (VIN = 1.8 V)	Full	−92		−135	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT/OUTPUT (SDIO/DCS)[1]					
High Level Input Voltage	Full	1.22		DRVDD + 0.2	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	38		128	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
LOGIC INPUTS (OEB, PDWN)[2]					
High Level Input Voltage	Full	1.22		DRVDD + 0.2	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current (VIN = 1.8 V)	Full	−90		−134	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS					
CMOS Mode—DRVDD = 1.8 V					
High Level Output Voltage					
I_{OH} = 50 µA	Full	1.79			V
I_{OH} = 0.5 mA	Full	1.75			V
Low Level Output Voltage					
I_{OL} = 1.6 mA	Full			0.2	V
I_{OL} = 50 µA	Full			0.05	V
LVDS Mode—DRVDD = 1.8 V					
Differential Output Voltage (V_{OD}), ANSI Mode	Full	290	345	400	mV
Output Offset Voltage (V_{OS}), ANSI Mode	Full	1.15	1.25	1.35	V
Differential Output Voltage (V_{OD}), Reduced Swing Mode	Full	160	200	230	mV
Output Offset Voltage (V_{OS}), Reduced Swing Mode	Full	1.15	1.25	1.35	V

[1] Pull up.
[2] Pull down.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, and DCS enabled, unless otherwise noted.

Table 4.

		AD9648-105			AD9648-125			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUT PARAMETERS								
Input Clock Rate	Full			1000			1000	MHz
Conversion Rate[1]								
DCS Enabled	Full	20		105	20		125	MSPS
DCS Disabled	Full	10		105	10		125	MSPS
CLK Period—Divide-by-1 Mode (t_{CLK})	Full		9.52			8		ns
CLK Pulse Width High (t_{CH})	Full		4.76			4		ns
Aperture Delay (t_A)	Full		1.0			1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.137			0.137		ps rms
DATA OUTPUT PARAMETERS								
CMOS Mode (DRVDD = 1.8 V)								
Data Propagation Delay (t_{PD})	Full	1.8	2.9	4.4	1.8	2.9	4.4	ns
DCO Propagation Delay (t_{DCO})[2]	Full	2.0	3.1	4.4	2.0	3.1	4.4	ns
DCO to Data Skew (t_{SKEW})	Full	−1.2	−0.1	+1.0	−1.2	−0.1	+1.0	ns
LVDS Mode (DRVDD = 1.8 V)								
Data Propagation Delay (t_{PD})	Full		2.4			2.4		ns
DCO Propagation Delay (t_{DCO})[2]	Full		2.4			2.4		ns
DCO to Data Skew (t_{SKEW})	Full	−0.20	+0.03	+0.25	−0.20	+0.03	+0.25	ns
CMOS Mode Pipeline Delay (Latency)	Full		16			16		Cycles
LVDS Mode Pipeline Delay (Latency) Channel A/Channel B	Full		16/16.5			16/16.5		Cycles
Wake-Up Time (Power Down)[3]	Full		350			350		µs
Wake-Up Time (Standby)	Full		250			250		ns
Out-of-Range Recovery Time	Full		2			2		Cycles

[1] Conversion rate is the clock rate after the divider.
[2] Additional DCO delay can be added by writing to Bits[2:0] in SPI Register 0x17 (see Table 18).
[3] Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Description	Limit	Unit
SYNC TIMING REQUIREMENTS			
t_{SSYNC}	SYNC to rising edge of CLK+ setup time	0.24	ns typ
t_{HSYNC}	SYNC to rising edge of CLK+ hold time	0.40	ns typ
SPI TIMING REQUIREMENTS			
t_{DS}	Setup time between the data and the rising edge of SCLK	2	ns min
t_{DH}	Hold time between the data and the rising edge of SCLK	2	ns min
t_{CLK}	Period of the SCLK	40	ns min
t_S	Setup time between CSB and SCLK	2	ns min
t_H	Hold time between CSB and SCLK	2	ns min
t_{HIGH}	SCLK pulse width high	10	ns min
t_{LOW}	SCLK pulse width low	10	ns min
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10	ns min
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10	ns min

Timing Diagrams

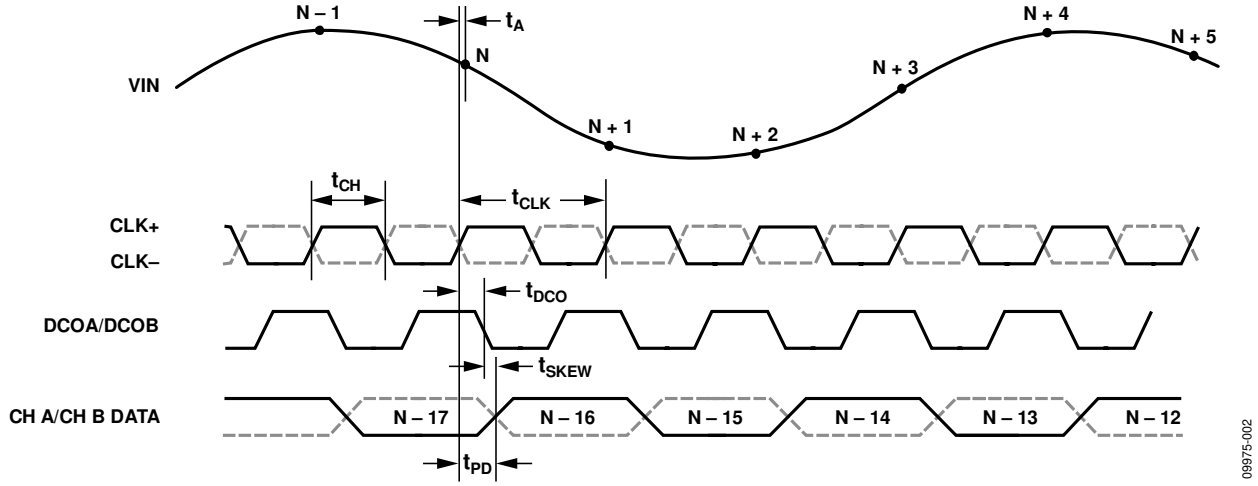


Figure 2. CMOS Default Output Mode Data Output Timing

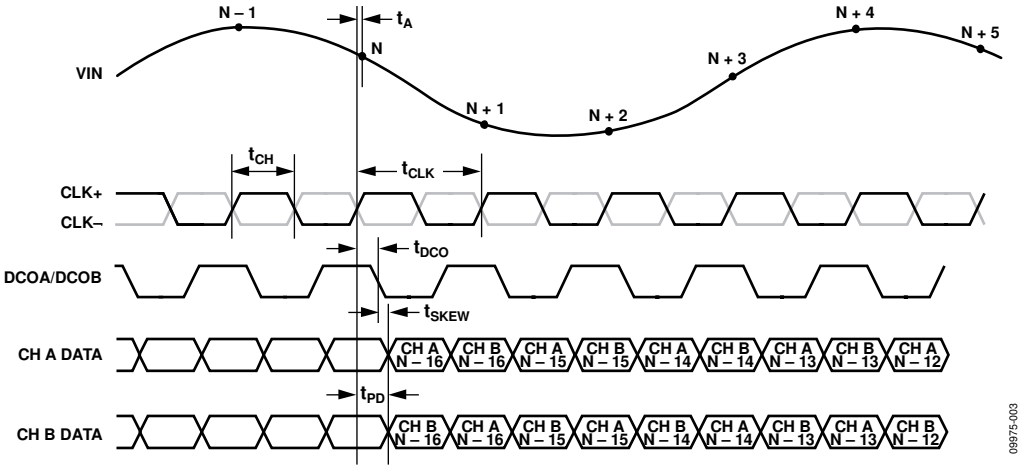


Figure 3. CMOS Interleaved Output Mode Data Output Timing

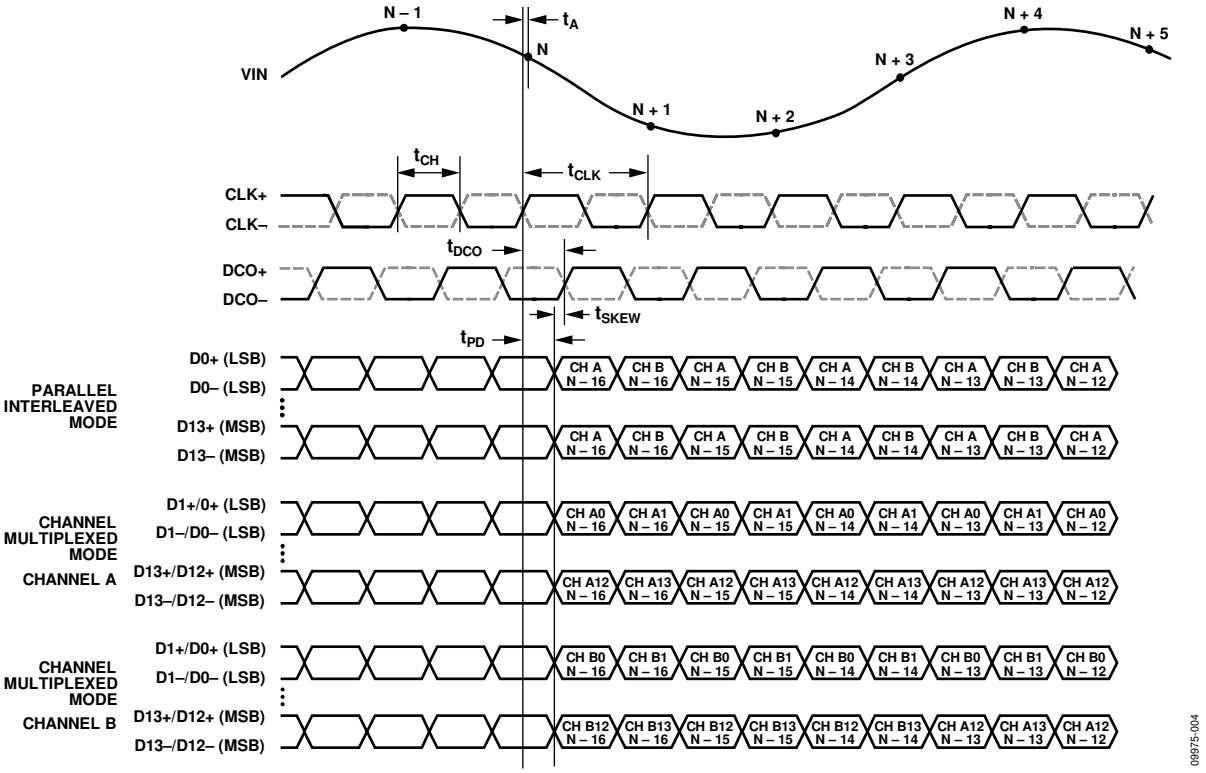


Figure 4. LVDS Modes for Data Output Timing

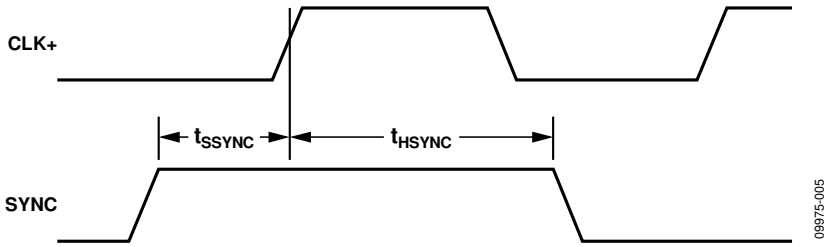


Figure 5. SYNC Input Timing Requirements

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
VIN+A/VIN+B, VIN−A/VIN−B to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
SYNC to DRVDD	−0.3 V to AVDD + 0.2 V
VCM to AGND	−0.3 V to AVDD + 0.2 V
RBIAS to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to DRVDD + 0.2 V
SCLK/DFS to AGND	−0.3 V to DRVDD + 0.2 V
SDIO/DCS to AGND	−0.3 V to DRVDD + 0.2 V
OEB	−0.3 V to DRVDD + 0.2 V
PDWN	−0.3 V to DRVDD + 0.2 V
D0A/D0B through D13A/D13B to AGND	−0.3 V to DRVDD + 0.2 V
DCOA/DCOB to AGND	−0.3 V to DRVDD + 0.2 V
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the printed circuit board (PCB) increases the reliability of the solder joints and maximizes the thermal capability of the package.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JC}[1, 3]	θ_{JB}[1, 4]	Ψ_{JT}[1, 2]	Unit
64-Lead LFCSP 9 mm × 9 mm (CP-64-4)	0	22.3	1.4	11.8	0.1	°C/W
	1.0	19.5	N/A[5]	N/A[5]	0.2	°C/W
	2.5	17.5	N/A[5]	N/A[5]	0.2	°C/W

[1] Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).
[5] N/A means not applicable.

Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. As shown Table 7, airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

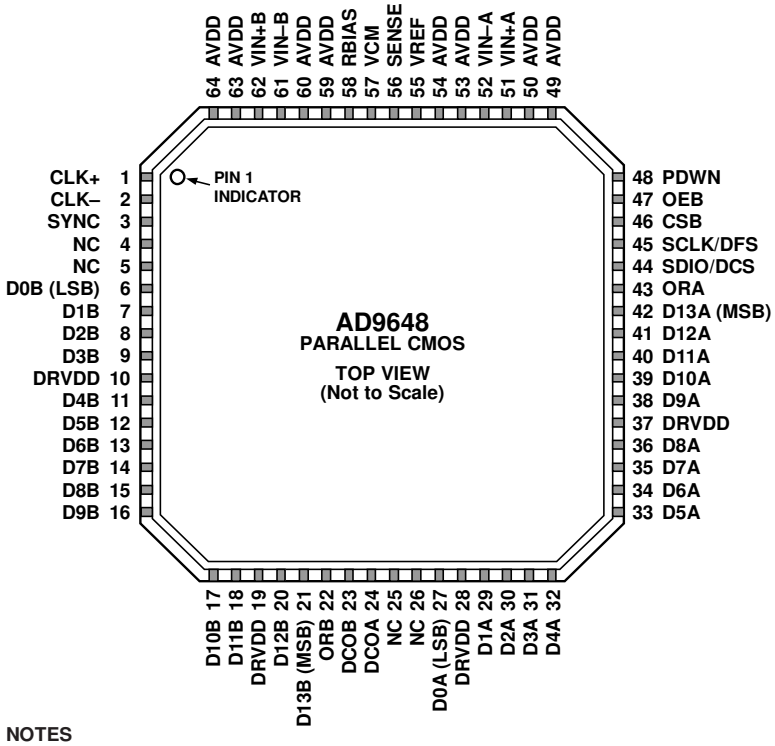
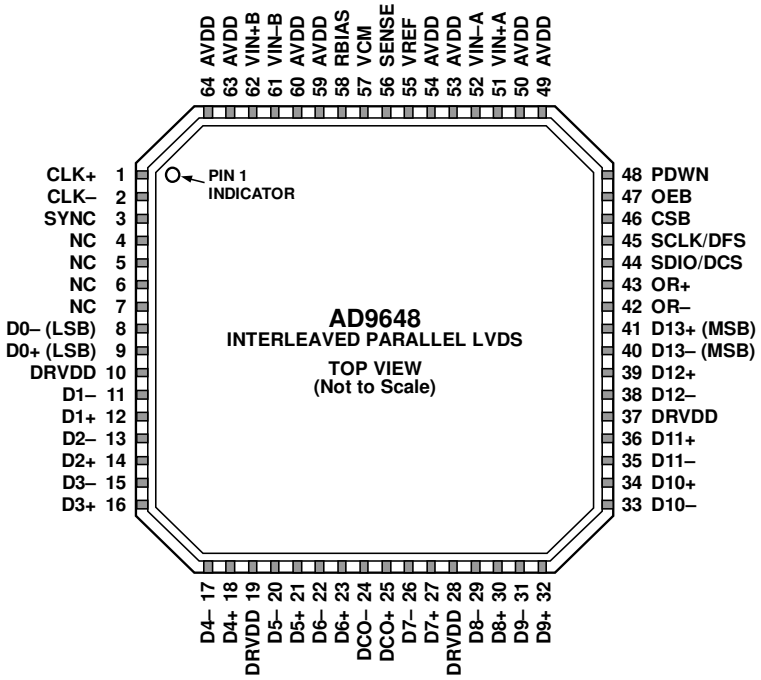


Figure 6. Parallel CMOS Pin Configuration (Top View)

Table 8. Pin Function Descriptions (Parallel CMOS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
10, 19, 28, 37	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
49, 50, 53, 54, 59, 60, 63, 64	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
4, 5, 25, 26	NC		No Connect. Do not connect to these pins.
0	AGND, Exposed Pad	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
ADC Analog			
51	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
52	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
62	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
61	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
55	VREF	Input/Output	Voltage Reference Input/Output.
56	SENSE	Input	Reference Mode Selection.
58	RBIAS	Input/Output	External Reference Bias Resistor. Connect to 10 kΩ (1% tolerance) resistor to ground.
57	VCM	Output	Common-Mode Level Bias Output for Analog Inputs.
1	CLK+	Input	ADC Clock Input—True.
2	CLK−	Input	ADC Clock Input—Complement.
Digital Input			
3	SYNC	Input	Digital Synchronization Pin. Slave mode only.

Pin No.	Mnemonic	Type	Description
Digital Outputs			
27	D0A (LSB)	Output	Channel A CMOS Output Data.
29	D1A	Output	Channel A CMOS Output Data.
30	D2A	Output	Channel A CMOS Output Data.
31	D3A	Output	Channel A CMOS Output Data.
32	D4A	Output	Channel A CMOS Output Data.
33	D5A	Output	Channel A CMOS Output Data.
34	D6A	Output	Channel A CMOS Output Data.
35	D7A	Output	Channel A CMOS Output Data.
36	D8A	Output	Channel A CMOS Output Data.
38	D9A	Output	Channel A CMOS Output Data.
39	D10A	Output	Channel A CMOS Output Data.
40	D11A	Output	Channel A CMOS Output Data.
41	D12A	Output	Channel A CMOS Output Data.
42	D13A (MSB)	Output	Channel A CMOS Output Data.
43	ORA	Output	Channel A Overrange Output.
6	D0B (LSB)	Output	Channel B CMOS Output Data.
7	D1B	Output	Channel B CMOS Output Data.
8	D2B	Output	Channel B CMOS Output Data.
9	D3B	Output	Channel B CMOS Output Data.
11	D4B	Output	Channel B CMOS Output Data.
12	D5B	Output	Channel B CMOS Output Data.
13	D6B	Output	Channel B CMOS Output Data.
14	D7B	Output	Channel B CMOS Output Data.
15	D8B	Output	Channel B CMOS Output Data.
16	D9B	Output	Channel B CMOS Output Data.
17	D10B	Output	Channel B CMOS Output Data.
18	D11B	Output	Channel B CMOS Output Data.
20	D12B	Output	Channel B CMOS Output Data.
21	D13B (MSB)	Output	Channel B CMOS Output Data.
22	ORB	Output	Channel B Overrange Output
24	DCOA	Output	Channel A Data Clock Output.
23	DCOB	Output	Channel B Data Clock Output.
SPI Control			
45	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
44	SDIO/DCS	Input/Output	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.
46	CSB	Input	SPI Chip Select (Active Low).
ADC Configuration			
47	OEB	Input	Output Enable Input (Active Low).
48	PDWN	Input	Power-Down Input in External Pin Mode. In SPI mode, this input can be configured as power-down or standby.



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE PART. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

09975-007

Figure 7. Interleaved Parallel LVDS Pin Configuration (Top View)

Table 9. Pin Function Descriptions (Interleaved Parallel LVDS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
10, 19, 28, 37	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
49, 50, 53, 54, 59, 60, 63, 64	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
4, 5, 6, 7	NC		No Connect. Do not connect to these pins.
0	AGND, Exposed Pad	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
ADC Analog			
51	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
52	VIN–A	Input	Differential Analog Input Pin (–) for Channel A.
62	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
61	VIN–B	Input	Differential Analog Input Pin (–) for Channel B.
55	VREF	Input/Output	Voltage Reference Input/Output.
56	SENSE	Input	Reference Mode Selection.
58	RBIAS	Input/Output	External Reference Bias Resistor. Connect to 10 kΩ (1% tolerance) resistor to ground.
57	VCM	Output	Common-Mode Level Bias Output for Analog Inputs.
1	CLK+	Input	ADC Clock Input—True.
2	CLK–	Input	ADC Clock Input—Complement.
Digital Input			
3	SYNC	Input	Digital Synchronization Pin. Slave mode only.
Digital Outputs			
9	D0+ (LSB)	Output	Channel A/Channel B LVDS Output Data 0—True.
8	D0– (LSB)	Output	Channel A/Channel B LVDS Output Data 0—Complement.
12	D1+	Output	Channel A/Channel B LVDS Output Data 1—True.
11	D1–	Output	Channel A/Channel B LVDS Output Data 1—Complement.

Pin No.	Mnemonic	Type	Description
14	D2+	Output	Channel A/Channel B LVDS Output Data 2—True.
13	D2−	Output	Channel A/Channel B LVDS Output Data 2—Complement.
16	D3+	Output	Channel A/Channel B LVDS Output Data 3—True.
15	D3−	Output	Channel A/Channel B LVDS Output Data 3—Complement.
18	D4+	Output	Channel A/Channel B LVDS Output Data 4 —True.
17	D4−	Output	Channel A/Channel B LVDS Output Data 4—Complement.
21	D5+	Output	Channel A/Channel B LVDS Output Data 5—True.
20	D5−	Output	Channel A/Channel B LVDS Output Data 5—Complement.
23	D6+	Output	Channel A/Channel B LVDS Output Data 6—True.
22	D6−	Output	Channel A/Channel B LVDS Output Data 6—Complement.
27	D7+	Output	Channel A/Channel B LVDS Output Data 7—True.
26	D7−	Output	Channel A/Channel B LVDS Output Data 7—Complement.
30	D8+	Output	Channel A/Channel B LVDS Output Data 8—True.
29	D8−	Output	Channel A/Channel B LVDS Output Data 8—Complement.
32	D9+	Output	Channel A/Channel B LVDS Output Data 9—True.
31	D9−	Output	Channel A/Channel B LVDS Output Data 9—Complement.
34	D10+	Output	Channel A/Channel B LVDS Output Data 10—True.
33	D10−	Output	Channel A/Channel B LVDS Output Data 10—Complement.
36	D11+	Output	Channel A/Channel B LVDS Output Data 11—True.
35	D11−	Output	Channel A/Channel B LVDS Output Data 11—Complement.
39	D12+	Output	Channel A/Channel B LVDS Output Data 12—True.
38	D12−	Output	Channel A/Channel B LVDS Output Data 12—Complement.
41	D13+ (MSB)	Output	Channel A/Channel B LVDS Output Data 13—True.
40	D13− (MSB)	Output	Channel A/Channel B LVDS Output Data 13—Complement.
43	OR+	Output	Channel A/Channel B LVDS Overrange Output—True.
42	OR−	Output	Channel A/Channel B LVDS Overrange Output—Complement.
25	DCO+	Output	Channel A/Channel B LVDS Data Clock Output—True.
24	DCO−	Output	Channel A/Channel B LVDS Data Clock Output—Complement.
SPI Control			
45	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
44	SDIO/DCS	Input/Output	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.
46	CSB	Input	SPI Chip Select (Active Low).
ADC Configuration			
47	OEB	Input	Output Enable Input (Active Low).
48	PDWN	Input	Power-Down Input in External Pin Mode. In SPI mode, this input can be configured as power-down or standby.

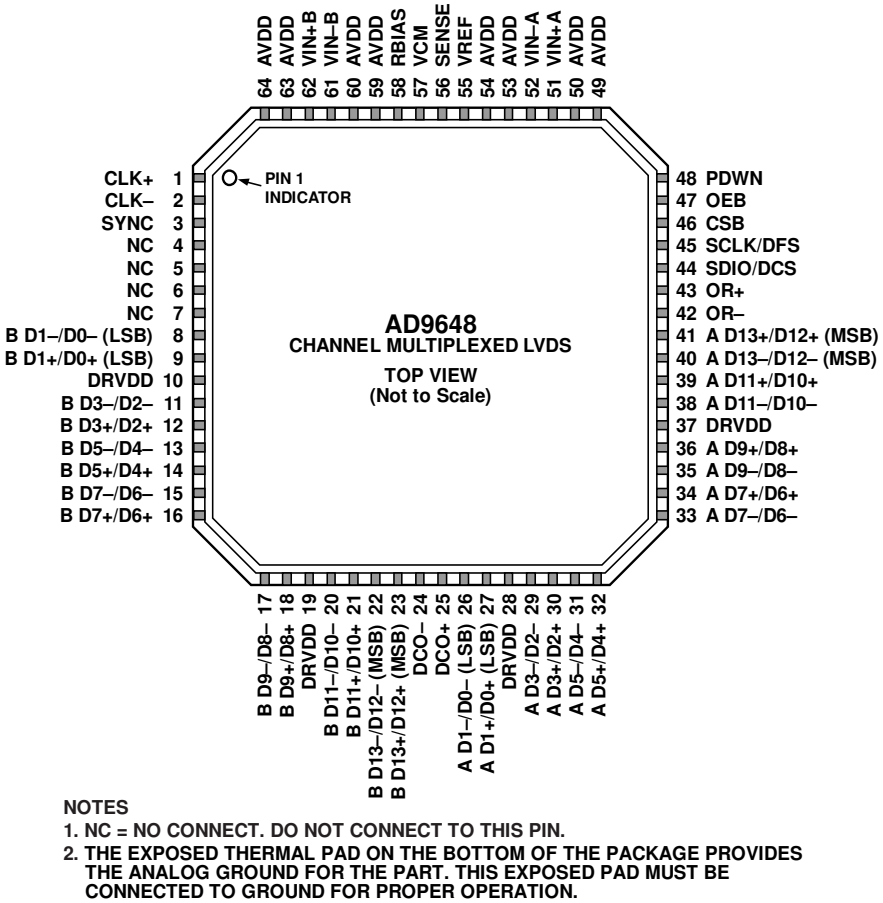


Figure 8. Channel Multiplexed LVDS Pin Configuration (Top View)

Table 10 Pin Function Descriptions (Channel Multiplexed Parallel LVDS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
10, 19, 28, 37	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
49, 50, 53, 54, 59, 60, 63, 64	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
4, 5, 6, 7	NC		Do Not Connect.
0	AGND, Exposed Pad	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
ADC Analog			
51	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
52	VIN−A	Input	Differential Analog Input Pin (–) for Channel A.
62	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
61	VIN−B	Input	Differential Analog Input Pin (–) for Channel B.
55	VREF	Input/Output	Voltage Reference Input/Output.
56	SENSE	Input	Reference Mode Selection.
58	RBIAS	Input/Output	External Reference Bias Resistor. Connect to 10 kΩ (1% tolerance) resistor to ground.
57	VCM	Output	Common-Mode Level Bias Output for Analog Inputs.
1	CLK+	Input	ADC Clock Input—True.
2	CLK–	Input	ADC Clock Input—Complement.
Digital Input			
3	SYNC	Input	Digital Synchronization Pin. Slave mode only.

Pin No.	Mnemonic	Type	Description
Digital Outputs			
8	B D1−/D0− (LSB)	Output	Channel B LVDS Output Data 1/Data 0—Complement.
9	B D1+/D0+ (LSB)	Output	Channel B LVDS Output Data 1/Data 0—True.
11	B D3−/D2−	Output	Channel B LVDS Output Data 3/Data 2—Complement.
12	B D3+/D2+	Output	Channel B LVDS Output Data 3/Data 2—True.
13	B D5−/D4−	Output	Channel B LVDS Output Data 5/Data 4—Complement.
14	B D5+/D4+	Output	Channel B LVDS Output Data 5/Data 4—True.
15	B D7−/D6−	Output	Channel B LVDS Output Data 7/Data 6—Complement.
16	B D7+/D6+	Output	Channel B LVDS Output Data 7/Data 6—True.
17	B D9−/D8−	Output	Channel B LVDS Output Data 9/Data 8—Complement.
18	B D9+/D8+	Output	Channel B LVDS Output Data 9/Data 8—True.
20	B D11−/D10−	Output	Channel B LVDS Output Data 11/Data 10—Complement.
21	B D11+/D10+	Output	Channel B LVDS Output Data 11/Data 10—True.
22	B D13−/D12− (MSB)	Output	Channel B LVDS Output Data 13/Data 12—Complement.
23	B D13+/D12+ (MSB)	Output	Channel B LVDS Output Data 13/Data 12—True.
26	A D1−/D0− (LSB)	Output	Channel A LVDS Output Data 1/Data 0—Complement.
27	A D1+/D0+ (LSB)	Output	Channel A LVDS Output Data 1/Data 0—True.
29	A D3−/D2−	Output	Channel A LVDS Output Data 3/Data 2—Complement.
30	A D3+/D2+	Output	Channel A LVDS Output Data 3/Data 2—True.
32	A D5+/D4+	Output	Channel A LVDS Output Data 5/Data 4—True.
31	A D5−/D4−	Output	Channel A LVDS Output Data 5/Data 4—Complement.
34	A D7+/D6+	Output	Channel A LVDS Output Data 7/Data 6—True.
33	A D7−/D6−	Output	Channel A LVDS Output Data 7/Data 6—Complement.
36	A D9+/D8+	Output	Channel A LVDS Output Data 9/Data 8—True.
35	A D9−/D8−	Output	Channel A LVDS Output Data 9/Data 8—Complement.
39	A D11+/D10+	Output	Channel A LVDS Output Data 11/Data 10—True.
38	A D11−/D10−	Output	Channel A LVDS Output Data 11/Data 10—Complement.
41	A D13+/D12+ (MSB)	Output	Channel A LVDS Output Data 13/Data 12—True.
40	A D13−/D12− (MSB)	Output	Channel A LVDS Output Data 13/Data 12—Complement.
43	OR+	Output	Channel A/Channel B LVDS Overrange Output—True.
42	OR−	Output	Channel A/Channel B LVDS Overrange Output—Complement.
25	DCO+	Output	Channel A/Channel B LVDS Data Clock Output—True.
24	DCO−	Output	Channel A/Channel B LVDS Data Clock Output—Complement.
SPI Control			
45	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
44	SDIO/DCS	Input/Output	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.
46	CSB	Input	SPI Chip Select (Active Low).
ADC Configuration			
47	OEB	Input	Output Enable Input (Active Low).
48	PDWN	Input	Power-Down Input in External Pin Mode. In SPI mode, this input can be configured as power-down or standby.

TYPICAL PERFORMANCE CHARACTERISTICS

AD9648-125

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, and DCS enabled, unless otherwise noted.

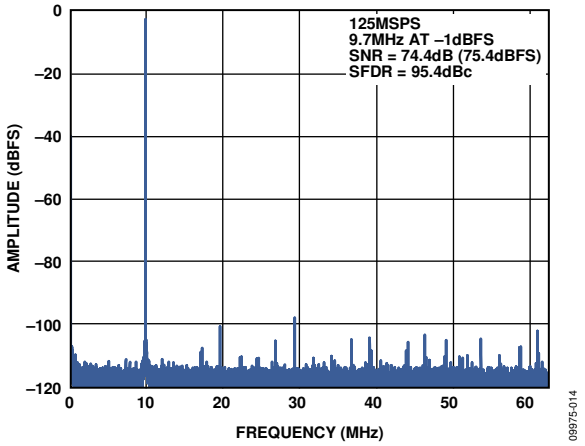


Figure 9. Single-Tone FFT with f_{IN} = 9.7 MHz

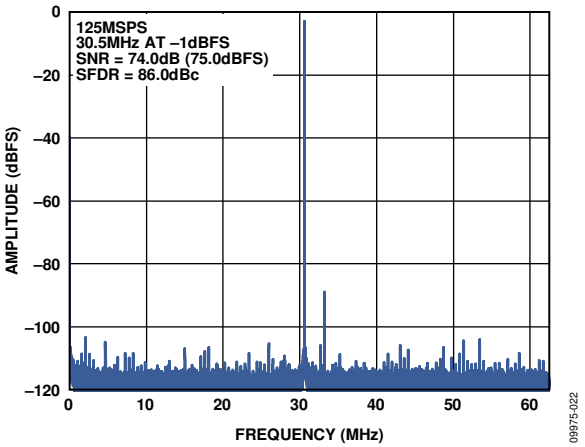


Figure 10. Single-Tone FFT with f_{IN} = 30.5 MHz

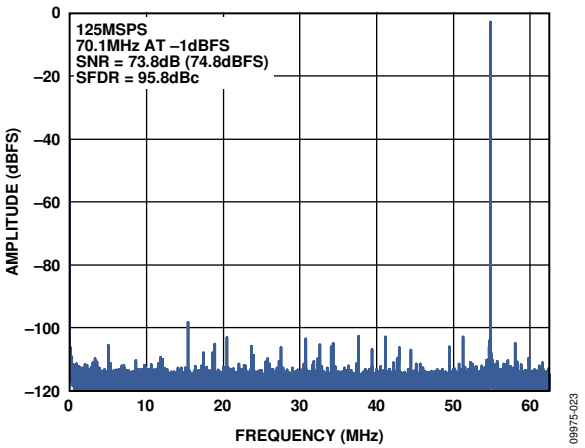


Figure 11. Single-Tone FFT with f_{IN} = 70.1 MHz

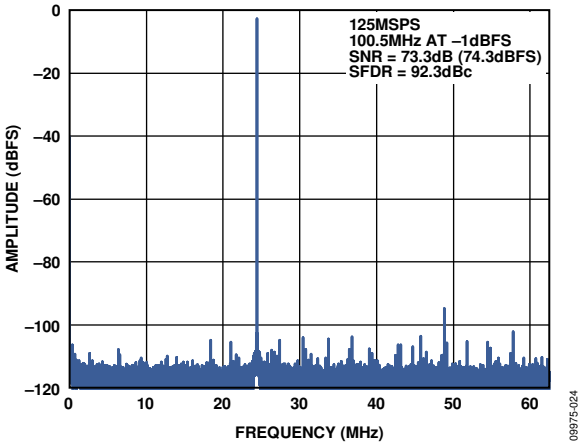


Figure 12. Single-Tone FFT with f_{IN} = 100.5 MHz

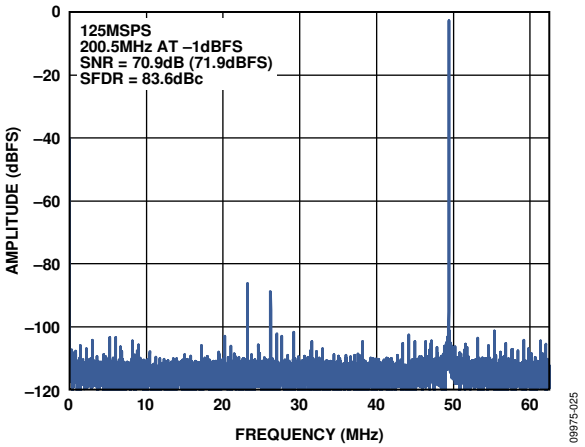


Figure 13. Single-Tone FFT with f_{IN} = 200.5 MHz

AD9648-125

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, and DCS enabled, unless otherwise noted.

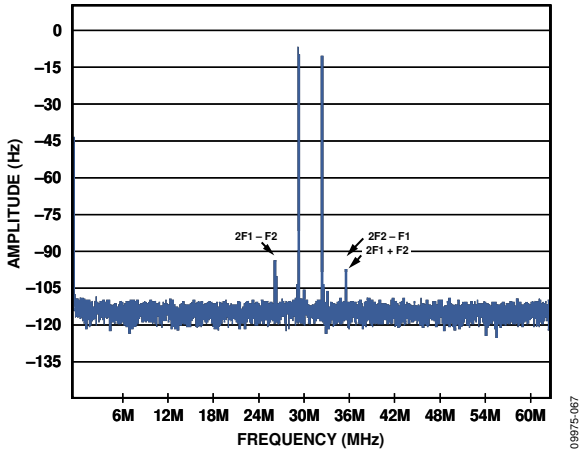


Figure 14. Two-Tone FFT with f_{IN1} = 29 MHz and f_{IN2} = 32 MHz

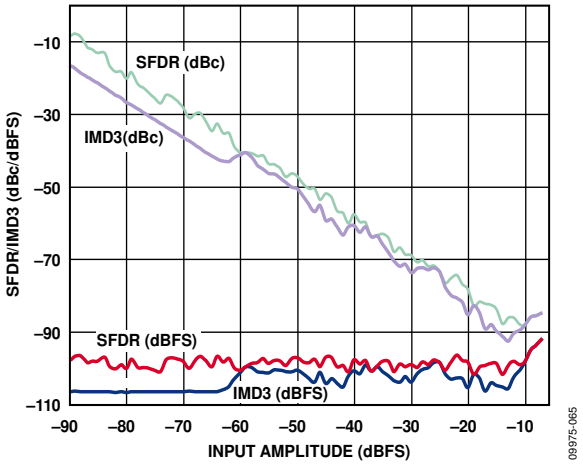


Figure 17. Two-Tone SFDR/IMD3 vs. Input Amplitude (AIN) with f_{IN1} = 29 MHz and f_{IN2} = 32 MHz

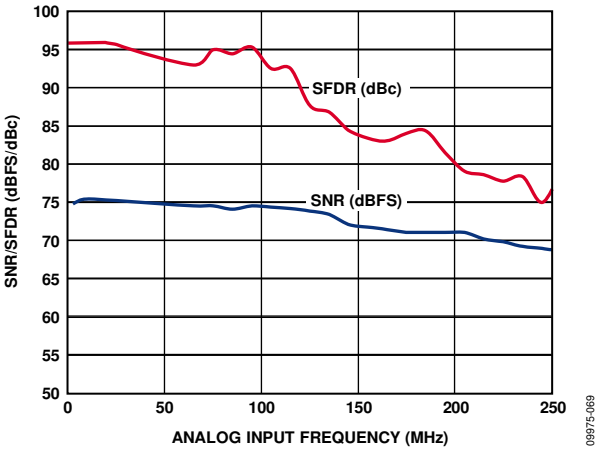


Figure 15. SNR/SFDR vs. Input Frequency (AIN) with 2 V p-p Full Scale

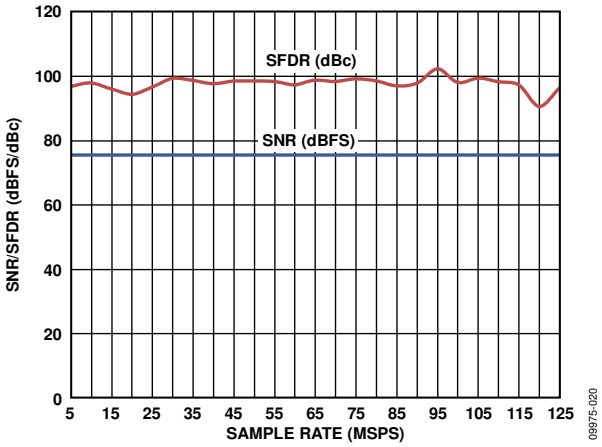


Figure 18. SNR/SFDR vs. Sample Rate with AIN = 9.7 MHz

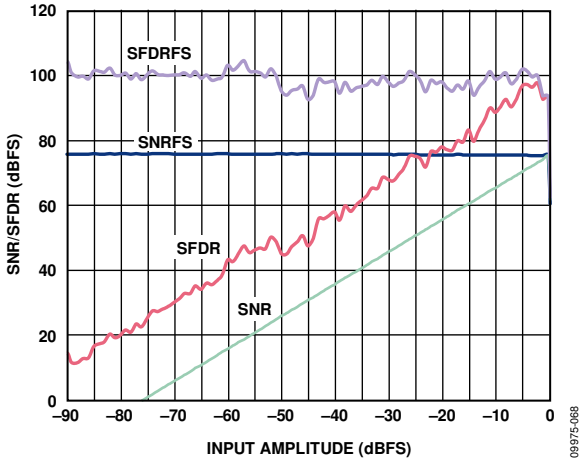


Figure 16. SNR/SFDR vs. Input Amplitude (AIN) with f_{IN} = 9.7 MHz

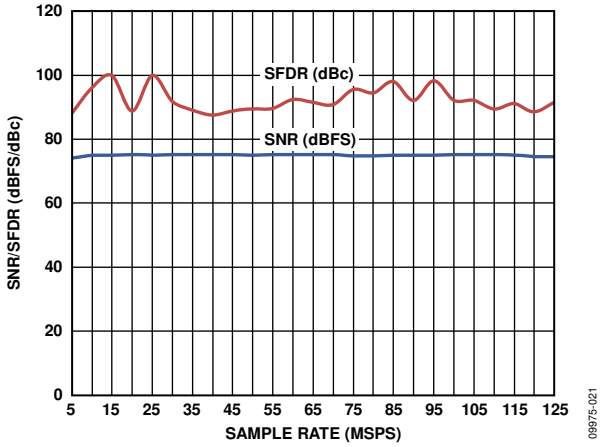


Figure 19. SNR/SFDR vs. Sample Rate with AIN = 70.1 MHz

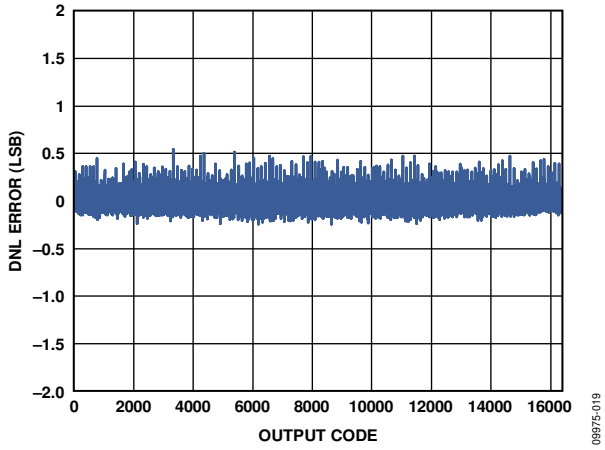


Figure 20. DNL Error with f_{IN} = 9.7 MHz

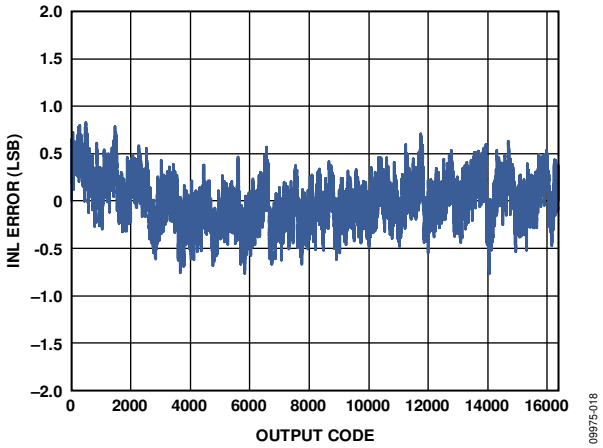


Figure 22. INL Error with f_{IN} = 9.7 MHz

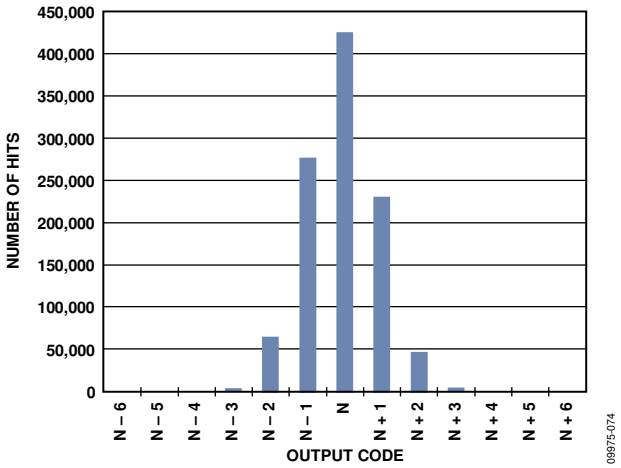


Figure 21. Shorted Input Histogram

AD9648-105

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, and DCS enabled, unless otherwise noted.

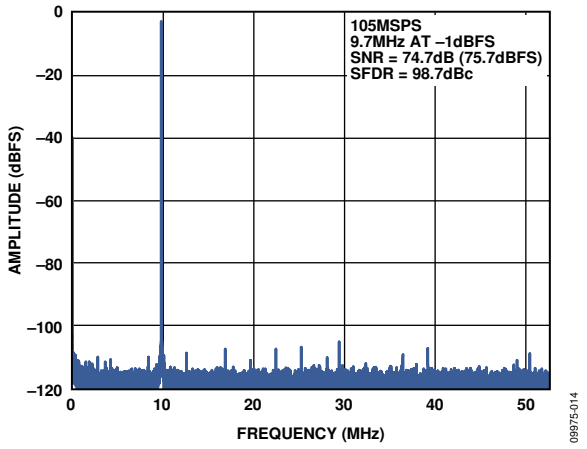


Figure 23. Single-Tone FFT with f_{IN} = 9.7 MHz

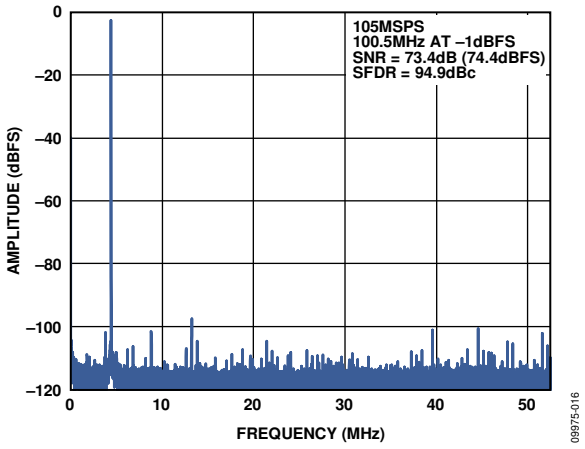


Figure 26. Single-Tone FFT with f_{IN} = 100.5 MHz

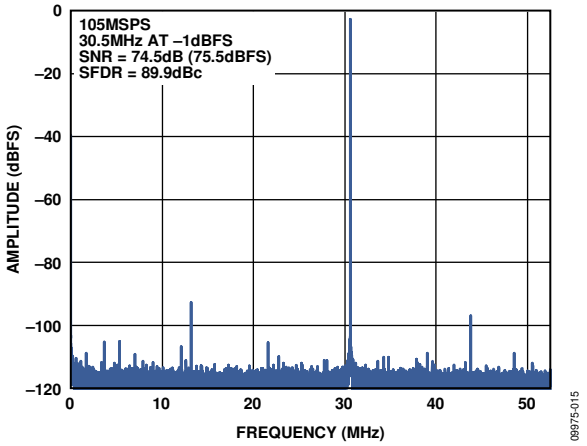


Figure 24. Single-Tone FFT with f_{IN} = 30.5 MHz

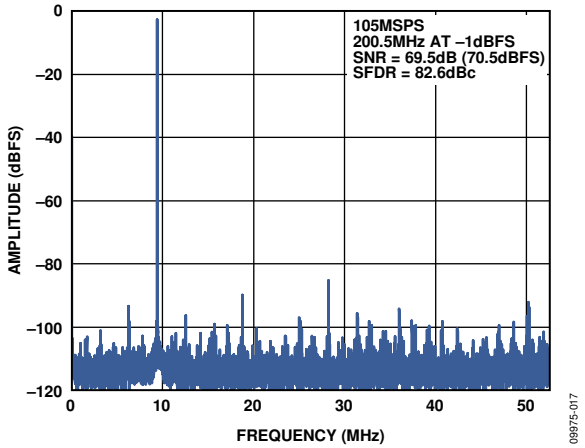


Figure 27. Single-Tone FFT with f_{IN} = 200.5 MHz

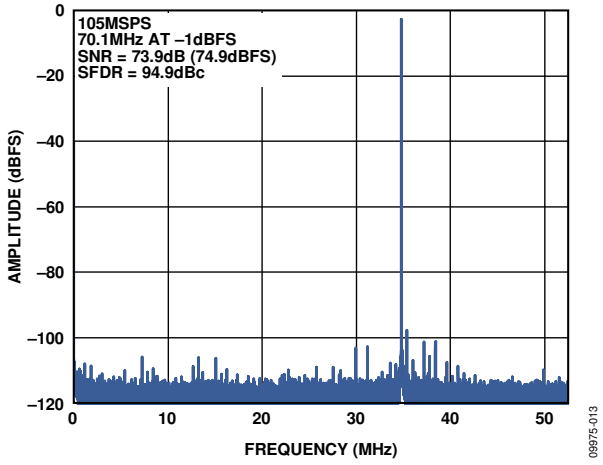


Figure 25. Single-Tone FFT with f_{IN} = 70.1 MHz

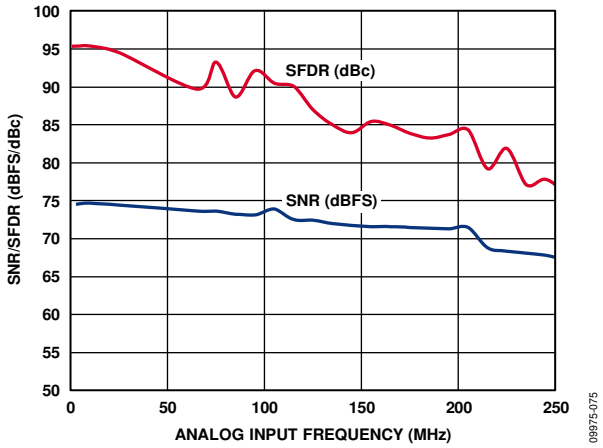


Figure 28. SNR/SFDR vs. Input Frequency (AIN) with 2 V p-p Full Scale

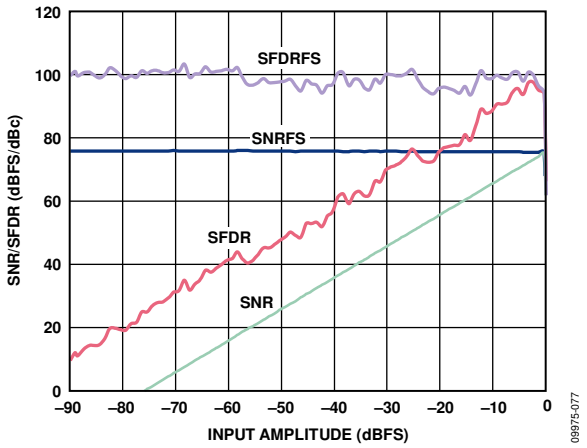


Figure 31. SNR/SFDR vs. Input Amplitude (AIN) with f_{IN} = 9.7 MHz

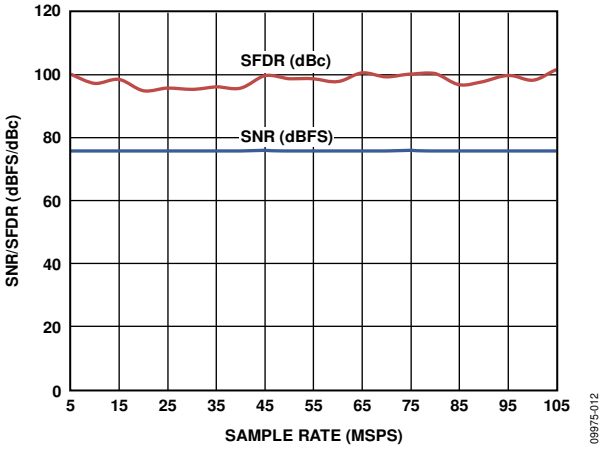


Figure 29. SNR/SFDR vs. Sample Rate with AIN = 9.7 MHz

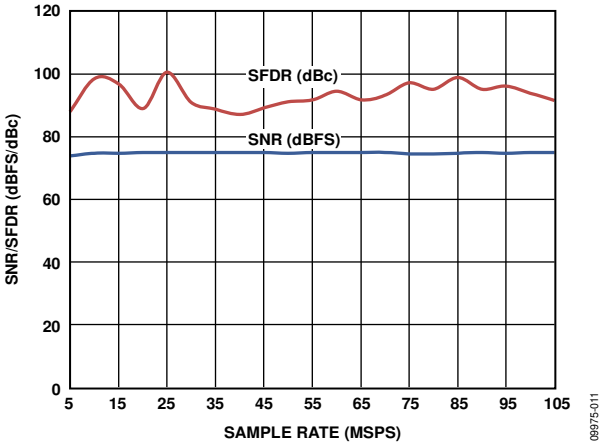


Figure 32. SNR/SFDR vs. Sample Rate with AIN = 70.1 MHz

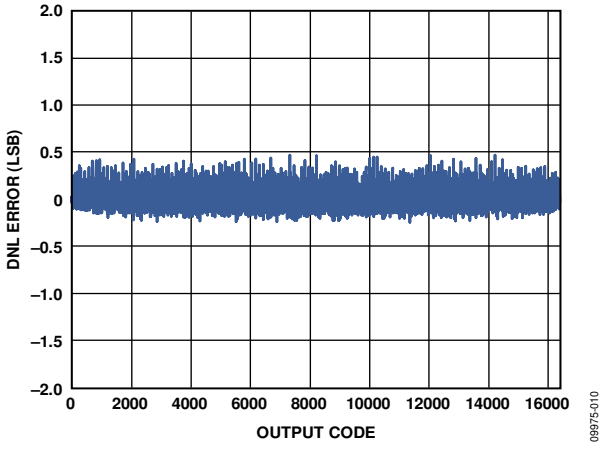


Figure 30. DNL Error with f_{IN} = 9.7 MHz

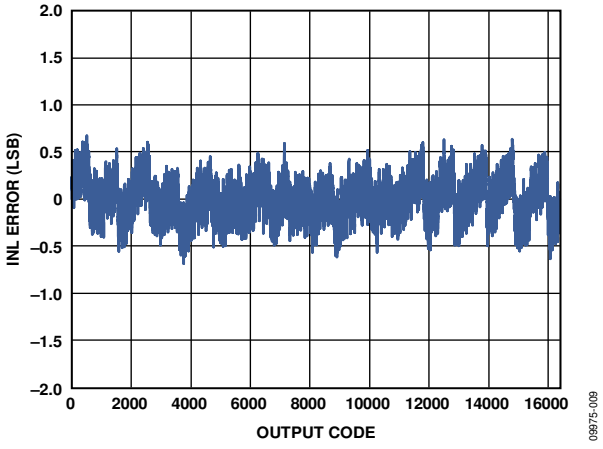


Figure 33. INL Error with f_{IN} = 9.7 MHz

EQUIVALENT CIRCUITS

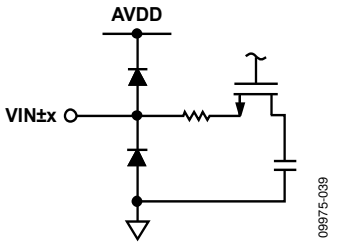


Figure 34. Equivalent Analog Input Circuit

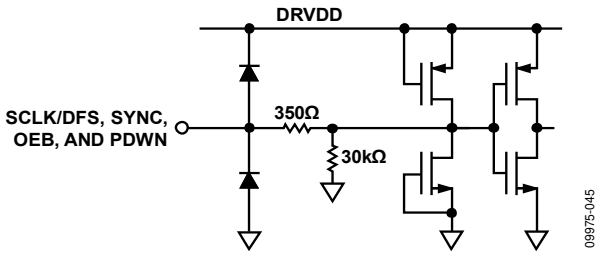


Figure 38. Equivalent SCLK/DFS, SYNC, OEB, and PDWN Input Circuit

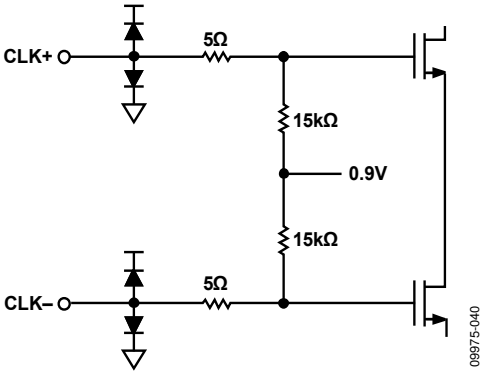


Figure 35. Equivalent Clock Input Circuit

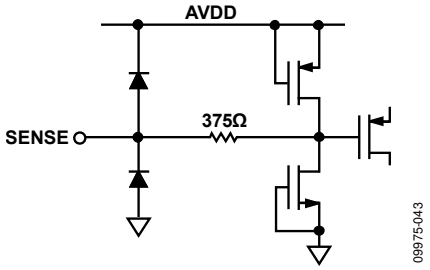


Figure 39. Equivalent SENSE Circuit

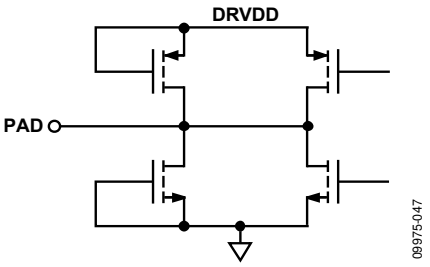


Figure 36. Equivalent Digital Output Circuit

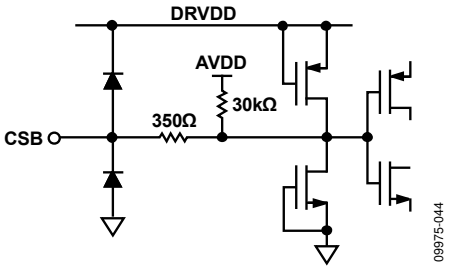


Figure 40. Equivalent CSB Input Circuit

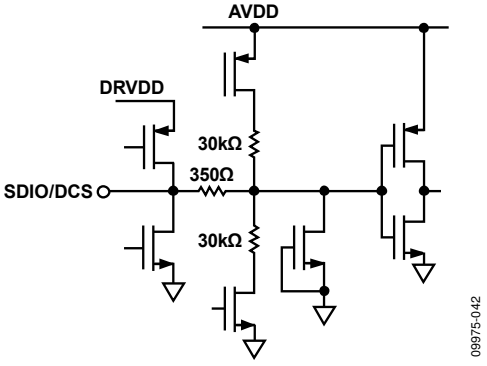


Figure 37. Equivalent SDIO/DCS Input Circuit

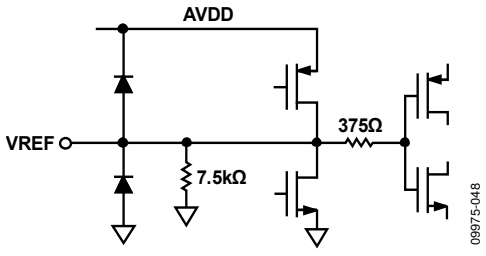


Figure 41. Equivalent VREF Circuit

THEORY OF OPERATION

The AD9648 dual ADC design can be used for diversity reception of signals, where the ADCs are operating identically on the same carrier but from two separate antennae. The ADCs can also be operated with independent analog inputs. The user can sample any $f_S/2$ frequency segment from dc to 200 MHz, using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in ADC performance. Operation to 300 MHz analog input is permitted but occurs at the expense of increased ADC noise and distortion.

In nondiversity applications, the AD9648 can be used as a baseband or direct downconversion receiver, where one ADC is used for I input data and the other is used for Q input data.

Synchronization capability is provided to allow synchronized timing between multiple channels or multiple devices.

Programming and control of the AD9648 is accomplished using a 3-bit SPI-compatible serial interface.

ADC ARCHITECTURE

The AD9648 architecture consists of a multistage, pipelined ADC. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the CMOS/LVDS output buffers. The output buffers are powered from a separate (DRVDD) supply, allowing digital output noise to be separated from the analog core. During power-down, the output buffers go into a high impedance state.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9648 is a differential switched-capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. By using an input common-mode voltage of midsupply, users can minimize signal-dependent errors and achieve optimum performance.

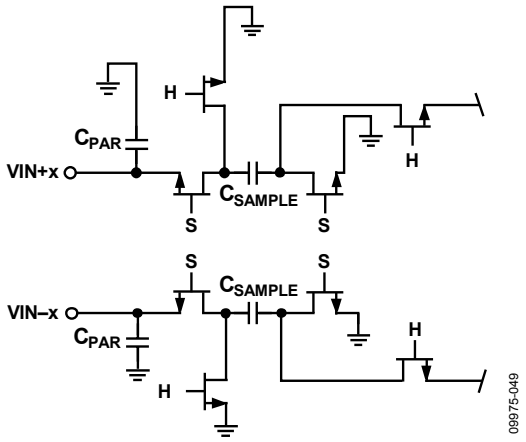


Figure 42. Switched-Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample-and-hold mode (see Figure 42). When the input circuit is switched to sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current injected from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and, therefore, achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Either a shunt capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005) for more information. In general, the precise values depend on the application.