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16-Bit, 25 MSPS/65 MSPS/80 MSPS/105 MSPS, 1.8 V Dual Analog-to-Digital Converter (ADC)

Data Sheet **AD9650**

FEATURES

- 1.8 V analog supply operation
- 1.8 V CMOS or LVDS output supply
- SNR
  - 82 dBFS at 30 MHz input and 105 MSPS data rate
  - 83 dBFS at 9.7 MHz input and 25 MSPS data rate
- SFDR
  - 90 dBc at 30 MHz input and 105 MSPS data rate
  - 95 dBc at 9.7 MHz input and 25 MSPS data rate
- Low power
  - 328 mW per channel at 105 MSPS
  - 119 mW per channel at 25 MSPS
- Integer 1-to-8 input clock divider
- IF sampling frequencies to 300 MHz
- Analog input range of 2.7 V p-p
- Optional on-chip dither
- Integrated ADC sample-and-hold inputs
- Differential analog inputs with 500 MHz bandwidth
- ADC clock duty cycle stabilizer

APPLICATIONS

- Industrial instrumentation
- X-Ray, MRI, and ultrasound equipment
- High speed pulse acquisition
- Chemical and spectrum analysis
- Direct conversion receivers
- Multimode digital receivers
- Smart antenna systems
- General-purpose software radios

GENERAL DESCRIPTION

The AD9650 is a dual, 16-bit, 25 MSPS/65 MSPS/80 MSPS/105 MSPS analog-to-digital converter (ADC) designed for digitizing high frequency, wide dynamic range signals with input frequencies of up to 300 MHz.

The dual ADC core features a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth, differential sample-and-hold analog input amplifiers, and shared integrated voltage reference, which eases design considerations. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

The ADC output data can be routed directly to the two external 16-bit output ports or multiplexed on a single 16-bit bus. These outputs can be set to either 1.8 V CMOS or LVDS.

FUNCTIONAL BLOCK DIAGRAM

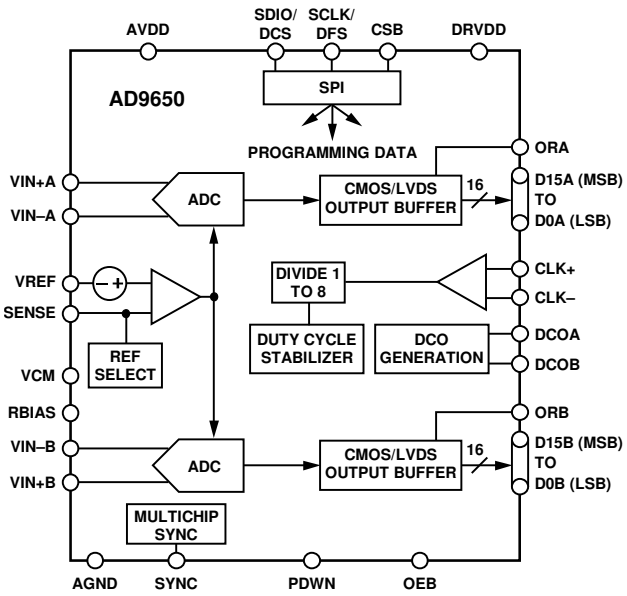

Figure 1.

Flexible power-down options allow significant power savings, when desired.

Programming for setup and control is accomplished using a 3-wire SPI-compatible serial interface.

The AD9650 is available in a 64-lead LFCSP and is specified over the industrial temperature range of −40°C to +85°C.

PRODUCT HIGHLIGHTS

1. On-chip dither option for improved SFDR performance with low power analog input.
2. Proprietary differential input that maintains excellent SNR performance for input frequencies up to 300 MHz.
3. Operation from a single 1.8 V supply and a separate digital output driver supply accommodating 1.8 V CMOS or LVDS outputs.
4. Standard serial port interface (SPI) that supports various product features and functions, such as data formatting (offset binary, twos complement, or gray coding), enabling the clock DCS, power-down, and test modes.
5. Pin compatible with the AD9268 and other dual families, AD9269, AD9251, AD9231, and AD9204. This allows a simple migration across resolutions and bandwidth.

Rev. B

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Technical Support www.analog.com

AD9650* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9650 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-586: LVDS Outputs for High Speed A/D Converters
- AN-742: Frequency Domain Response of Switched-Capacitor ADCs
- AN-807: Multicarrier WCDMA Feasibility
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-812: MicroController-Based Serial Port Interface (SPI) Boot Circuit
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-878: High Speed ADC SPI Control Software

Data Sheet

- AD9650-EP: Enhanced Product Data Sheet
- AD9650: 16-Bit, 25 MSPS/65 MSPS/80 MSPS/105 MSPS, 1.8 V Dual Analog-to-Digital Converter (ADC) Data Sheet

User Guides

- UG-003: Evaluating the AD9650/AD9268/AD9258/AD9251/AD9231/AD9204 Analog-to-Digital Converters

TOOLS AND SIMULATIONS

- Visual Analog
- AD9650 IBIS Model

REFERENCE MATERIALS

Technical Articles

- Improve The Design Of Your Passive Wideband ADC Front-End Network
- MS-2210: Designing Power Supplies for High Speed ADC
- MS-2677: JESD204B Subclasses - Part 2: Subclass 1 vs. Subclass 2 System Considerations

DESIGN RESOURCES

- AD9650 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9650 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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SPECIFICATIONS

ADC DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, V_{IN} = −1.0 dBFS differential input, 1.35 V internal reference, DCS disabled, unless otherwise noted.

Table 1.

		AD9650BCPZ-25			AD9650BCPZ-65			AD9650BCPZ-80			AD9650BCPZ-105			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full		16			16			16			16		Bits
ACCURACY														
No Missing Codes	Full		Guaranteed			Guaranteed			Guaranteed			Guaranteed		
Offset Error	Full		±0.2	±0.5		±0.2	±0.5		±0.4	±0.70		±0.4	±0.7	% FSR
Gain Error	Full		±0.4	±2.5		±0.4	±2.5		±0.4	±2.5		±0.4	±2.5	% FSR
Differential Nonlinearity (DNL)[1]	Full	−1		+1.3	−1		+1.3	−1		+1.3	−1		+1.3	LSB
	25°C		±0.7			±0.7			±0.7			±0.7		LSB
Integral Nonlinearity (INL)[1]	Full			±3			±5			±6			±6	LSB
	25°C		±1.6			±2.5			±2.5			±3		LSB
MATCHING CHARACTERISTIC														
Offset Error	Full		±0.1	±0.4		±0.1	±0.4		±0.1	±0.4		±0.1	±0.4	% FSR
Gain Error	Full		±0.5	±1.3		±0.5	±1.3		±0.5	±1.3		±0.5	±1.3	% FSR
TEMPERATURE DRIFT														
Offset Error	Full		±2			±2			±2			±2		ppm/°C
Gain Error	Full		±15			±15			±15			±15		ppm/°C
INTERNAL VOLTAGE REFERENCE														
Output Voltage Error (1.35 V Mode)	Full		±7	±14		±7	±14		±7	±14		±7	±14	mV
Load Regulation at 1.0 mA	Full		10			10			10			10		mV
INPUT REFERRED NOISE														
VREF = 1.35 V	25°C		1.5			1.5			1.5			1.5		LSB rms
ANALOG INPUT														
Input Span, VREF = 1.35 V	Full		2.7			2.7			2.7			2.7		V p-p
Input Capacitance[2]	Full		11			11			11			11		pF
Input Common-Mode Voltage	Full		0.9			0.9			0.9			0.9		V
REFERENCE INPUT RESISTANCE	Full		6			6			6			6		kΩ
POWER SUPPLIES														
Supply Voltage														
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
Supply Current														
IAVDD[1]	Full		125	131		202	209		267	275		332	340	mA
IDRVDD[1] (1.8 V CMOS)	Full		8			23			29			36		mA
IDRVDD[1] (1.8 V LVDS)	Full		72			86			90			100		mA
POWER CONSUMPTION														
DC Input	Full		237	254		397	408		522	537		656	675	mW
Sine Wave Input[1] (DRVDD = 1.8 V CMOS Output Mode)	Full		240			405			533			663		mW
Sine Wave Input[1] (DRVDD = 1.8 V LVDS Output Mode)	Full		355			520			642			778		mW
Standby Power[3]	Full		50			50			50			50		mW
Power-Down Power	Full		0.25	2.5		0.25	2.5		0.25	2.5		0.25	2.5	mW

[1] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND.
[3] Standby power is measured with a dc input and with the CLK+ and CLK− pins inactive (set to AVDD or AGND).

ADC AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, V_{IN} = −1.0 dBFS differential input, 1.35 V internal reference, DCS disabled, unless otherwise noted.

Table 2.

Parameter[1]	Temp	AD9650BCPZ-25 Min	AD9650BCPZ-25 Typ	AD9650BCPZ-25 Max	AD9650BCPZ-65 Min	AD9650BCPZ-65 Typ	AD9650BCPZ-65 Max	AD9650BCPZ-80 Min	AD9650BCPZ-80 Typ	AD9650BCPZ-80 Max	AD9650BCPZ-105 Min	AD9650BCPZ-105 Typ	AD9650BCPZ-105 Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)														
f_{IN} = 9.7 MHz	25°C		83			83			83			82.5		dBFS
f_{IN} = 30 MHz	25°C		81.5			82			82			82		dBFS
	Full	81.8			81.5			81.6			80.5			dBFS
f_{IN} = 70 MHz	25°C		79.5			81			81			80		dBFS
f_{IN} = 141 MHz[2]	25°C					79.5			80			80		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION (SINAD)														
f_{IN} = 9.7 MHz	25°C		82.2			82			82			82		dBFS
f_{IN} = 30 MHz	25°C		80			81.2			82			80.4		dBFS
	Full	81.5			81			80.7			80			dBFS
f_{IN} = 70 MHz	25°C		78			79.2			78.5			78.8		dBFS
f_{IN} = 141 MHz[2]	25°C					75			75.1			75.5		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)														
f_{IN} = 9.7 MHz	25°C		13.5			13.5			13.5			13.3		Bits
f_{IN} = 30 MHz	25°C		13.0			13.2			13.2			13.2		Bits
f_{IN} = 70 MHz	25°C		12.7			13.0			13.0			13.0		Bits
f_{IN} = 141 MHz[2]	25°C					12.9			13.0			12.3		Bits
WORST SECOND OR THIRD HARMONIC														
f_{IN} =9.7 MHz	25°C		−95			−94			−95.5			−91		dBc
f_{IN} = 30 MHz	25°C		−85			−93			−92			−90		dBc
	Full			−91.5			−88			−87			−87	dBc
f_{IN} = 70 MHz	25°C		−87			−86			−86			−92		dBc
f_{IN} = 141 MHz	25°C					−79			−79			−80		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)														
f_{IN} = 9.7 MHz	25°C		95			94			95.5			91		dBc
f_{IN} = 30 MHz	25°C		85			93			92			90		dBc
	Full	91.5			88			87			87			dBc
f_{IN} = 70 MHz	25°C		87			86			86			92		dBc
f_{IN} = 141 MHz	25°C					79			79			80		dBc
WORST OTHER (HARMONIC OR SPUR)														
f_{IN} = 9.7 MHz	25°C		−110			−105			−105			−100		dBc
f_{IN} = 30 MHz	25°C		−102			−105			−105			−101		dBc
	Full			−97			−97			−97			−94	dBc
f_{IN} = 70 MHz	25°C		−97			−97			−97			−97		dBc
f_{IN} = 141 MHz	25°C					−97			−97			−88		dBc
TWO-TONE SFDR														
f_{IN} = 7.2 MHz (−7 dBFS), 8.4 MHz (−7 dBFS)	25°C		87											
f_{IN} = 25 MHz (−7 dBFS), 30 MHz (−7 dBFS)	25°C		84			90			87			87		dBc
f_{IN} = 125 MHz (−7 dBFS), 128 MHz (−7 dBFS)	25°C					83			83			84		dBc
CROSSTALK[3]	Full		−105			−105			−105			−105		dBFS
ANALOG INPUT BANDWIDTH	25°C		500			500			500			500		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Measurements made with a divide-by-4 clock rate to minimize the effects of clock jitter on the SNR performance.
[3] Crosstalk is measured with a 170 MHz tone at −1 dBFS on one channel and no input on the alternate channel.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, V_{IN} = −1.0 dBFS differential input, 1.35 V internal reference, and DCS enabled, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK–)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	−100		+100	µA
Low Level Input Current	Full	−100		+100	µA
Input Capacitance	Full		9		pF
Input Resistance	Full	8	10	12	kΩ
SYNC INPUT					
Logic Compliance			CMOS		
Internal Bias	Full		0.9		V
Input Voltage Range	Full	AGND		AVDD	V
High Level Input Voltage	Full	1.2		AVDD	V
Low Level Input Voltage	Full	AGND		0.6	V
High Level Input Current	Full	−100		+100	µA
Low Level Input Current	Full	−100		+100	µA
Input Capacitance	Full		1		pF
Input Resistance	Full	12	16	20	kΩ
LOGIC INPUT (CSB)[1]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	40		132	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SCLK/DFS)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current (V_{IN} = 1.8 V)	Full	−92		−135	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT/OUTPUT (SDIO/DCS)[1]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	38		128	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
LOGIC INPUTS (OEB, PDWN)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current (V_{IN} = 1.8 V)	Full	−90		−134	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF

Parameter	Temperature	Min	Typ	Max	Unit
DIGITAL OUTPUTS					
CMOS Mode—DRVDD = 1.8 V					
High Level Output Voltage					
I_{OH} = 50 µA	Full	1.79			V
I_{OH} = 0.5 mA	Full	1.75			V
Low Level Output Voltage					
I_{OL} = 1.6 mA	Full			0.2	V
I_{OL} = 50 µA	Full			0.05	V
LVDS Mode—DRVDD = 1.8 V					
Differential Output Voltage (V_{OD}), ANSI Mode	Full	290	345	400	mV
Output Offset Voltage (V_{OS}), ANSI Mode	Full	1.15	1.25	1.35	V
Differential Output Voltage (V_{OD}), Reduced Swing Mode	Full	160	200	230	mV
Output Offset Voltage (V_{OS}), Reduced Swing Mode	Full	1.15	1.25	1.35	V

[1] Pull up.
[2] Pull down.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, V_{IN} = −1.0 dBFS differential input, 1.35 V internal reference, and DCS enabled, unless otherwise noted.

Table 4.

		AD9650BCPZ-25			AD9650BCPZ-65			AD9650BCPZ-80			AD9650BCPZ-105			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUT PARAMETERS														
Input Clock Rate	Full			200			520			640			640	MHz
Conversion Rate[1]														
DCS Enabled	Full	20		25	20		65	20		80	20		105	MSPS
DCS Disabled	Full	10		25	10		65	10		80	10		105	MSPS
CLK Period—Divide-by-1 Mode (t_{CLK})	Full	40			15.4			12.5			9.5			ns
CLK Pulse Width High (t_{CH})														
Divide-by-1 Mode, DCS Enabled	Full	12	20	28	4.65	7.70	10.75	3.75	6.25	8.75	2.85	4.75	6.65	ns
Divide-by-1 Mode, DCS Disabled	Full	19	20	21	7.33	7.70	8.07	5.95	6.25	6.55	4.5	4.75	5.0	ns
Divide-by-2 Mode Through Divide-by-8 Mode	Full	0.8			0.8			0.8			0.8			ns
Aperture Delay (t_A)	Full		1.0			1.0			1.0			1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.100			0.090			0.080			0.075		ps rms
DATA OUTPUT PARAMETERS														
CMOS Mode														
Data Propagation Delay (t_{PD})	Full	2.8	3.5	4.2	2.8	3.5	4.2	2.8	3.5	4.2	2.8	3.5	4.2	ns
DCO Propagation Delay (t_{DCO})[2]	Full		3.1			3.1			3.1			3.1		ns
DCO to Data Skew (t_{SKEW})	Full	−0.6	−0.4	0	−0.6	−0.4	0	−0.6	−0.4	0	−0.6	−0.4	0	ns
LVDS Mode														
Data Propagation Delay (t_{PD})	Full	2.9	3.7	4.5	2.9	3.7	4.5	2.9	3.7	4.5	2.9	3.7	4.5	ns
DCO Propagation Delay (t_{DCO})[2]	Full		3.9			3.9			3.9			3.9		ns
DCO to Data Skew (t_{SKEW})	Full	−0.1	+0.2	+0.5	−0.1	+0.2	+0.5	−0.1	+0.2	+0.5	−0.1	+0.2	+0.5	ns
CMOS Mode Pipeline Delay (Latency)	Full		12			12			12			12		Cycles
LVDS Mode Pipeline Delay (Latency) Channel A/ Channel B	Full		12/12.5			12/12.5			12/12.5			12/12.5		Cycles
Wake-Up Time[3]	Full		500			500			500			500		µs
Out-of-Range Recovery Time	Full		2			2			2			2		Cycles

[1] Conversion rate is the clock rate after the divider.
[2] Additional DCO delay can be added by writing to Bit 0 through Bit 4 in SPI Register 0x17 (see Table 17).
[3] Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Conditions	Limit	Unit
SYNC TIMING REQUIREMENTS			
t_{SSYNC}	SYNC to rising edge of CLK+ setup time	0.3	ns typ
t_{HSYNC}	SYNC to rising edge of CLK+ hold time	0.40	ns typ
SPI TIMING REQUIREMENTS[1]			
t_{DS}	Setup time between the data and the rising edge of SCLK	2	ns min
t_{DH}	Hold time between the data and the rising edge of SCLK	2	ns min
t_{CLK}	Period of the SCLK	40	ns min
t_S	Setup time between CSB and SCLK	2	ns min
t_H	Hold time between CSB and SCLK	2	ns min
t_{HIGH}	SCLK pulse width high	10	ns min
t_{LOW}	SCLK pulse width low	10	ns min
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10	ns min
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10	ns min

[1] See Figure 93.

Timing Diagrams

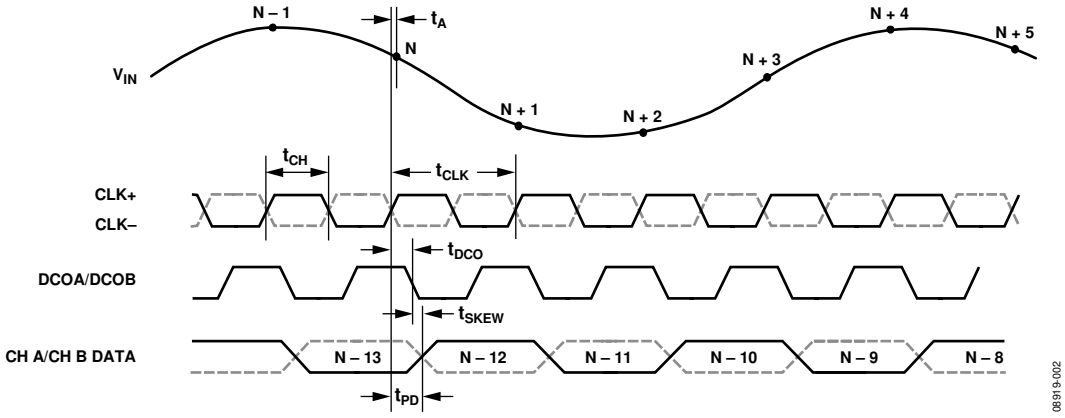


Figure 2. CMOS Default Output Mode Data Output Timing

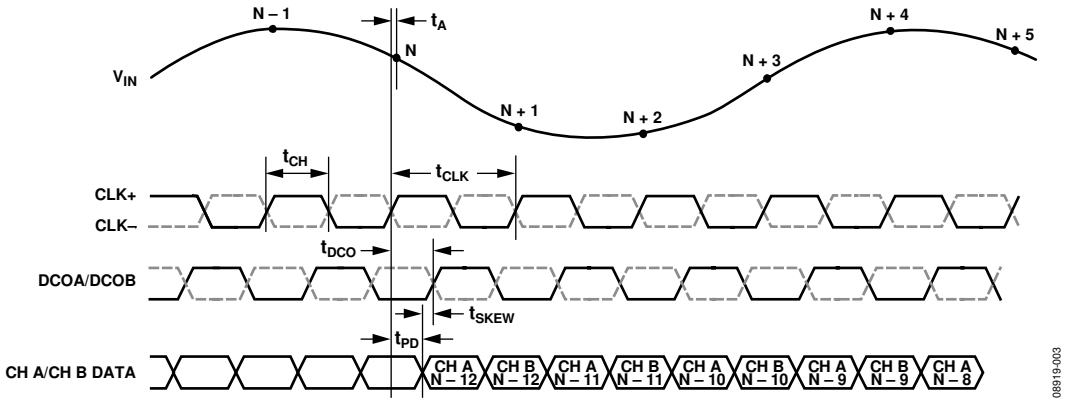


Figure 3. CMOS Interleaved Output Mode Data Output Timing

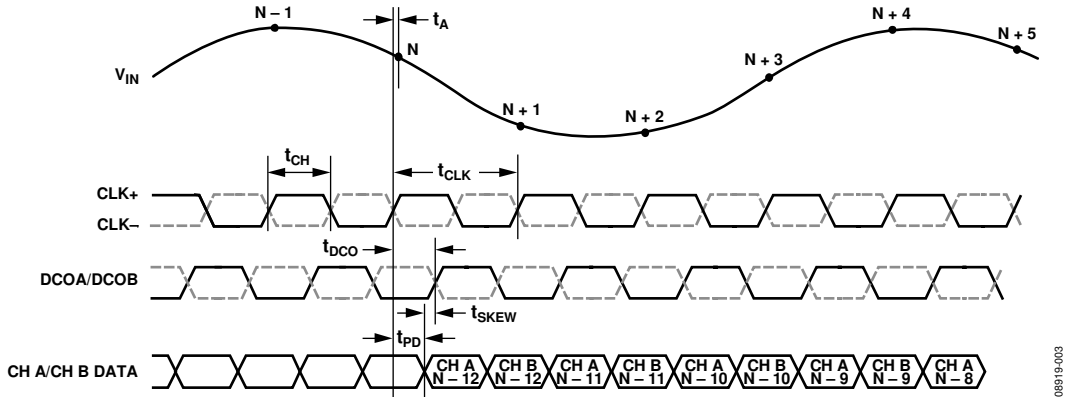


Figure 4. LVDS Mode Data Output Timing

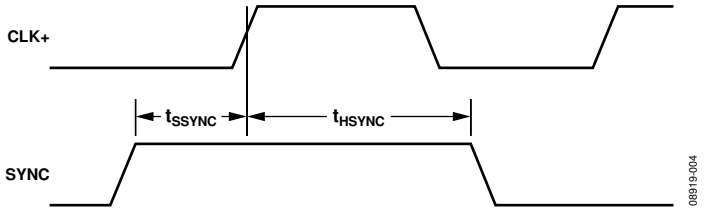


Figure 5. SYNC Input Timing Requirements

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical[1]	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
VIN+A/VIN+B, VIN−A/VIN−B to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
SYNC to AGND	−0.3 V to AVDD + 0.2 V
VREF to AGND	−0.3 V to AVDD + 0.2 V
SENSE to AGND	−0.3 V to AVDD + 0.2 V
VCM to AGND	−0.3 V to AVDD + 0.2 V
RBIAS to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to DRVDD + 0.2 V
SCLK/DFS to AGND	−0.3 V to DRVDD + 0.2 V
SDIO/DCS to AGND	−0.3 V to DRVDD + 0.2 V
OEB	−0.3 V to DRVDD + 0.2 V
PDWN	−0.3 V to DRVDD + 0.2 V
D0A/D0B Through D15A/D15B to AGND	−0.3 V to DRVDD + 0.2 V
DCOA/DCOB to AGND	−0.3 V to DRVDD + 0.2 V
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

[1] The inputs and outputs are rated to the supply voltage (AVDD or DRVDD) + 0.2 V but should not exceed 2.1 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the PCB increases the reliability of the solder joints and maximizes the thermal capability of the package.

Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. As shown in Table 7, airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces θ_{JA}.

Table 7. Thermal Resistance

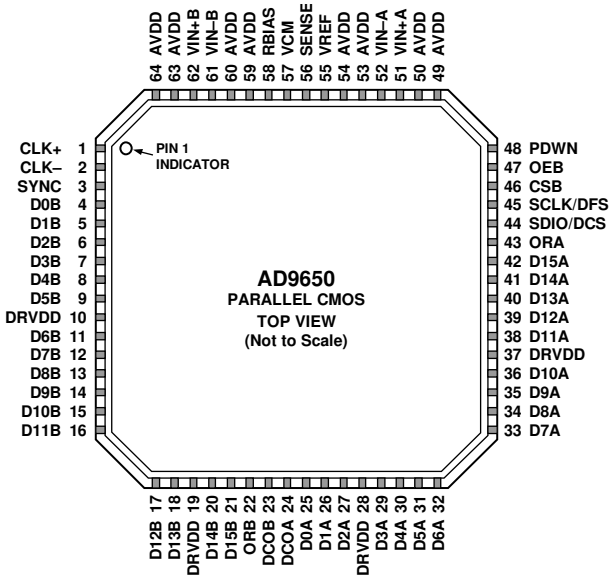
Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JC}[1, 3]	θ_{JB}[1, 4]	Unit
64-Lead LFCSP (CP-64-6)	0	18.5	1.0		°C/W
	1.0	16.1		9.2	°C/W
	2.5	14.5			°C/W

[1] Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-STD 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE PART. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

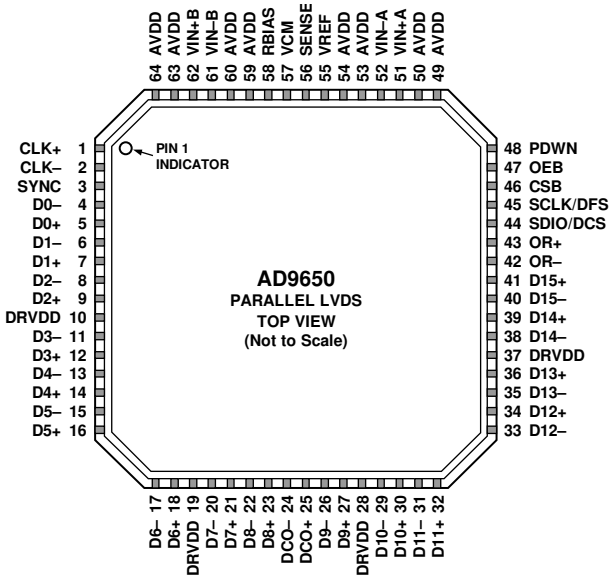
08919-005

Figure 6. LFCSP Parallel CMOS Pin Configuration (Top View)

Table 8. Pin Function Descriptions (Parallel CMOS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
10, 19, 28, 37	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
49, 50, 53, 54, 59, 60, 63, 64	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
0	AGND, Exposed Pad	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
ADC Analog			
51	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
52	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
62	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
61	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
55	VREF	Input/output	Voltage Reference Input/Output.
56	SENSE	Input	Voltage Reference Mode Select. See Table 11 for details.
58	RBIAS	Input/output	External Reference Bias Resistor.
57	VCM	Output	Common-Mode Level Bias Output for Analog Inputs.
1	CLK+	Input	ADC Clock Input—True.
2	CLK−	Input	ADC Clock Input—Complement.
Digital Input			
3	SYNC	Input	Digital Synchronization Pin. Slave mode only.
Digital Outputs			
25	D0A	Output	Channel A CMOS Output Data (LSB).
26	D1A	Output	Channel A CMOS Output Data.
27	D2A	Output	Channel A CMOS Output Data.
29	D3A	Output	Channel A CMOS Output Data.
30	D4A	Output	Channel A CMOS Output Data.
31	D5A	Output	Channel A CMOS Output Data.
32	D6A	Output	Channel A CMOS Output Data.

Pin No.	Mnemonic	Type	Description
33	D7A	Output	Channel A CMOS Output Data.
34	D8A	Output	Channel A CMOS Output Data.
35	D9A	Output	Channel A CMOS Output Data.
36	D10A	Output	Channel A CMOS Output Data.
38	D11A	Output	Channel A CMOS Output Data.
39	D12A	Output	Channel A CMOS Output Data.
40	D13A	Output	Channel A CMOS Output Data.
41	D14A	Output	Channel A CMOS Output Data.
42	D15A	Output	Channel A CMOS Output Data (MSB).
43	ORA	Output	Channel A Overrange Output.
4	D0B	Output	Channel B CMOS Output Data (LSB).
5	D1B	Output	Channel B CMOS Output Data.
6	D2B	Output	Channel B CMOS Output Data.
7	D3B	Output	Channel B CMOS Output Data.
8	D4B	Output	Channel B CMOS Output Data.
9	D5B	Output	Channel B CMOS Output Data.
11	D6B	Output	Channel B CMOS Output Data.
12	D7B	Output	Channel B CMOS Output Data.
13	D8B	Output	Channel B CMOS Output Data.
14	D9B	Output	Channel B CMOS Output Data.
15	D10B	Output	Channel B CMOS Output Data.
16	D11B	Output	Channel B CMOS Output Data.
17	D12B	Output	Channel B CMOS Output Data.
18	D13B	Output	Channel B CMOS Output Data.
20	D14B	Output	Channel B CMOS Output Data.
21	D15B	Output	Channel B CMOS Output Data (MSB).
22	ORB	Output	Channel B Overrange Output
24	DCOA	Output	Channel A Data Clock Output.
23	DCOB	Output	Channel B Data Clock Output.
SPI Control			
45	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
44	SDIO/DCS	Input/output	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.
46	CSB	Input	SPI Chip Select (Active Low).
ADC Configuration			
47	OEB	Input	Output Enable Input (Active Low) in External Pin Mode.
48	PDWN	Input	Power-Down Input in External Pin Mode. In SPI mode, this input can be configured as power-down or standby.



NOTES
1. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE PART. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

08919-006

Figure 7. LFCSP Interleaved Parallel LVDS Pin Configuration (Top View)

Table 9. Pin Function Descriptions (Interleaved Parallel LVDS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
10, 19, 28, 37	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
49, 50, 53, 54, 59, 60, 63, 64	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
0	AGND, Exposed Pad	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
ADC Analog			
51	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
52	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
62	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
61	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
55	VREF	Input/output	Voltage Reference Input/Output.
56	SENSE	Input	Voltage Reference Mode Select. See Table 11 for details.
58	RBIAS	Input/output	External Reference Bias Resistor.
57	VCM	Output	Common-Mode Level Bias Output for Analog Inputs.
1	CLK+	Input	ADC Clock Input—True.
2	CLK−	Input	ADC Clock Input—Complement.
Digital Input			
3	SYNC	Input	Digital Synchronization Pin. Slave mode only.
Digital Outputs			
5	D0+	Output	Channel A/Channel B LVDS Output Data 0—True (LSB).
4	D0−	Output	Channel A/Channel B LVDS Output Data 0—Complement (LSB).
7	D1+	Output	Channel A/Channel B LVDS Output Data 1—True.
6	D1−	Output	Channel A/Channel B LVDS Output Data 1—Complement.
9	D2+	Output	Channel A/Channel B LVDS Output Data 2—True.
8	D2−	Output	Channel A/Channel B LVDS Output Data 2—Complement.
12	D3+	Output	Channel A/Channel B LVDS Output Data 3—True.

Pin No.	Mnemonic	Type	Description
11	D3−	Output	Channel A/Channel B LVDS Output Data 3—Complement.
14	D4+	Output	Channel A/Channel B LVDS Output Data 4—True.
13	D4−	Output	Channel A/Channel B LVDS Output Data 4—Complement.
16	D5+	Output	Channel A/Channel B LVDS Output Data 5—True.
15	D5−	Output	Channel A/Channel B LVDS Output Data 5—Complement.
18	D6+	Output	Channel A/Channel B LVDS Output Data 6—True.
17	D6−	Output	Channel A/Channel B LVDS Output Data 6—Complement.
21	D7+	Output	Channel A/Channel B LVDS Output Data 7—True.
20	D7−	Output	Channel A/Channel B LVDS Output Data 7—Complement.
23	D8+	Output	Channel A/Channel B LVDS Output Data 8—True.
22	D8−	Output	Channel A/Channel B LVDS Output Data 8—Complement.
27	D9+	Output	Channel A/Channel B LVDS Output Data 9—True.
26	D9−	Output	Channel A/Channel B LVDS Output Data 9—Complement.
30	D10+	Output	Channel A/Channel B LVDS Output Data 10—True.
29	D10−	Output	Channel A/Channel B LVDS Output Data 10—Complement.
32	D11+	Output	Channel A/Channel B LVDS Output Data 11—True.
31	D11−	Output	Channel A/Channel B LVDS Output Data 11—Complement.
34	D12+	Output	Channel A/Channel B LVDS Output Data 12—True.
33	D12−	Output	Channel A/Channel B LVDS Output Data 12—Complement.
36	D13+	Output	Channel A/Channel B LVDS Output Data 13—True.
35	D13−	Output	Channel A/Channel B LVDS Output Data 13—Complement.
39	D14+	Output	Channel A/Channel B LVDS Output Data 14—True.
38	D14−	Output	Channel A/Channel B LVDS Output Data 14—Complement.
41	D15+	Output	Channel A/Channel B LVDS Output Data 15—True (MSB).
40	D15−	Output	Channel A/Channel B LVDS Output Data 15—Complement (MSB).
43	OR+	Output	Channel A/Channel B LVDS Overrange Output—True.
42	OR−	Output	Channel A/Channel B LVDS Overrange Output—Complement.
25	DCO+	Output	Channel A/Channel B LVDS Data Clock Output—True.
24	DCO−	Output	Channel A/Channel B LVDS Data Clock Output—Complement.
SPI Control			
45	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
44	SDIO/DCS	Input/output	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.
46	CSB	Input	SPI Chip Select (Active Low).
ADC Configuration			
47	OEB	Input	Output Enable Input (Active Low) in External Pin Mode.
48	PDWN	Input	Power-Down Input in External Pin Mode. In SPI mode, this input can be configured as power-down or standby.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, rated sample rate, DCS disabled, 1.35 V internal reference, 2.7 V p-p differential input, VIN = −1.0 dBFS, and 32k sample, T_A = 25°C, unless otherwise noted.

AD9650-25

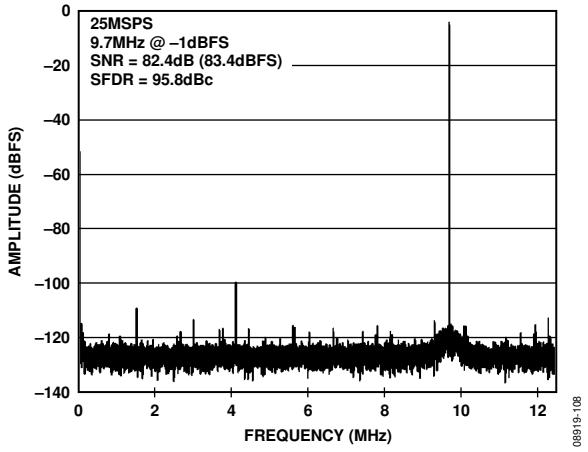


Figure 8. AD9650-25 Single-Tone FFT with f_{IN} = 9.7 MHz

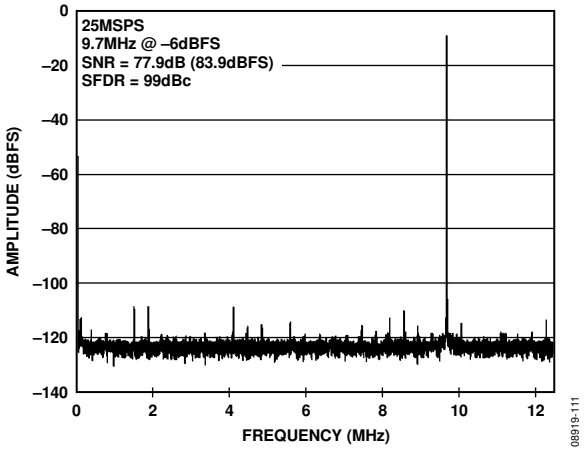


Figure 11. AD9650-25 Single-Tone FFT with f_{IN} = 9.7 MHz at −6 dBFS with Dither Disabled

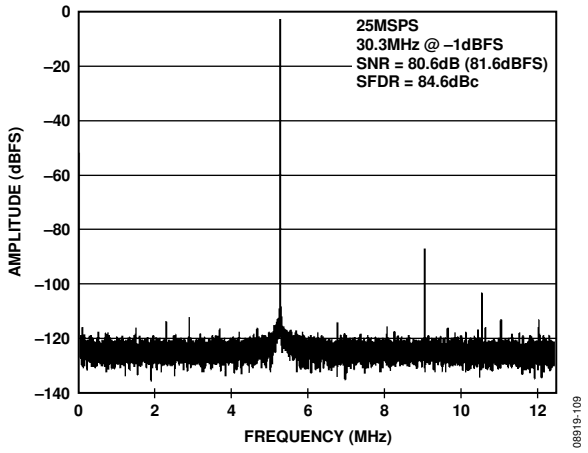


Figure 9. AD9650-25 Single-Tone FFT with f_{IN} = 30.3 MHz

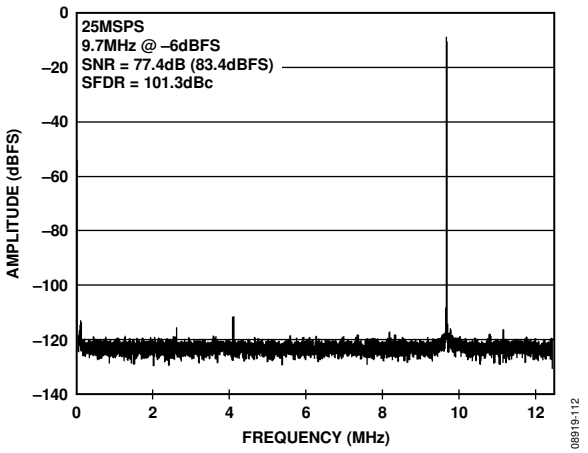


Figure 12. AD9650-25 Single-Tone FFT with f_{IN} = 9.7 MHz at −6 dBFS with Dither Enabled

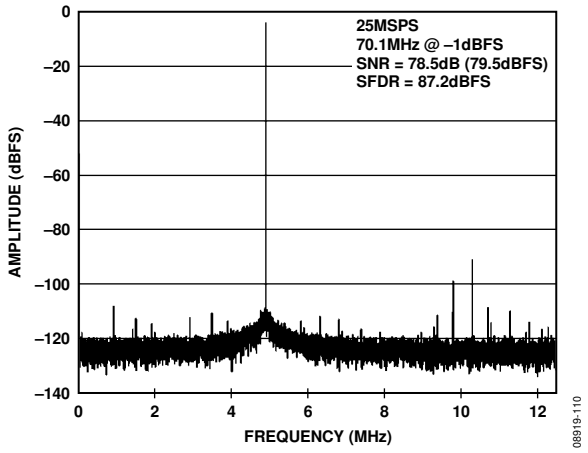


Figure 10. AD9650-25 Single-Tone FFT with f_{IN} = 70.1 MHz

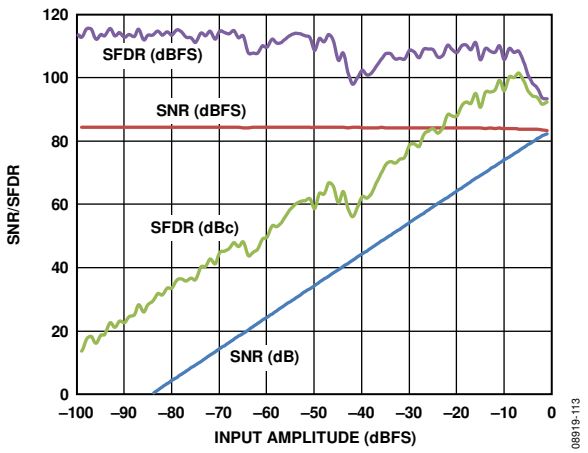


Figure 13. AD9650-25 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 9.7 MHz

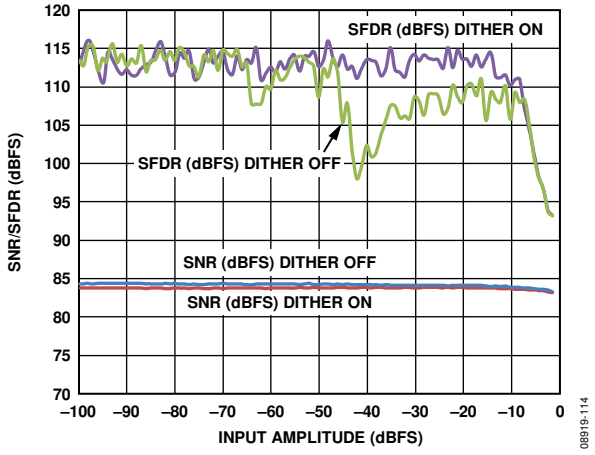


Figure 14. AD9650-25 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 9.7 MHz with and Without Dither Enabled

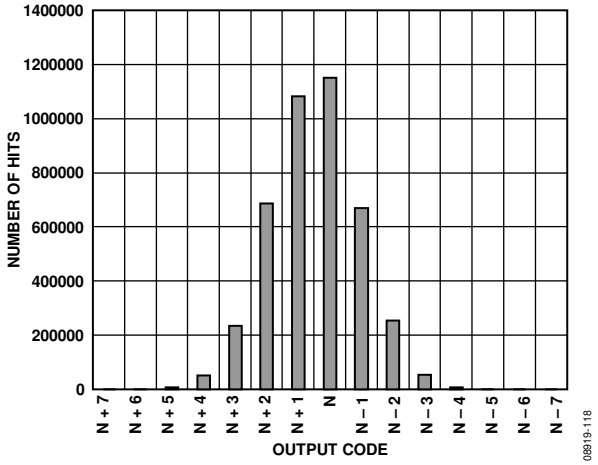


Figure 17. AD9650-25 Grounded Input Histogram

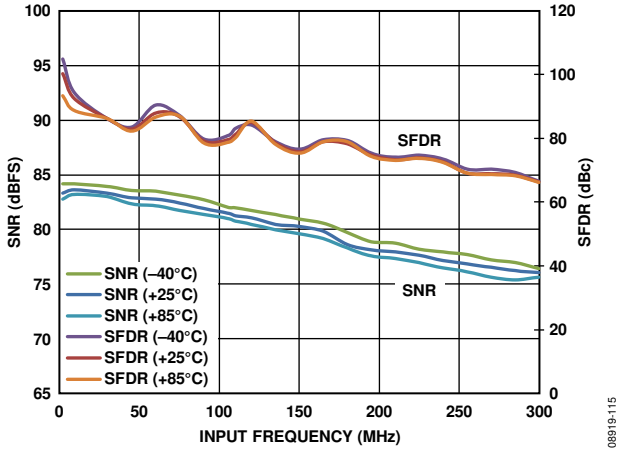


Figure 15. AD9650-25 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) with 2.7 V p-p Full Scale

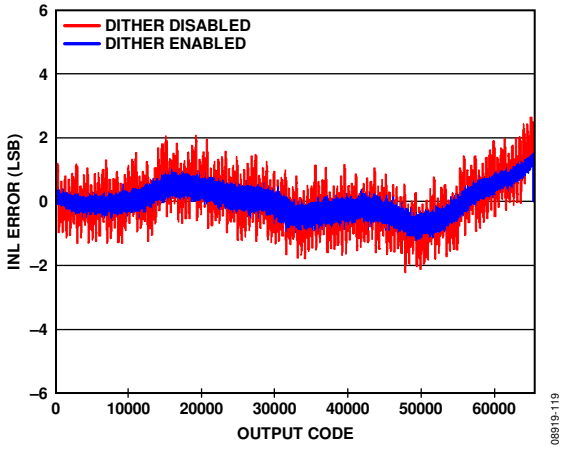


Figure 18. AD9650-25 INL with f_{IN} = 9.7 MHz

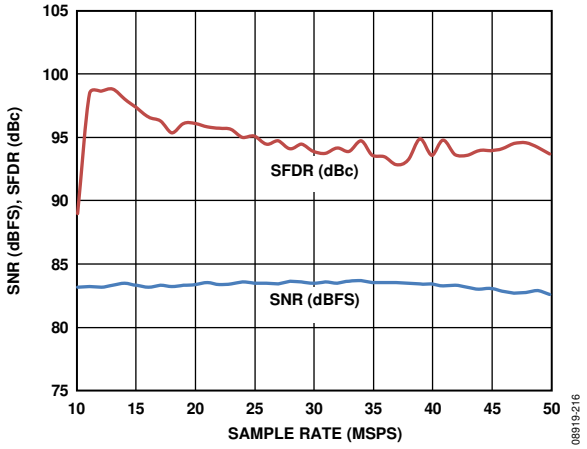


Figure 16. AD9650-25 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 9.7 MHz

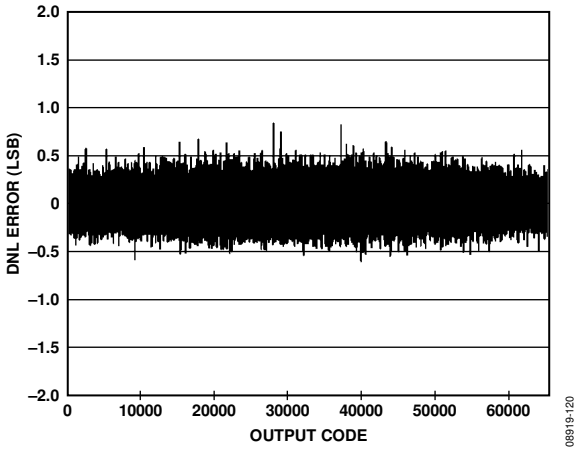


Figure 19. AD9650-25 DNL with f_{IN} = 9.7 MHz

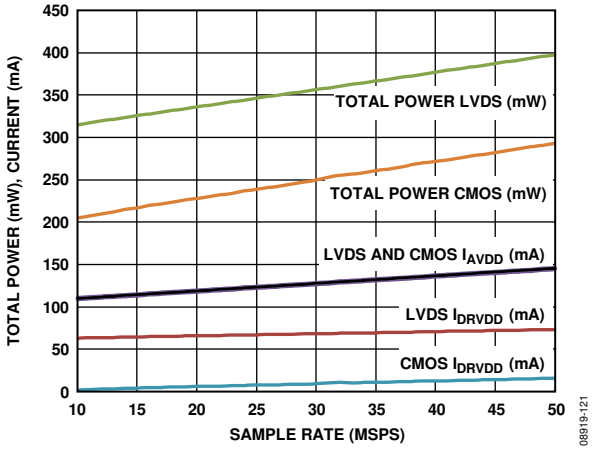


Figure 20. AD9650-25 Power and Current vs. Sample Rate

AD9650-65

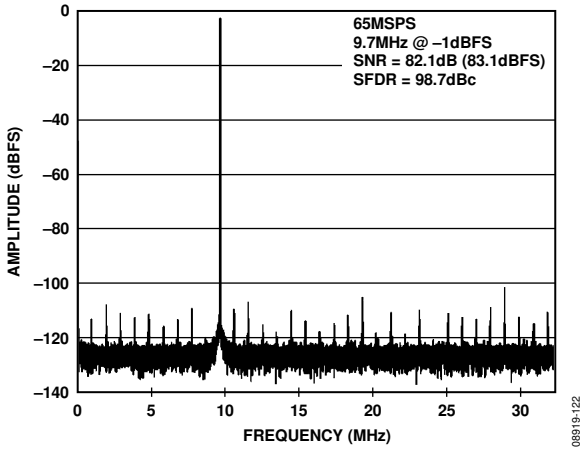


Figure 21. AD9650-65 Single-Tone FFT with f_{IN} = 9.7 MHz

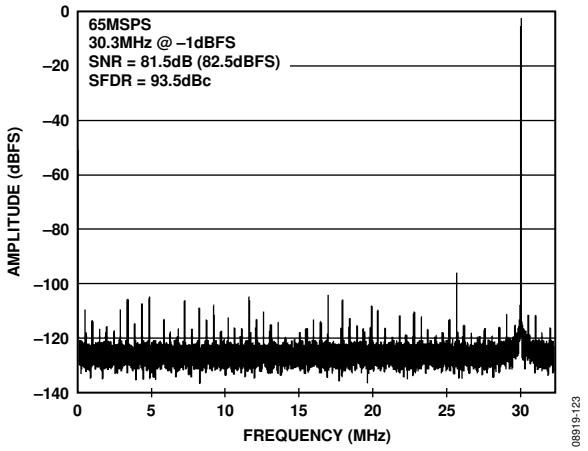


Figure 22. AD9650-65 Single-Tone FFT with f_{IN} = 30.3 MHz

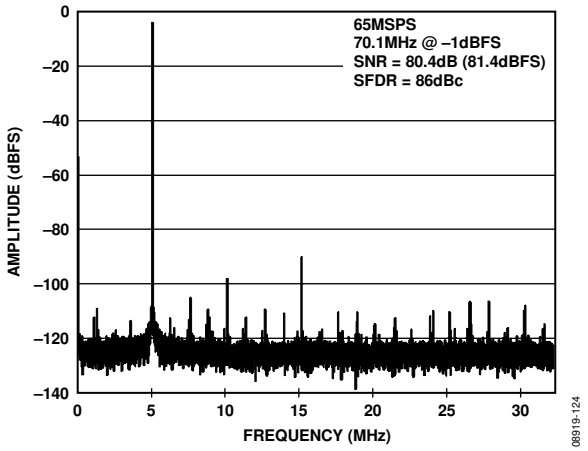


Figure 23. AD9650-65 Single-Tone FFT with f_{IN} = 70.1 MHz

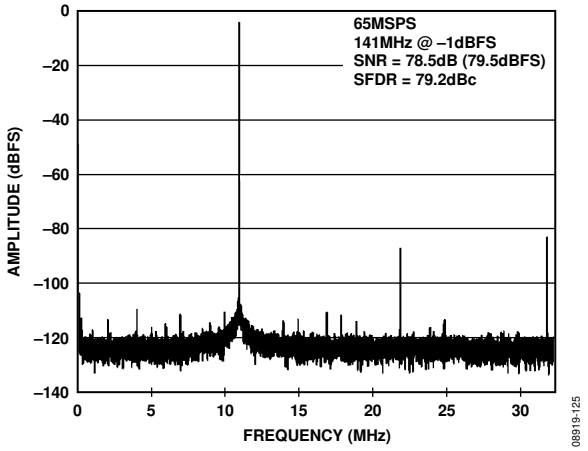


Figure 24. AD9650-65 Single-Tone FFT with f_{IN} = 141 MHz

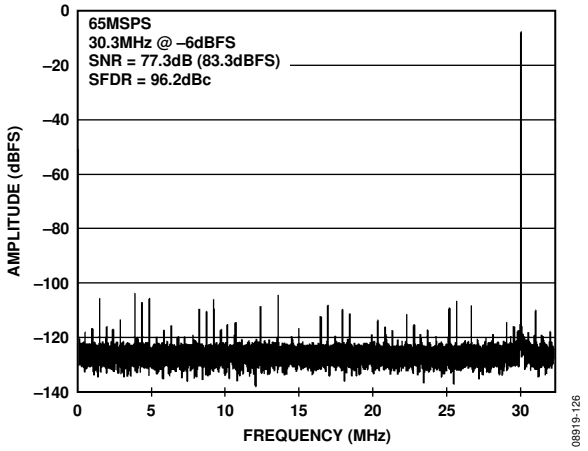


Figure 25. AD9650-65 Single-Tone FFT with f_{IN} = 30.3 MHz at –6 dBFS with Dither Disabled

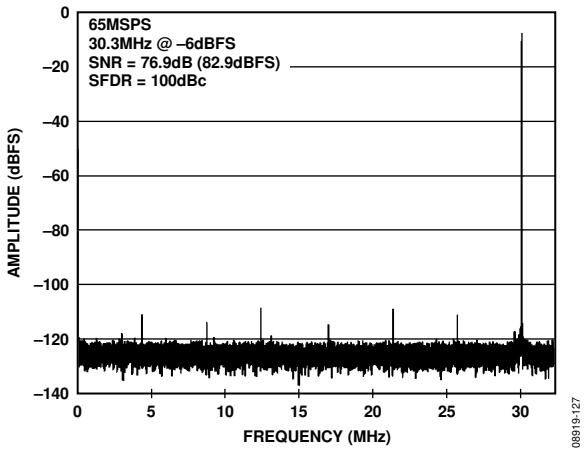


Figure 26. AD9650-65 Single-Tone FFT with f_{IN} = 30.3 MHz @ –6 dBFS with Dither Enabled

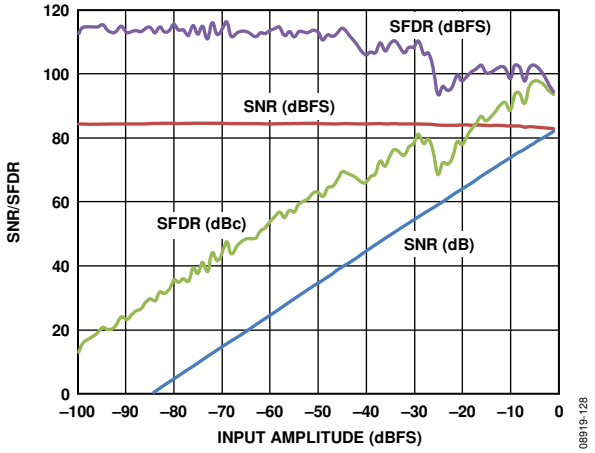


Figure 27. AD9650-65 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} =30.3 MHz

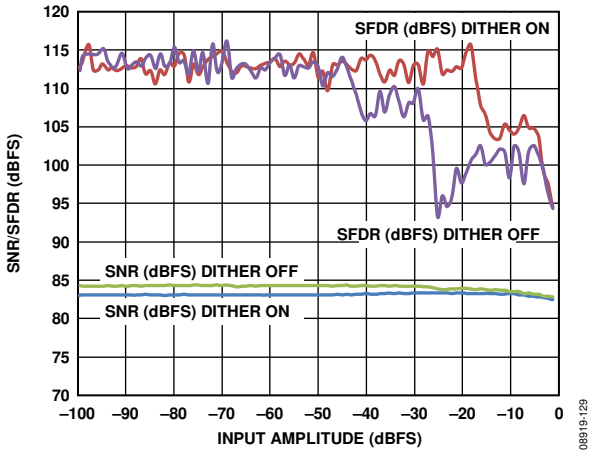


Figure 28. AD9650-65 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 30.3 MHz with and Without Dither Enabled

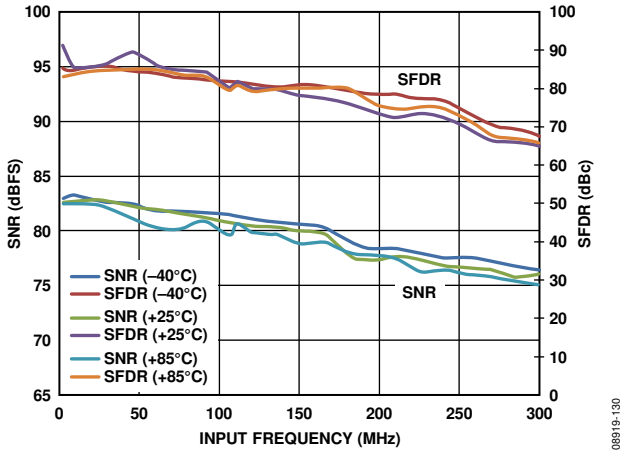


Figure 29. AD9650-65 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) with 2.7 V p-p Full Scale

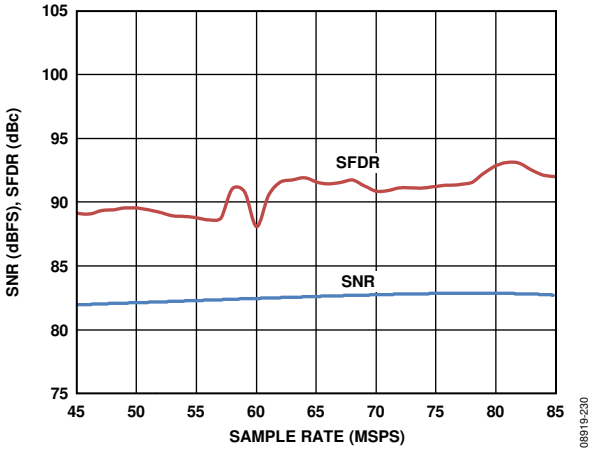


Figure 30. AD9650-65 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 30 MHz

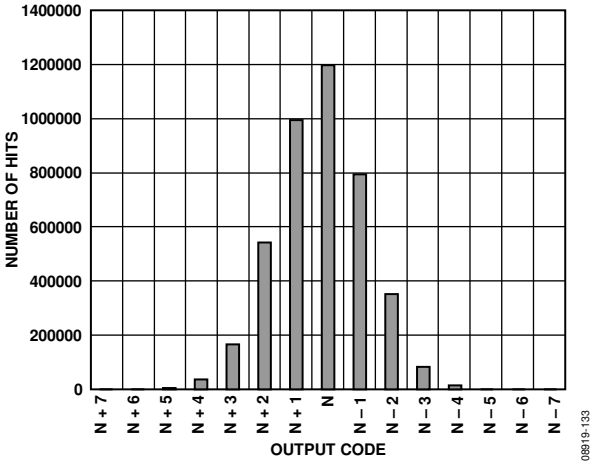


Figure 31. AD9650-65 Grounded Input Histogram

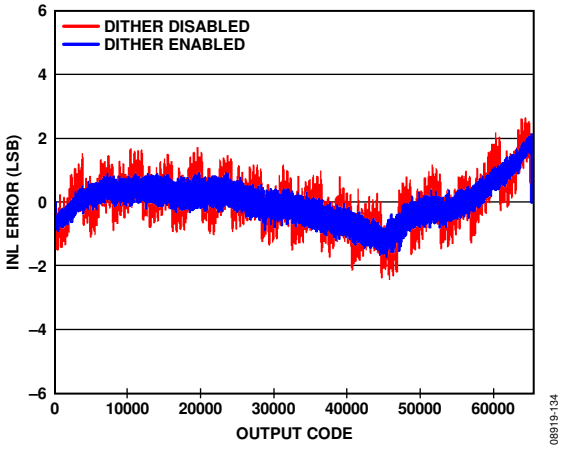


Figure 32. AD9650-65 INL with f_{IN} = 9.7 MHz

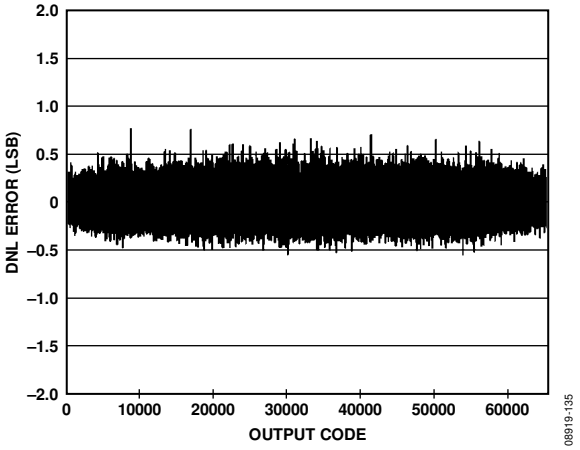


Figure 33. AD9650-65 DNL with f_{IN} = 9.7 MHz

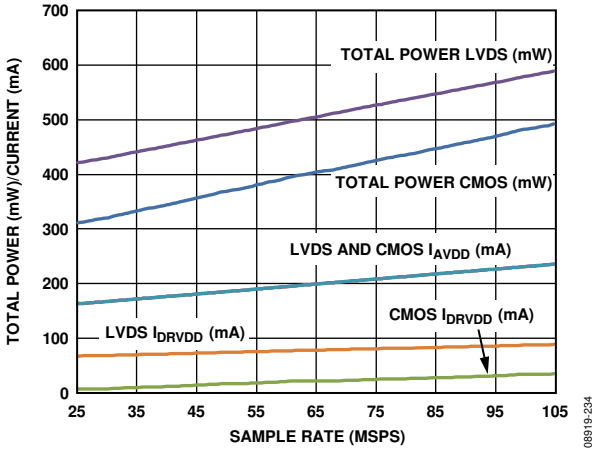


Figure 34. AD9650-65 Power and Current vs. Sample Rate

AD9650-80

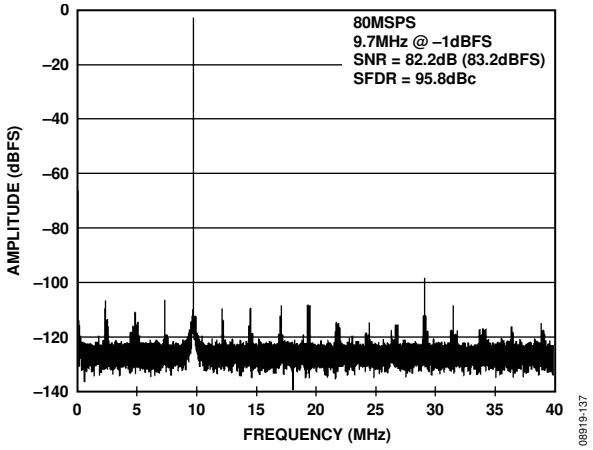


Figure 35. AD9650-80 Single-Tone FFT with f_{IN} = 9.7 MHz

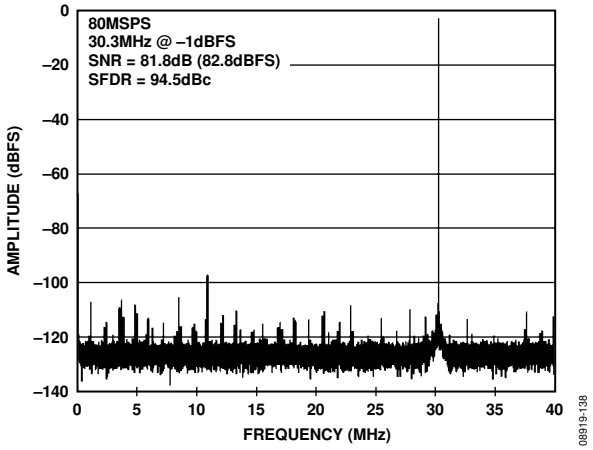


Figure 36. AD9650-80 Single-Tone FFT with f_{IN} = 30.3 MHz

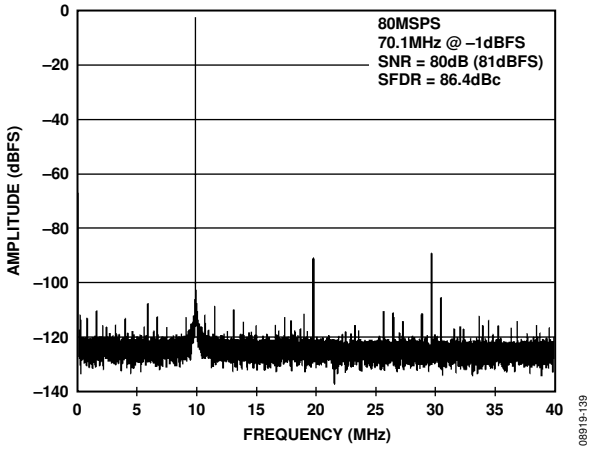


Figure 37. AD9650-80 Single-Tone FFT with f_{IN} = 70.1 MHz

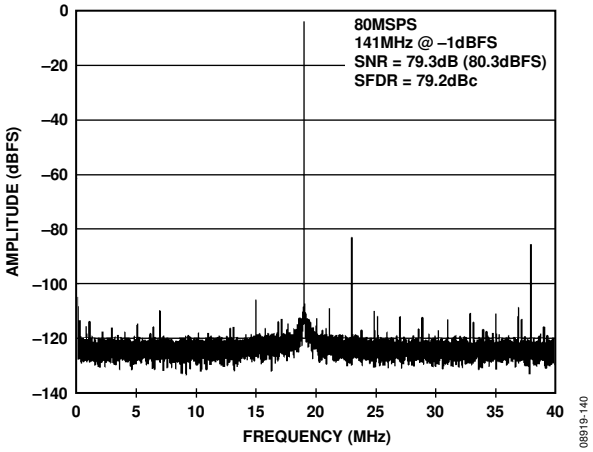


Figure 38. AD9650-80 Single-Tone FFT with f_{IN} = 141 MHz

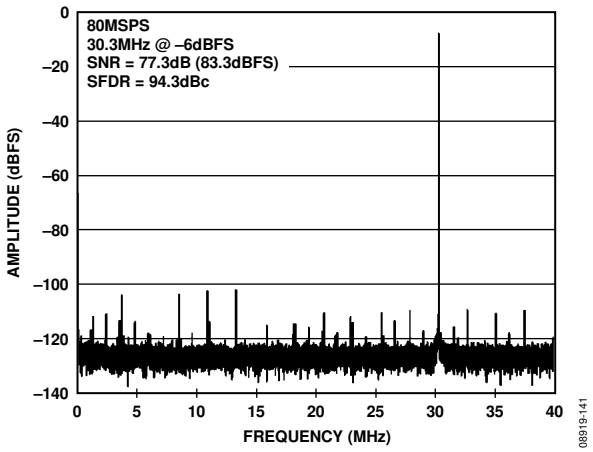


Figure 39. AD9650-80 Single-Tone FFT with f_{IN} = 30.3 MHz at –6 dBFS with Dither Disabled

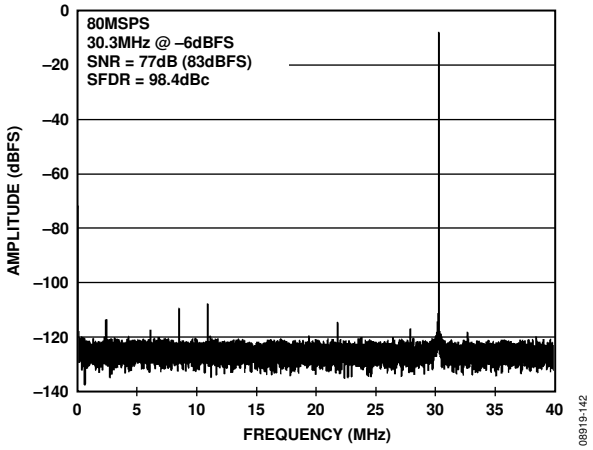


Figure 40. AD9650-80 Single-Tone FFT with f_{IN} = 30.3 MHz at –6 dBFS with Dither Enabled

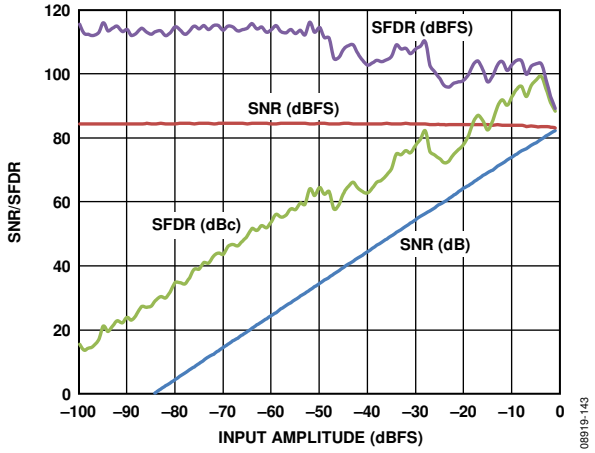


Figure 41. AD9650-80 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 30.3 MHz

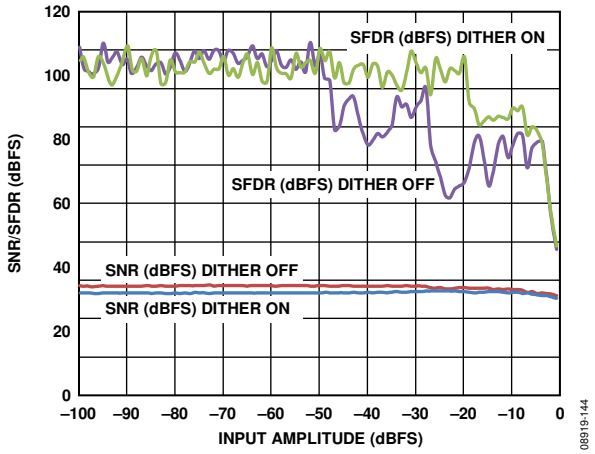


Figure 42. AD9650-80 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 30.3 MHz with and Without Dither Enabled

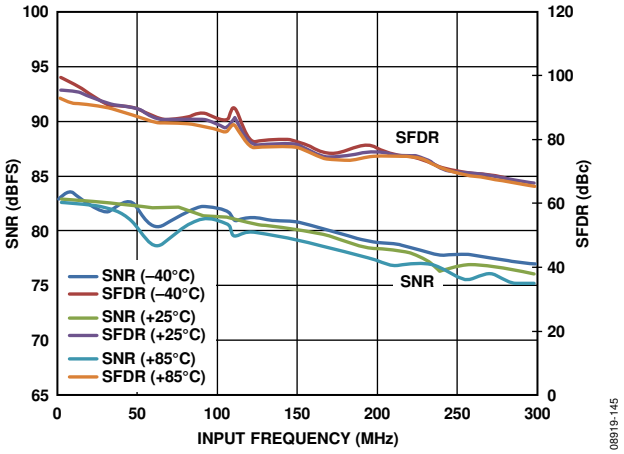


Figure 43. AD9650-80 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN})

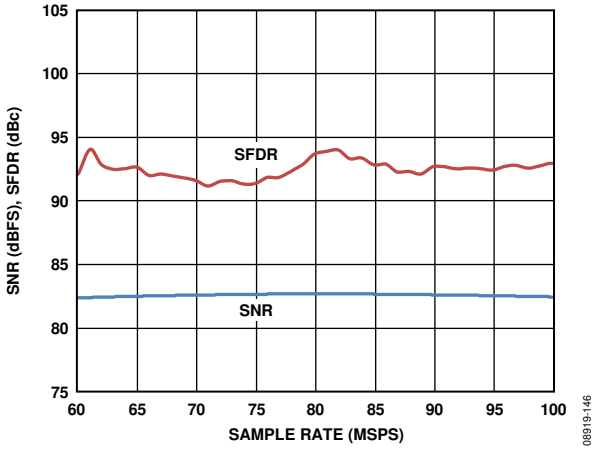


Figure 44. AD9650-80 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 30 MHz

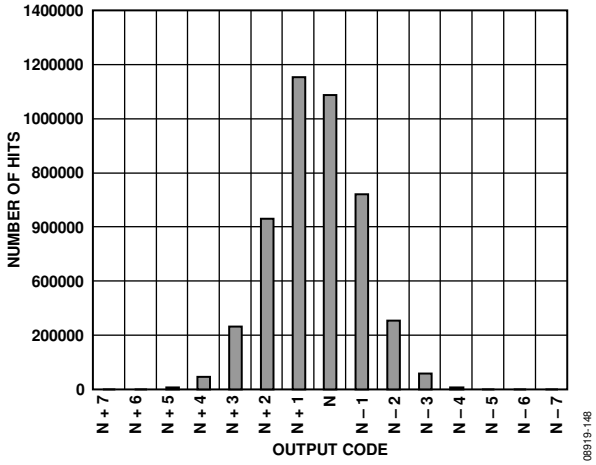


Figure 45. AD9650-80 Grounded Input Histogram

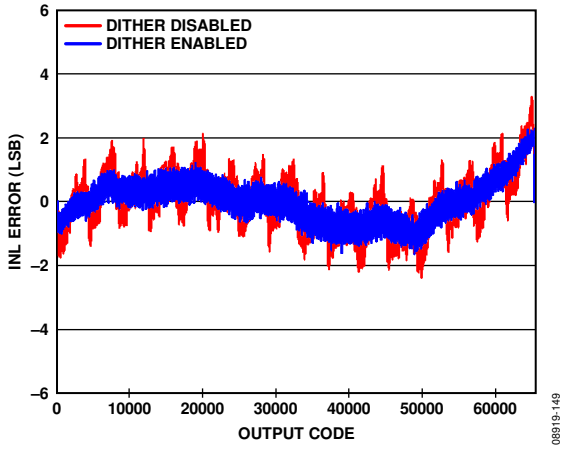


Figure 46. AD9650-80 INL with f_{IN} = 9.7 MHz

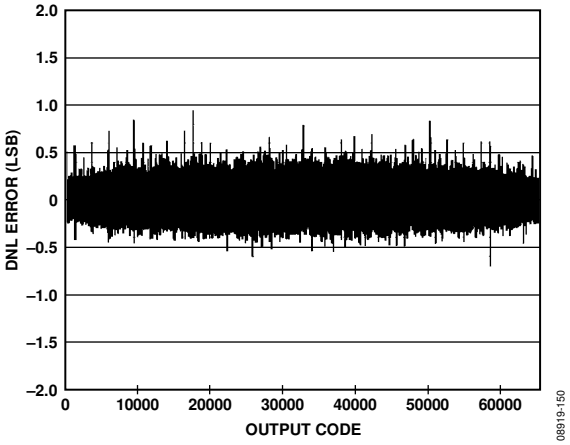


Figure 47. AD9650-80 DNL with f_{IN} = 9.7 MHz

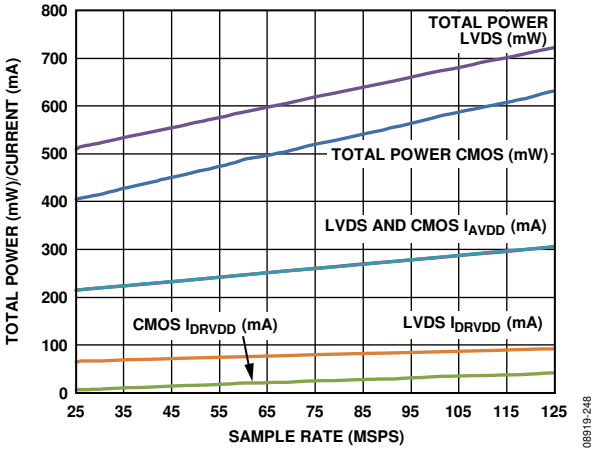


Figure 48. AD9650-80 Power and Current vs. Sample Rate

AD9650-105

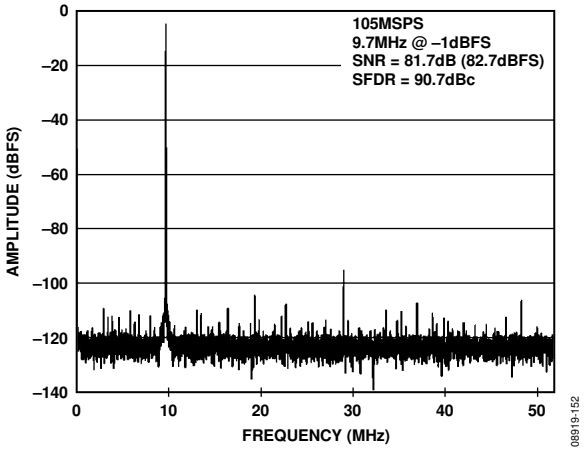


Figure 49. AD9650-105 Single-Tone FFT with f_{IN} = 9.7 MHz

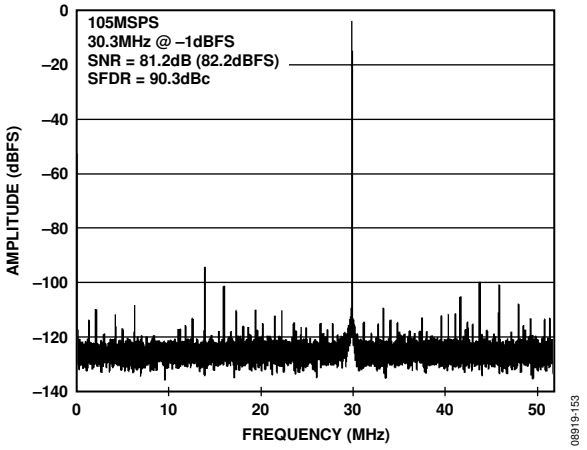


Figure 50. AD9650-105 Single-Tone FFT with f_{IN} = 30.3 MHz

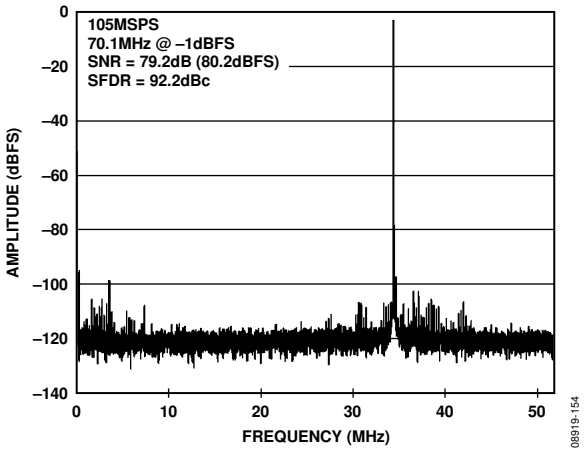


Figure 51. AD9650-105 Single-Tone FFT with f_{IN} = 70.1 MHz

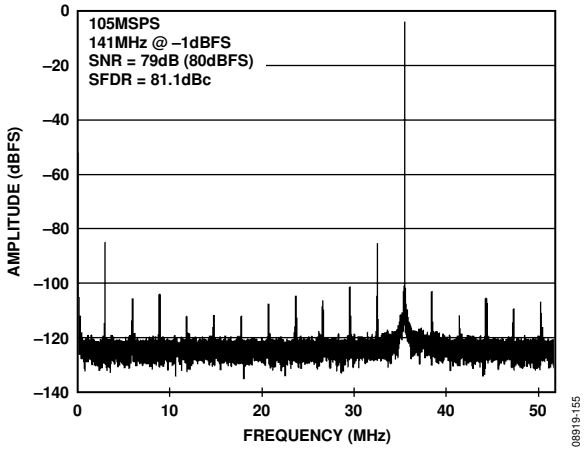


Figure 52. AD9650-105 Single-Tone FFT with f_{IN} = 141 MHz

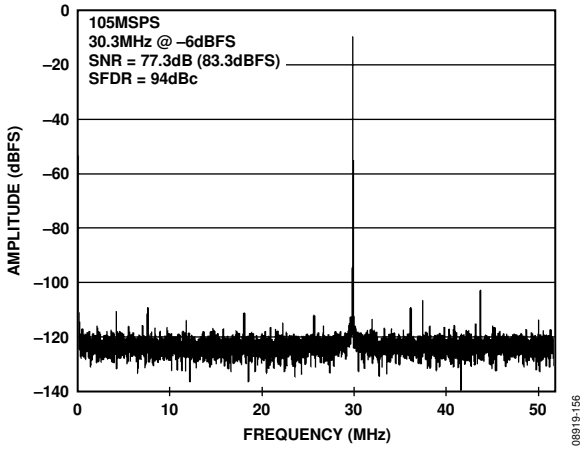


Figure 53. AD9650-105 Single-Tone FFT with f_{IN} = 30.3 MHz @ –6 dBFS with Dither Disabled

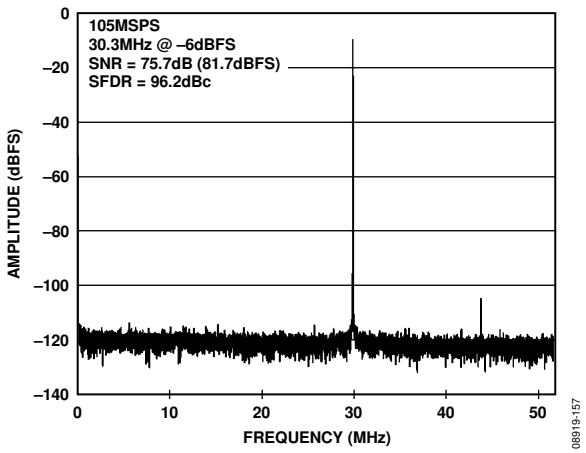


Figure 54. AD9650-105 Single-Tone FFT with f_{IN} = 30.3 MHz @ –6 dBFS with Dither Enabled