Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Quad, 16-Bit, 125 MSPS, Serial LVDS 1.8 V Analog-to-Digital Converter

Data Sheet **AD9653**

FEATURES

- 1.8 V supply operation
- Low power: 164 mW per channel at 125 MSPS
- SNR = 76.5 dBFS at 70 MHz (2.0 V p-p input span)
- SNR = 77.5 dBFS at 70 MHz (2.6 V p-p input span)
- SFDR = 90 dBc (to Nyquist, 2.0 V p-p input span)
- DNL = ±0.7 LSB; INL = ±3.5 LSB (2.0 V p-p input span)
- Serial LVDS (ANSI-644, default) and low power, reduced range option (similar to IEEE 1596.3)
- 650 MHz full power analog bandwidth
- 2 V p-p input voltage range (supports up to 2.6 V p-p)
- Serial port control
  - Full chip and individual channel power-down modes
  - Flexible bit orientation
  - Built-in and custom digital test pattern generation
  - Multichip sync and clock divider
  - Programmable output clock and data alignment
  - Standby mode

APPLICATIONS

- Medical ultrasound and MRI
- High speed imaging
- Quadrature radio receivers
- Diversity radio receivers
- Test equipment

GENERAL DESCRIPTION

The AD9653 is a quad, 16-bit, 125 MSPS analog-to-digital converter (ADC) with an on-chip sample-and-hold circuit designed for low cost, low power, small size, and ease of use. The product operates at a conversion rate of up to 125 MSPS and is optimized for outstanding dynamic performance and low power in applications where a small package size is critical.

The ADC requires a single 1.8 V power supply and LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock output (DCO) for capturing data on the output and a frame clock output (FCO) for signaling a new output byte are provided. Individual channel power-down is supported and typically consumes less than 2 mW when all channels are disabled. The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable output clock and data alignment and digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

The AD9653 is available in a RoHS-compliant, 48-lead LFCSP. It is specified over the industrial temperature range of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

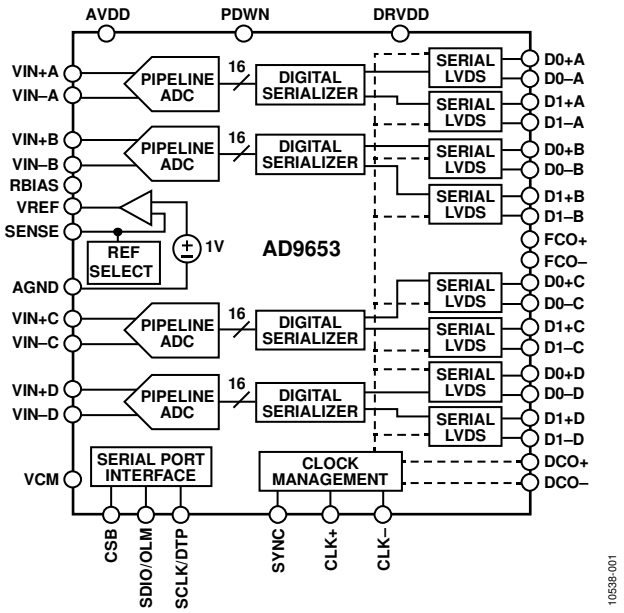


Figure 1.

PRODUCT HIGHLIGHTS

1. Small Footprint.
   Four ADCs are contained in a small, space-saving package.
2. Low power of 164 mW/channel at 125 MSPS with scalable power options.
3. Pin compatible to the AD9253 14-bit quad and the AD9633 12-bit quad ADC.
4. Ease of Use.
   A data clock output (DCO) operates at frequencies of up to 500 MHz and supports double data rate (DDR) operation.
5. User Flexibility.
   The SPI control offers a wide range of flexible features to meet specific system requirements.

Rev. E

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

AD9653* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9653 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD9653: Quad, 16-Bit, 125 MSPS, Serial LVDS 1.8 V Analog-to-Digital Converter Data Sheet

User Guides

- Evaluating the AD9253/AD9633/AD9653 Analog-to-Digital Converters

TOOLS AND SIMULATIONS

- Visual Analog
- AD9653 IBIS Model
- AD9653 Input Impedance

REFERENCE MATERIALS

Press

- Four-channel, 16-bit, 125-MSPS Analog-to-Digital Converter Delivers Superior Dynamic Performance and Industry's Lowest Power and Package-size for its Class.

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

Tutorials

- MT-230: Noise Considerations in High Speed Converter Signal Chains

DESIGN RESOURCES

- AD9653 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9653 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

3/16—Rev. D to Rev. E

Changes to General Description Section 1
Changes to Figure 15 15
Changes to Table 13 29

11/15—Rev. C to Rev. D

Changes to General Description Section 1
Added Note 4, Table 6 8
Changes to Digital Outputs and Timing Section 28

8/15—Rev. B to Rev. C

Change to Applications Section 1
Change to Jitter Considerations Section 25

7/15—Rev. A to Rev. B

Added Patent Note, Note 1 1
Change to Applications Section and General Description Section 1
Change to Effective Number of Bits (ENOB) Parameter, Table 3 5
Changes to Table 5 7
Change to Table 8 11
Changes to Reading the Memory Map Register Table Section and Channel-Specific Registers Section 32
Changes to Table 19 33
Changes to Device Index (Register 0x04, Register 0x05) Section 36
Changes to Clock Stability Considerations Section 38

11/14—Rev. 0 to Rev. A

Changed Output Voltage (1.0 V Mode) from 1.01 V to 1.02 V (max); Table 1 3
Changes to Table 3 5
Added t_{PD} of 1.5 ns (min) and 3.1 ns (max); Table 6 8
Changed t_{SSYNC} from 0.24 ns (typ) to 1.2 ns (min) and Changed t_{HSYNC} from 0.40 ns (typ) to −0.2 ns (min); Table 7 9
Changes to Table 10 12
Changes to Clock Input Options Section 24
Changes to Digital Outputs and Timing Section 27
Changes to Table 13 28
Changes to Table 14 29
Changes to Channel-Specific Registers Section 32
Changes to Register 0x14 Bit 1 and Default Value 34
Changes to Register 0x16; Bits[6:4]—Input Clock Phase Adjust Section and Sample Rate Override (Register 0x100) Section 37
Added Clock Stability Considerations Section 38

5/12—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2.0 V p-p full-scale differential input at −1.0 dBFS; V_{REF} = 1.0 V, DCS off, unless otherwise noted.

Table 1.

Parameter[1]	Temperature	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	−0.49	−0.3	0.17	% FSR
Offset Matching	Full	−0.14	+0.2	0.39	% FSR
Gain Error	Full	−12.3	−5	2.37	% FSR
Gain Matching	Full	1.0	1.1	5.8	% FSR
Differential Nonlinearity (DNL)	Full	−0.77		0.95	LSB
	25°C		±0.7		LSB
Integral Nonlinearity (INL)	Full	−7.26		8.18	LSB
	25°C		±3.5		LSB
TEMPERATURE DRIFT					
Offset Error	Full		3.5		ppm/°C
INTERNAL VOLTAGE REFERENCE					
Output Voltage (1.0 V Mode)	Full	0.98	1.0	1.02	V
Load Regulation at 1.0 mA (V_{REF} = 1.0 V)	Full		2		mV
Input Resistance	25°C		7.5		kΩ
INPUT-REFERRED NOISE					
V_{REF} = 1.0 V	25°C		2.7		LSB rms
ANALOG INPUTS					
Differential Input Voltage (V_{REF} = 1.0 V)	Full		2		V p-p
Common-Mode Voltage	Full		0.9		V
Common-Mode Range	25°C	0.5		1.3	V
Differential Input Resistance	25°C		2.6		kΩ
Differential Input Capacitance	25°C		7		pF
POWER SUPPLY					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
I_{AVDD}[2]	Full		305	330	mA
I_{DRVDD} (ANSI-644 Mode)[2]	Full		60	64	mA
I_{DRVDD} (Reduced Range Mode)[2]	25°C		45		mA
TOTAL POWER CONSUMPTION					
DC Input	Full		607	649	mW
Sine Wave Input (Four Channels Including Output Drivers, ANSI-644 Mode)	Full		657	708	mW
Sine Wave Input (Four Channels Including Output Drivers, Reduced Range Mode)	25°C		630		mW
Power-Down	25°C		2		mW
Standby[3]	Full		356	392	mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Measured with a low input frequency, full-scale sine wave on all four channels.
[3] Can be controlled via the SPI.

AVDD = 1.8 V, DRVDD = 1.8 V, 2.6 V p-p full-scale differential input at −1.0 dBFS; V_{REF} = 1.3 V; 0°C to 85°C, DCS off, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ACCURACY					
No Missing Codes	25°C		Guaranteed		
Offset Error	25°C		−0.3		% FSR
Offset Matching	25°C		+0.2		% FSR
Gain Error	25°C		−5		% FSR
Gain Matching	25°C		1.1		% FSR
Differential Nonlinearity (DNL)	25°C		±0.8		LSB
Integral Nonlinearity (INL)	25°C		±5.0		LSB
TEMPERATURE DRIFT					
Offset Error	25°C		3.5		ppm/°C
INTERNAL VOLTAGE REFERENCE					
Output Voltage (1.3 V Programmable Mode)	25°C		1.3		V
Load Regulation at 1.0 mA (V_{REF} = 1.3 V)	25°C		6.5		mV
Input Resistance	25°C		7.5		kΩ
INPUT-REFERRED NOISE					
V_{REF} = 1.3 V	25°C		2.1		LSB rms
ANALOG INPUTS					
Differential Input Voltage (V_{REF} = 1.3 V)	25°C		2.6		V p-p
Common-Mode Voltage	25°C		0.9		V
Common-Mode Range	25°C	0.6		1.3	V
Differential Input Resistance	25°C		2.6		kΩ
Differential Input Capacitance	25°C		7		pF
POWER SUPPLY					
AVDD	25°C		1.8		V
DRVDD	25°C		1.8		V
I_{AVDD}[2]	25°C		314		mA
I_{DRVDD} (ANSI-644 Mode)[2]	25°C		60		mA
I_{DRVDD} (Reduced Range Mode)[2]	25°C		45		mA
TOTAL POWER CONSUMPTION					
DC Input	25°C		614		mW
Sine Wave Input (Four Channels Including Output Drivers, ANSI-644 Mode)	25°C		673		mW
Sine Wave Input (Four Channels Including Output Drivers, Reduced Range Mode)	25°C		646		mW
Power-Down	25°C		2		mW
Standby[3]	25°C		371		mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Measured with a low input frequency, full-scale sine wave on all four channels.
[3] Can be controlled via the SPI.

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2.0 V p-p full-scale differential input at −1.0 dBFS; V_{REF} = 1.0 V, DCS off, unless otherwise noted.

Table 3.

Parameter[1]	Temperature	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 9.7 MHz	25°C		78		dBFS
f_{IN} = 15 MHz	25°C		77.8		dBFS
f_{IN} = 70 MHz	Full	75.5	76.5		dBFS
f_{IN} = 128 MHz	25°C		73.9		dBFS
f_{IN} = 200 MHz	25°C		71.5		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)					
f_{IN} = 9.7 MHz	25°C		78		dBFS
f_{IN} = 15 MHz	25°C		77.7		dBFS
f_{IN} = 70 MHz	Full	74.6	76.1		dBFS
f_{IN} = 128 MHz	25°C		73.6		dBFS
f_{IN} = 200 MHz	25°C		70.3		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 9.7 MHz	25°C		12.7		Bits
f_{IN} = 15 MHz	25°C		12.6		Bits
f_{IN} = 70 MHz	Full	12.1	12.3		Bits
f_{IN} = 128 MHz	25°C		11.9		Bits
f_{IN} = 200 MHz	25°C		11.4		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 9.7 MHz	25°C		96		dBc
f_{IN} = 15 MHz	25°C		93		dBc
f_{IN} = 70 MHz	Full	78	89		dBc
f_{IN} = 128 MHz	25°C		87		dBc
f_{IN} = 200 MHz	25°C		77		dBc
WORST HARMONIC (SECOND OR THIRD)					
f_{IN} = 9.7 MHz	25°C		−98		dBc
f_{IN} = 15 MHz	25°C		−93		dBc
f_{IN} = 70 MHz	Full		−89	−78	dBc
f_{IN} = 128 MHz	25°C		−87		dBc
f_{IN} = 200 MHz	25°C		−77		dBc
WORST OTHER HARMONIC OR SPUR					
f_{IN} = 9.7 MHz	25°C		−96		dBc
f_{IN} = 15 MHz	25°C		−98		dBc
f_{IN} = 70 MHz	Full		−94	−85	dBc
f_{IN} = 128 MHz	25°C		−89		dBc
f_{IN} = 200 MHz	25°C		−83		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)—AIN1 AND AIN2 = −7.0 dBFS					
f_{IN1} = 70.5 MHz, f_{IN2} = 72.5 MHz	25°C		−90		dBc
CROSSTALK[2]	25°C		−91		dB
CROSSTALK (OVERRANGE CONDITION)[3]	25°C		−87		dB
POWER SUPPLY REJECTION RATIO (PSRR)[4]					
AVDD	25°C		31		dB
DRVDD	25°C		79		dB
ANALOG INPUT BANDWIDTH, FULL POWER	25°C		650		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Crosstalk is measured at 70 MHz with −1.0 dBFS analog input on one channel and no input on the adjacent channel.
[3] Overrange condition is defined as the input being 3 dB above full scale.
[4] PSRR is measured by injecting a sinusoidal signal at 10 MHz to the power supply pin and measuring the output spur on the FFT. PSRR is calculated as the ratio of the amplitudes of the spur voltage over the pin voltage, expressed in decibels.

AVDD = 1.8 V, DRVDD = 1.8 V, 2.6 V p-p full-scale differential input at −1.0 dBFS; V_{REF} = 1.3 V; 0°C to 85°C, DCS off, unless otherwise noted.

Table 4.

Parameter[1]	Temperature	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 9.7 MHz	25°C		80		dBFS
f_{IN} = 15 MHz	25°C		79.4		dBFS
f_{IN} = 70 MHz	25°C		77.5		dBFS
f_{IN} = 128 MHz	25°C		74.4		dBFS
f_{IN} = 200 MHz	25°C		71.7		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)					
f_{IN} = 9.7 MHz	25°C		79.8		dBFS
f_{IN} = 15 MHz	25°C		79.2		dBFS
f_{IN} = 70 MHz	25°C		76.1		dBFS
f_{IN} = 128 MHz	25°C		74		dBFS
f_{IN} = 200 MHz	25°C		69.9		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 9.7 MHz	25°C		13		Bits
f_{IN} = 15 MHz	25°C		12.9		Bits
f_{IN} = 70 MHz	25°C		12.3		Bits
f_{IN} = 128 MHz	25°C		12		Bits
f_{IN} = 200 MHz	25°C		11.3		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 9.7 MHz	25°C		94		dBc
f_{IN} = 15 MHz	25°C		94		dBc
f_{IN} = 70 MHz	25°C		82		dBc
f_{IN} = 128 MHz	25°C		86		dBc
f_{IN} = 200 MHz	25°C		75		dBc
WORST HARMONIC (SECOND OR THIRD)					
f_{IN} = 9.7 MHz	25°C		−94		dBc
f_{IN} = 15 MHz	25°C		−94		dBc
f_{IN} = 70 MHz	25°C		−82		dBc
f_{IN} = 128 MHz	25°C		−87		dBc
f_{IN} = 200 MHz	25°C		−75		dBc
WORST OTHER HARMONIC OR SPUR					
f_{IN} = 9.7 MHz	25°C		−100		dBc
f_{IN} = 15 MHz	25°C		−99		dBc
f_{IN} = 70 MHz	25°C		−96		dBc
f_{IN} = 128 MHz	25°C		−86		dBc
f_{IN} = 200 MHz	25°C		−84		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)—AIN1 AND AIN2 = −7.0 dBFS					
f_{IN1} = 70.5 MHz, f_{IN2} = 72.5 MHz	25°C		−90		dBc
CROSSTALK[2]	25°C		91		dB
CROSSTALK (OVERRANGE CONDITION)[3]	25°C		87		dB
POWER SUPPLY REJECTION RATIO (PSRR)[4]					
AVDD	25°C		31		dB
DRVDD	25°C		79		dB
ANALOG INPUT BANDWIDTH, FULL POWER	25°C		650		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Crosstalk is measured at 70 MHz with −1.0 dBFS analog input on one channel and no input on the adjacent channel.
[3] Overrange condition is defined as the input being 3 dB above full scale.
[4] PSRR is measured by injecting a sinusoidal signal at 10 MHz to the power supply pin and measuring the output spur on the FFT. PSRR is calculated as the ratio of the amplitudes of the spur voltage over the pin voltage, expressed in decibels.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, unless otherwise noted.

Table 5.

Parameter[1]	Temp	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK–)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	0.2		3.6	V p-p
Input Voltage Range	Full	AGND − 0.2		AVDD + 0.2	V
Input Common-Mode Voltage	Full		0.9		V
Input Resistance (Differential)	25°C		15		kΩ
Input Capacitance	25°C		4		pF
LOGIC INPUTS (PDWN, SYNC, SCLK)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		2		pF
LOGIC INPUT (CSB)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		2		pF
LOGIC INPUT (SDIO)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		5		pF
LOGIC OUTPUT (SDIO)[3]					
Logic 1 Voltage (I_{OH} = 800 µA)	Full		1.79		V
Logic 0 Voltage (I_{OL} = 50 µA)	Full			0.05	V
DIGITAL OUTPUTS (D0±x, D1±x), ANSI-644					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	±290	±345	±400	mV
Output Offset Voltage (V_{OS})	Full	1.15	1.25	1.35	V
Output Coding (Default)			Twos complement		
DIGITAL OUTPUTS (D0±x, D1±x), LOW POWER, REDUCED SIGNAL OPTION					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	±160	±200	±230	mV
Output Offset Voltage (V_{OS})	Full	1.15	1.25	1.35	V
Output Coding (Default)			Twos complement		

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] This is specified for LVDS and LVPECL only.
[3] This is specified for 13 SDIO/OLM pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, unless otherwise noted.

Table 6.

Parameter[1, 2]	Temp	Min	Typ	Max	Unit
CLOCK[3]					
Input Clock Rate	Full	20		1000	MHz
Conversion Rate[4]	Full	20		125	MSPS
Clock Pulse Width High (t_{EH})	Full		4.00		ns
Clock Pulse Width Low (t_{EL})	Full		4.00		ns
OUTPUT PARAMETERS[3]					
Propagation Delay (t_{PD})	Full	1.5	2.3	3.1	ns
Rise Time (t_R) (20% to 80%)	Full		300		ps
Fall Time (t_F) (20% to 80%)	Full		300		ps
FCO Propagation Delay (t_{FCO})	Full	1.5	2.3	3.1	ns
DCO Propagation Delay (t_{CPD})[5]	Full		t_{FCO} + (t_{SAMPLE}/16)		ns
DCO to Data Delay (t_{DATA})[5]	Full	(t_{SAMPLE}/16) − 300	(t_{SAMPLE}/16)	(t_{SAMPLE}/16) + 300	ps
DCO to FCO Delay (t_{FRAME})[5]	Full	(t_{SAMPLE}/16) − 300	(t_{SAMPLE}/16)	(t_{SAMPLE}/16) + 300	ps
Lane Delay (t_{LD})			90		ps
Data to Data Skew ($t_{DATA-MAX}$ − $t_{DATA-MIN}$)	Full		±50	±200	ps
Wake-Up Time (Standby)	25°C		250		ns
Wake-Up Time (Power-Down)[6]	25°C		375		µs
Pipeline Latency	Full		16		Clock cycles
APERTURE					
Aperture Delay (t_A)	25°C		1		ns
Aperture Uncertainty (Jitter, t_J)	25°C		135		fs rms
Out-of-Range Recovery Time	25°C		1		Clock cycles

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Measured on standard FR-4 material.
[3] Can be adjusted via the SPI. The conversion rate is the clock rate after the divider.
[4] The maximum conversion rate is based on two-lane output mode. See the Digital Outputs and Timing section for the maximum conversion rate in one-lane output mode.
[5] t_{SAMPLE}/16 is based on the number of bits in two LVDS data lanes. $t_{SAMPLE} = 1/f_S$.
[6] Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 7.

Parameter	Description	Limit	Unit
SYNC TIMING REQUIREMENTS			
t_{SSYNC}	SYNC to rising edge of CLK+ setup time	1.2	ns min
t_{HSYNC}	SYNC to rising edge of CLK+ hold time	−0.2	ns min
SPI TIMING REQUIREMENTS	See Figure 75		
t_{DS}	Setup time between the data and the rising edge of SCLK	2	ns min
t_{DH}	Hold time between the data and the rising edge of SCLK	2	ns min
t_{CLK}	Period of the SCLK	40	ns min
t_S	Setup time between CSB and SCLK	2	ns min
t_H	Hold time between CSB and SCLK	2	ns min
t_{HIGH}	SCLK pulse width high	10	ns min
t_{LOW}	SCLK pulse width low	10	ns min
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 75)	10	ns min
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 75)	10	ns min

Timing Diagrams

Refer to the Memory Map Register Descriptions section and Table 23 for SPI register settings.

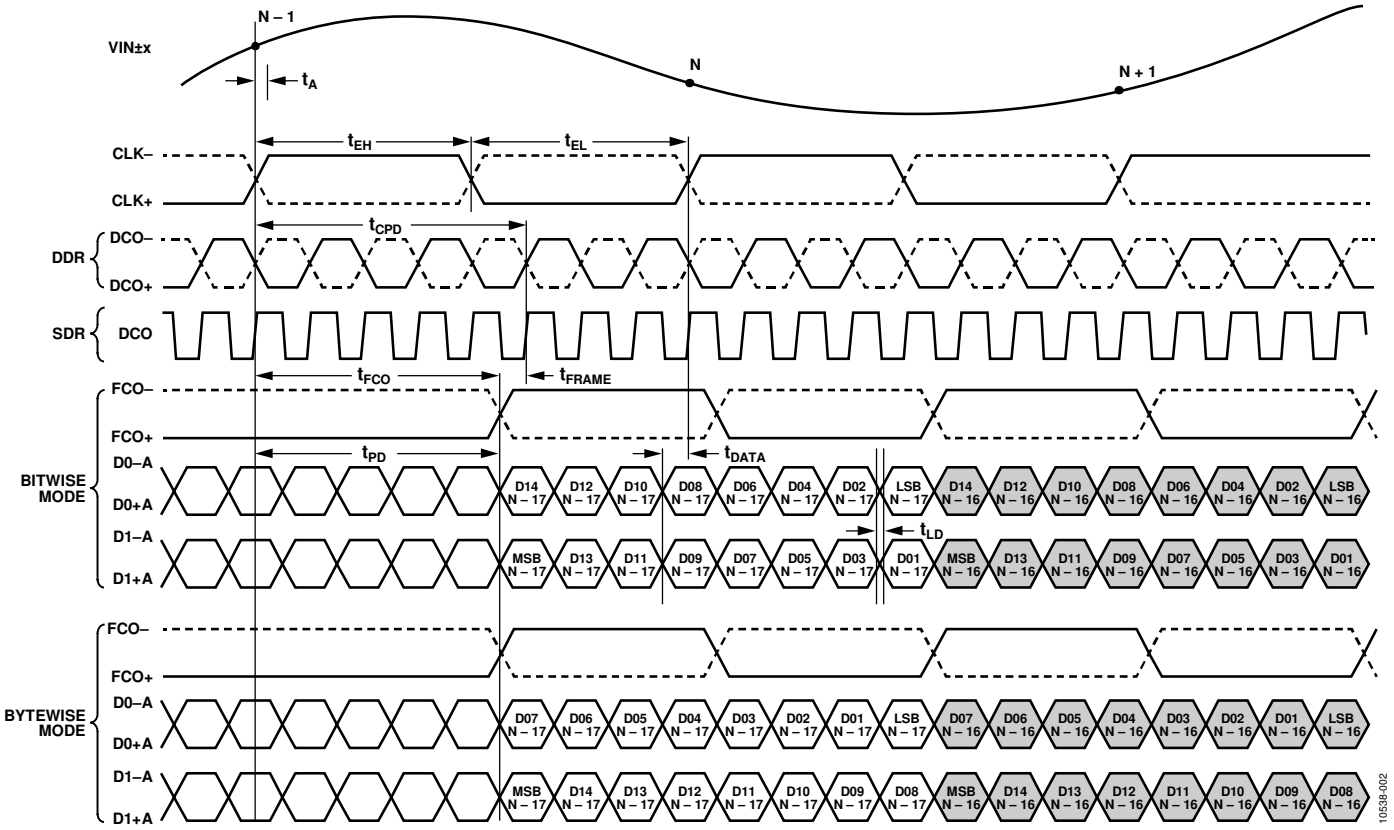


Figure 2. 16-Bit DDR/SDR, Two-Lane, 1× Frame Mode (Default)

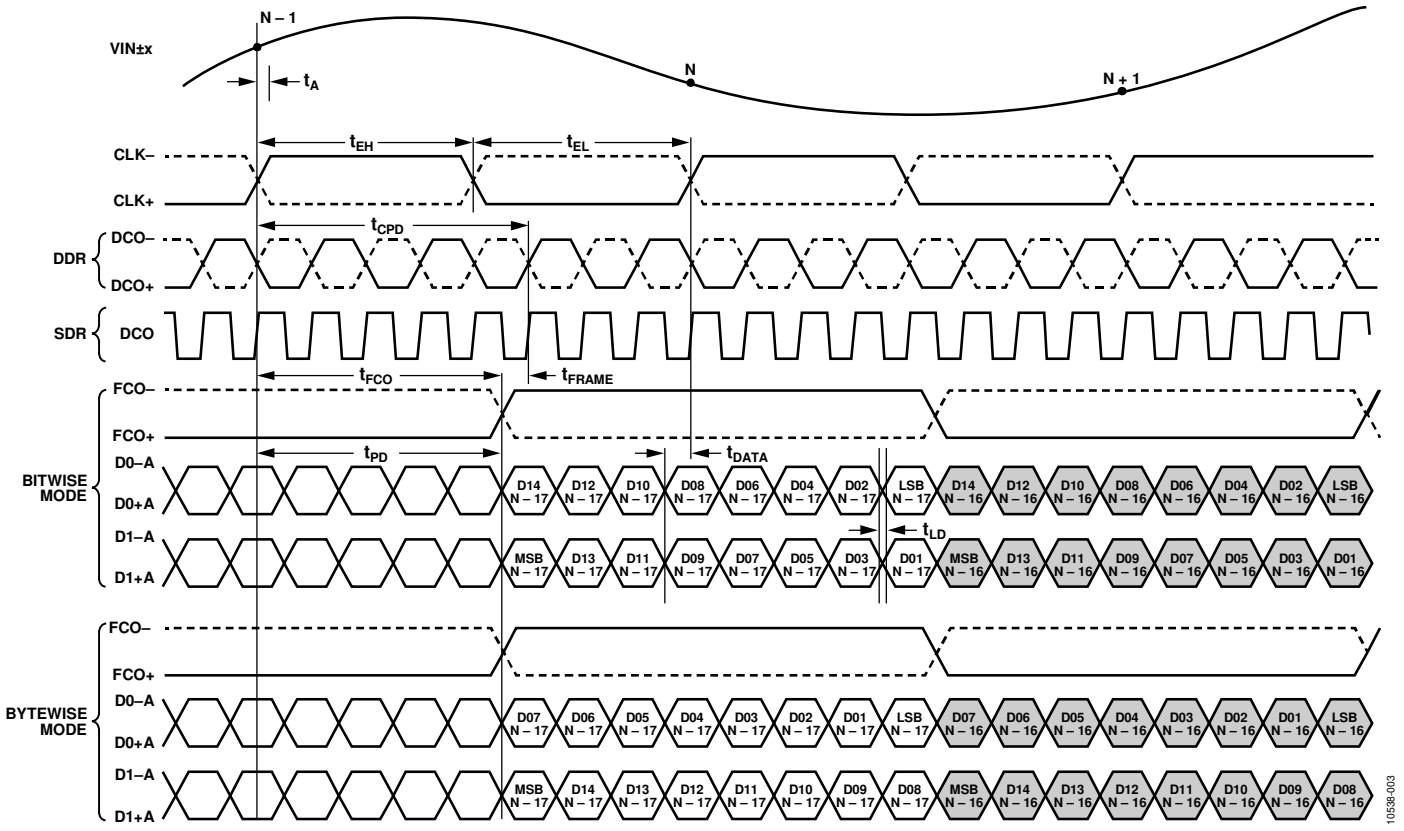


Figure 3. 16-Bit DDR/SDR, Two-Lane, 2× Frame Mode

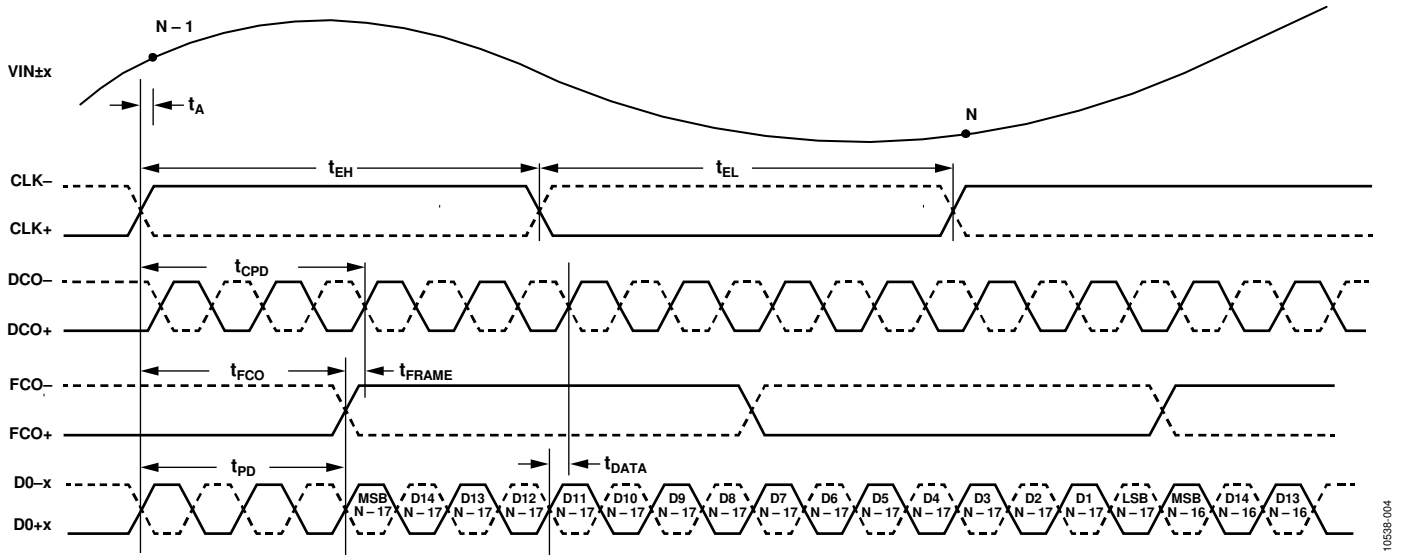


Figure 4. Wordwise DDR, One-Lane, 1× Frame, 16-Bit Output Mode

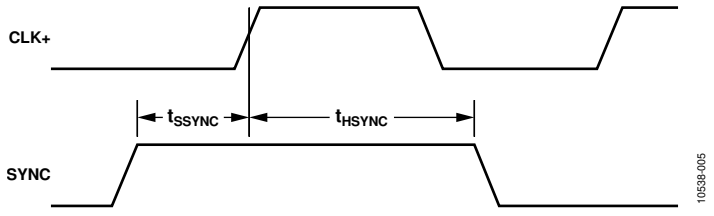


Figure 5. SYNC Input Timing Requirements

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
Digital Outputs (D0±x, D1±x, DCO+, DCO−, FCO+, FCO−) to AGND	−0.3 V to +2.0 V
CLK+, CLK− to AGND	−0.3 V to +2.0 V
VIN+x, VIN−x to AGND	−0.3 V to +2.0 V
SCLK/DTP, SDIO/OLM, CSB to AGND	−0.3 V to +2.0 V
SYNC, PDWN to AGND	−0.3 V to +2.0 V
RBIAS, VCM to AGND	−0.3 V to +2.0 V
VREF, SENSE to AGND	−0.3 V to +2.0 V
Environmental	
Operating Temperature Range (Ambient, V_{REF} = 1.0 V)	−40°C to +85°C
Operating Temperature Range (Ambient, V_{REF} = 1.3 V)	0°C to 85°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 9. Thermal Resistance

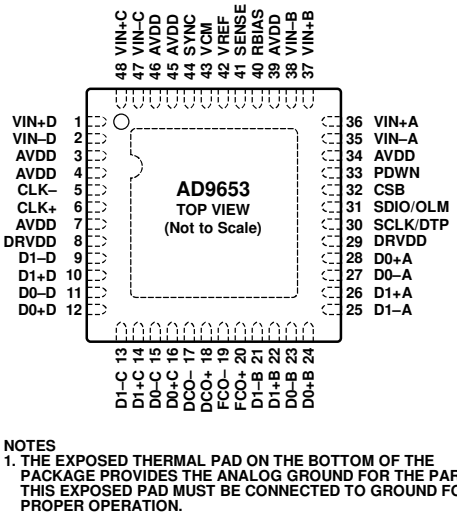
Package Type	Air Flow Velocity (m/sec)	θ_{JA}[1]	θ_{JB}	θ_{JC}	Unit
48-Lead LFCSP	0.0	23.7	7.8	7.1	°C/W
7 mm × 7 mm	1.0	20.0	N/A[2]	N/A[2]	°C/W
(CP-48-13)	2.5	18.7	N/A[2]	N/A[2]	°C/W

[1] θ_{JA} for a 4-layer PCB with solid ground plane (simulated). Exposed pad soldered to PCB.
[2] N/A means not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE PART. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

10538-006

Figure 6. 48-Lead LFCSP Pin Configuration, Top View

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	AGND, Exposed Pad	Analog Ground, Exposed Pad. The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
1	VIN+D	ADC D Analog Input True.
2	VIN−D	ADC D Analog Input Complement.
3, 4, 7, 34, 39, 45, 46	AVDD	1.8 V Analog Supply Pins.
5, 6	CLK−, CLK+	Differential Encode Clock. PECL, LVDS, or 1.8 V CMOS inputs.
8, 29	DRVDD	Digital Output Driver Supply.
9, 10	D1−D, D1+D	Channel D Digital Outputs, (Disabled in One-Lane Mode[1]).
11, 12	D0−D, D0+D	Channel D Digital Outputs, (disabled in One-Lane Mode[1]).
13, 14	D1−C, D1+C	Channel C Digital Outputs, (Channel D Digital Outputs in One-Lane Mode[1]).
15, 16	D0−C, D0+C	Channel C Digital Outputs.
17, 18	DCO−, DCO+	Data Clock Outputs.
19, 20	FCO−, FCO+	Frame Clock Outputs.
21, 22	D1−B, D1+B	Channel B Digital Outputs.
23, 24	D0−B, D0+B	Channel B Digital Outputs, (Channel A Digital Outputs in One-Lane Mode[1]).
25, 26	D1−A, D1+A	Channel A Digital Outputs, (Disabled in One-Lane Mode[1]).
27, 28	D0−A, D0+A	Channel A Digital Outputs, (Disabled in One-Lane Mode[1]).
30	SCLK/DTP	SPI Clock Input/Digital Test Pattern.
31	SDIO/OLM	SPI Data Input and Output Bidirectional SPI Data/Output Lane Mode.
32	CSB	SPI Chip Select Bar. Active low enable; 30 kΩ internal pull-up.
33	PDWN	Digital Input, 30 kΩ Internal Pull-Down. PDWN high = power-down device. PDWN low = run device, normal operation.
35	VIN−A	ADC A Analog Input Complement.
36	VIN+A	ADC A Analog Input True.
37	VIN+B	ADC B Analog Input True.
38	VIN−B	ADC B Analog Input Complement.
40	RBIAS	Sets Analog Current Bias. Connect to 10 kΩ (1% tolerance) resistor to ground.
41	SENSE	Reference Mode Selection.
42	VREF	Voltage Reference Input and Output.
43	VCM	Analog Input Common-Mode Voltage.
44	SYNC	Digital Input. SYNC input to clock divider.
47	VIN−C	ADC C Analog Input Complement.
48	VIN+C	ADC C Analog Input True.

[1] Output channel assignments are shown first for THE default two-lane mode. If one-lane mode is used, output channel assignments change as indicated in parenthesis. Register 0x21 Bits[6:4] invoke one-lane mode.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{REF} = 1.0 V

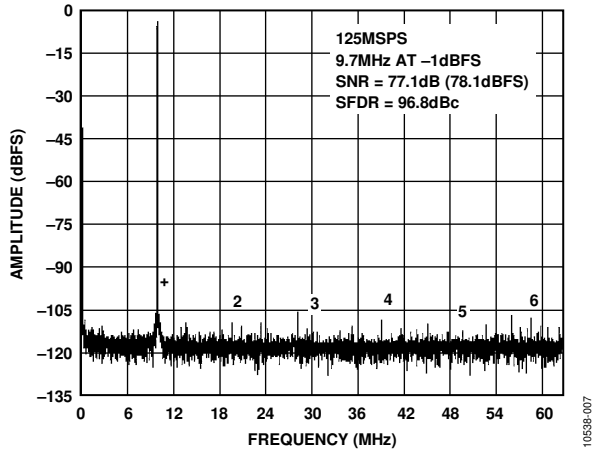


Figure 7. Single-Tone 16k FFT with f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

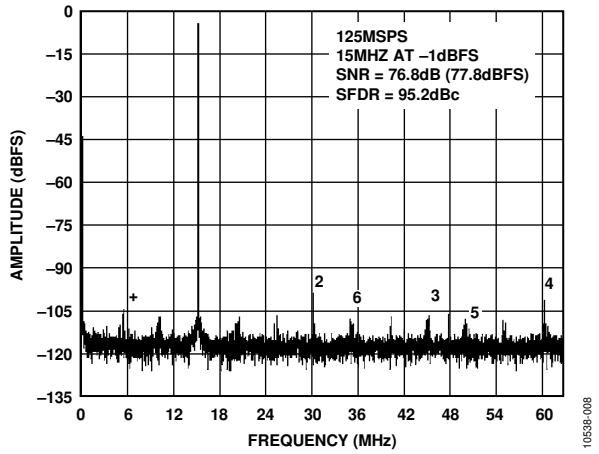


Figure 8. Single-Tone 16k FFT with f_{IN} = 15 MHZ, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

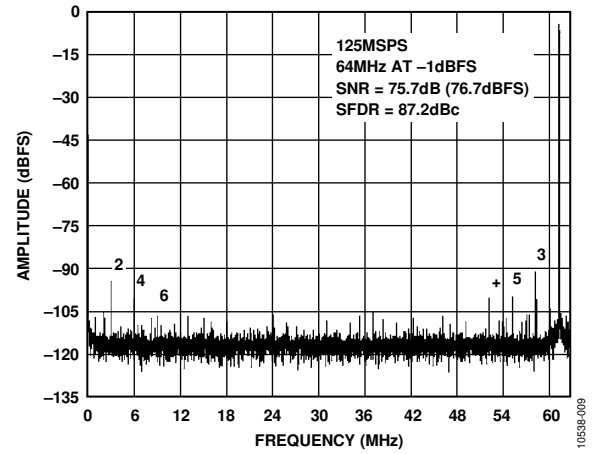


Figure 9. Single-Tone 16k FFT with f_{IN} = 64 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

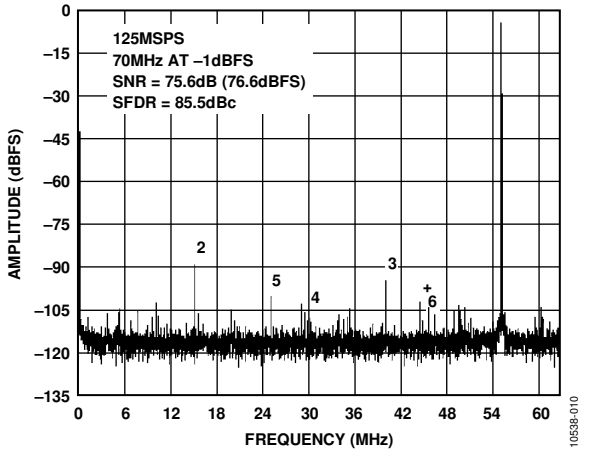


Figure 10. Single-Tone 16k FFT with f_{IN} = 70 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

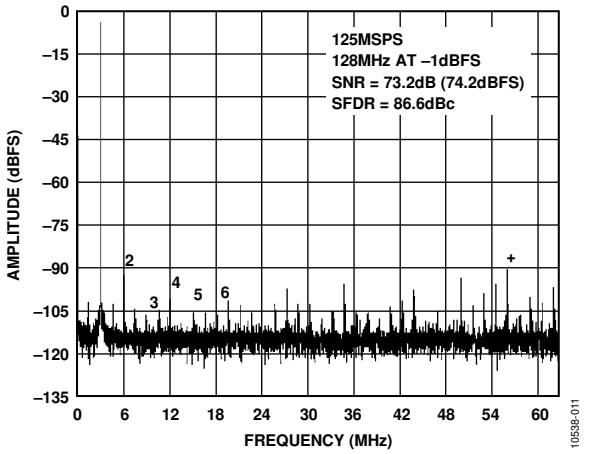


Figure 11. Single-Tone 16k FFT with f_{IN} = 128 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

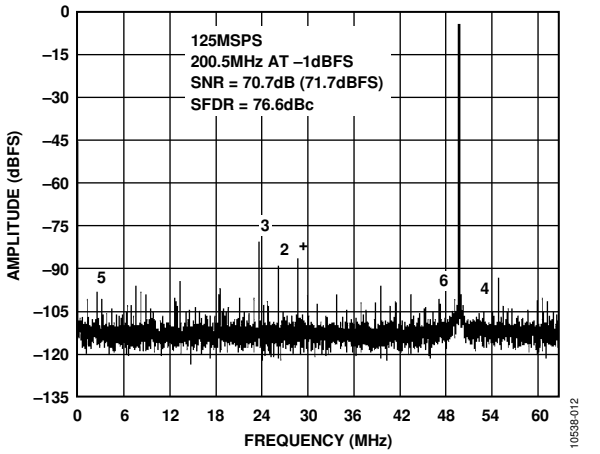


Figure 12. Single-Tone 16k FFT with f_{IN} = 200.5 MHz at f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

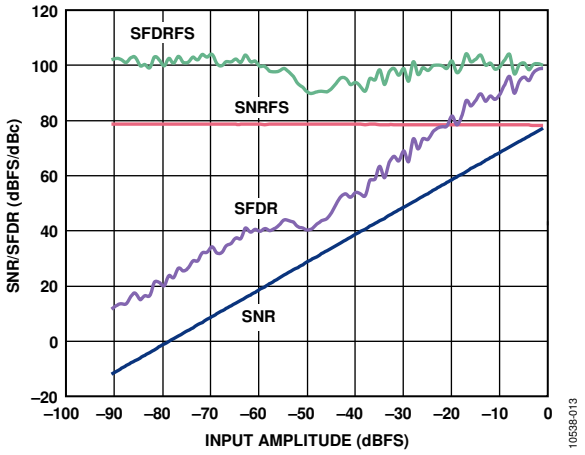


Figure 13. SNR/SFDR vs. Input Amplitude (AIN), f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

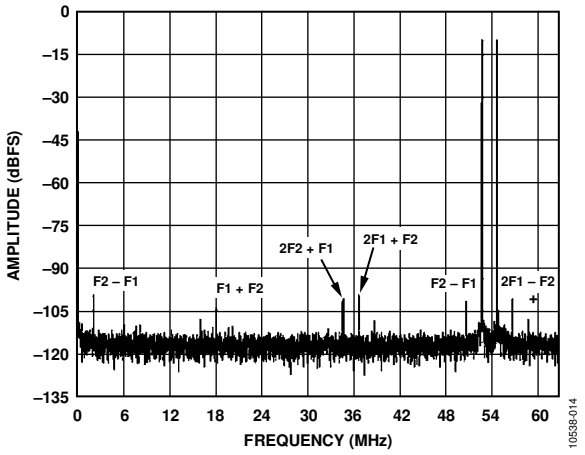


Figure 14. Two-Tone 16k FFT with f_{IN1} = 70.5 MHz and f_{IN2} = 72.5 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

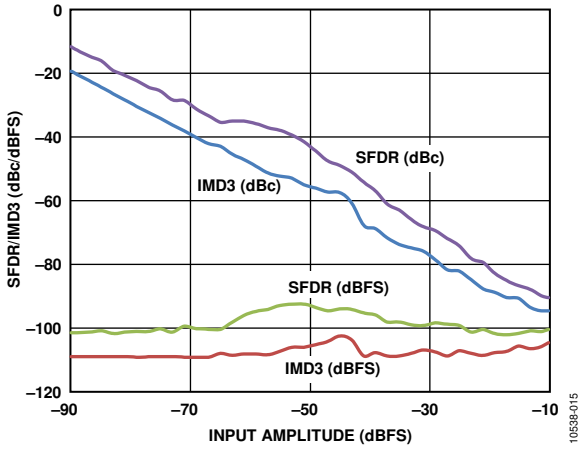


Figure 15. Two-Tone SFDR/IMD3 vs. Input Amplitude (AIN) with f_{IN1} = 70.5 MHz and f_{IN2} = 72.5 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

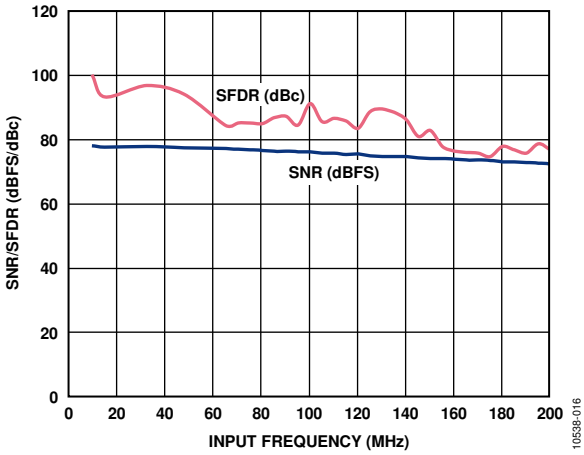


Figure 16. SNR/SFDR vs. f_{IN}, f_{SAMPLE} = 125 MSPS, Clock Divider = 8, V_{REF} = 1.0 V

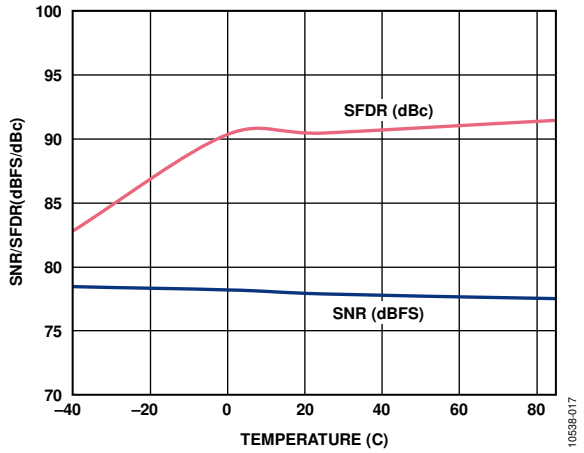


Figure 17. SNR/SFDR vs. Temperature, f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

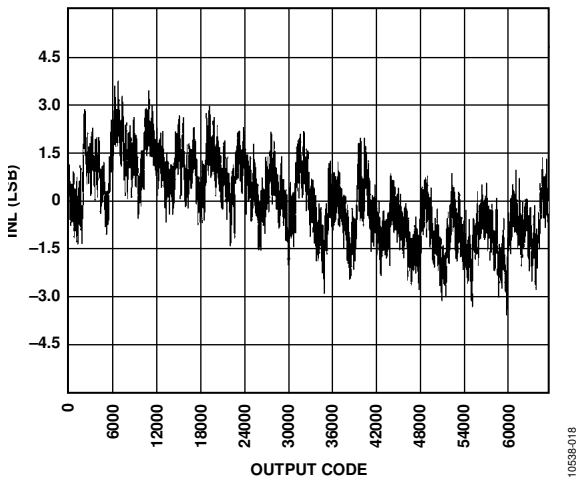


Figure 18. INL, f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

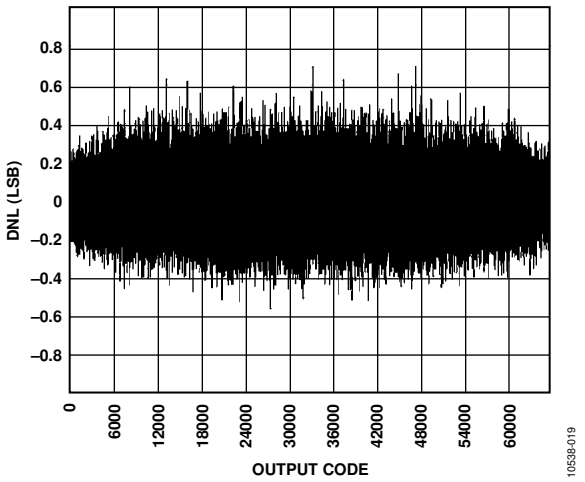


Figure 19. DNL, f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

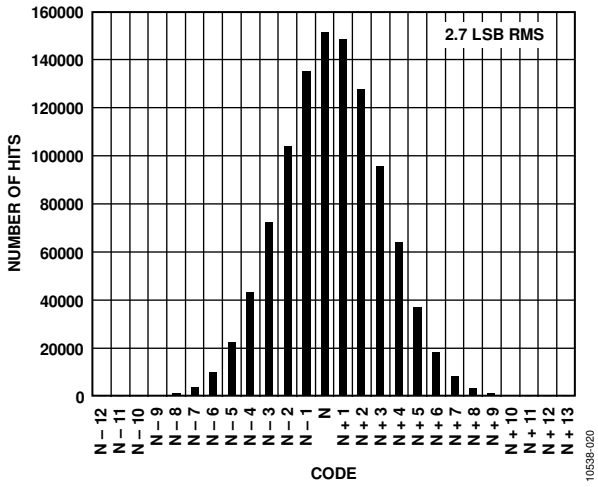


Figure 20. Input-Referred Noise Histogram, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

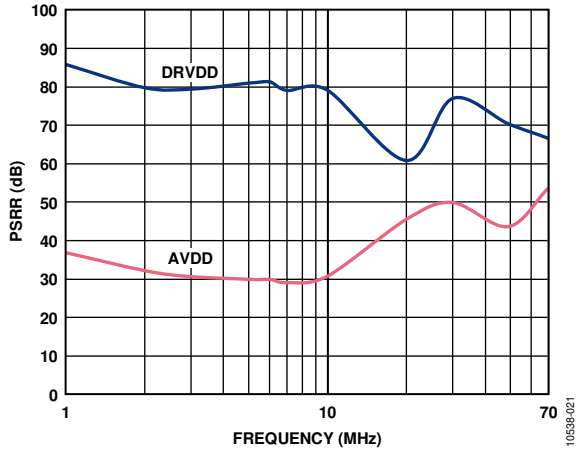


Figure 21. PSRR vs. Frequency, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

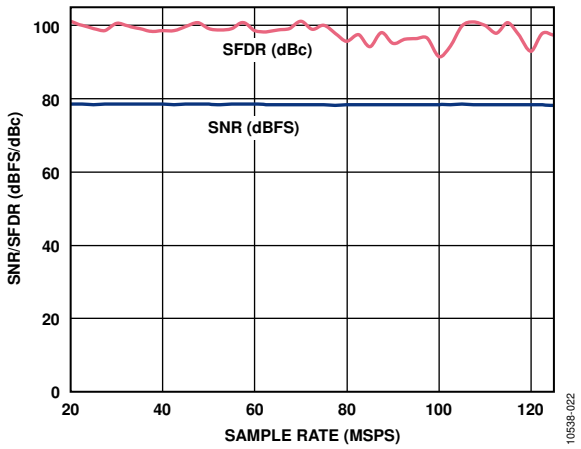


Figure 22. SNR/SFDR vs. Sample Rate, f_{IN} = 9.7 MHz, V_{REF} = 1.0 V

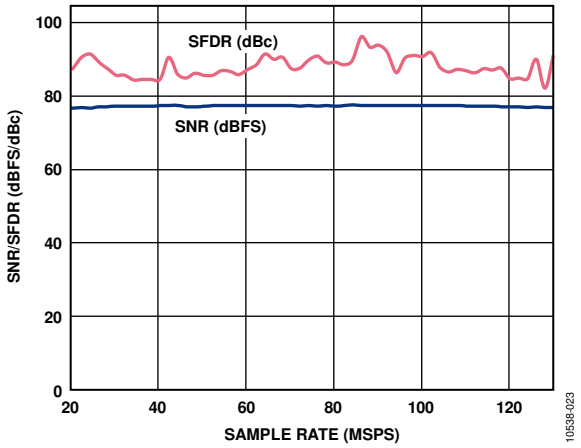


Figure 23. SNR/SFDR vs. Sample Rate, f_{IN} = 64 MHz, Clock Divider = 4, V_{REF} = 1.0 V

V_{REF} = 1.3 V

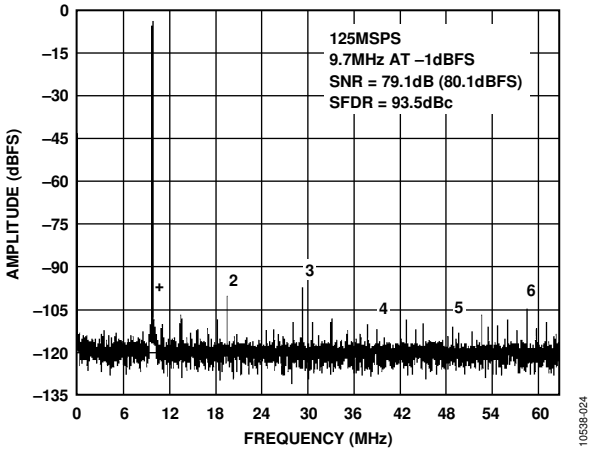


Figure 24. Single-Tone 16k FFT with f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.3 V

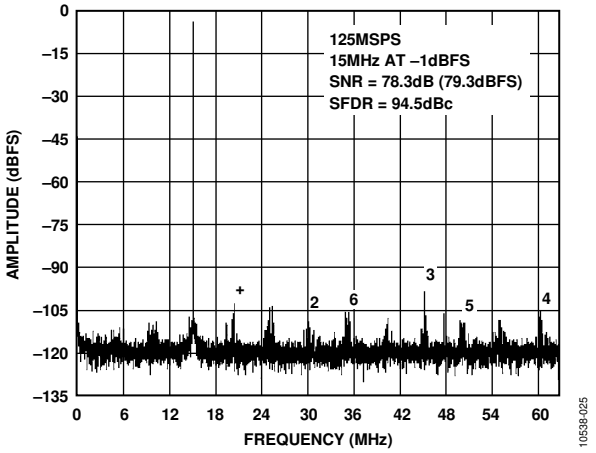


Figure 25. Single-Tone 16k FFT with f_{IN} = 15 MHZ, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.3 V

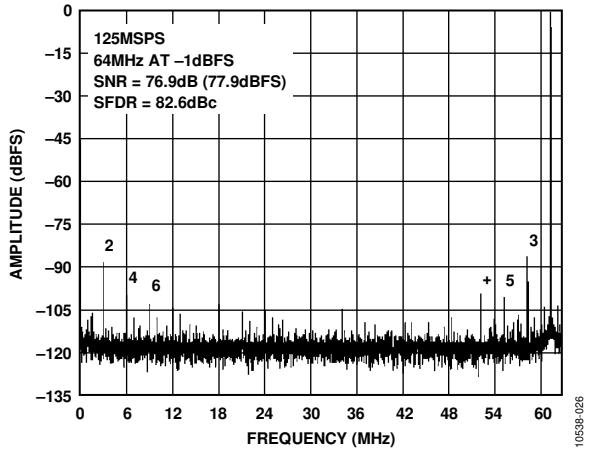


Figure 26. Single-Tone 16k FFT with f_{IN} = 64 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.3 V

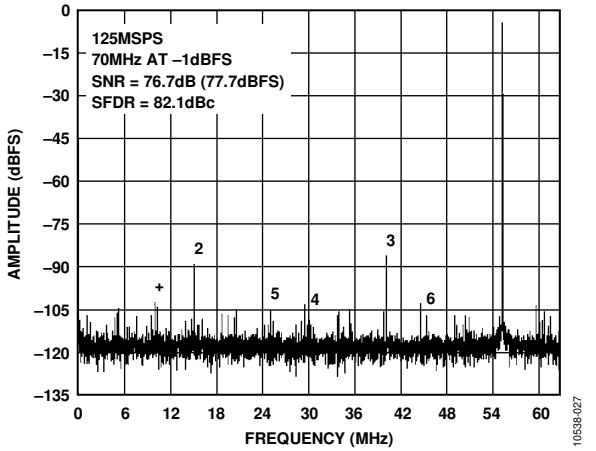


Figure 27. Single-Tone 16k FFT with f_{IN} = 70 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.3 V

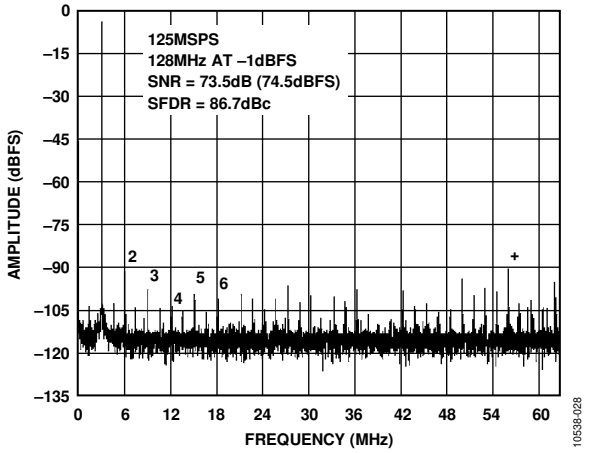


Figure 28. Single-Tone 16k FFT with f_{IN} = 128 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.3 V

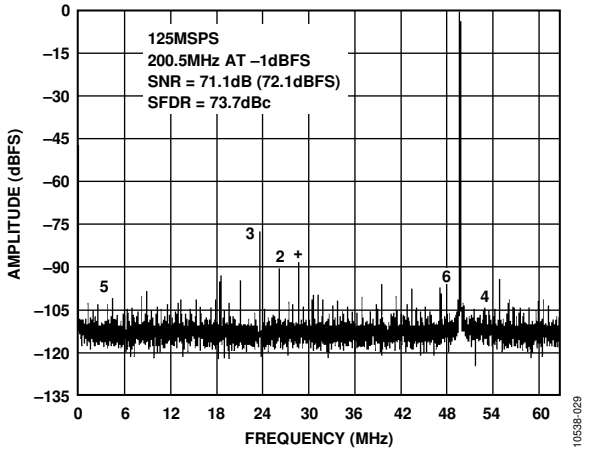


Figure 29. Single-Tone 16k FFT with f_{IN} = 200.5 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.3 V

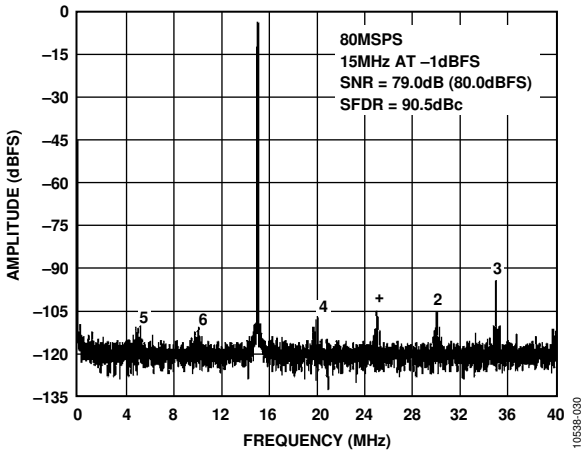


Figure 30. Single-Tone 16k FFT with f_{IN} = 15 MHz, f_{SAMPLE} = 80 MSPS, V_{REF} = 1.3 V

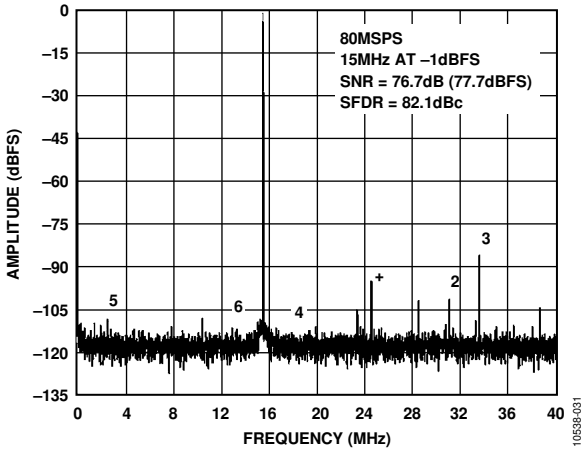


Figure 31. Single-Tone 16k FFT with f_{IN} = 64.5 MHz, f_{SAMPLE} = 80 MSPS, V_{REF} = 1.3 V

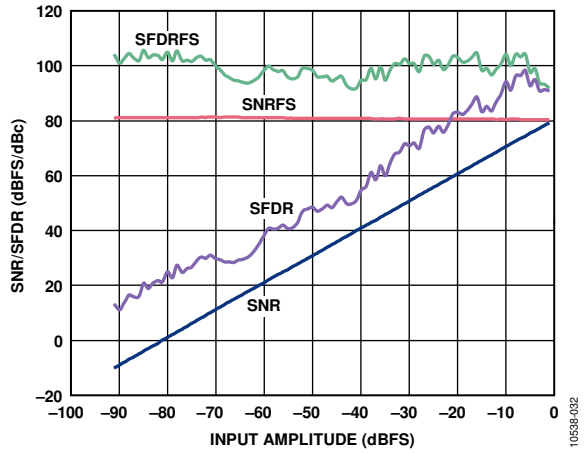


Figure 32. SNR/SFDR vs. Input Amplitude (AIN), f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.3 V

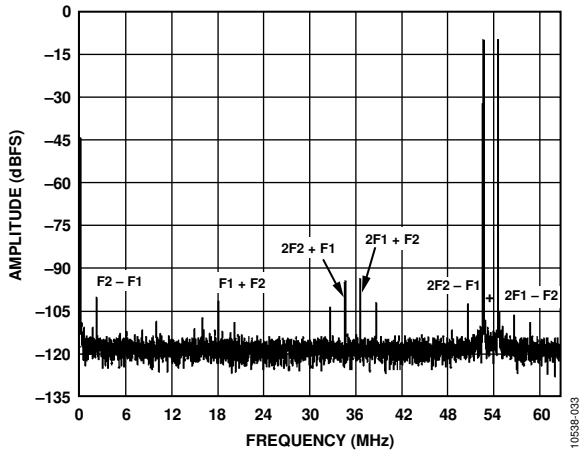


Figure 33. Two-Tone 16k FFT with f_{IN1} = 70.5 MHz and f_{IN2} = 72.5 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.3 V

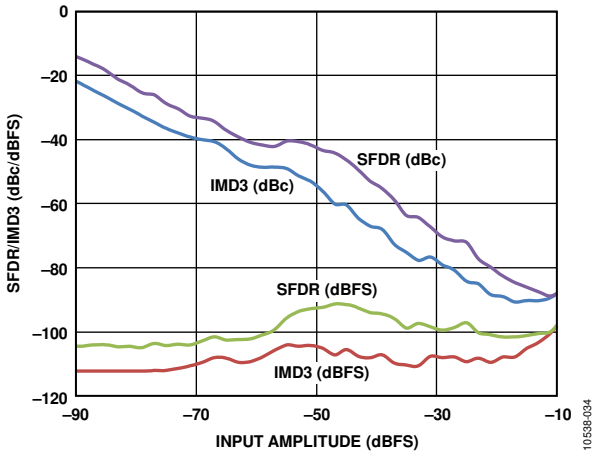


Figure 34. Two-Tone SFDR/IMD3 vs. Input Amplitude (AIN) with f_{IN1} = 70.5 MHz and f_{IN2} = 72.5 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.3 V

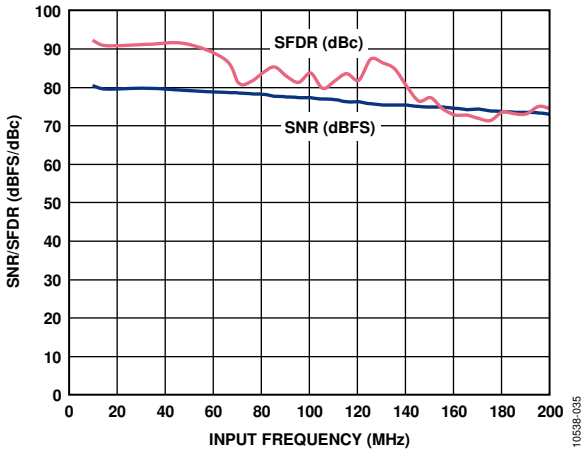


Figure 35. SNR/SFDR vs. f_{IN}, f_{SAMPLE} = 125 MSPS, Clock Divider = 8, V_{REF} = 1.3 V

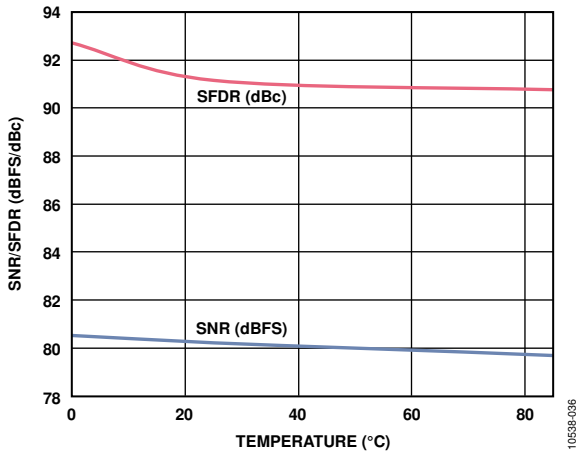


Figure 36. SNR/SFDR vs. Temperature, f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.3 V

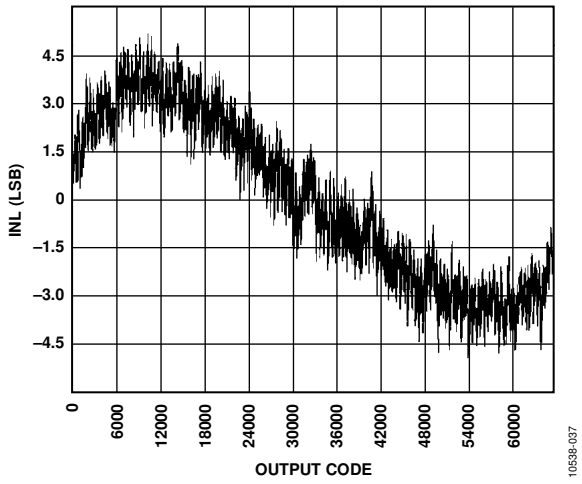


Figure 37. INL, f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.3 V

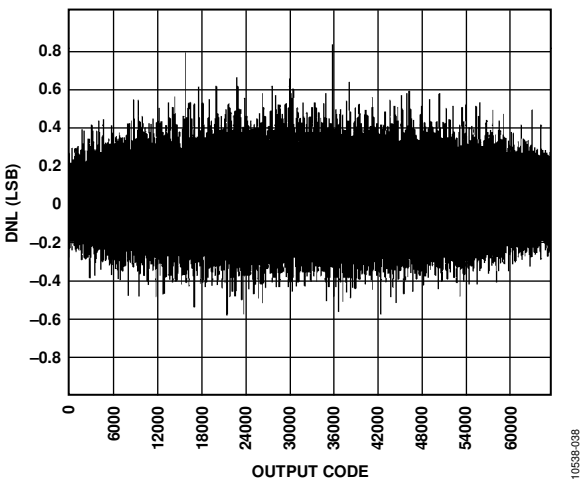


Figure 38. DNL, f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.3 V

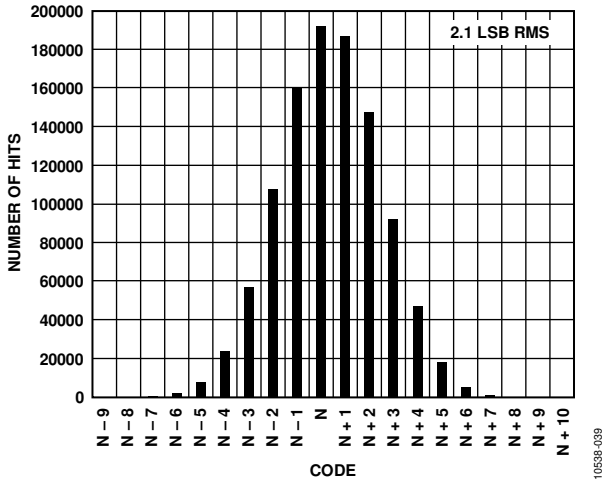


Figure 39. Input-Referred Noise Histogram, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.3 V

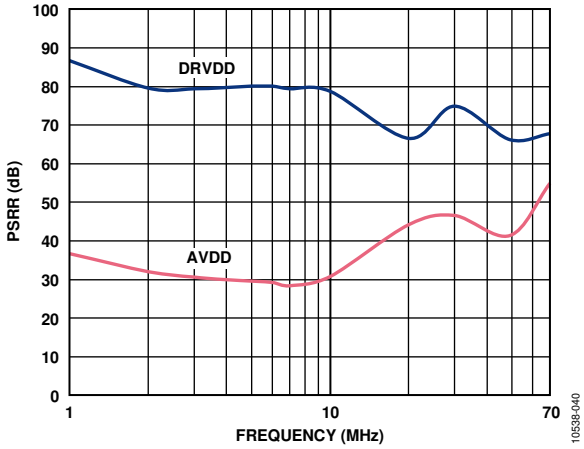


Figure 40. PSRR vs. Frequency, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.3 V

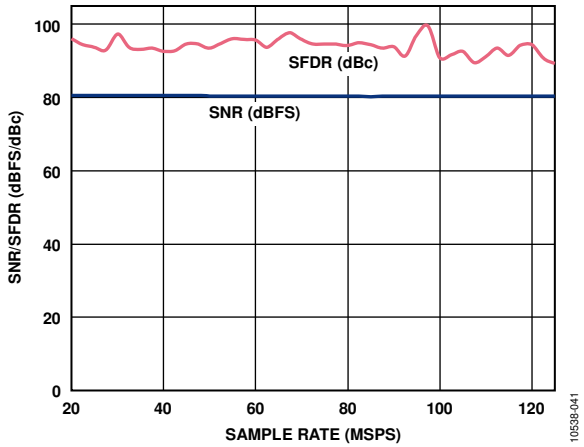


Figure 41. SNR/SFDR vs. Sample Rate, f_{IN} = 9.7 MHz, V_{REF} = 1.3 V

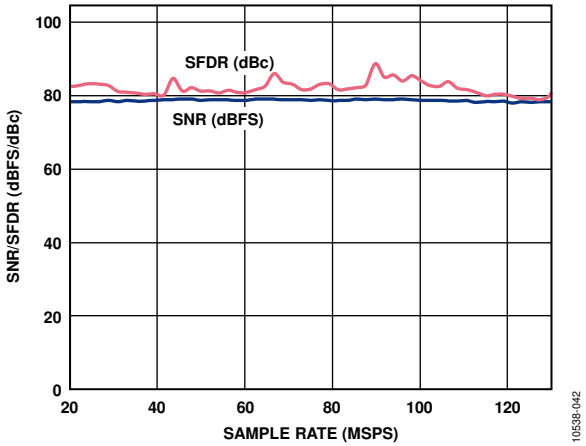


Figure 42. SNR/SFDR vs. Sample Rate, f_{IN} = 64 MHz, Clock Divider = 4, V_{REF} = 1.3 V

EQUIVALENT CIRCUITS

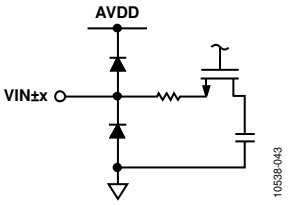


Figure 43. Equivalent Analog Input Circuit

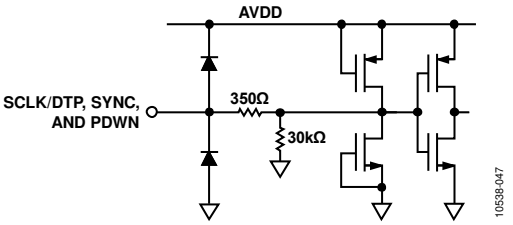


Figure 47. Equivalent SCLK/DTP, SYNC, and PDWN Input Circuit

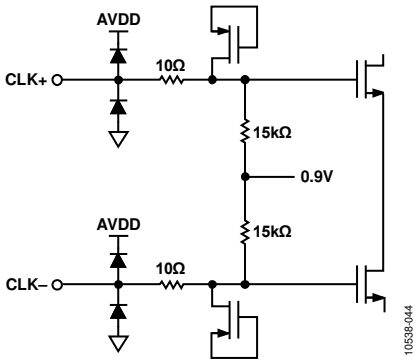


Figure 44. Equivalent Clock Input Circuit

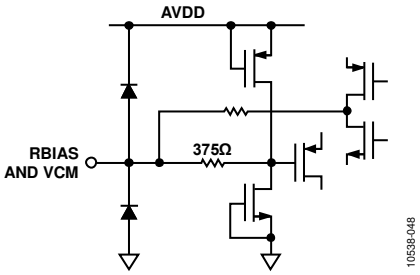


Figure 48. Equivalent RBIAS and VCM Circuit

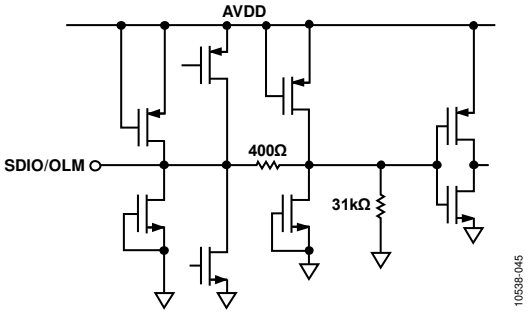


Figure 45. Equivalent SDIO/OLM Input Circuit

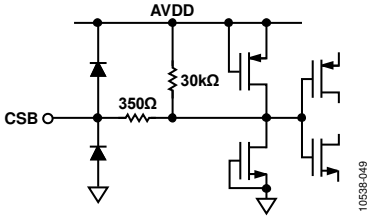


Figure 49. Equivalent $\overline{CS}$ Input Circuit

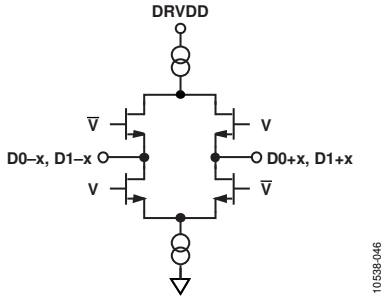


Figure 46. Equivalent Digital Output Circuit

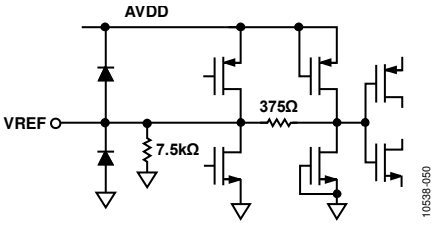


Figure 50. Equivalent VREF Circuit

THEORY OF OPERATION

The AD9653 is a multistage, pipelined ADC. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 16-bit result in the digital correction logic. The serializer transmits this converted data in a 16-bit output. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The data is then serialized and aligned to the frame and data clocks.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9653 is a differential switched-capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. By using an input common-mode voltage of midsupply, users can minimize signal-dependent errors and achieve optimum performance.

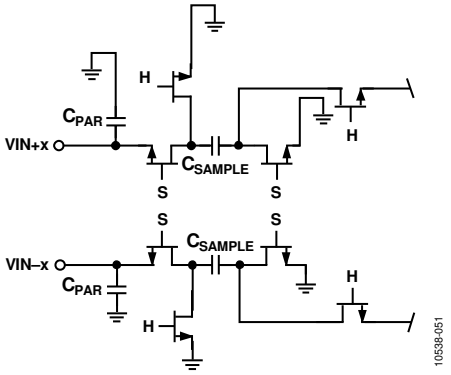


Figure 51. Switched-Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample mode and hold mode (see Figure 51). When the input circuit is switched to sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current injected from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and therefore achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Either a differential capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005) for more information. In general, the precise values depend on the application.

Input Common Mode

The analog inputs of the AD9653 are not internally dc-biased. Therefore, in ac-coupled applications, the user must provide this bias externally. Setting the device so that V_{CM} = AVDD/2 is recommended for optimum performance, but the device can function over a wider range with reasonable performance, as shown in Figure 52 and Figure 53.

An on-chip, common-mode voltage reference is included in the design and is available from the VCM pin. The VCM pin must be bypassed to ground by a 0.1 µF capacitor, as described in the Applications Information section.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9653, the input span is dependent on the reference voltage (see Table 11).

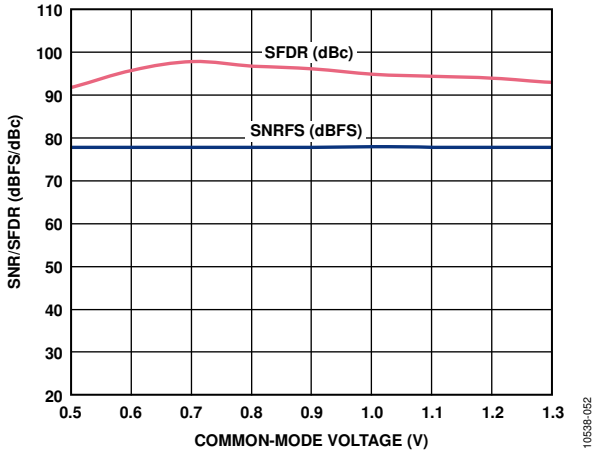


Figure 52. SNR/SFDR vs. Common-Mode Voltage, f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

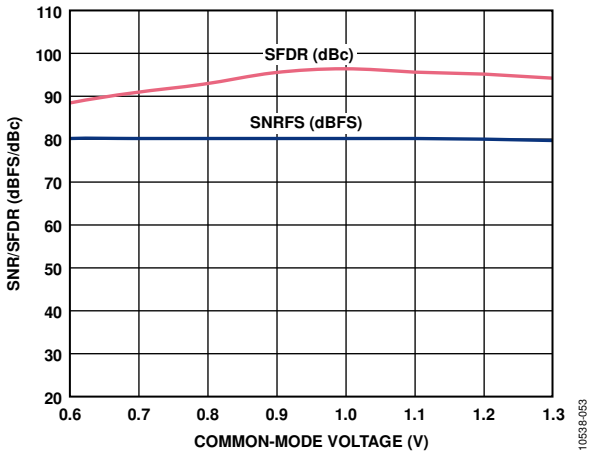


Figure 53. SNR/SFDR vs. Common-Mode Voltage, f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.3 V

Differential Input Configurations

There are several ways to drive the AD9653 either actively or passively. However, optimum performance is achieved by driving the analog inputs differentially. Using a differential double balun configuration to drive the AD9653 provides excellent performance and a flexible interface to the ADC (see Figure 56) for baseband applications.

For applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration (see Figure 57), because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9653.

Regardless of the configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

It is not recommended to drive the AD9653 inputs single-ended.

VOLTAGE REFERENCE

A stable and accurate voltage reference is built into the AD9653. VREF can be configured using either the internal 1.0 V reference, an externally applied 1.0 V to 1.3 V reference voltage, or using an external resistor divider applied to the internal reference to produce a reference voltage of the user's choice. The various reference modes are summarized in the Internal Reference Connection section and the External Reference Operation section. The VREF pin should be externally bypassed to ground with a low ESR, 1.0 µF capacitor in parallel with a low ESR, 0.1 µF ceramic capacitor.

Internal Reference Connection

A comparator within the AD9653 detects the potential at the SENSE pin and configures the reference into one of three possible modes, which are summarized in Table 11. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 54), setting the voltage at the VREF pin, V_{REF}, to 1.0 V. If SENSE is connected to an external resistor divider (see Figure 55), V_{REF} is defined as

$$V_{REF} = 0.5 \times \left(1 + \frac{R2}{R1}\right)$$

where:

$$7\ \text{k}\Omega \leq (R1 + R2) \leq 10\ \text{k}\Omega$$

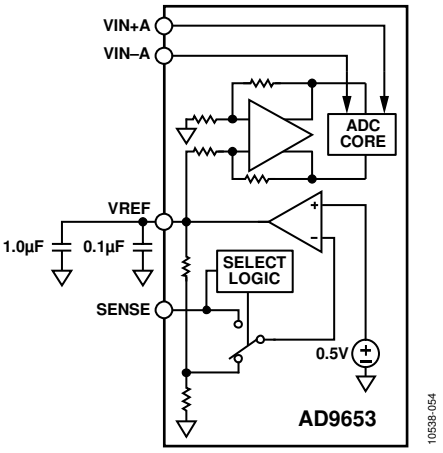


Figure 54. 1.0 V Internal Reference Configuration

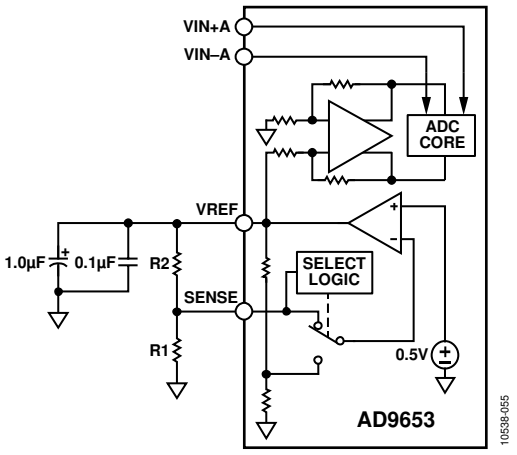


Figure 55. Programmable Internal Reference Configuration

Table 11. Reference Configuration Summary

Selected Mode	SENSE Voltage (V)	Resulting V_{REF} (V)	Resulting Differential Span (V p-p)
Fixed Internal Reference	AGND to 0.2	1.0 internal	2.0
Programmable Internal Reference	Tie to external R-divider (see Figure 55)	0.5 × (1 + R2/R1), example: R1 = 3.5 kΩ, R2 = 5.6 kΩ for V_{REF} = 1.3 V[1]	2 × V_{REF}
Fixed External Reference	AVDD	1.0 to 1.3 applied to external VREF pin[1]	2.0 to 2.6

[1] Normal operation for V_{REF} = 1.3 V is supported over the 0°C to 85°C temperature range.

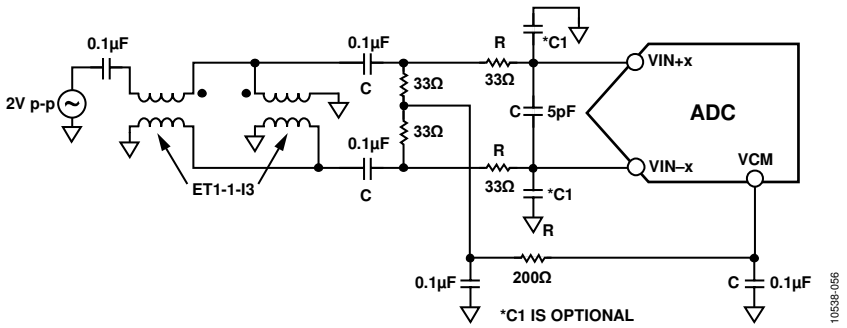


Figure 56. Differential Double Balun Input Configuration for Baseband Applications

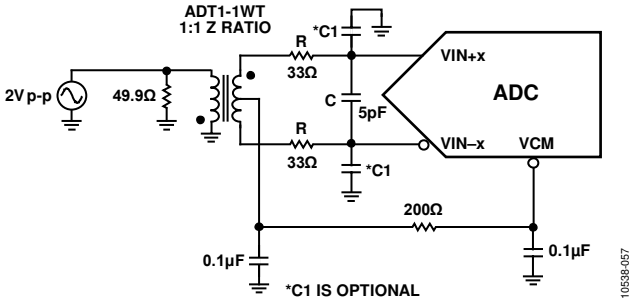


Figure 57. Differential Transformer-Coupled Configuration for Baseband Applications

If the internal reference of the AD9653 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 58 and Figure 59 show how the internal reference voltage is affected by loading.

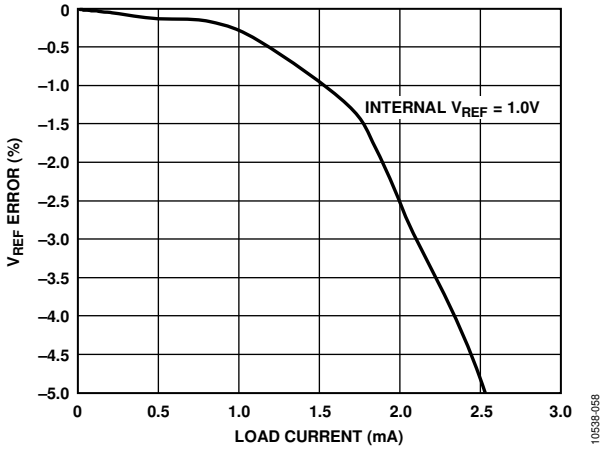


Figure 58. V_{REF} = 1.0 V Error vs. Load Current

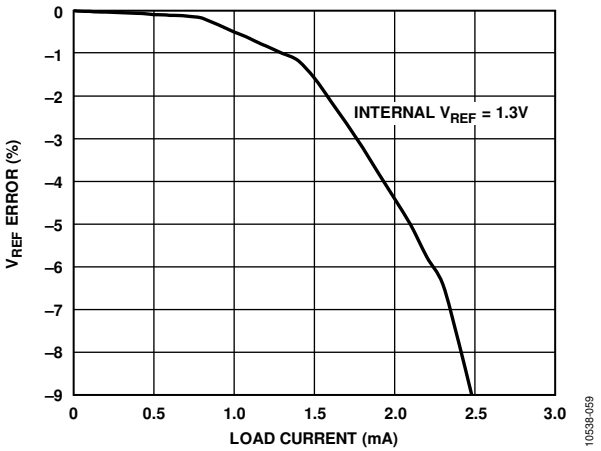


Figure 59. V_{REF} = 1.3 V Error vs. Load Current

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 60 and Figure 61 show the typical drift characteristics of the internal reference in 1.0 V mode and programmable 1.3 V mode, respectively.