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Dual, 16-Bit, 125 MSPS Serial LVDS, 1.8 V Analog-to-Digital Converter

Data Sheet **AD9655**

FEATURES

- 1.8 V supply operation
- Low power: approximately 150 mW/channel at 125 MSPS, 2 V p-p input range (typical)
- SNR/SFDR at 69.5 MHz
  - 77.5 dBFS/88 dBc, 2.0 V p-p input range (typical)
  - 79.3 dBFS/84 dBc, 2.8 V p-p input range (typical)
- Linearity
  - DNL = ±0.7 LSB; INL = ±4.0 LSB (typical, 2.0 V p-p input span)
  - DNL = ±0.7 LSB; INL = ±3.4 LSB (typical, 2.8 V p-p input span)
- Serial LVDS, two data lanes per ADC channel
- 500 MHz full power analog bandwidth
- Serial port control
  - Full chip and individual channel power-down modes
  - Flexible bit orientation
  - Built-in and custom digital test pattern generation
  - Clock divider
  - Programmable output clock and data alignment
  - Standby mode

APPLICATIONS

- Communications
- Diversity radio systems
- Multimode digital receivers
  - GSM, EDGE, W-CDMA, LTE, CDMA2000, WiMAX, TD-SCDMA
- I/Q demodulation systems
- Smart antenna systems
- Broadband data applications
- Battery-powered instruments
- Handheld scope meters
- Portable medical imaging and ultrasound
- Radar/LIDAR

GENERAL DESCRIPTION

The AD9655 is a dual, 16-bit, 125 MSPS analog-to-digital converter (ADC) with an on-chip sample-and-hold circuit designed for low cost, low power, small size, and ease of use. The product operates at a conversion rate of up to 125 MSPS and is optimized for outstanding dynamic performance and low power in applications where a small package size is critical.

The ADC requires a single 1.8 V power supply and an LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. External reference or driver components are not required for many applications.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock output (DCO) for capturing data on the output and a frame clock output (FCO) for signaling a new output byte are provided.

FUNCTIONAL BLOCK DIAGRAM

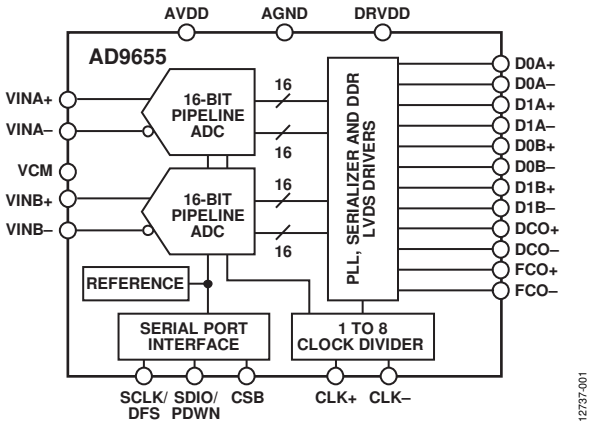

Figure 1.

Individual channel power-down is supported. The AD9655 typically consumes less than 2 mW in serial port interface (SPI) power-down mode. The available digital test pat-terns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the SPI.

The AD9655 is available in an RoHS-compliant, 32-lead LFCSP. It is specified over the industrial temperature range of −40°C to +85°C. This device is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Small Footprint.
   Two ADCs are contained in a small, space-saving package.
2. Pin Compatible.
   The AD9655 is pin compatible to the AD9645 14-bit and AD9635 12-bit dual ADCs.
3. Ease of Use.
   A DCO operates at frequencies of up to 500 MHz and supports double data rate (DDR) operation.
4. User Flexibility.
   The SPI control offers a wide range of flexible features to meet specific system requirements.

Rev. 0 Document Feedback

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Tel: 781.329.4700

Technical Support www.analog.com

AD9655* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9655 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9655: Dual, 16-Bit, 125 MSPS Serial LVDS, 1.8 V Analog-to-Digital Converter Data Sheet

User Guides

- AD9655/AD9645/AD9635 Evaluation Documentation

TOOLS AND SIMULATIONS

- AD9655 S Parameter

DESIGN RESOURCES

- AD9655 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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TABLE OF CONTENTS

REVISION HISTORY

1/15—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p full-scale differential input mode, internal reference voltage (V_{REF}) = 1.0 V, input amplitude (A_{IN}) = −1.0 dBFS, 125 MSPS, unless otherwise noted.

Table 1.

Parameter[1]	Temperature	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed[2]		
Offset Error	25°C		0.2		% FSR
Offset Matching	25°C		0.1		% FSR
Gain Error	25°C		3.4		% FSR
Gain Matching	25°C		0.4		% FSR
Differential Nonlinearity (DNL)	25°C		±0.7		LSB
Integral Nonlinearity (INL)	25°C		±4.0		LSB
TEMPERATURE DRIFT					
Gain Error	Full		−23		ppm/°C
Offset Error	Full		0.9		ppm/°C
INTERNAL VOLTAGE REFERENCE					
Output Voltage (1 V Mode)	25°C		1.0		V
Load Regulation at 1.0 mA (V_{REF} = 1 V)	25°C		2.9		mV
Input Resistance	25°C		7.5		kΩ
INPUT-REFERRED NOISE					
V_{REF} = 1.0 V	25°C		2.7		LSB rms
ANALOG INPUTS					
Differential Input Voltage (V_{REF} = 1 V)	Full		2		V p-p
Common-Mode Voltage	Full		0.9		V
Common-Mode Range	25°C	0.5		1.2	V
Differential Input Resistance	25°C		1.9		kΩ
Differential Input Capacitance	25°C		6.6		pF
POWER SUPPLY					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
I_{AVDD}[3]	25°C		93		mA
I_{DRVDD} (ANSI-644 Mode)[3]	25°C		73		mA
I_{DRVDD} (Reduced Range Mode)[3]	25°C		62		mA
TOTAL POWER CONSUMPTION					
Sine Wave Input (Two Channels, Including Output Drivers ANSI-644 Mode)	25°C		299		mW
Sine Wave Input (Two Channels, Including Output Drivers Reduced Range Mode)	25°C		279		mW
Power-Down	25°C		2		mW
Standby[4]	25°C		142		mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] No missing codes guaranteed if Register 0x18 = 0x04 (default, no digital scaling of the output).
[3] Measured with a low input frequency, −1 dBFS sine wave on both channels, DDR operation, and two-lane operation.
[4] Standby mode can be controlled via the SPI.

AVDD = 1.8 V, DRVDD = 1.8 V, 2.8 V p-p full-scale differential input mode, V_{REF} = 1.4 V, A_{IN} = −1.0 dBFS, 125 MSPS, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed[2]		
Offset Error	Full	−0.12	+0.2	+0.48	% FSR
Offset Matching	Full	−0.2	+0.1	+0.33	% FSR
Gain Error	Full	−2.4	+2.8	+8.2	% FSR
Gain Matching	Full	−1.2	+0.4	+1.9	% FSR
Differential Nonlinearity (DNL)	Full	−0.99		+1.43	LSB
	25°C		±0.7		LSB
Integral Nonlinearity (INL)	Full	−8.5		+8.5	LSB
	25°C		±3.4		LSB
TEMPERATURE DRIFT					
Gain Error	Full		−66		ppm/°C
Offset Error	Full		0.9		ppm/°C
INTERNAL VOLTAGE REFERENCE					
Output Voltage (1.4 V Mode)	Full	1.37	1.38	1.41	V
Load Regulation at 1.0 mA (V_{REF} = 1.4 V)	25°C		186		mV
Input Resistance	25°C		7.5		kΩ
INPUT-REFERRED NOISE					
V_{REF} = 1.4 V	25°C		2		LSB rms
ANALOG INPUTS					
Differential Input Voltage (V_{REF} = 1.4 V)	Full		2.8		V p-p
Common-Mode Voltage	Full		0.9		V
Common-Mode Range	25°C	0.7		1.0	V
Differential Input Resistance	25°C		1.9		kΩ
Differential Input Capacitance	25°C		6.6		pF
POWER SUPPLY					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
I_{AVDD}[3]	Full		101	111	mA
I_{DRVDD} (ANSI-644 Mode)[3]	Full		73	79	mA
I_{DRVDD} (Reduced Range Mode)[3]	Full		62	68	mA
TOTAL POWER CONSUMPTION					
Sine Wave Input (Two Channels, Including Output Drivers ANSI-644 Mode)	Full		313	342	mW
Sine Wave Input (Two Channels, Including Output Drivers Reduced Range Mode)	Full		293	322	mW
Power-Down	Full		2	4	mW
Standby[4]	Full		155	172	mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] No missing codes guaranteed if Register 0x18 = 0x04 (default, no digital scaling of the output).
[3] Measured with a low input frequency, −1 dBFS sine wave on both channels, DDR operation, and two-lane operation.
[4] Standby mode can be controlled via the SPI.

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p full-scale differential input mode, V_{REF} = 1.0 V, A_{IN} = −1.0 dBFS, 125 MSPS, unless otherwise noted.

Table 3.

Parameter[1]	Temperature	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 9.7 MHz	25°C		77.9		dBFS
f_{IN} = 19.7 MHz	25°C		77.9		dBFS
f_{IN} = 69.5 MHz	25°C		77.5		dBFS
f_{IN} = 100.5 MHz	25°C		76.6		dBFS
f_{IN} = 139.5 MHz	25°C		75.6		dBFS
f_{IN} = 301 MHz	25°C		71.0		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)					
f_{IN} = 9.7 MHz	25°C		77.5		dBFS
f_{IN} = 19.7 MHz	25°C		77.1		dBFS
f_{IN} = 69.5 MHz	25°C		77.1		dBFS
f_{IN} = 100.5 MHz	25°C		76.5		dBFS
f_{IN} = 139.5 MHz	25°C		75.2		dBFS
f_{IN} = 301 MHz	25°C		68.0		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 9.7 MHz	25°C		12.6		Bits
f_{IN} = 19.7 MHz	25°C		12.5		Bits
f_{IN} = 69.5 MHz	25°C		12.5		Bits
f_{IN} = 100.5 MHz	25°C		12.4		Bits
f_{IN} = 139.5 MHz	25°C		12.2		Bits
f_{IN} = 301 MHz	25°C		11		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 9.7 MHz	25°C		88		dBc
f_{IN} = 19.7 MHz	25°C		86		dBc
f_{IN} = 69.5 MHz	25°C		88		dBc
f_{IN} = 100.5 MHz	25°C		91		dBc
f_{IN} = 139.5 MHz	25°C		85		dBc
f_{IN} = 301 MHz	25°C		70		dBc
WORST HARMONIC (SECOND OR THIRD)					
f_{IN} = 9.7 MHz	25°C		−88		dBc
f_{IN} = 19.7 MHz	25°C		−86		dBc
f_{IN} = 69.5 MHz	25°C		−88		dBc
f_{IN} = 100.5 MHz	25°C		−91		dBc
f_{IN} = 139.5 MHz	25°C		−85		dBc
f_{IN} = 301 MHz	25°C		−70		dBc
WORST OTHER (EXCLUDING SECOND OR THIRD HARMONIC)					
f_{IN} = 9.7 MHz	25°C		−95		dBc
f_{IN} = 19.7 MHz	25°C		−99		dBc
f_{IN} = 69.5 MHz	25°C		−92		dBc
f_{IN} = 100.5 MHz	25°C		−91		dBc
f_{IN} = 139.5 MHz	25°C		−89		dBc
f_{IN} = 301 MHz	25°C		−80		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)—A_{IN1} AND A_{IN2} = −7.0 dBFS					
f_{IN1} = 100.1 MHz, f_{IN2} = 102.1 MHz	25°C		90		dBc
CROSSTALK[2]	25°C		−104		dB
CROSSTALK (OVERRANGE CONDITION)[3]	25°C		−100		dB
ANALOG INPUT BANDWIDTH, FULL POWER	25°C		500		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Crosstalk is measured at 69.5 MHz with −1.0 dBFS analog input on one channel and no input on the adjacent channel. Measurements are taken using a less dense board to demonstrate the AD9655 crosstalk performance, not board limitations.
[3] Overrange condition is specified as being 3 dB above the full-scale input range.

AVDD = 1.8 V, DRVDD = 1.8 V, 2.8 V p-p full-scale differential input mode, V_{REF} = 1.4 V, A_{IN} = −1.0 dBFS, 125 MSPS, unless otherwise noted.

Table 4.

Parameter[1]	Temperature	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 9.7 MHz	25°C		79.6		dBFS
f_{IN} = 19.7 MHz	25°C		79.4		dBFS
f_{IN} = 69.5 MHz	Full	78.0	79.3		dBFS
f_{IN} = 100.5 MHz	25°C		78.0		dBFS
f_{IN} = 139.5 MHz	25°C		76.5		dBFS
f_{IN} = 301 MHz	25°C		55.0		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)					
f_{IN} = 9.7 MHz	25°C		79.1		dBFS
f_{IN} = 19.7 MHz	25°C		78.3		dBFS
f_{IN} = 69.5 MHz	Full	77.2	77.8		dBFS
f_{IN} = 100.5 MHz	25°C		77.0		dBFS
f_{IN} = 139.5 MHz	25°C		75.8		dBFS
f_{IN} = 301 MHz	25°C		54.8		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 9.7 MHz	25°C		12.8		Bits
f_{IN} = 19.7 MHz	25°C		12.7		Bits
f_{IN} = 69.5 MHz	Full	12.5	12.6		Bits
f_{IN} = 100.5 MHz	25°C		12.5		Bits
f_{IN} = 139.5 MHz	25°C		12.3		Bits
f_{IN} = 301 MHz	25°C		8.8		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 9.7 MHz	25°C		88		dBc
f_{IN} = 19.7 MHz	25°C		85		dBc
f_{IN} = 69.5 MHz	Full	80	84		dBc
f_{IN} = 100.5 MHz	25°C		83		dBc
f_{IN} = 139.5 MHz	25°C		82		dBc
f_{IN} = 301 MHz	25°C		68		dBc
WORST HARMONIC (SECOND OR THIRD)					
f_{IN} = 9.7 MHz	25°C		−88		dBc
f_{IN} = 19.7 MHz	25°C		−85		dBc
f_{IN} = 69.5 MHz	Full		−84	−80	dBc
f_{IN} = 100.5 MHz	25°C		−83		dBc
f_{IN} = 139.5 MHz	25°C		−82		dBc
f_{IN} = 301 MHz	25°C		−68		dBc
WORST OTHER (EXCLUDING SECOND OR THIRD HARMONIC)					
f_{IN} = 9.7 MHz	25°C		−97		dBc
f_{IN} = 19.7 MHz	25°C		−98		dBc
f_{IN} = 69.5 MHz	Full		−93	−85	dBc
f_{IN} = 100.5 MHz	25°C		−91		dBc
f_{IN} = 139.5 MHz	25°C		−89		dBc
f_{IN} = 301 MHz	25°C		−72		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)—A_{IN1} AND A_{IN2} = −7.0 dBFS					
f_{IN1} = 100.1 MHz, f_{IN2} = 102.1 MHz	25°C		85		dBc
CROSSTALK[2]	25°C		−104		dB
CROSSTALK (OVERRANGE CONDITION)[3]	25°C		−103		dB
ANALOG INPUT BANDWIDTH, FULL POWER	25°C		500		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Crosstalk is measured at 69.5 MHz with −1.0 dBFS analog input on one channel and no input on the adjacent channel. Measurements are taken using a less dense board to demonstrate AD9655 crosstalk performance, not board limitations.
[3] Overrange condition is specified as being 3 dB above the full-scale input range.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V and DRVDD = 1.8 V, unless otherwise noted.

Table 5.

Parameter[1]	Temperature	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK–)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	0.2		3.6	V p-p
Input Voltage Range	Full	AGND – 0.2		AVDD + 0.2	V
Input Common-Mode Voltage	Full		0.9		V
Input Resistance (Differential)	25°C		15		kΩ
Input Capacitance	25°C		4		pF
LOGIC INPUTS (SCLK/DFS)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		2		pF
LOGIC INPUT (CSB)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		2		pF
LOGIC INPUT (SDIO/PDWN)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		5		pF
LOGIC OUTPUT (SDIO/PDWN)[3]					
Logic 1 Voltage (I_{OH} = 800 µA)	Full		1.79		V
Logic 0 Voltage (I_{OL} = 50 µA)	Full			0.05	V
DIGITAL OUTPUTS (D0x±, D1x±), ANSI-644					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	±298	±350	±400	mV
Output Offset Voltage (V_{OS})	Full	1.15	1.22	1.30	V
Output Coding (Default)			Twos complement		
DIGITAL OUTPUTS (D0x±, D1x±), LOW POWER, REDUCED SIGNAL OPTION					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	±170	±200	±231	mV
Output Offset Voltage (V_{OS})	Full	1.15	1.22	1.30	V
Output Coding (Default)			Twos complement		

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Specified for LVDS and LVPECL only.
[3] Specified for 13 SDIO/PDWN pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V and DRVDD = 1.8 V, unless otherwise noted.

Table 6.

Parameter[1, 2]	Temperature	Min	Typ	Max	Unit
CLOCK[3]					
Input Clock Rate	Full	20		1000	MHz
Conversion Rate	Full	20		125	MSPS
Clock Pulse Width High (t_{EH})	Full	4.00			ns
Clock Pulse Width Low (t_{EL})	Full	4.00			ns
OUTPUT PARAMETERS[3]					
Propagation Delay (t_{PD})[4]	Full	(t_{SAMPLE}/4) + 5	(t_{SAMPLE}/4) + 6.1	(t_{SAMPLE}/4) + 7	ns
Rise Time (t_R)[5] (20% to 80%)	Full		170		ps
Fall Time (t_F)[5] (20% to 80%)	Full		160		ps
FCO Propagation Delay (t_{FCO})[4]	Full	(t_{SAMPLE}/4) + 5	(t_{SAMPLE}/4) + 6.1	(t_{SAMPLE}/4) + 7	ns
DCO Propagation Delay (t_{CPD})[4]	Full		t_{FCO} + (t_{SAMPLE}/16) + 0.2		ns
DCO to Data Delay (t_{DATA})[4, 6]	Full	(t_{SAMPLE}/16) − 500		(t_{SAMPLE}/16) + 100	ps
FCO to DCO Delay (t_{FRAME})[4, 7]	Full	(t_{SAMPLE}/16) + 10		(t_{SAMPLE}/16) + 330	ps
Data to Data Skew	Full		±37	±80	ps
Wake-Up Time (Standby)	25°C		250		ns
Wake-Up Time (Power-Down)[8]	25°C		250		ms
Pipeline Latency	Full		16		Clock cycles
APERTURE					
Aperture Delay (t_A)[9]	25°C		1		ns
Aperture Uncertainty (Jitter, t_J[5, 9])	25°C		80		fs rms
Out-of-Range Recovery Time	25°C		1		Clock cycles

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Measured on standard FR-4 material.
[3] The Output parameters can be adjusted via the SPI. The conversion rate is the clock rate after the divider. Valid for 2-lane operation.
[4] $t_{SAMPLE} = t_{EH} + t_{EL} = 1/f_S$. t_{CPD}, t_{DATA} and t_{FRAME} are adjustable with SPI Register 0x16.
[5] This term does not appear in the Timing Diagrams section, which includes Figure 2 and Figure 3.
[6] t_{DATA} is the time from DCO rise or fall to output data rise or fall.
[7] t_{FRAME} is the time from FCO rise to DCO rise.
[8] Wake-up time from power-down is defined as the time required to return to normal operation from SPI power-down mode. The value of 250 ms assumes a sample rate of 125 MSPS. About 31 × 10^6 sample clock cycles are required.
[9] t_A and t_J are with Register 0x09 = 0x04 (default, duty cycle stabilizer and clock divider are bypassed).

TIMING SPECIFICATIONS

Table 7.

Parameter	Description	Limit	Unit
SPI TIMING REQUIREMENTS	See Figure 68, unless otherwise noted		
t_{DS}	Setup time between the data and the rising edge of SCLK	4	ns min
t_{DH}	Hold time between the data and the rising edge of SCLK	2	ns min
t_{CLK}	Period of the SCLK	40	ns min
t_S	Setup time between CSB and SCLK	2	ns min
t_H	Hold time between CSB and SCLK	2	ns min
t_{HIGH}	SCLK pulse width high	10	ns min
t_{LOW}	SCLK pulse width low	10	ns min
t_{EN_SDIO}[1]	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10	ns min
t_{DIS_SDIO}[1]	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10	ns min

[1] This parameter is not shown in Figure 68.

Timing Diagrams

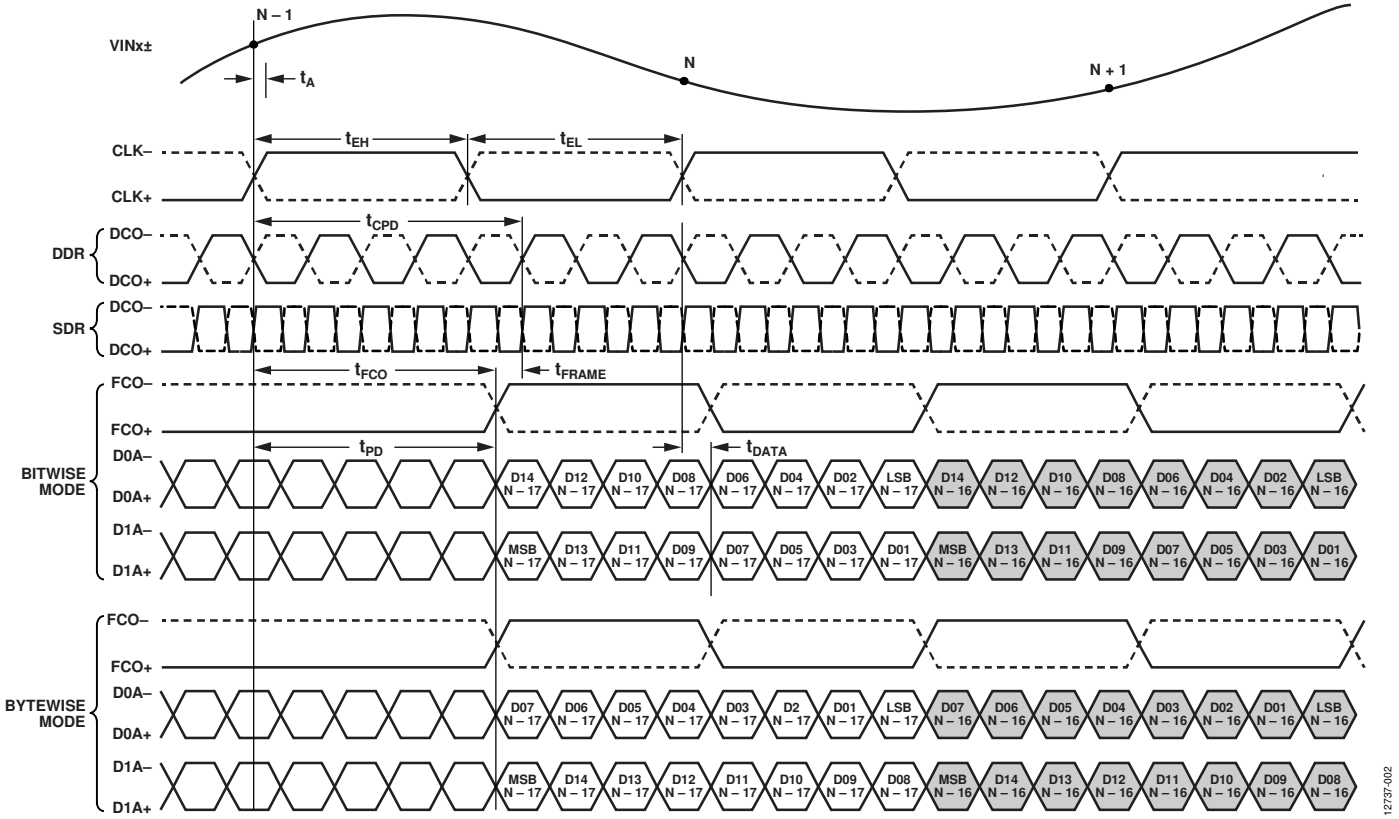

Figure 2. 16-Bit DDR/Single Data Rate (SDR), Two-Lane, 1× Frame Mode (Default)

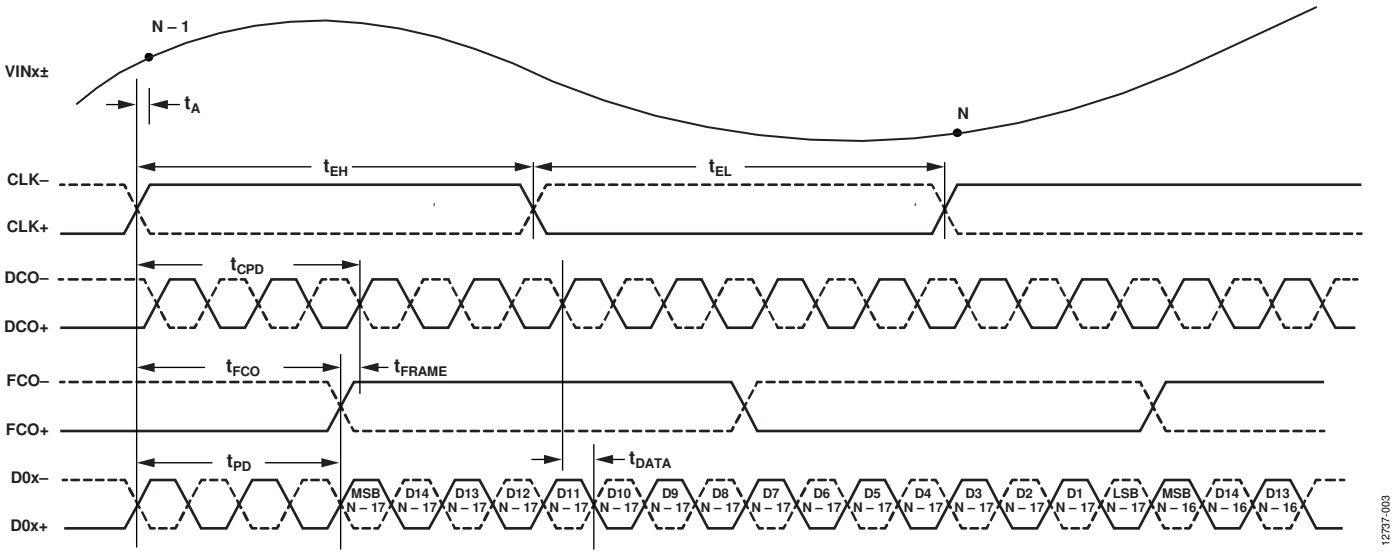

Figure 3. Wordwise DDR, One-Lane, 1× Frame, 16-Bit Output Mode

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
Digital Outputs (D0x±, D1x±, DCO±, FCO±) to AGND	−0.3 V to +2.0 V
CLK+, CLK− to AGND	−0.3 V to +2.0 V
VINx+, VINx− to AGND	−0.3 V to +2.0 V
SCLK/DFS, SDIO/PDWN, CSB to AGND	−0.3 V to +2.0 V
RBIAS to AGND	−0.3 V to +2.0 V
VREF to AGND	−0.3 V to +2.0 V
VCM to AGND	−0.3 V to +2.0 V
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

The exposed pad is the only ground connection for the chip. The exposed pad must be soldered to the AGND plane of the circuit board. Soldering the exposed pad to the board also increases the reliability of the solder joints and maximizes the thermal capability of the package.

Table 9. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JC}[1, 3]	θ_{JB}[1, 4]	Ψ_{JT}[1, 2]	Unit
32-Lead LFCSP, 5 mm × 5 mm	0	37.1	3.1	20.7	0.3	°C/W
	1.0	32.4	N/A[5]	N/A[5]	0.5	°C/W
	2.5	29.1	N/A[5]	N/A[5]	0.8	°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).
[5] N/A means not applicable.

Typical θ_{JA} is specified for a 4-layer printed circuit board (PCB) with a solid ground plane. As shown in Table 9, airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

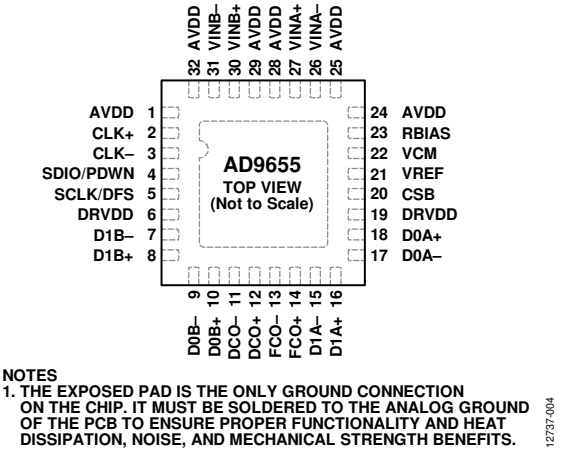

Figure 4. Pin Configuration, Top View

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
0, Exposed Pad	AGND, Exposed Pad	Exposed Pad. The exposed pad is the only ground connection on the chip. It must be soldered to the analog ground of the PCB to ensure proper functionality and heat dissipation, noise, and mechanical strength benefits.
1, 24, 25, 28, 29, 32	AVDD	1.8 V Supply Pins for the ADC Core Domain.
2, 3	CLK+, CLK–	Differential Encode Clock. These pins are PECL-, LVDS-, or 1.8 V CMOS-compatible inputs.
4	SDIO/PDWN	SPI Data Input/Output (SDIO). This pin is a bidirectional SPI data input/output with a 31 kΩ internal pull-down resistor.
		Non-SPI Mode Power-Down (PDWN). This pin provides static control of chip power-down, and has a 31 kΩ internal pull-down resistor.
5	SCLK/DFS	SPI Clock Input in SPI Mode (SCLK). This pin has a 30 kΩ internal pull-down resistor.
		Non-SPI Mode Data Format Select (DFS). This provides static control of the data output format. This pin has a 30 kΩ internal pull-down resistor. Pull DFS high for a twos complement output; pull DFS low for an offset binary output.
6, 19	DRVDD	1.8 V Supply Pins for Output Driver Domain.
7, 8	D1B–, D1B+	Channel B Lane 1 Digital Outputs.
9, 10	D0B–, D0B+	Channel B Lane 0 Digital Outputs.
11, 12	DCO–, DCO+	Data Clock Outputs.
13, 14	FCO–, FCO+	Frame Clock Outputs.
15, 16	D1A–, D1A+	Channel A Lane 1 Digital Outputs.
17, 18	D0A–, D0A+	Channel A Lane 0 Digital Outputs.
20	CSB	SPI Chip Select. Active low enable; this pin has a 15 kΩ internal pull-up resistor.
21	VREF	1.0 V to 1.4 V Voltage Reference Output. Bypass this pin to ground with a 1.0 µF capacitor in parallel with a 0.1 µF capacitor; this pin internally provides reference voltage to the ADC. This pin can be disabled via Register 0x114 if external V_{REF} is desired.
22	VCM	Analog Output Voltage at Mid AVDD Supply. Bypass this pin to ground with a 0.1 µF capacitor; this pin can be used to set the common mode of the analog inputs externally.
23	RBIAS	Sets Analog Current Bias. Connect this pin to a 10.0 kΩ (1% tolerance) resistor to ground.
26, 27	VINA–, VINA+	Channel A ADC Analog Inputs.
30, 31	VINB+, VINB–	Channel B ADC Analog Inputs.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{REF} = 1.0 V

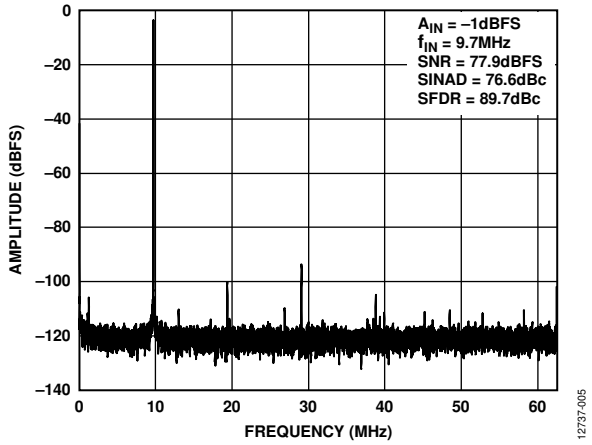

Figure 5. Single-Tone 32k FFT with f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

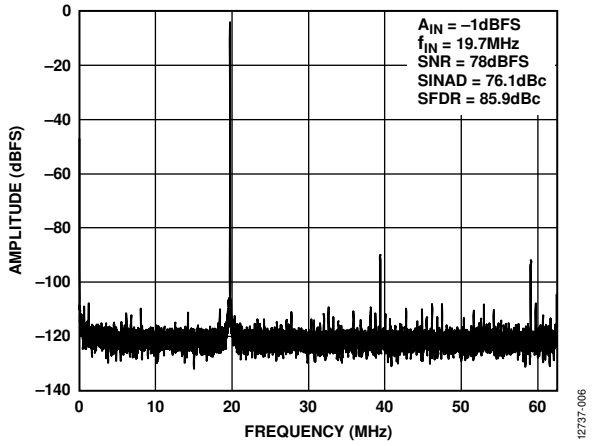

Figure 6. Single-Tone 32k FFT with f_{IN} = 19.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

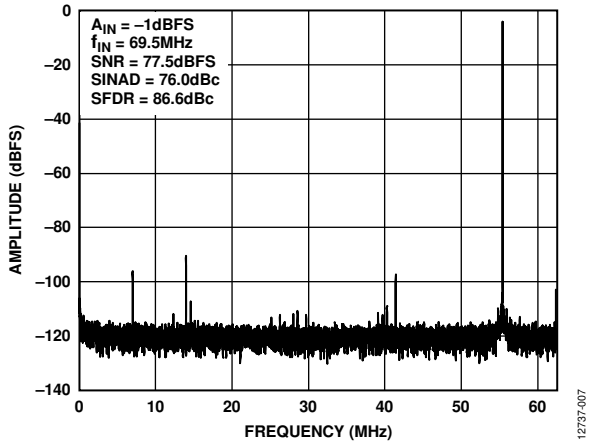

Figure 7. Single-Tone 32k FFT with f_{IN} = 69.5 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

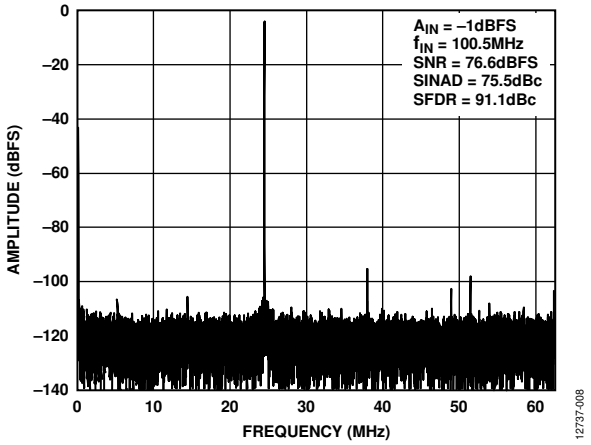

Figure 8. Single-Tone 32k FFT with f_{IN} = 100.5 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

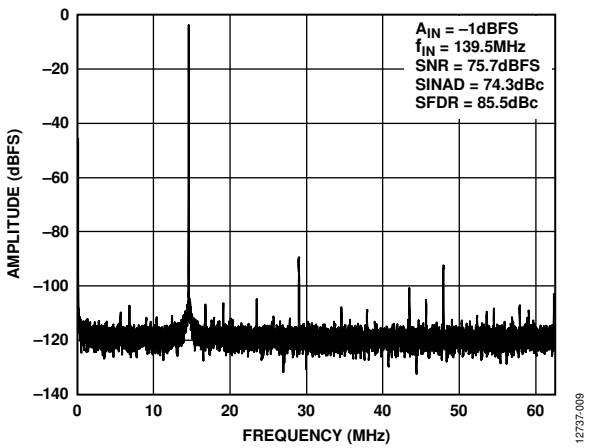

Figure 9. Single-Tone 32k FFT with f_{IN} = 139.5 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

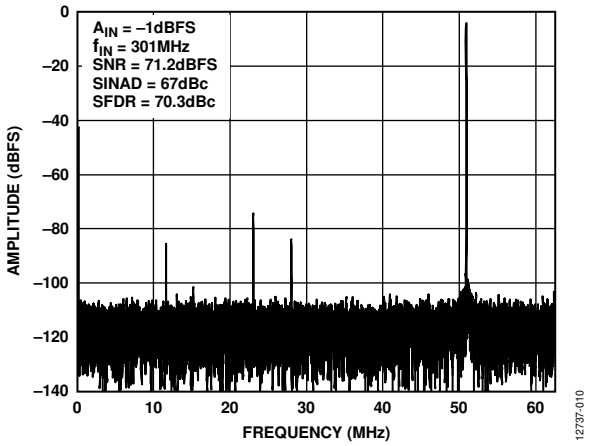

Figure 10. Single-Tone 32k FFT with f_{IN} = 301 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

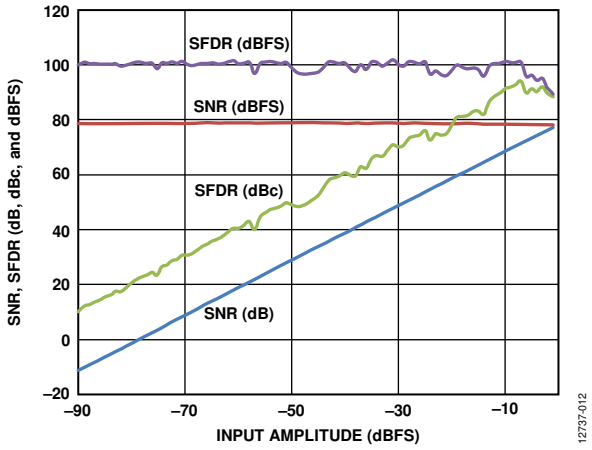

Figure 11. SNR, SFDR vs. Input Amplitude; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

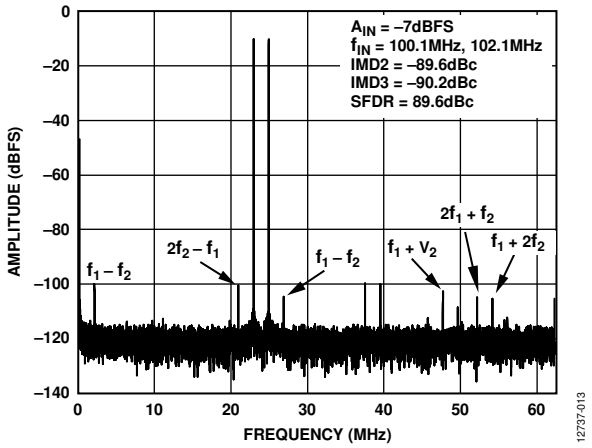

Figure 12. Two-Tone 32k FFT with f_{IN1} = 100.1 MHz and f_{IN2} = 102.1 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

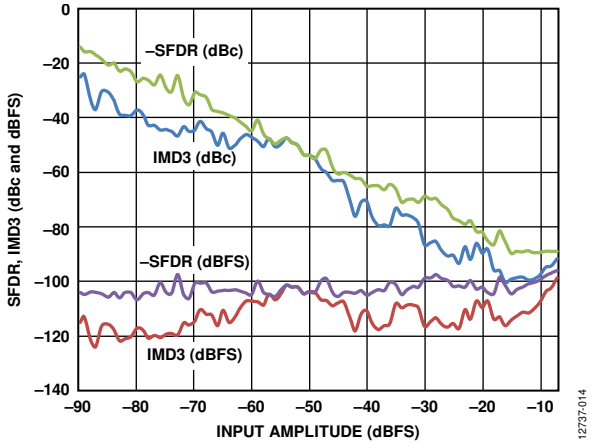

Figure 13. Two-Tone SFDR, IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 100.1 MHz and f_{IN2} = 102.1 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

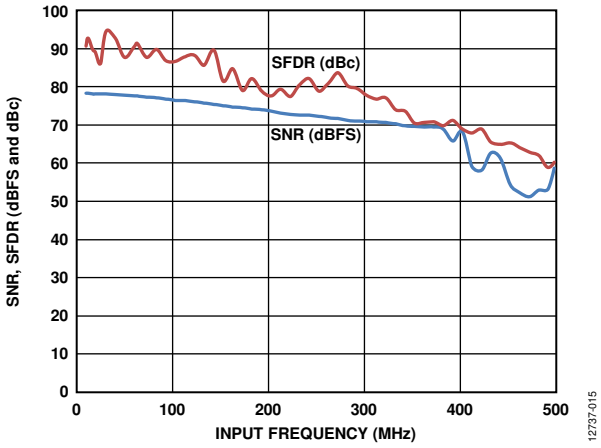

Figure 14. SNR, SFDR vs. Input Frequency (f_{IN}); f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

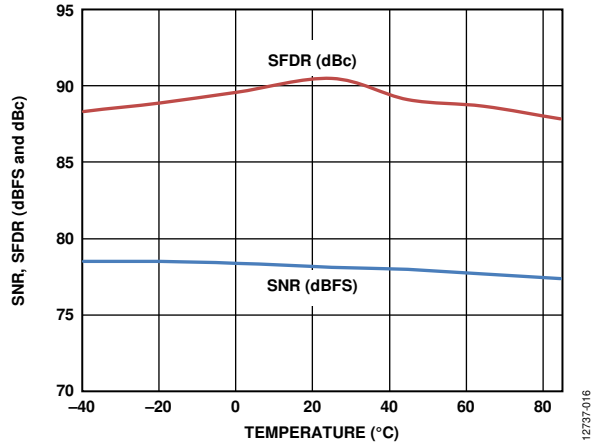

Figure 15. SNR, SFDR vs. Temperature; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

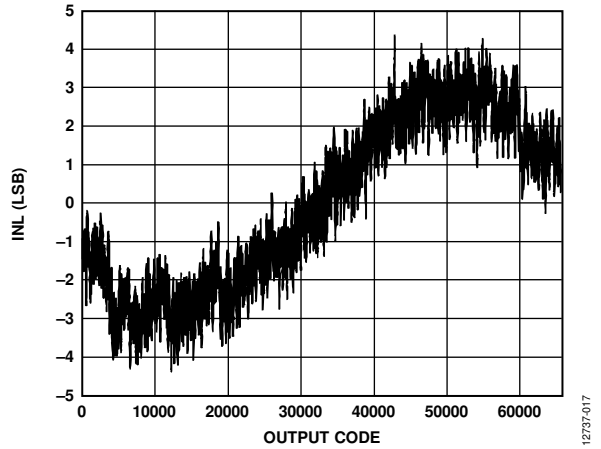

Figure 16. INL; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

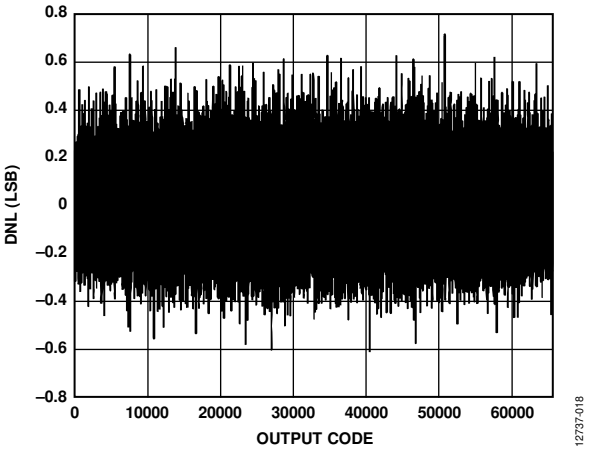

Figure 17. DNL; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

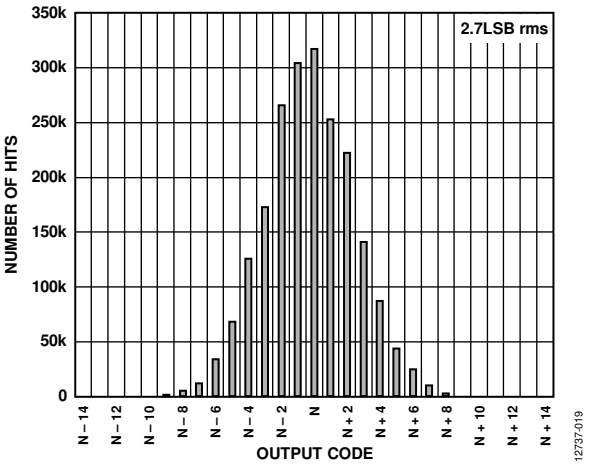

Figure 18. Input Referred Noise Histogram; f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

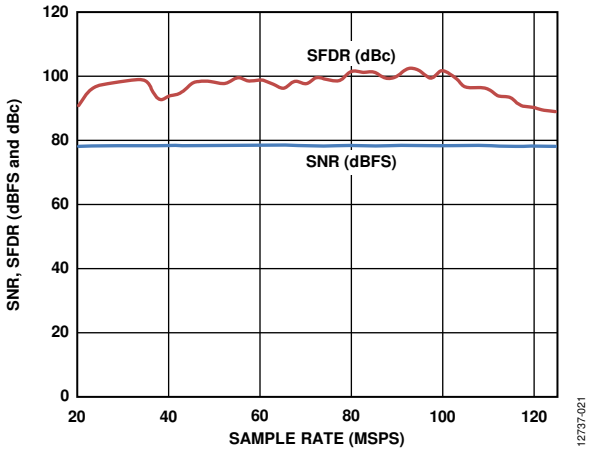

Figure 19. SNR, SFDR vs. Sample Rate; f_{IN} = 9.7 MHz, V_{REF} = 1.0 V

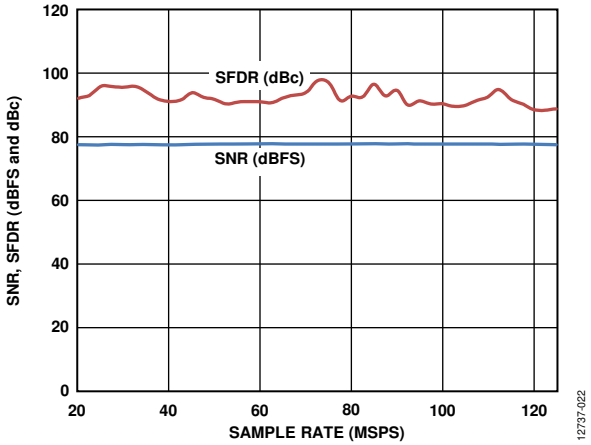

Figure 20. SNR, SFDR vs. Sample Rate; f_{IN} = 69.5 MHz, V_{REF} = 1.0 V, Clock Divider = 4

V_{REF} = 1.4 V

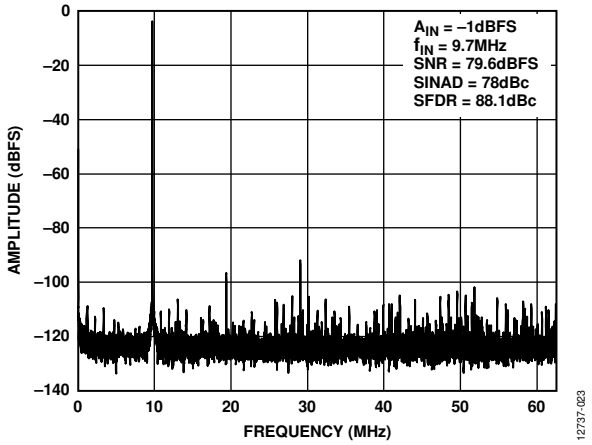

Figure 21. Single-Tone 32k FFT with f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

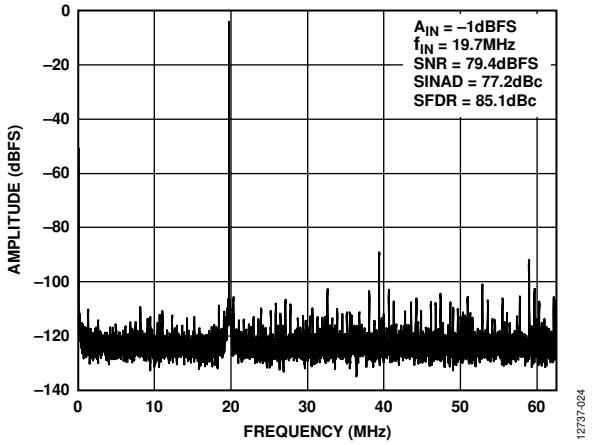

Figure 22. Single-Tone 32k FFT with f_{IN} = 19.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

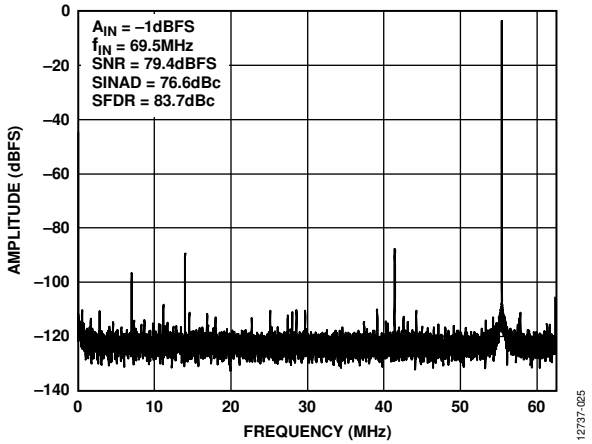

Figure 23. Single-Tone 32k FFT with f_{IN} = 69.5 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

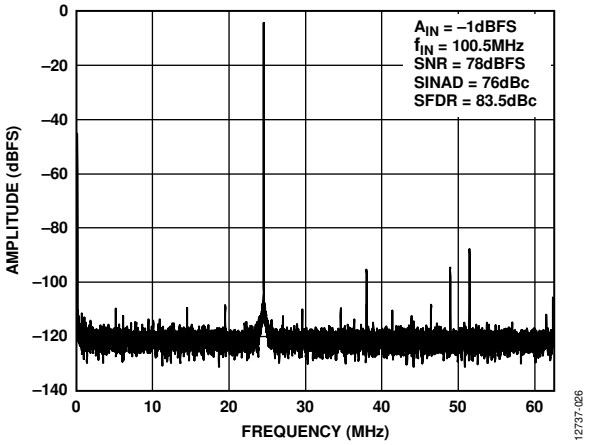

Figure 24. Single-Tone 32k FFT with f_{IN} = 100.5 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

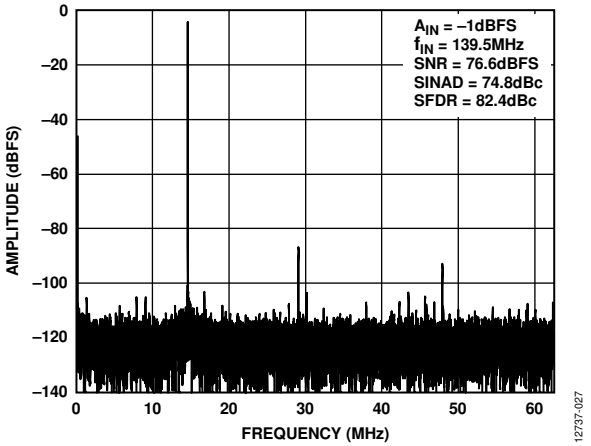

Figure 25. Single-Tone 32k FFT with f_{IN} = 139.5 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

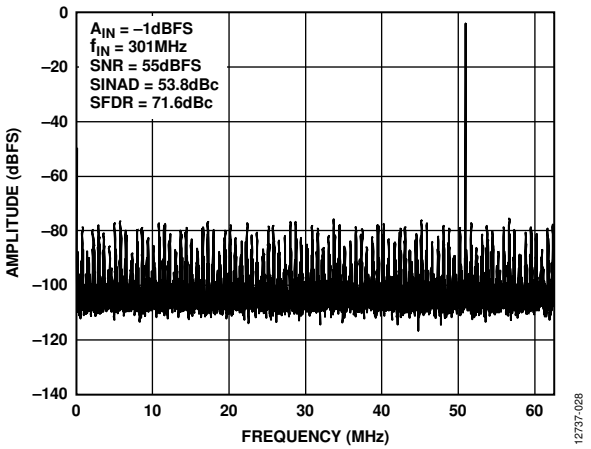

Figure 26. Single-Tone 32k FFT with f_{IN} = 301 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

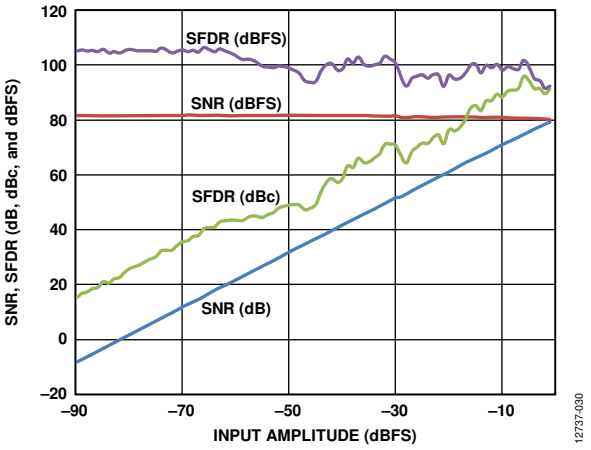

Figure 27. SNR, SFDR vs. Input Amplitude; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

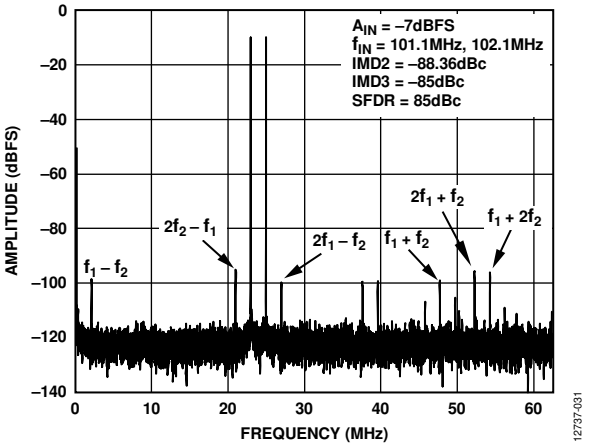

Figure 28. Two-Tone 32k FFT with f_{IN1} = 100.1 MHz and f_{IN2} = 102.1 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

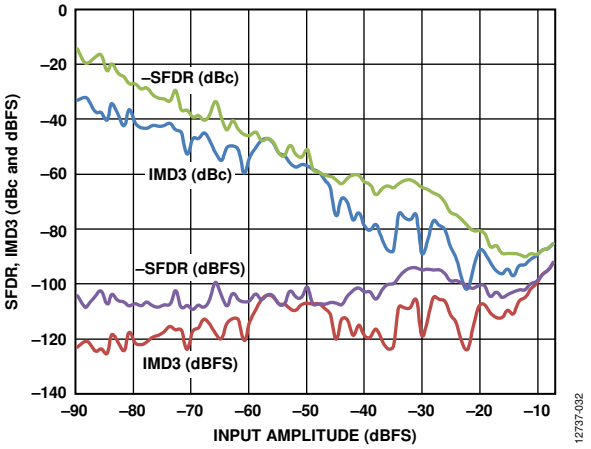

Figure 29. Two-Tone SFDR, IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 100.1 MHz and f_{IN2} = 102.1 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

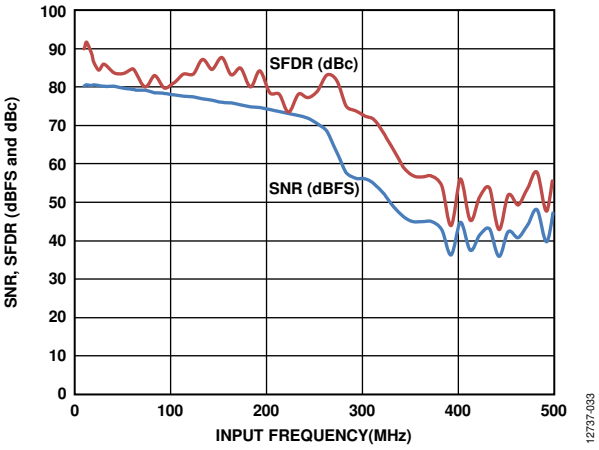

Figure 30. SNR, SFDR vs. Input Frequency (f_{IN}); f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

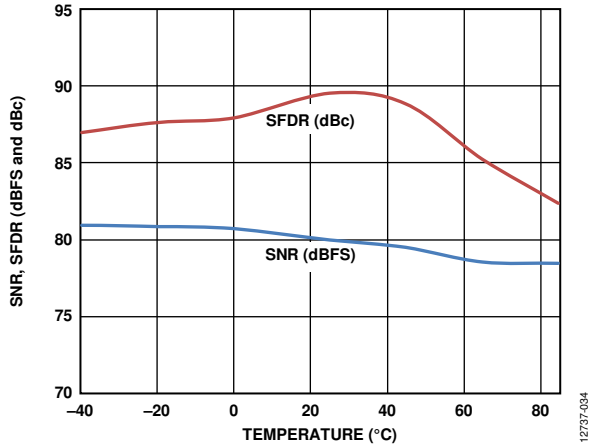

Figure 31. SNR, SFDR vs. Temperature; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

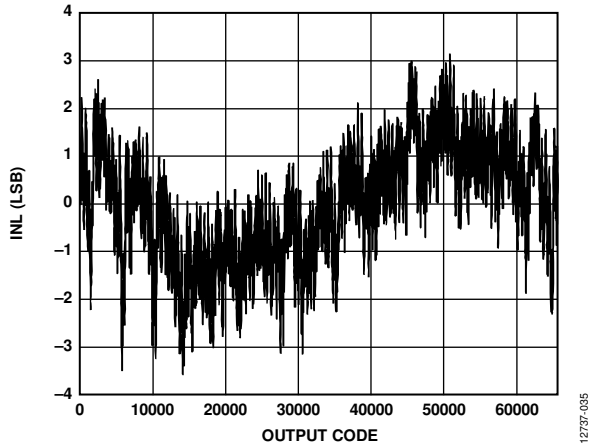

Figure 32. INL; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

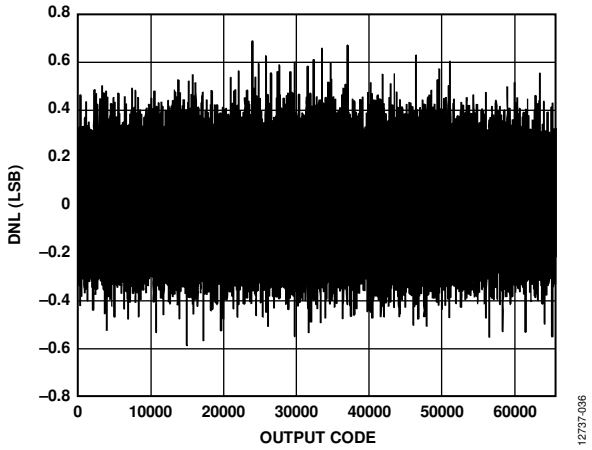

Figure 33. DNL; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

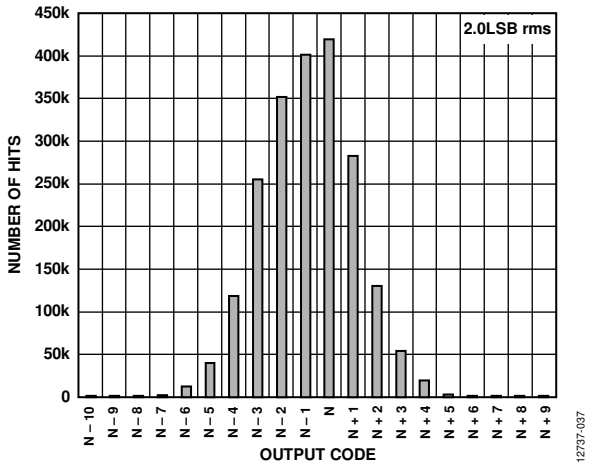

Figure 34. Input Referred Noise Histogram; f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

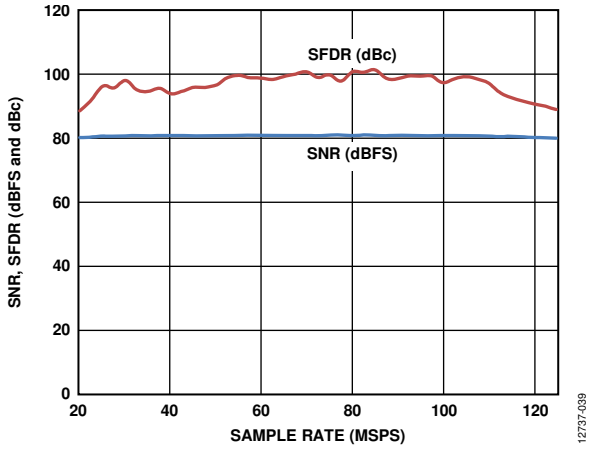

Figure 35. SNR, SFDR vs. Sample Rate; f_{IN} = 9.7 MHz, V_{REF} = 1.4 V

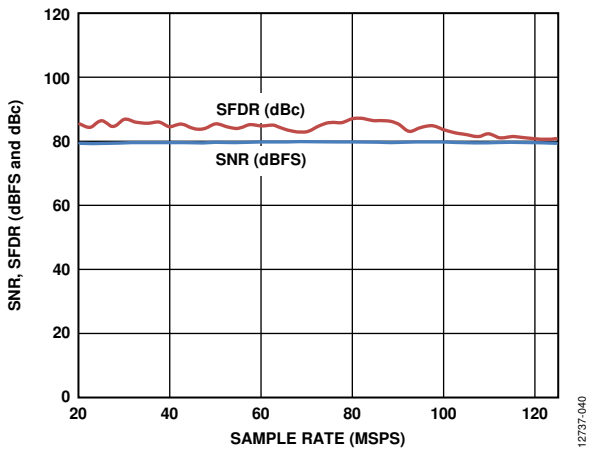

Figure 36. SNR, SFDR vs. Sample Rate; f_{IN} = 69.5 MHz, V_{REF} = 1.4 V, Clock Divider = 4

EQUIVALENT CIRCUITS

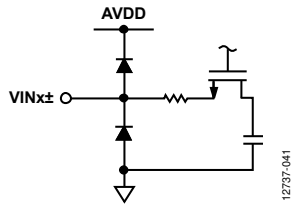

Figure 37. Equivalent Analog Input Circuit

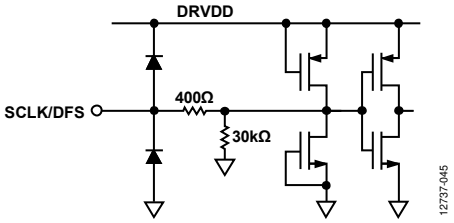

Figure 41. Equivalent SCLK/DFS Input Circuit

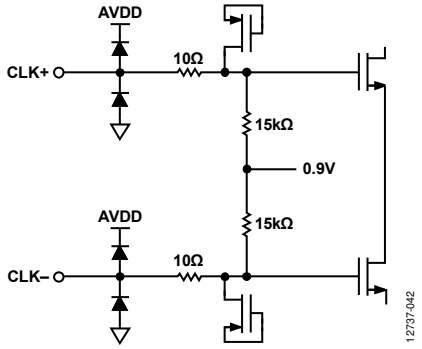

Figure 38. Equivalent Clock Input Circuit

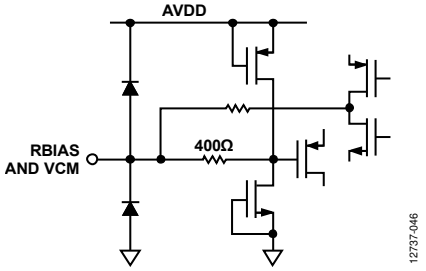

Figure 42. Equivalent RBIAS and VCM Circuit

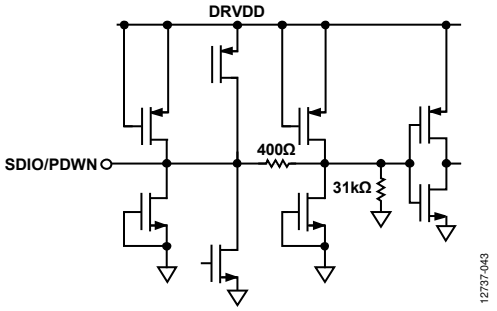

Figure 39. Equivalent SDIO/PDWN Input Circuit

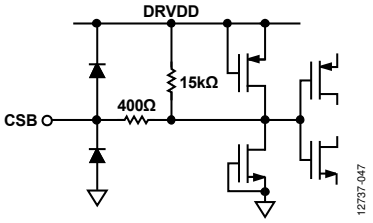

Figure 43. Equivalent CSB Input Circuit

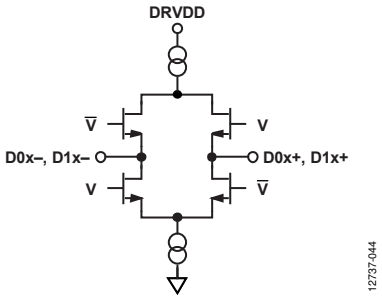

Figure 40. Equivalent Digital Output Circuit

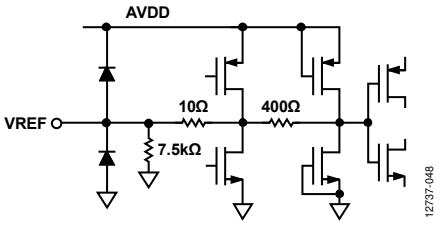

Figure 44. Equivalent VREF Circuit

THEORY OF OPERATION

The AD9655 is a multistage, pipelined ADC. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 16-bit result in the digital correction logic. The serializer transmits this converted data in a 16-bit output. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and an interstage residue amplifier, for example, a multiplying digital-to-analog converter (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy in each stage facilitates digital correction of flash errors. The last stage consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers. Then, the data is serialized and aligned to the frame and data clocks.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9655 is a differential switched capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. By using an input common-mode voltage of midsupply, users can minimize signal dependent errors and achieve optimum performance.

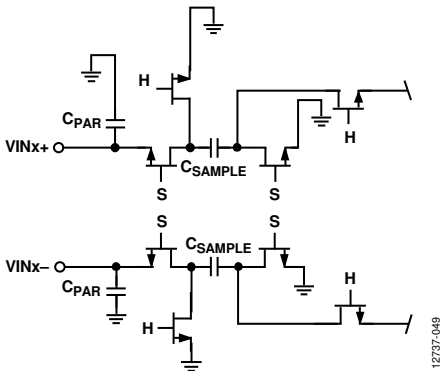

Figure 45. Switched Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample mode and hold mode (see Figure 45). When the input circuit switches to sample mode, the signal source must be capable of charging the sample capacitors and settling within one half of a clock cycle.

A small resistor in series with each input can help reduce the peak transient current injected from the output stage of the driving source. A differential capacitor, two single-ended capacitors, or a combination of these capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005) for more information. In general, the precise values depend on the application.

Input Common Mode

The AD9655 analog inputs are not internally dc-biased. Therefore, in ac-coupled applications, the user must provide this bias externally. Setting the device so that V_{CM} = AVDD/2 is recommended for optimum performance, but the device can function over a wider range with reasonable performance, as shown in Figure 46 and Figure 47.

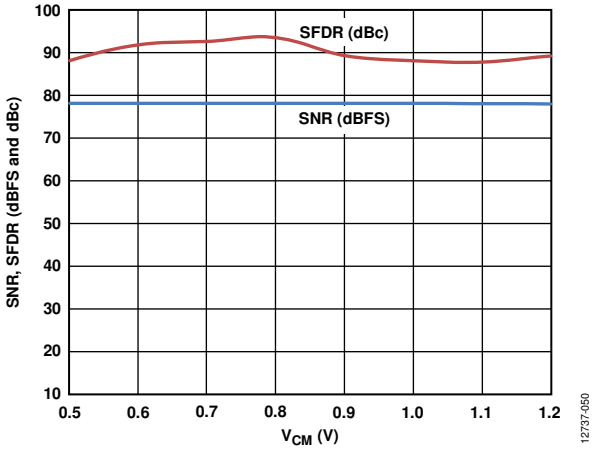

Figure 46. SNR, SFDR vs. Input Common-Mode Voltage (V_{CM}), f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

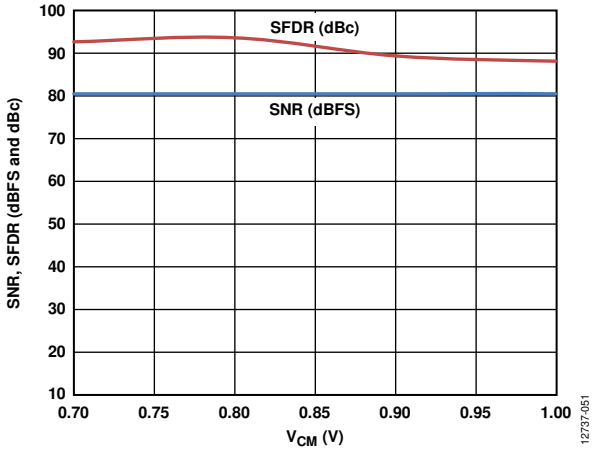

Figure 47. SNR, SFDR vs. Input Common-Mode Voltage (V_{CM}), f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

An on-chip, common-mode dc voltage reference is included in the design and is available from the VCM pin. The VCM pin must be bypassed to ground by a 0.1 µF capacitor, as described in the Applications Information section. VCM error vs. load current is shown in Figure 48.

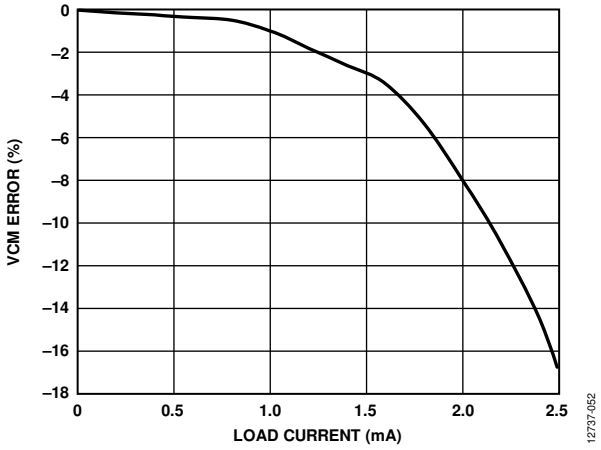

Figure 48. VCM Error vs. Load Current

Differential Input Configurations

There are several ways to drive the AD9655 either actively or passively. However, optimum performance is achieved by driving the analog inputs differentially. Using a differential double balun configuration to drive the AD9655 provides excellent performance and a flexible interface to the ADC for baseband applications (see Figure 53).

For applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration (see Figure 54) because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9655.

Regardless of the configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

It is not recommended to drive the AD9655 inputs single-ended.

VOLTAGE REFERENCE

A stable and accurate 1.0 V to 1.4 V dc voltage reference is built into the AD9655. Externally bypass the VREF pin to ground with a low ESR, 1.0 µF capacitor in parallel with a low ESR, 0.1 µF ceramic capacitor.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9655, the largest input span available is 2.8 V p-p, which is achieved by setting V_{REF} to 1.4 V.

If the internal reference of the AD9655 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 49 and Figure 50 show how the internal reference voltage is affected by loading. It is recommended that VREF not be used to drive the reference voltage of other devices at 1.4 V. Figure 51 and Figure 52 show the typical drift characteristics of the internal reference.

The internal buffer generates the positive and negative full-scale references for the ADC core. A digital reset using Register 0x08 must follow any programmatic change in internal analog V_{REF}.

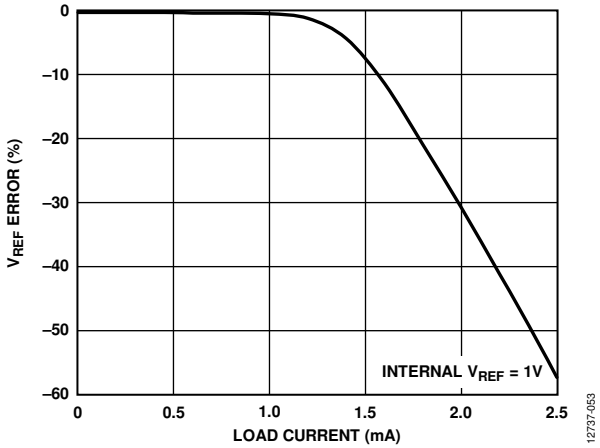

Figure 49. V_{REF} Error vs. Load Current, V_{REF} = 1.0 V

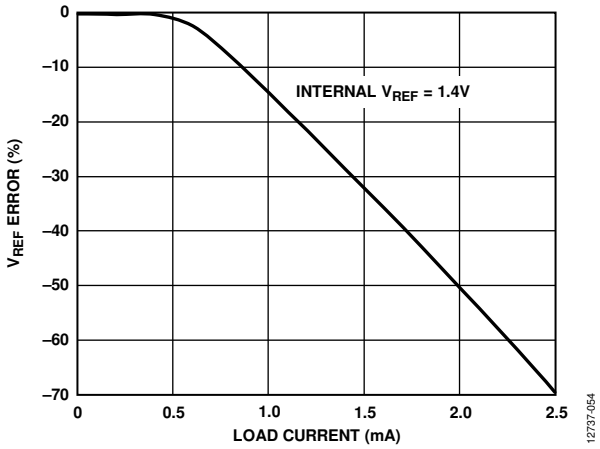

Figure 50. V_{REF} Error vs. Load Current, V_{REF} = 1.4 V

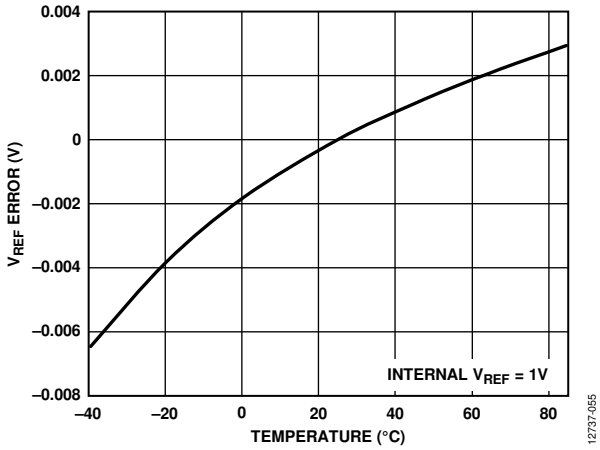

Figure 51. Typical V_{REF} Drift, V_{REF} = 1.0 V

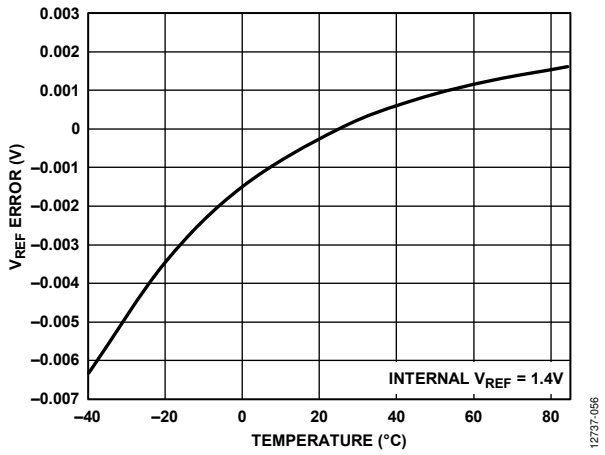

Figure 52. Typical V_{REF} Drift, V_{REF} = 1.4 V

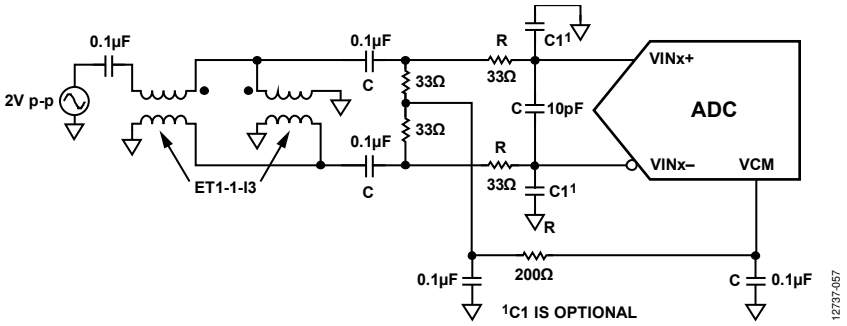

Figure 53. Differential Double Balun Input Configuration for Baseband Applications

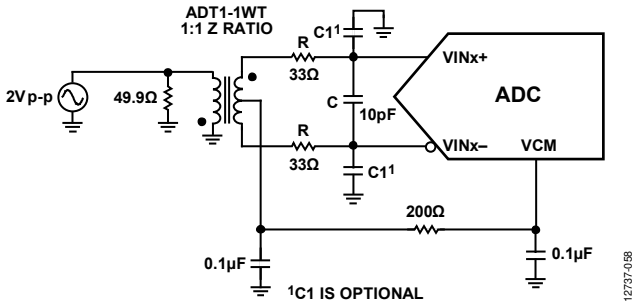

Figure 54. Differential Transformer Coupled Configuration for Baseband Applications

CLOCK INPUT CONSIDERATIONS

For optimum performance, clock the AD9655 sample clock inputs, CLK+ and CLK−, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK− pins via a transformer or capacitors. These pins are biased internally (see Figure 38) and require no external bias.

Clock Input Options

The AD9655 has a flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal used, clock source jitter is an important consideration, as described in the Jitter Considerations section.

Figure 55 and Figure 56 show two preferred methods for clocking the AD9655 at clock rates up to 1 GHz prior to the internal clock divider. A low jitter clock source is converted from a single-ended signal to a differential signal using either a radio frequency (RF) transformer or an RF balun.

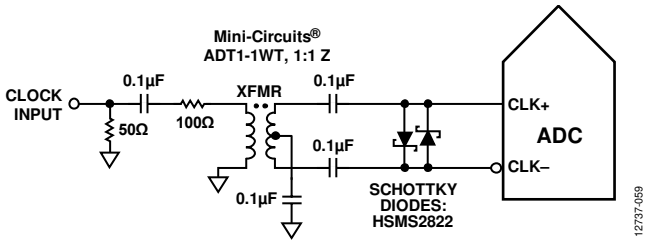

Figure 55. Transformer Coupled Differential Clock (Up to 200 MHz)

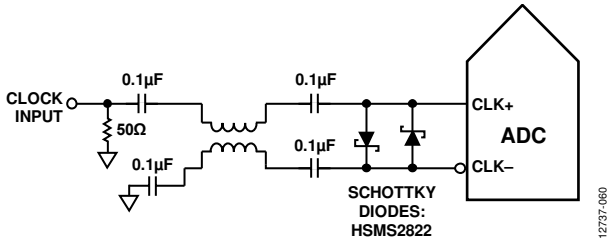

Figure 56. Balun-Coupled Differential Clock (Up to 1 GHz)

The RF balun configuration is recommended for clock frequencies between 125 MHz and 1 GHz, and the RF transformer configuration is recommended for clock frequencies from 20 MHz to 200 MHz. The antiparallel Schottky diodes across the transformer/balun secondary winding limit clock excursions into the AD9655 to approximately 0.8 V p-p differential.

This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9655 while preserving the fast rise and fall times of the signal that are critical to achieving low jitter performance. However, the diode capacitance comes into play at frequencies above 500 MHz. Care must be taken when choosing the appropriate signal limiting diode.

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 57. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517 clock drivers, noted as AD951x in Figure 57, Figure 58, and Figure 59, offer excellent jitter performance.

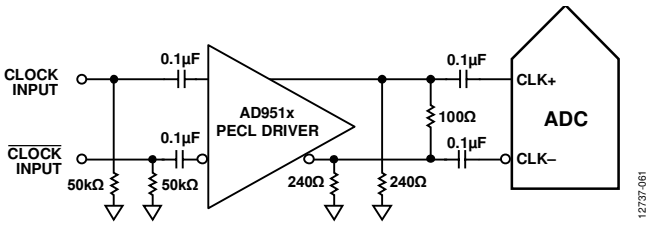

Figure 57. Differential PECL Sample Clock (Up to 1 GHz)

A third option is to ac couple a differential LVDS signal to the sample clock input pins, as shown in Figure 58. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517 clock drivers offer excellent jitter performance.

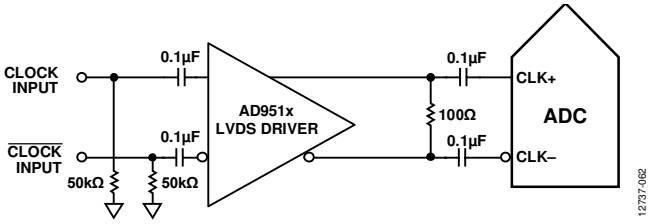

Figure 58. Differential LVDS Sample Clock (Up to 1 GHz)

In some applications, it may be acceptable to drive the sample clock inputs with a single-ended 1.8 V CMOS signal. In such applications, drive the CLK+ pin directly from a CMOS gate, and bypass the CLK− pin to ground with a 0.1 µF capacitor (see Figure 59).

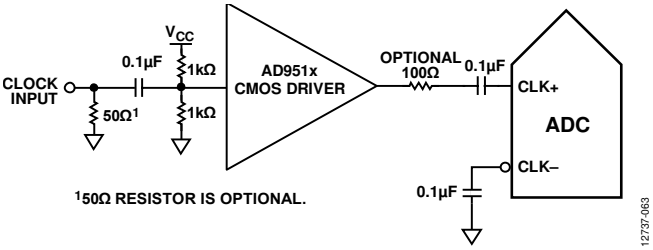

Figure 59. Single-Ended 1.8 V CMOS Input Clock (Up to 200 MHz)

Input Clock Divider

The AD9655 contains an input clock divider that can divide the input clock by integer values from 1 to 8. To achieve a given sample rate, the frequency of the externally applied clock must be multiplied by the divide value. The increased rate of the external clock normally results in lower clock jitter, which is beneficial for intermediate frequency (IF) undersampling applications.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to the clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9655 contains a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD9655. Noise and distortion performance are nearly flat for a wide range of duty cycles with the DCS on.

Jitter in the rising edge of the clock is still of concern and is not easily reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates of less than 20 MHz, nominally. The loop has a time constant associated with it that must be considered in applications in which the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The following equation shows how SNR degrades at a given input frequency (f_A) due only to aperture jitter (t_J):

$$SNR\ Degradation = 20 \log_{10}\left(\frac{1}{2\pi \times f_A \times t_J}\right)$$

In this equation, the rms aperture jitter represents the root sum square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter. The effect of jitter alone on SNR, with no other noise contributors, is shown in Figure 60.

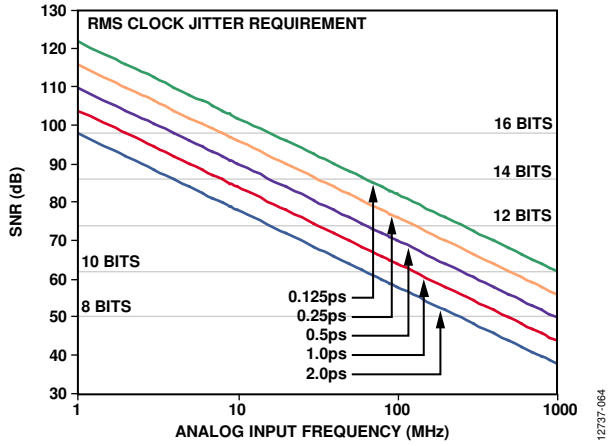

Figure 60. Ideal SNR vs. Analog Input Frequency and Jitter

Treat the clock input as an analog signal when aperture jitter may affect the dynamic range of the AD9655. Separate clock driver power supplies from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal controlled oscillators are the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it is recommended that the clock be retimed by the original clock as the last step.

See the AN-501 Application Note and the AN-756 Application Note for more information about jitter performance as it relates to ADCs.

POWER DISSIPATION AND POWER-DOWN MODE

As shown in Figure 61, the power dissipated by the AD9655 is proportional to its sample rate. The AD9655 is placed in power-down mode either by the SPI port or by asserting the SDIO/PDWN pin high when in non-SPI mode. In this state, the ADC typically dissipates 2 mW. During power-down, the output drivers are placed in a high impedance state. In non-SPI mode, asserting the SDIO/PDWN pin low returns the AD9655 to its normal operating mode. Note that SDIO/PDWN is referenced to the digital output driver supply (DRVDD) and must not exceed that supply voltage.

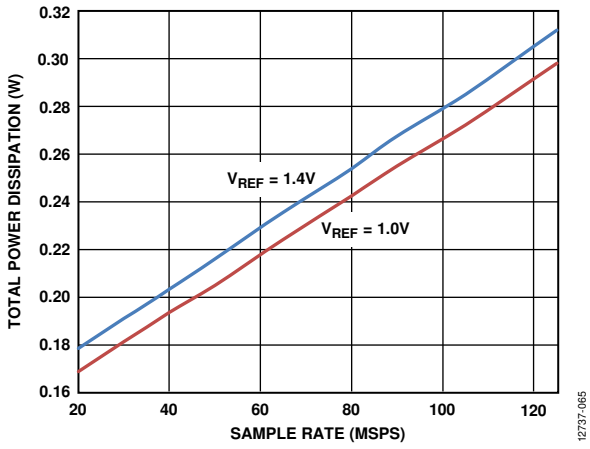

Figure 61. Total Power Dissipation vs. Sample Rate (f_{SAMPLE}) for f_{IN} = 9.7 MHz, V_{REF} = 1.0 V and V_{REF} = 1.4 V

The AD9655 achieves low power dissipation in power-down mode by shutting down the reference, reference buffer, biasing networks, and clock. When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. Do not invoke standby mode while foreground calibration is in progress. Foreground calibration is invoked automatically at power-up, and by executing a digital reset with Register 0x08. Completion is indicated by the contents of Register 0x107 = 0x00. See the Memory Map section for more details on using these features.

DIGITAL OUTPUTS AND TIMING

The AD9655 differential outputs conform to the ANSI-644 LVDS standard on default power-up. This default setting can be changed to a low power, reduced signal option (similar to the IEEE 1596.3 standard) via the SPI. The LVDS driver current is derived on chip and sets the output current at each output equal to a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing (or 700 mV p-p differential) at the receiver.

When operating in reduced range mode, the output current reduces to 2 mA. This results in a 200 mV swing (or 400 mV p-p differential) across a 100 Ω termination at the receiver.

The LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor placed as close as possible to the receiver. Timing errors may result if there is no far-end receiver termination, or if there is poor differential trace routing. To avoid such timing errors, ensure that the trace length is less than 24 inches and that the differential output traces are close together and at equal lengths.

Figure 62 shows an example of the FCO and data stream with proper trace length and position.

Figure 63 shows the LVDS output timing example in reduced range mode.

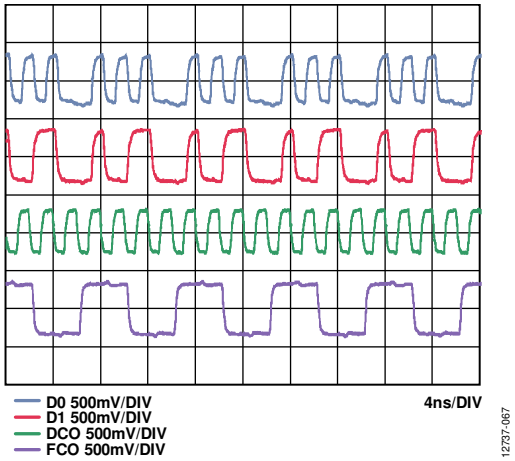

Figure 62. LVDS Output Timing Example in ANSI-644 Mode (Default)

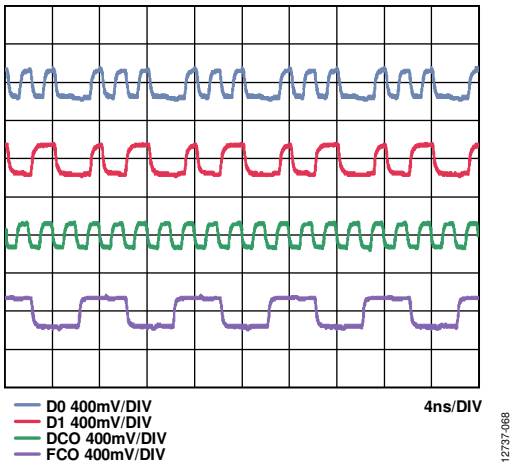

Figure 63. LVDS Output Timing Example in Reduced Range Mode