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Octal Ultrasound AFE with Digital Demodulator

Data Sheet

AD9670

FEATURES

- 8 channels of LNA, VGA, antialiasing filter, ADC, and digital demodulator/decimator
  - Low power
    - 150 mW per channel, time gain compensation (TGC) mode, 40 MSPS
    - 62.5 mW per channel, continuous wave (CW) mode; <30 mW in power-down mode
  - 10 mm × 10 mm, 144-ball CSP_BGA
- TGC channel, input referred noise voltage: 0.82 nV/√Hz, maximum gain
- Flexible power-down modes
- Fast recovery from low power standby mode: <2 µs
- Low noise preamplifier (LNA)
  - Input noise voltage: 0.78 nV/√Hz, gain = 21.6 dB
  - Programmable gain: 15.6 dB/17.9 dB/21.6 dB
  - 0.1 dB input compression point: 1.00 V p-p/0.75 V p-p/0.45 V p-p
  - Flexible active input impedance matching
- Variable gain amplifier (VGA)
  - Attenuator range: 45 dB, linear-in-dB gain control
  - Postamplifier gain (PGA): 21 dB/24 dB/27 dB/30 dB
- Antialiasing filter
  - Programmable, second-order low-pass filter from 8 MHz to 18 MHz or 13.5 MHz to 30 MHz and high-pass filter
- Analog-to-digital converter (ADC)
  - Signal-to-noise ratio (SNR): 75 dB, 14 bits up to 125 MSPS
- Configurable serial low voltage differential signaling (LVDS)
- CW mode harmonic rejection I/Q demodulator
  - Individual programmable phase rotation
  - Dynamic range per channel: >160 dBFS/√Hz
  - Close in SNR: 156 dBc/√Hz, 1 kHz offset, −3 dBFS
- Digital demodulator/decimator
  - I/Q demodulator with programmable oscillator FIR decimation filter

APPLICATIONS

- Medical imaging/ultrasound
- Nondestructive testing (NDT)

GENERAL DESCRIPTION

The AD9670 is designed for low cost, low power, small size, and ease of use for medical ultrasound applications. It contains eight channels of a VGA with an LNA, a CW harmonic rejection I/Q demodulator with programmable phase rotation, an antialiasing filter, an ADC, and a digital demodulator and decimator for data processing and bandwidth reduction.

Each channel features a maximum gain of up to 52 dB, a fully differential signal path, and an active input preamplifier termination. The channel is optimized for high dynamic performance and low power in applications where a small package size is critical.

The LNA has a single-ended-to-differential gain that is selectable through the serial port interface (SPI). Assuming a 15 MHz noise bandwidth (NBW) and a 21.6 dB LNA gain, the LNA input SNR is 94 dB. In CW Doppler mode, each LNA output drives an I/Q demodulator that has independently programmable phase rotation with 16 phase settings.

Power-down of individual channels is supported to increase battery life for portable applications. Standby mode allows quick power-up for power cycling. In CW Doppler operation, the VGA, antialiasing filter, and ADC are powered down. The ADC contains several features designed to maximize flexibility and minimize system cost, such as a programmable clock, data alignment, and programmable digital test pattern generation. The digital test patterns include built-in fixed patterns, built-in pseudorandom patterns, and custom user-defined test patterns entered via the SPI.

Rev. A
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COMPARABLE PARTS

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EVALUATION KITS

- AD9670 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9670: Octal Ultrasound AFE with Digital Demodulator Data Sheet

REFERENCE MATERIALS

Press

- Industry's First Octal Ultrasound Receiver with Digital I/Q Demodulator and Decimation Filter Reduces Processor Overhead in Ultrasound Systems
- Industry's First Octal Ultrasound Receiver with JESD204B Serial Interface Reduces Data I/O Routing and Simplifies Ultrasound System Design
- Low Cost, Octal Ultrasound Receiver with On-Chip RF Decimator and JESD204B Serial Interface

DESIGN RESOURCES

- AD9670 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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REVISION HISTORY

2/16—Revision A: Initial Version

FUNCTIONAL BLOCK DIAGRAM

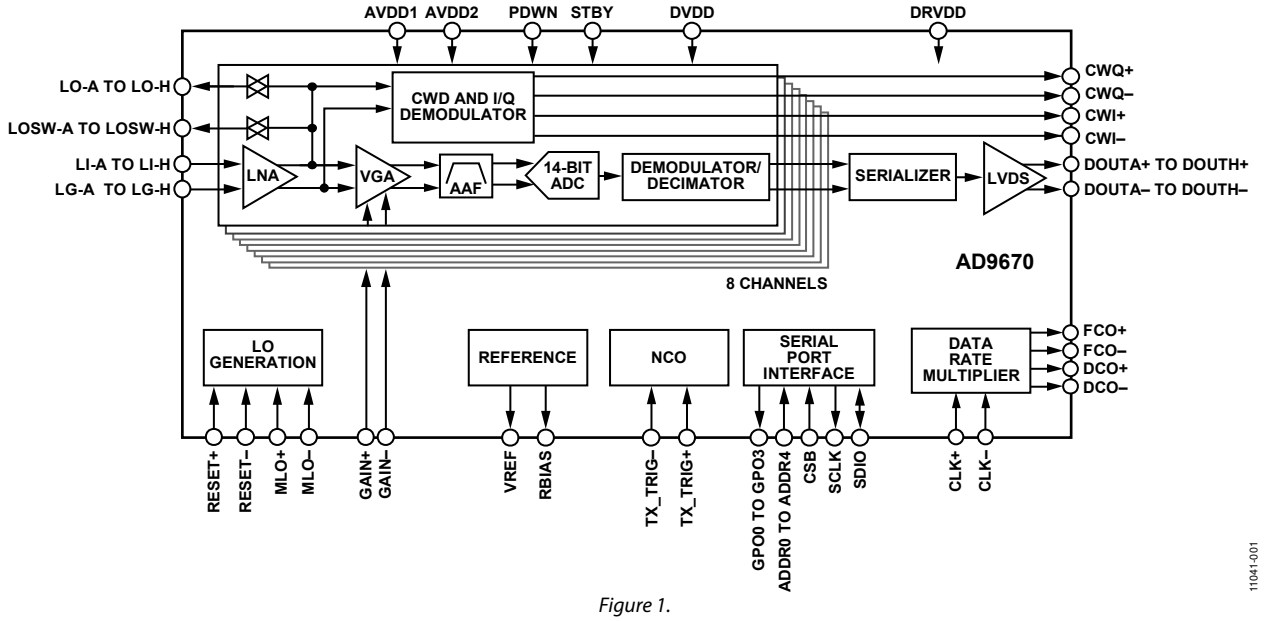

Figure 1.

SPECIFICATIONS

AC SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.0 V, DVDD = 1.4 V, DRVDD = 1.8 V, 1.0 V internal ADC reference, full temperature range (0°C to 85°C), f_{IN} = 5 MHz, local oscillator (LO) band mode, R_S = 50 Ω, R_{FB} = ∞ (unterminated), LNA gain = 21.6 dB, LNA bias = midhigh, PGA gain = 27 dB, analog gain control, VGAIN = (GAIN+) − (GAIN−) = 1.6 V, antialiasing filter, low-pass filter (LPF) cutoff = f_{SAMPLE}/3 in Mode I/Mode II, antialiasing filter LPF cutoff = f_{SAMPLE} /4.5 in Mode III/Mode IV, high-pass filter (HPF) cutoff = LPF cutoff/12.00, Mode I = f_{SAMPLE} = 40 MSPS, Mode II = f_{SAMPLE} = 65 MSPS, Mode III = f_{SAMPLE} = 80 MSPS, Mode IV = 125 MSPS, radio frequency (RF) decimator bypassed, digital demodulator and baseband decimator bypassed, digital high-pass filter bypassed, low power LVDS mode, unless otherwise noted. All gain setting options are listed, which can be configured via SPI registers, and all power supply currents and power dissipations are listed for the four mode settings (Mode I, Mode II, Mode III, and Mode IV), respectively, via slashes in Table 1.

Table 1.

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
LNA CHARACTERISTICS					
Gain	Single-ended input to differential output		15.6/17.9/21.6		dB
	Single-ended input to single-ended output		9.6/11.9/15.6		dB
0.1 dB Input Compression Point	LNA gain = 15.6 dB		1.00		V p-p
	LNA gain = 17.9 dB		0.75		V p-p
	LNA gain = 21.6 dB		0.45		V p-p
1 dB Input Compression Point	LNA gain = 15.6 dB		1.20		V p-p
	LNA gain = 17.9 dB		0.90		V p-p
	LNA gain = 21.6 dB		0.60		V p-p
Input Common Mode (LI-x, LG-x)			2.2		V
Output Common Mode					
LO-x	Switch off		High-Z		Ω
	Switch on		1.5		V
LOSW-x	Switch off		High-Z		Ω
	Switch on		1.5		V
Input Resistance (LI-x)	R_{FB} = 300 Ω		50		Ω
	R_{FB} = 1350 Ω		200		Ω
			6		kΩ
Input Capacitance (LI-x)			20		pF
Input Noise Voltage	R_S = 0 Ω				
	LNA gain = 15.6 dB		0.83		nV/√Hz
	LNA gain = 17.9 dB		0.82		nV/√Hz
	LNA gain = 21.6 dB		0.78		nV/√Hz
Input Noise Current			2.6		pA/√Hz
FULL CHANNEL (TGC) CHARACTERISTICS					
Antialiasing Filter Low-Pass Cutoff	−3 dB, programmable, low band mode	8		18	MHz
	−3 dB, programmable, high band mode	13.5		30	MHz
In Range Antialiasing Filter Bandwidth Tolerance			±10		%
Group Delay Variation	f = 1 MHz to 18 MHz, V_{GAIN} = −1.6 V to +1.6 V		±350		ps
Input Referred Noise Voltage	LNA gain = 15.6 dB		0.96		nV/√Hz
	LNA gain = 17.9 dB		0.90		nV/√Hz
	LNA gain = 21.6 dB		0.82		nV/√Hz
Noise Figure	R_S = 50 Ω				
Active Termination Matched	LNA gain = 15.6 dB, R_{FB} = 150 Ω		5.6		dB
	LNA gain = 17.9 dB, R_{FB} = 200 Ω		4.8		dB
	LNA gain = 21.6 dB, R_{FB} = 300 Ω		3.8		dB
Unterminated	LNA gain = 15.6 dB		3.2		dB
	LNA gain = 17.9 dB		2.9		dB
	LNA gain = 21.6 dB		2.6		dB
Correlated Noise Ratio	No signal, correlated/uncorrelated		−30		dB
Output Offset		−100		+100	LSB

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
Signal-to-Noise Ratio (SNR)	f_{IN} = 5 MHz at −12 dBFS, V_{GAIN} = −1.6 V		69		dBFS
	f_{IN} = 5 MHz at −1 dBFS		59		dBFS
Close In SNR	f_{IN} = 3.5 MHz at −1 dBFS, V_{GAIN} = 0 V, 1 kHz offset		−130		dBc/√Hz
Second Harmonic	f_{IN} = 5 MHz at −12 dBFS, V_{GAIN} = −1.6 V		−70		dBc
	f_{IN} = 5 MHz at −1 dBFS, V_{GAIN} = 1.6 V		−62		dBc
Third Harmonic	f_{IN} = 5 MHz at −12 dBFS, V_{GAIN} = −1.6 V		−61		dBc
	f_{IN} = 5 MHz at −1 dBFS, V_{GAIN} = 1.6 V		−55		dBc
Two-Tone Intermodulation Distortion (IMD3)	f_{RF1} = 5.015 MHz, f_{RF2} = 5.020 MHz, A_{RF1} = −1 dBFS, A_{RF2} = −21 dBFS, V_{GAIN} = 1.6 V, IMD3 relative to A_{RF2}		−54		dBc
Channel-to-Channel Crosstalk	f_{IN1} = 5.0 MHz at −1 dBFS		−60		dB
	Overrange condition[2]		−55		dB
GAIN ACCURACY	T_A = 25°C				
Gain Law Conformance Error	−1.6 < V_{GAIN} < −1.28 V		0.4		dB
	−1.28 V < V_{GAIN} ≤ +1.28 V	−1.3		+1.3	dB
	1.28 V < V_{GAIN} < 1.6 V		−0.5		dB
Linear Gain Error	V_{GAIN} = 0 V, normalized for ideal antialiasing filter loss	−1.3		+1.3	dB
Channel-to-Channel Matching	−1.28 V < V_{GAIN} < +1.28 V, 1 σ		0.1		dB
PGA Gain			21/24/27/30		dB
GAIN CONTROL INTERFACE					
Control Range	Differential	−1.6		+1.6	V
Control Common Mode	GAIN+, GAIN−	0.7	0.8	0.9	V
Input Impedance	GAIN+, GAIN−		10		MΩ
Gain Range			45		dB
Scale Factor	Analog		14		dB/V
	Digital step size		3.5		dB
Response Time	Analog 45 dB change		750		ns
CW DOPPLER MODE					
LO Frequency	$f_{LO} = f_{MLO}/M$	1		10	MHz
Phase Resolution	Per channel, 4LO[3] mode		45		Degrees
	Per channel, 8LO mode, 16LO mode		22.5		Degrees
Output DC Bias (Single-Ended)	CWI+, CWI−, CWQ+, and CWQ−		AVDD2/2		V
Output AC Current Range	Per CWI+, CWI−, CWQ+, and CWQ−, each channel enabled (2 f_{LO} and baseband signal)		±2.2	±2.5	mA
Transconductance (Differential)	Demodulated I_{OUT}/V_{IN}, per CWI+, CWI−, CWQ+, and CWQ−				
	LNA gain = 15.6 dB		3.3		mA/V
	LNA gain = 17.9 dB		4.3		mA/V
	LNA gain = 21.6 dB		6.6		mA/V
Input Referred Noise Voltage	R_S = 0 Ω, R_{FB} = ∞				
	LNA gain = 15.6 dB		1.6		nV/√Hz
	LNA gain = 17.9 dB		1.3		nV/√Hz
	LNA gain = 21.6 dB		1.0		nV/√Hz
Noise Figure	R_S = 50 Ω, R_{FB} = ∞				
	LNA gain = 15.6 dB		5.7		dB
	LNA gain = 17.9 dB		4.5		dB
	LNA gain = 21.6 dB		3.4		dB
Dynamic Range	R_S = 0 Ω, R_{FB} = ∞				
	LNA gain = 15.6 dB		164		dBFS/√Hz
	LNA gain = 17.9 dB		162		dBFS/√Hz
	LNA gain = 21.6 dB		160		dBFS/√Hz
Close In SNR	−3 dBFS input, f_{RF} = 2.5 MHz, f_{LO} = 40 MHz, 1 kHz offset, 16LO mode, 1 channel enabled		156		dBc/√Hz
	−3 dBFS input, f_{RF} = 2.5 MHz, f_{LO} = 40 MHz, 1 kHz offset, 16LO mode, 8 channels enabled		161		dBc/√Hz

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
Two-Tone Intermodulation Distortion (IMD3)	f_{RF1} = 5.015 MHz, f_{RF2} = 5.020 MHz, f_{LO} = 80 MHz, A_{RF1} = −1 dBFS, A_{RF2} = −21 dBFS, IMD3 relative to A_{RF2}		−58		dB
LO Harmonic Rejection	16LO, 8LO, and 4LO modes			−20	dBc
Quadrature Phase Error	I to Q, all phases, 1 σ		0.15		Degrees
I/Q Amplitude Imbalance	I to Q, all phases, 1 σ		0.015		dB
Channel-to-Channel Matching	Phase I to I, Q to Q, 1 σ		0.5		Degrees
	Amplitude I to I, Q to Q, 1 σ		0.25		dB
POWER SUPPLY, MODE I/MODE II/ MODE III/MODE IV					
AVDD1		1.7	1.8	1.9	V
AVDD2		2.85	3.0	3.6	V
DVDD	Demodulator/decimator enabled	1.3	1.4	1.9	V
	Demodulator/decimator disabled	1.3	1.8	1.9	V
DRVDD		1.7	1.8	1.9	V
I_{AVDD1}	TGC mode, LO band mode		148/187/ 223/291		mA
	CW Doppler mode		4		mA
I_{AVDD2}	TGC mode, no signal, low band mode		230		mA
	TGC mode, no signal, high band mode		239		mA
	CW Doppler mode, 8 channels enabled		140		mA
I_{DVDD}	RF decimator enabled in Mode III and Mode IV; demodulator/decimator enabled all modes		156/247/ 166/255		mA
I_{DRVDD}	ANSI-644 mode		133/184/ 141/146		mA
	Low power (IEEE 1596.3 similar) mode, 1 channel per lane mode		119/170/ 127/169		mA
Total Power Dissipation (Including Output Drivers)	TGC mode, no signal, RF decimator enabled in Mode III and Mode IV, demodulator/decimator disabled		1200/1400/ 1380/1630	1345/1555/ 1535/2100	mW
	TGC mode, no signal, RF decimator enabled in Mode III and Mode IV, demodulator/decimator enabled		1400/1695/ 1570/1900	1560/1880/ 1740/2100	mW
	CW Doppler mode, 8 channels enabled		500		mW
Power-Down Dissipation				30	mW
Standby Power Dissipation			630		mW
ADC RESOLUTION			14		Bits
ADC REFERENCE					
Output Voltage Error	VREF = 1 V			±50	mV
Load Regulation at 1.0 mA	VREF = 1 V		2		mV
Input Resistance			7.5		kΩ

[1] For a complete set of definitions and information about how these tests were completed, see the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*.
[2] The overrange condition is specified as 6 dB more than the full-scale input range.
[3] The internal LO frequency, f_{LO}, is generated from the supplied multiplier local oscillator frequency, f_{MLO}, by dividing it up by a configurable divider value (M) that can be 4, 8, or 16; the MLO signal is named 4LO, 8LO, or 16LO, accordingly.

DIGITAL SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.0 V, DVDD = 1.4 V, DRVDD = 1.8 V, 1.0 V internal ADC reference, full temperature range (0°C to 85°C), unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
INPUTS					
CLK+, CLK−, TX_TRIG+, TX_TRIG−					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage4[2]		0.2		3.6	V p-p
Input Voltage Range		GND − 0.2		AVDD1 + 0.2	V
Input Common-Mode Voltage			0.9		V
Input Resistance (Differential)	25°C		15		kΩ
Input Capacitance	25°C		4		pF
MLO+, MLO−, RESET+, RESET−					
Logic Compliance			LVDS/LVPECL		
Differential Input Voltage[2]		0.250		2 × AVDD2	V p-p
Input Voltage Range		GND − 0.2		AVDD2 + 0.2	V
Input Common-Mode Voltage		−0.3	AVDD2/2	+0.3	V
Input Resistance (Single-Ended)	25°C		20		kΩ
Input Capacitance	25°C		1.5		pF
LOGIC INPUTS					
PDWN, STBY, SCLK, SDIO, ADDRx					
Logic 1 Voltage		1.2		DRVDD + 0.3	V
Logic 0 Voltage				0.3	V
Input Resistance[3]	25°C		30 (26 for SDIO)		kΩ
Input Capacitance[3]	25°C		2 (5 for SDIO)		pF
CSB					
Logic 1 Voltage		1.2		DRVDD + 0.3	V
Logic 0 Voltage				0.3	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		2		pF
LOGIC OUTPUTS					
SDIO[4]					
Logic 1 Voltage (I_{OH} = 800 µA)			1.79		V
Logic 0 Voltage (I_{OL} = 50 µA)				0.05	V
GPO0/GPO1/GPO2/GPO3					
Logic 0 Voltage (I_{OL} = 50 µA)				0.05	V
DIGITAL OUTPUTS (DOUTx+, DOUTx−)					
ANSI-644					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})		247		454	mV
Output Offset Voltage (V_{OS})		1.125		1.375	V
Output Coding (Default)			Offset binary		
Low Power, Reduced Signal Option					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})		150		250	mV
Output Offset Voltage (V_{OS})		1.10		1.30	V
Output Coding (Default)			Offset binary		

[1] For a complete set of definitions and information about how these tests were completed, see the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*.
[2] Specified for LVDS and LVPECL only.
[3] The typical input resistance and input capacitance values deviate for SDIO; these deviations are noted in the Typ column.
[4] Specified for 13 SDIO pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.0 V, DVDD = 1.4 V, DRVDD = 1.8 V, full temperature range (0°C to 85°C), RF decimator bypassed, digital demodulator and baseband decimator bypassed, unless otherwise noted.

Table 3.

Parameter[1]	Temperature	Min	Typ	Max	Unit
CLOCK[2]					
Clock Rate					
40 MSPS (Mode I)	Full	20.5		40	MHz
65 MSPS (Mode II)	Full	20.5		65	MHz
80 MSPS (Mode III)[3]	Full	20.5		80	MHz
125 MSPS (Mode IV)[4]	Full	20.5		125	MHz
Clock Pulse Width High (t_{EH})	Full		3.75		ns
Clock Pulse Width Low (t_{EL})	Full		3.75		ns
OUTPUT PARAMETERS[2, 5]					
Propagation Delay (t_{PD})	Full	$10.8 - 1.5 \times t_{DCO}$	10.8	$10.8 + 1.5 \times t_{DCO}$	ns
Rise Time (t_R) (20% to 80%)	Full		300		ps
Fall Time (t_F) (20% to 80%)	Full		300		ps
DCO Period (t_{DCO})[6]	Full		$t_{SAMPLE}/7$		ns
FCO Propagation Delay (t_{FCO})	Full	$10.8 - 1.5 \times t_{DCO}$	10.8	$10.8 + 1.5 \times t_{DCO}$	ns
DCO Propagation Delay (t_{CPD})[7]	Full		$t_{FCO} + (t_{SAMPLE}/28)$		ns
DCO to Data Delay (t_{DATA})[7]	Full	$(t_{SAMPLE}/28) - 300$	$(t_{SAMPLE}/28)$	$(t_{SAMPLE}/28) + 300$	ps
DCO to FCO Delay (t_{FRAME})[7]	Full	$(t_{SAMPLE}/28) - 300$	$(t_{SAMPLE}/28)$	$(t_{SAMPLE}/28) + 300$	ps
Data-to-Data Skew ($t_{DATA-MAX} - t_{DATA-MIN}$)	Full		±225	±400	ps
TX_TRIG to CLK Setup Time (t_{SETUP})	25°C	1			ns
TX_TRIG to CLK Hold Time (t_{HOLD})	25°C	1			ns
Wake-Up Time					
Standby	25°C		2		µs
Power-Down	25°C		375		µs
ADC Pipeline Latency	Full		16		Clock cycles
APERTURE					
Aperture Uncertainty (Jitter)	25°C		<1		ps rms
LO GENERATION					
MLO[8] Frequency					
4LO Mode	Full	4		40	MHz
8LO Mode	Full	8		80	MHz
16LO Mode	Full	16		160	MHz
RESET[9] to MLO Setup Time (t_{SETUP})	Full	1	t_{MLO}[10]/2		ns
RESET to MLO Hold Time (t_{HOLD})	Full	1	t_{MLO}[10]/2		ns

[1] For a complete set of definitions and information about how these tests were completed, see the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*.
[2] The clock can be adjusted via the SPI.
[3] Mode III must have the RF decimator enabled because the maximum data rate of the baseband demodulator and decimator is 65 MSPS.
[4] Mode IV must have the RF decimator enabled because the maximum data rate of the baseband demodulator and decimator is 65 MSPS.
[5] Measurements were taken using a device soldered to FR-4 material.
[6] In the typical value, $t_{SAMPLE}/7$, 7 is based on the number of bits (14) divided by 2 because the interface uses double data rate (DDR) sampling.
[7] $t_{SAMPLE}/28$ is based on the number of bits divided by 2 because the delays are based on half duty cycles.
[8] MLO refers to the differential signal created via the MLO− pin and the MLO+ pin. This notation is used throughout the data sheet.
[9] RESET refers to the differential signal created via the RESET− pin and the RESET+ pin. This notation is used throughout the data sheet.
[10] The period of the MLO clock signal is represented by t_{MLO}.

TIMING DIAGRAMS

ADC Timing Diagram

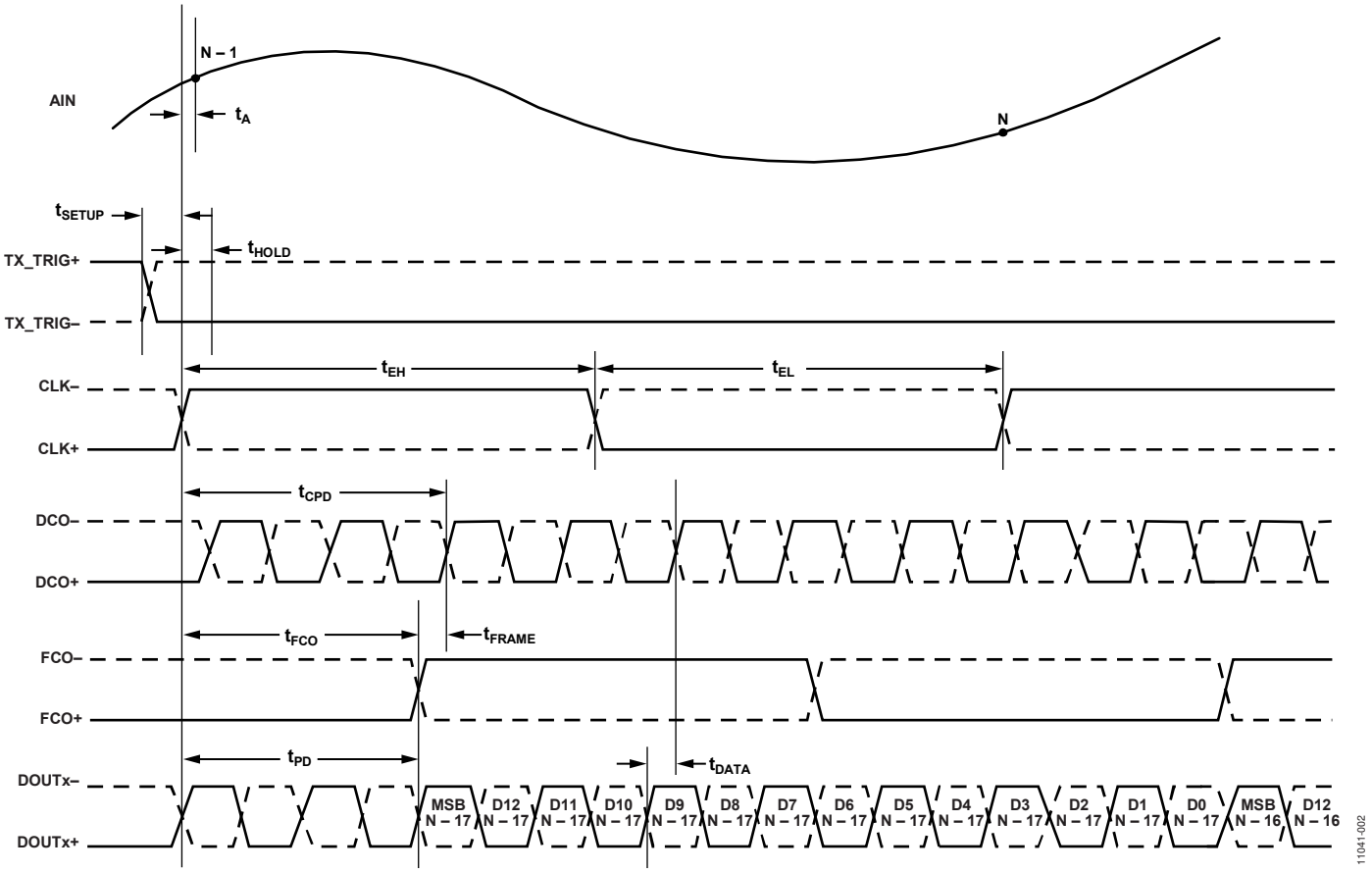

Figure 2. 14-Bit Data Serial Stream (Default, RF Decimator Bypassed, Demodulator Bypassed, Baseband Decimator Bypassed), 1 Channel/Lane Mode, FCO Mode = Word

CW Timing Diagrams

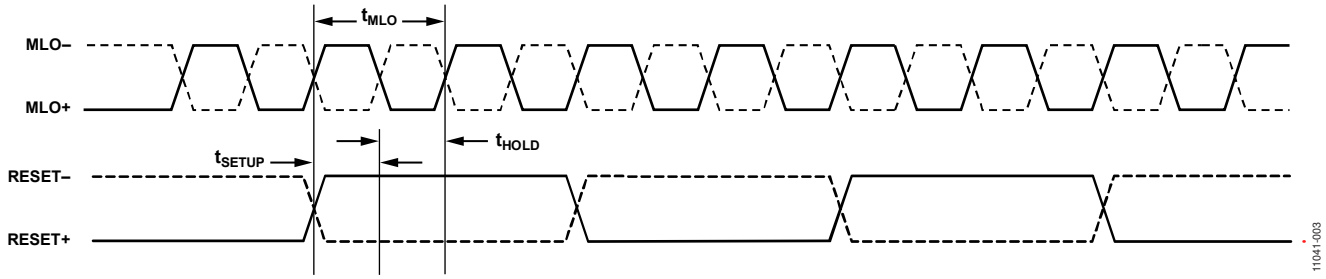

Figure 3. CW Doppler Mode Input MLO±, Continuous Synchronous RESET± Timing, Sampled on the Falling MLO± Edge, 4LO Mode

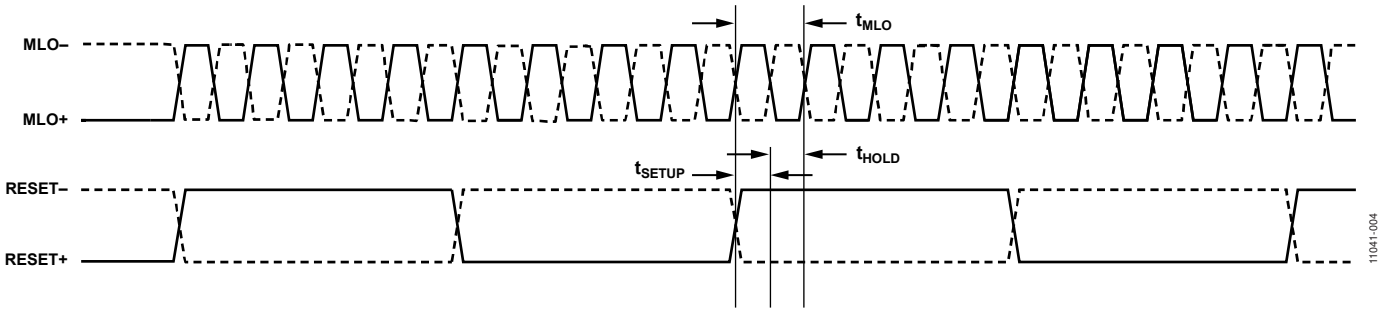

Figure 4. CW Doppler Mode Input MLO±, Continuous Synchronous RESET± Timing, Sampled on the Falling MLO± Edge, 8LO Mode

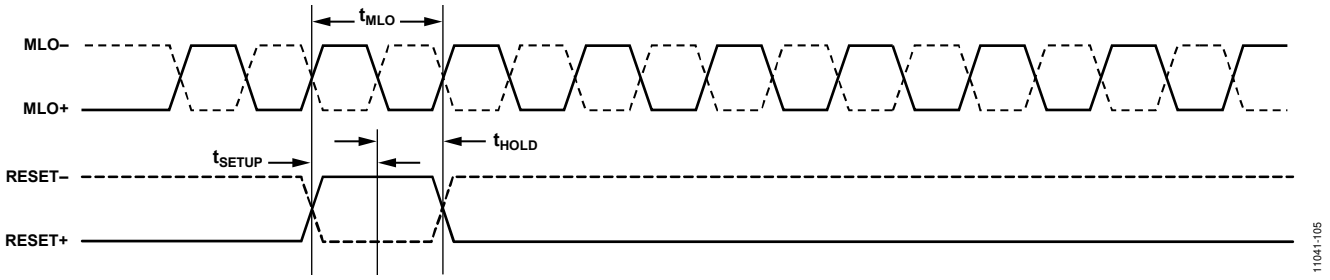

Figure 5. CW Doppler Mode Input MLO±, Pulse Synchronous RESET± Timing, 4LO/8LO/16LO Mode

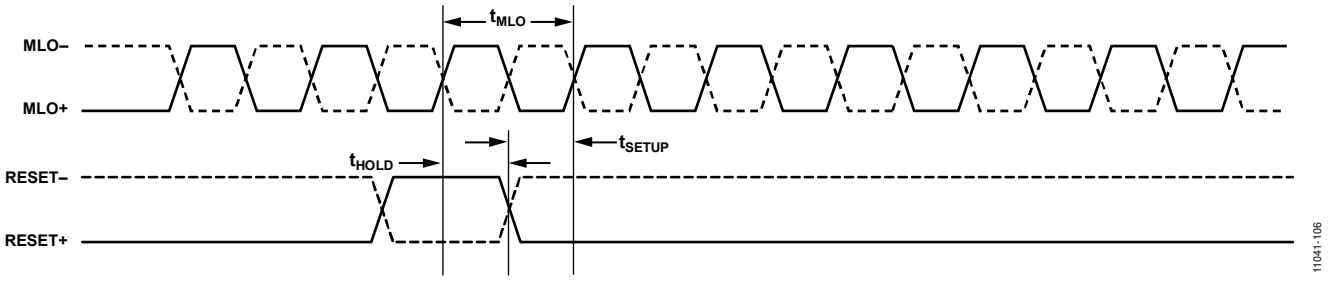

Figure 6. CW Doppler Mode Input MLO±, Pulse Asynchronous RESET± Timing, 4LO/8LO/16LO Mode

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
AVDD1 to GND	−0.3 V to +2.0 V
AVDD2 to GND	−0.3 V to +3.9 V
DVDD to GND	−0.3 V to +2.0 V
DRVDD to GND	−0.3 V to +2.0 V
GND to GND	−0.3 V to +0.3 V
AVDD2 to AVDD1	−2.0 V to +3.9 V
AVDD1 to DRVDD	−2.0 V to +2.0 V
AVDD2 to DRVDD	−2.0 V to +3.9 V
Digital Outputs (DOUTx+, DOUTx−, DCO+, DCO−, FCO+, FCO−) to GND	−0.3 V to DRVDD + 0.3 V
LI-x, LG-x, LO-x, LOSW-x, CWI−, CWI+, CWQ−, CWQ+, GAIN+, GAIN−, RESET+, RESET−, MLO+, MLO−, GPO0, GPO1, GPO2, GPO3 to GND	−0.3 V to AVDD2 + 0.3 V
CLK+, CLK−, TX_TRIG+, TX_TRIG−, VREF to GND	−0.3 V to AVDD1 + 0.3 V
SDIO, PDWN, STBY, SCLK, CSB, ADDRx	−0.3 V to DRVDD + 0.3 V
Operating Temperature Range (Ambient)	0°C to 85°C
Storage Temperature Range (Ambient)	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL IMPEDANCE

Table 5. Thermal Impedance

Symbol	Description	Value[1]	Unit
θ_{JA}	Junction-to-ambient thermal resistance, 0.0 m/sec air flow per JEDEC JESD51-2 (still air)	22.0	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter, 0 m/sec air flow per JEDEC JESD51-8 (still air)	9.2	°C/W
Ψ_{JT}	Junction-to-top-of-package characterization parameter, 0 m/sec air flow per JEDEC JESD51-2 (still air)	0.12	°C/W

[1] Thermal impedance results are from simulations. The printed circuit board (PCB) is JEDEC multilayer. The thermal performance for actual applications requires careful inspection of the conditions in the application to determine if they are similar to those assumed in these calculations.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12
A	LI-E	LI-F	LI-G	LI-H	VREF	RBIAS	GAIN+	GAIN–	LI-A	LI-B	LI-C	LI-D
B	LG-E	LG-F	LG-G	LG-H	GND	GND	CLNA	GND	LG-A	LG-B	LG-C	LG-D
C	LO-E	LO-F	LO-G	LO-H	GND	GND	GND	GND	LO-A	LO-B	LO-C	LO-D
D	LOSW-E	LOSW-F	LOSW-G	LOSW-H	GND	GND	GND	GND	LOSW-A	LOSW-B	LOSW-C	LOSW-D
E	GND	AVDD2	AVDD2	AVDD2	GND	GND	GND	GND	AVDD2	AVDD2	AVDD2	GND
F	AVDD1	GND	AVDD1	GND	AVDD1	GND	GND	AVDD1	GND	AVDD1	GND	AVDD1
G	GND	AVDD1	GND	DVDD	GND	GND	GND	GND	AVDD1	GND	DVDD	GND
H	CLK–	TX_TRIG–	GND	GND	GND	GND	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	CSB
J	CLK+	TX_TRIG+	CWQ+	GND	CWI+	AVDD2	MLO+	RESET–	GPO3	GPO1	PDWN	SDIO
K	GND	GND	CWQ–	GND	CWI–	AVDD2	MLO–	RESET+	GPO2	GPO0	STBY	SCLK
L	DRVDD	DOUTH+	DOUTG+	DOUTF+	DOUTE+	DCO+	FCO+	DOUTD+	DOUTC+	DOUTB+	DOUTA+	DRVDD
M	GND	DOUTH–	DOUTG–	DOUTF–	DOUTE–	DCO–	FCO–	DOUTD–	DOUTC–	DOUTB–	DOUTA–	GND

11041-005

Figure 7. Pin Configuration

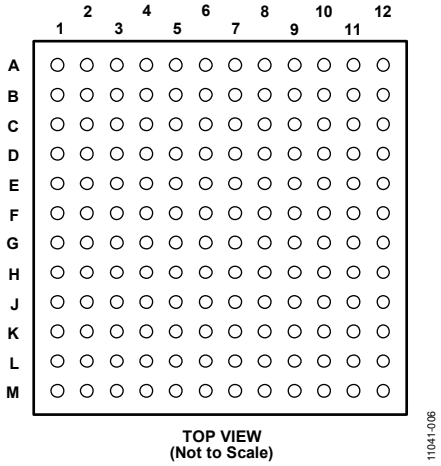

Figure 8. CSP_BGA Pin Location

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
B5, B6, B8, C5 to C8, D5 to D8, E1, E5 to E8, E12, F2, F4, F6, F7, F9, F11, G1, G3, G5 to G8, G10, G12, H3 to H6, J4, K1, K2, K4, M1, M12	GND	Ground. Tie these pins to a quiet analog ground.
F1, F3, F5, F8, F10, F12, G2, G9,	AVDD1	1.8 V Analog Supply.
G4, G11	DVDD	1.4 V/1.8 V Digital Supply.
E2 to E4, E9 to E11, J6, K6	AVDD2	3.0 V Analog Supply.
B7	CLNA	LNA External Capacitor.
L1, L12	DRVDD	1.8 V Digital Output Driver Supply.
C1	LO-E	LNA Analog Inverted Output for Channel E.
D1	LOSW-E	LNA Analog Switched Output for Channel E.
A1	LI-E	LNA Analog Input for Channel E.
B1	LG-E	LNA Ground for Channel E.
C2	LO-F	LNA Analog Inverted Output for Channel F.
D2	LOSW-F	LNA Analog Switched Output for Channel F.
A2	LI-F	LNA Analog Input for Channel F.
B2	LG-F	LNA Ground for Channel F.
C3	LO-G	LNA Analog Inverted Output for Channel G.
D3	LOSW-G	LNA Analog Switched Output for Channel G.
A3	LI-G	LNA Analog Input for Channel G.
B3	LG-G	LNA Ground for Channel G.
C4	LO-H	LNA Analog Inverted Output for Channel H.
D4	LOSW-H	LNA Analog Switched Output for Channel H.
A4	LI-H	LNA Analog Input for Channel H.
B4	LG-H	LNA Ground for Channel H.
H1	CLK–	Clock Input Complement.
J1	CLK+	Clock Input True.
H2	TX_TRIG–	Transmit Trigger Complement.
J2	TX_TRIG+	Transmit Trigger True.
H11	ADDR0	Chip Address Bit 0.
H10	ADDR1	Chip Address Bit 1.
H9	ADDR2	Chip Address Bit 2.
H8	ADDR3	Chip Address Bit 3.
H7	ADDR4	Chip Address Bit 4.
M2	DOUTH–	ADC H Digital Output Complement.
L2	DOUTH+	ADC H Digital Output True.
M3	DOUTG–	ADC G Digital Output Complement.
L3	DOUTG+	ADC G Digital Output True.
M4	DOUTF–	ADC F Digital Output Complement.
L4	DOUTF+	ADC F Digital Output True.
M5	DOUTE–	ADC E Digital Output Complement.
L5	DOUTE+	ADC E Digital Output True.
M6	DCO–	Digital Clock Output Complement.
L6	DCO+	Digital Clock Output True.
M7	FCO–	Frame Clock Digital Output Complement.
L7	FCO+	Frame Clock Digital Output True.
M8	DOUTD–	ADC D Digital Output Complement.
L8	DOUTD+	ADC D Digital Output True.
M9	DOUTC–	ADC C Digital Output Complement.
L9	DOUTC+	ADC C Digital Output True.
M10	DOUTB–	ADC B Digital Output Complement.
L10	DOUTB+	ADC B Digital Output True.

Pin No.	Mnemonic	Description
M11	DOUTA−	ADC A Digital Output Complement.
L11	DOUTA+	ADC A Digital Output True.
K11	STBY	Standby Power-Down.
J11	PDWN	Full Power-Down.
K12	SCLK	Serial Clock.
J12	SDIO	Serial Data Input/Output.
H12	CSB	Chip Select Bar.
B9	LG-A	LNA Ground for Channel A.
A9	LI-A	LNA Analog Input for Channel A.
D9	LOSW-A	LNA Analog Switched Output for Channel A.
C9	LO-A	LNA Analog Inverted Output for Channel A.
B10	LG-B	LNA Ground for Channel B.
A10	LI-B	LNA Analog Input for Channel B.
D10	LOSW-B	LNA Analog Switched Output for Channel B.
C10	LO-B	LNA Analog Inverted Output for Channel B.
B11	LG-C	LNA Ground for Channel C.
A11	LI-C	LNA Analog Input for Channel C.
D11	LOSW-C	LNA Analog Switched Output for Channel C.
C11	LO-C	LNA Analog Inverted Output for Channel C.
B12	LG-D	LNA Ground for Channel D.
A12	LI-D	LNA Analog Input for Channel D.
D12	LOSW-D	LNA Analog Switched Output for Channel D.
C12	LO-D	LNA Analog Inverted Output for Channel D.
K10	GPO0	General-Purpose Open Drain Output 0.
J10	GPO1	General-Purpose Open Drain Output 1.
K9	GPO2	General-Purpose Open Drain Output 2.
J9	GPO3	General-Purpose Open Drain Output 3.
J8	RESET−	Synchronizing Input for LO Divide by M Counter Complement.
K8	RESET+	Synchronizing Input for LO Divide by M Counter True.
K7	MLO−	CW Doppler Multiplier Local Oscillator (MLO) Input Complement.
J7	MLO+	CW Doppler MLO Input True.
A8	GAIN−	Gain Control Voltage Input Complement.
A7	GAIN+	Gain Control Voltage Input True.
A6	RBIAS	External Resistor to Set the Internal ADC Core Bias Current.
A5	VREF	Voltage Reference Input/Output.
K5	CWI−	CW Doppler I Output Complement.
J5	CWI+	CW Doppler I Output True.
K3	CWQ−	CW Doppler Q Output Complement.
J3	CWQ+	CW Doppler Q Output True.

TYPICAL PERFORMANCE CHARACTERISTICS

TGC MODE CHARACTERISTICS

Mode I = f_{SAMPLE} = 40 MSPS, f_{IN} = 5 MHz, LO band mode, R_S = 50 Ω, R_{FB} = ∞ (unterminated), LNA gain = 21.6 dB, LNA bias = midhigh, PGA gain = 27 dB, V_{GAIN} = (GAIN+) − (GAIN−) = 1.6 V, antialiasing filter LPF cutoff = f_{SAMPLE} /3, HPF cutoff = LPF cutoff/12.00 (default), RF decimator bypassed, digital demodulator and baseband decimator bypassed, unless otherwise noted.

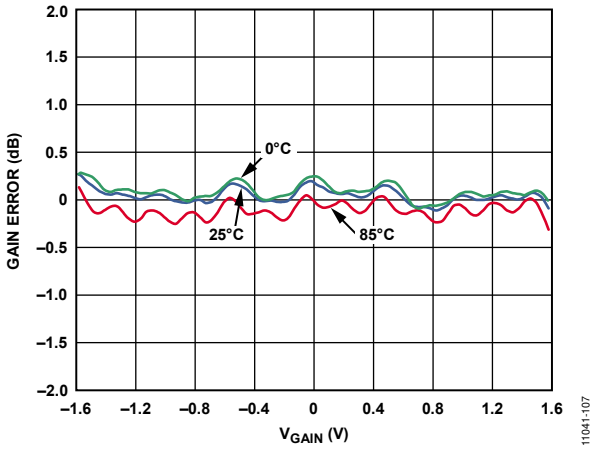

Figure 9. Gain Error vs. V_{GAIN}

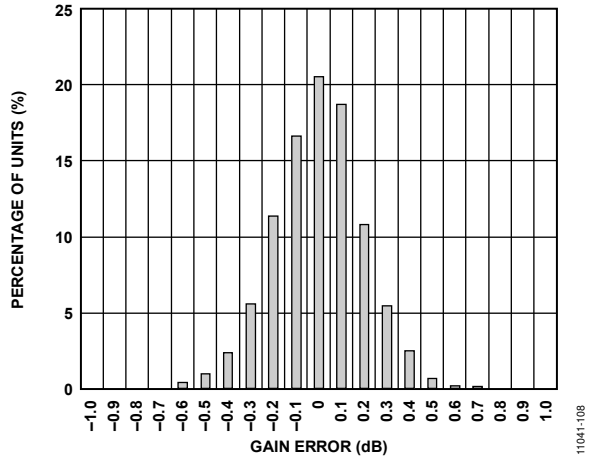

Figure 10. Gain Error Histogram, V_{GAIN} = −1.28 V

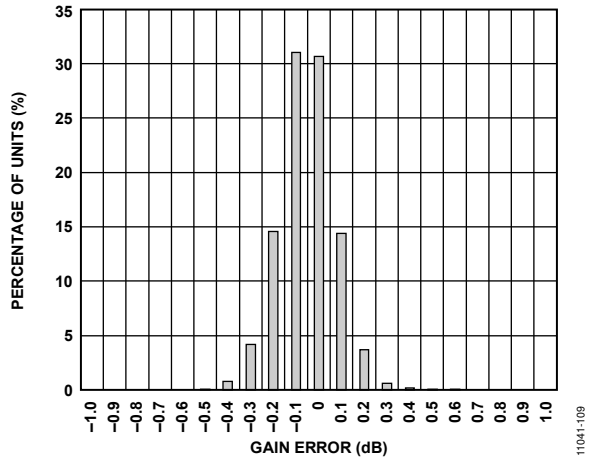

Figure 11. Gain Error Histogram, V_{GAIN} = 0 V

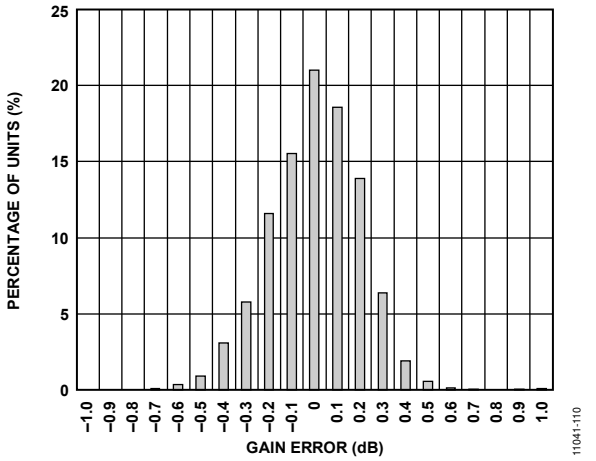

Figure 12. Gain Error Histogram, V_{GAIN} = 1.28 V

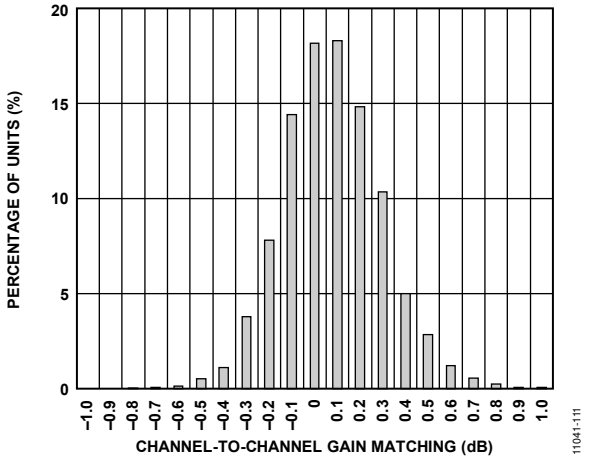

Figure 13. Gain Matching Histogram, V_{GAIN} = −1.2 V

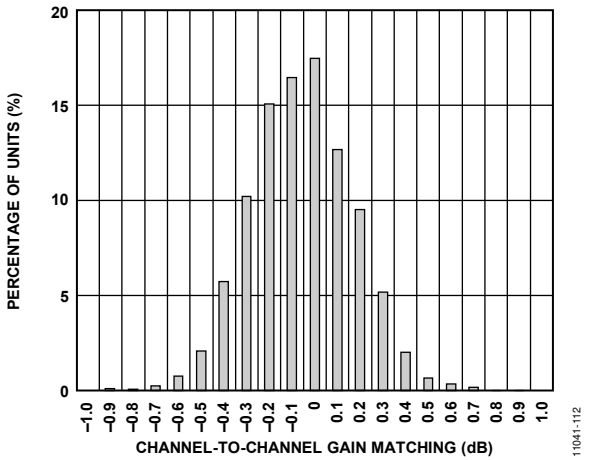

Figure 14. Gain Matching Histogram, V_{GAIN} = 1.2 V

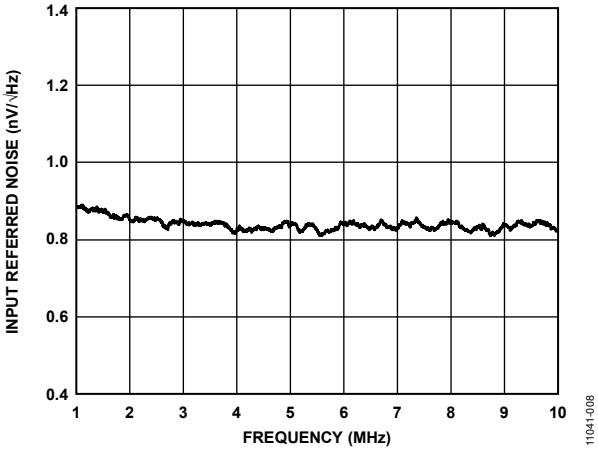

Figure 15. Short-Circuit, Input Referred Noise vs. Frequency

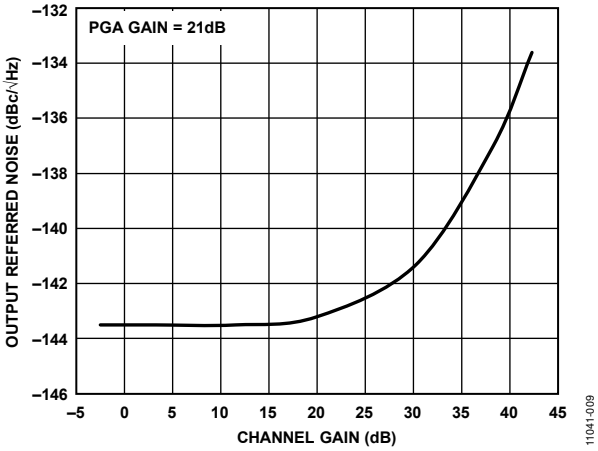

Figure 16. Short-Circuit, Output Referred Noise vs. Channel Gain, PGA Gain = 21 dB, V_{GAIN} = 1.6 V

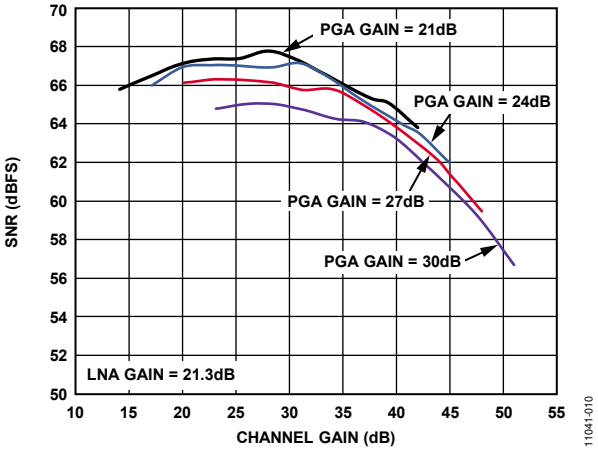

Figure 17. SNR vs. Channel Gain and PGA Gain, A_{OUT} = −1.0 dBFS

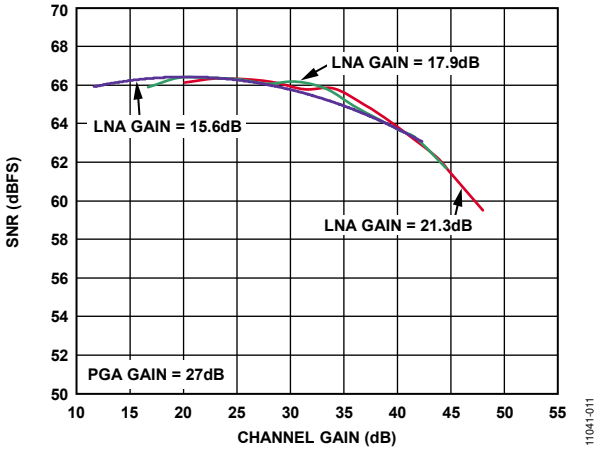

Figure 18. SNR vs. Channel Gain and LNA Gain, A_{OUT} = −1.0 dBFS

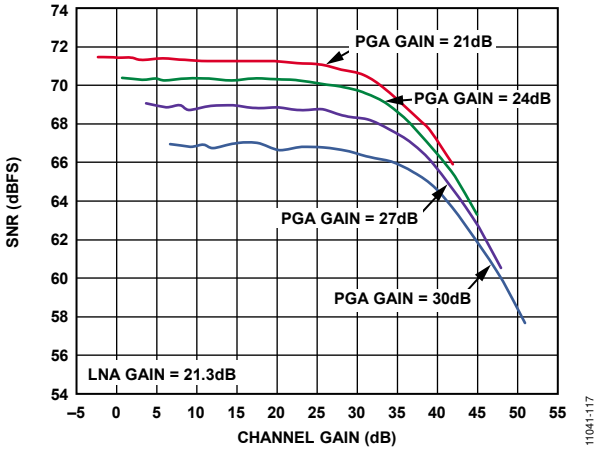

Figure 19. SNR vs. Channel Gain and PGA Gain, A_{IN} = −45 dBm

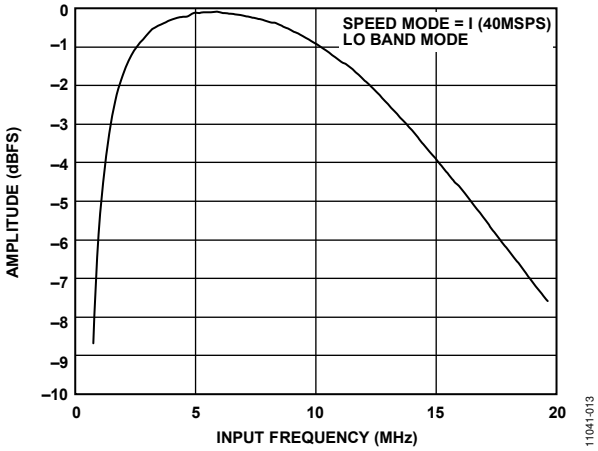

Figure 20. Antialiasing Filter Pass-Band Response, LPF Cutoff = 1/3 × f_{SAMPLE}, HPF = 1/12 × LPF Cutoff

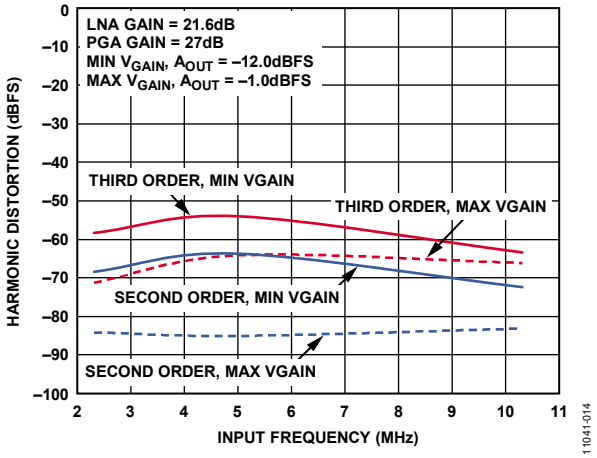

Figure 21. Second-Order and Third-Order Harmonic Distortion vs. Input Frequency, A_{OUT} = −1.0 dBFS

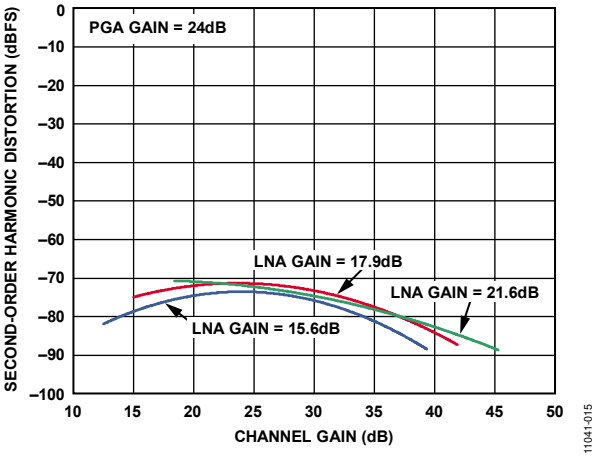

Figure 22. Second-Order Harmonic Distortion vs. Channel Gain, A_{OUT} = −1.0 dBFS

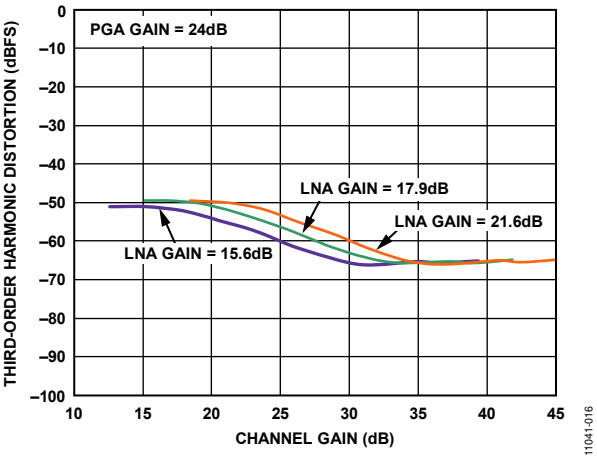

Figure 23. Third-Order Harmonic Distortion vs. Channel Gain, A_{OUT} = −1.0 dBFS

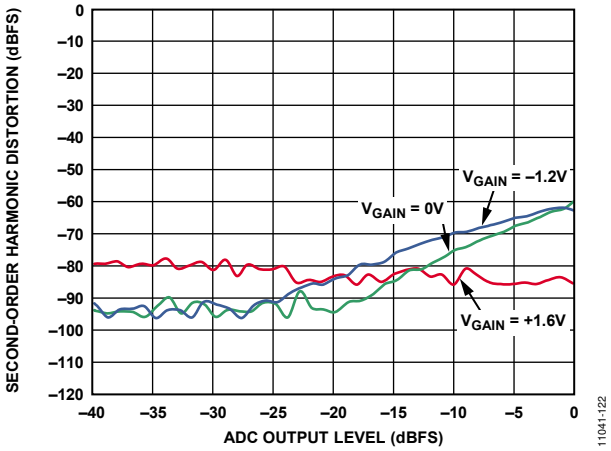

Figure 24. Second-Order Harmonic Distortion vs. ADC Output Level (A_{OUT})

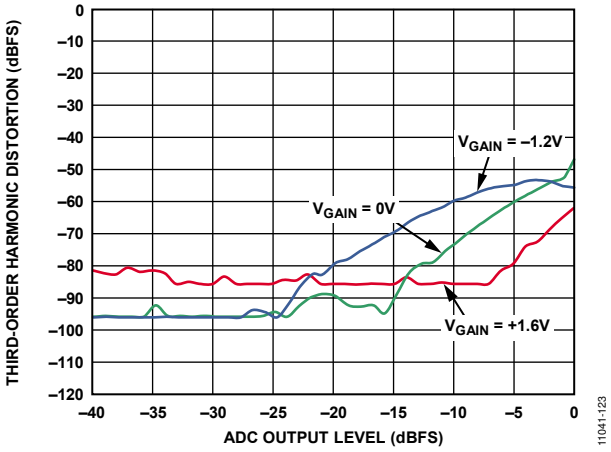

Figure 25. Third-Order Harmonic Distortion vs. ADC Output Level (A_{OUT})

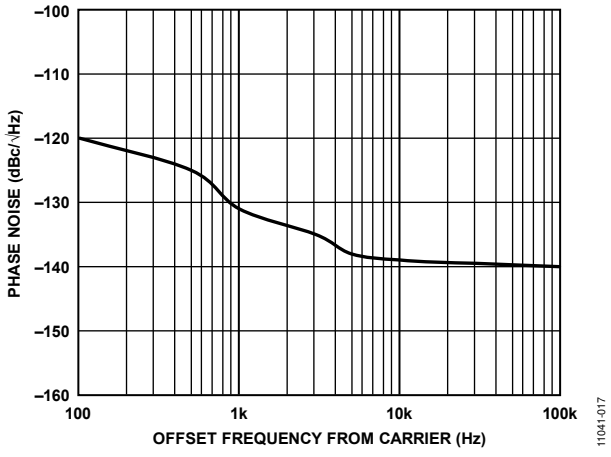

Figure 26. TGC Path Phase Noise, LNA Gain = 21.6 dB, PGA Gain = 27 dB, V_{GAIN} = 0 V

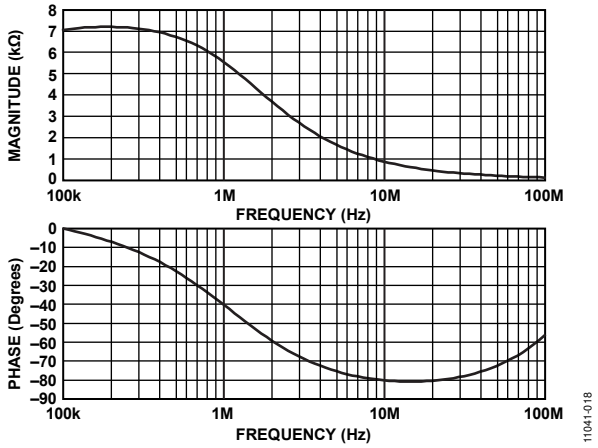

Figure 27. LNA Input Impedance Magnitude and Phase, Unterminated

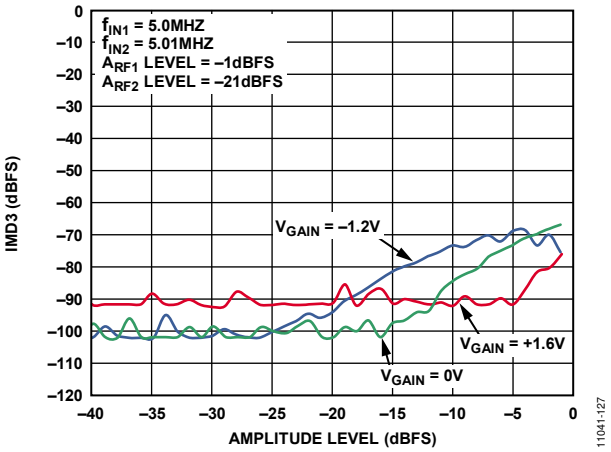

Figure 29. IMD3 vs. ADC Output Amplitude Level

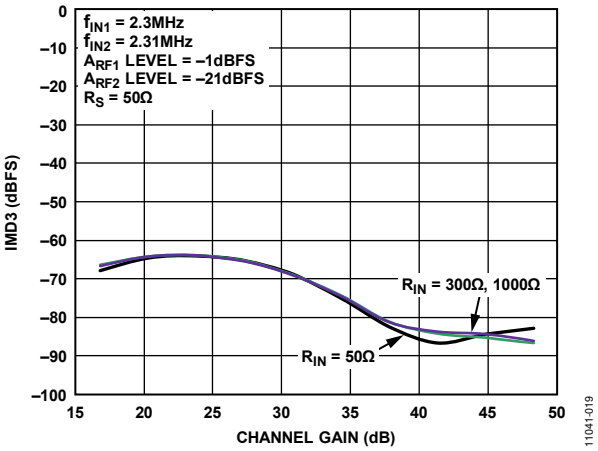

Figure 28. IMD3 vs. Channel Gain

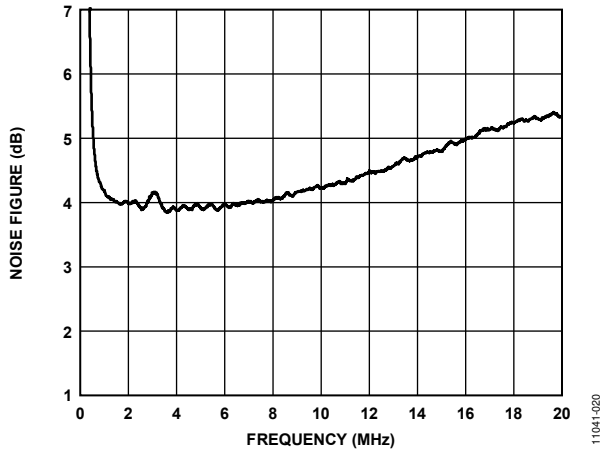

Figure 30. Noise Figure vs. Frequency,
$R_S = R_{IN}$ = 100 Ω, LNA Gain = 17.9 dB, PGA Gain = 30 dB, V_{GAIN} = 1.6 V

CW DOPPLER MODE CHARACTERISTICS

f_{IN} = 5 MHz, f_{LO} = 20 MHz, 4LO mode, R_S = 50 Ω, LNA gain = 21.6 dB, LNA bias = mid-high, all CW channels enabled, phase rotation = 0°.

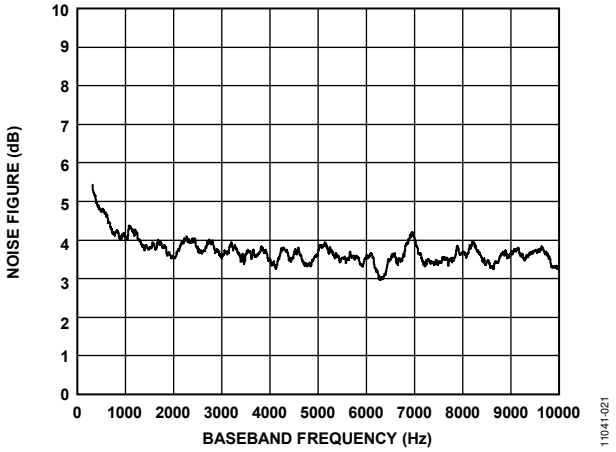

Figure 31. Noise Figure vs. Baseband Frequency

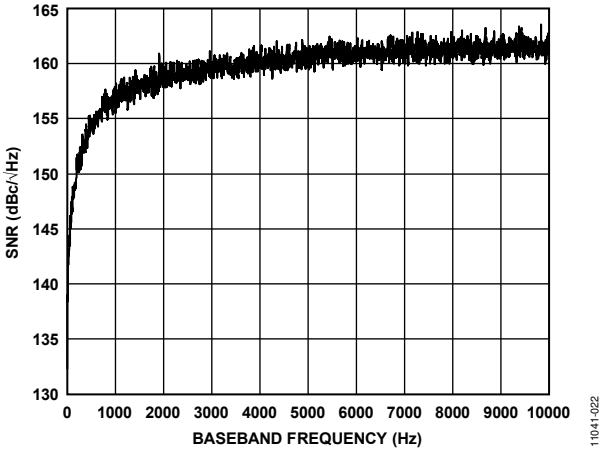

Figure 32. SNR vs. Baseband Frequency, −3 dBFS LNA Input

THEORY OF OPERATION

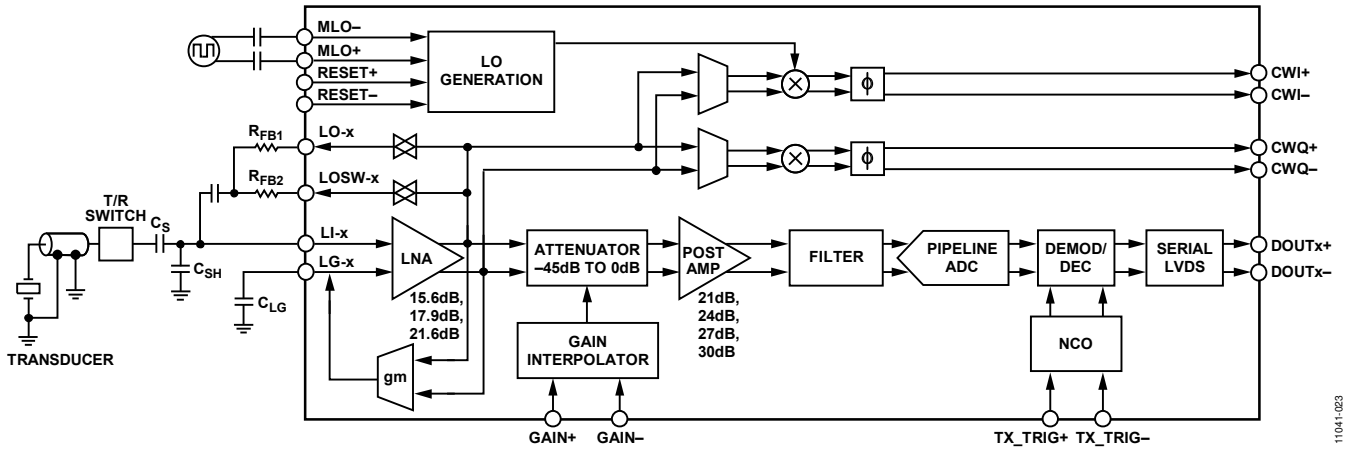

Figure 33. Simplified Block Diagram of a Single Channel

Each channel in the AD9670 contains both a TGC signal path and a CW Doppler signal path. Common to both signal paths, the LNA provides four user adjustable input impedance termination options for matching different probe impedances. The CW Doppler path includes an I/Q demodulator with programmable phase rotation needed for analog beamforming. The TGC path includes a differential X-AMP® VGA, an antialiasing filter, an ADC, and a digital demodulator and decimator. Figure 33 shows a simplified block diagram with external components.

TGC OPERATION

The system gain for TGC operation is distributed as shown in Table 7.

Table 7. Channel Analog Gain Distribution

Section	Nominal Gain (dB)
LNA	15.6/17.9/21.6 (LNA_{GAIN})
Attenuator	−45 to 0 (VGA_{ATT})
VGA	21/24/27/30 (PGA_{GAIN})
Filter	0
ADC	0

Each LNA output is dc-coupled to a VGA input. The VGA consists of an attenuator with a range of −45 dB to 0 dB, followed by an amplifier with 21 dB/24 dB/27 dB/30 dB of gain. The X-AMP gain interpolation technique results in low gain error and uniform bandwidth, and differential signal paths minimize distortion.

The linear in dB gain (law conformance) range of the TGC path is 45 dB. The slope of the gain control interface is 14 dB/V, and the gain control range is −1.6 V to +1.6 V. Equation 1 is the expression for the differential voltage, V_{GAIN}, at the gain control interface. Equation 2 is the expression for the VGA attenuation, VGA_{ATT}, as a function of V_{GAIN}.

$$V_{GAIN}\,(\text{V}) = (GAIN+) - (GAIN-) \quad (1)$$

$$VGA_{ATT}\,(\text{dB}) = -14\ \text{dB/V}\ (1.6) - V_{GAIN} \quad (2)$$

Then, calculate the total channel gain using Equation 3.

$$Channel\ Gain\ (\text{dB}) = LNA_{GAIN} + VGA_{ATT} + PGA_{GAIN} \quad (3)$$

In its default condition, the LNA has a gain of 21.6 dB (12×), and the VGA postamplifier gain is 24 dB. If the voltage on the GAIN+ pin is 0 V and the voltage on the GAIN− pin is 1.6 V (45.1 dB attenuation), the total gain of the channel is 0.5 dB if the LNA input is unmatched. The channel gain is −5.5 dB if the LNA is matched to 50 Ω (R_{FB} = 300 Ω). However, if the voltage on the GAIN+ pin is 1.6 V and the voltage on the GAIN− pin is 0 V (0 dB attenuation), VGA_{ATT} = 0 dB. This results in a total gain of 45.3 dB through the TGC path if the LNA input is unmatched or a total gain of 39.3 dB if the LNA input is matched.

In addition to the analog VGA attenuation described in Equation 2, the attenuation level can be digitally controlled in 3.5 dB increments. In this case, Equation 3 is still valid and the value of VGA_{ATT} is equal to the attenuation level set in SPI Register 0x011, Bits [7:4].

Low Noise Amplifier (LNA)

Good system sensitivity relies on a proprietary ultralow noise LNA at the beginning of the signal chain, which minimizes the noise contribution in the following VGA. Active impedance control optimizes noise performance for applications that benefit from input impedance matching.

The LNA inputs, LI-x, are capacitively coupled to the source. An on-chip bias generator establishes dc input bias voltages of approximately 2.2 V and centers the output common-mode levels at 1.5 V (AVDD2 divided by 2). A capacitor, C_{LG}, of the same value as the input coupling capacitor, C_S, is connected from the LG-x pins into ground.

The LNA supports three gain settings, 21.6 dB, 17.9 dB, or 15.6 dB, set through the SPI. Overload protection ensures quick recovery time from large input voltages.

Low value feedback resistors and the current driving capability of the output stage allow the LNA to achieve a low input referred noise voltage of 0.78 nV/√Hz (at a gain of 21.6 dB). On-chip resistor matching results in precise single-ended gains, which

are critical for accurate impedance control. The use of a fully differential topology and negative feedback minimizes distortion. Low second-order harmonic distortion is particularly important in harmonic ultrasound imaging applications.

Active Impedance Matching

The LNA consists of a single-ended voltage gain amplifier with differential outputs. The negative output is externally available on two output pins, LO-x and LOSW-x, that are controlled via internal switches. This configuration allows the active input impedance synthesis of three different impedance values (and an unterminated value) by connecting up to two external resistances in parallel and controlling the internal switch states via the SPI. For example, with a fixed gain of 8× (17.9 dB), an active input termination is synthesized by connecting a feedback resistor between the negative output pin, LO-x, and the positive input pin, LI-x. This well known technique is used for interfacing multiple probe impedances to a single system. The input resistance (R_{IN}) calculation is shown in Equation 4.

$$R_{IN} = \frac{(R_{FB1} + 20\,\Omega) \,||\, (R_{FB2} + 20\,\Omega) + 30\,\Omega}{(1 + A/2)} \quad (4)$$

where:
R_{FB1} and R_{FB2} are the external feedback resistors.
20 Ω is the internal switch on resistance.
30 Ω is an internal series resistance common to the two internal switches.
$A/2$ is the single-ended gain or the gain from the LI-x inputs to the LO-x outputs.

R_{FB} can be equal to R_{FB1}, R_{FB2}, or (R_{FB1} + 20 Ω)||(R_{FB2} + 20 Ω), depending on the connection status of the internal switches.

Because the amplifier has a gain of 8× from its input to its differential output, it is important to note that the gain, A/2, is the gain from the LI-x pin to the LO-x pin and that it is 6 dB less than the gain of the amplifier, or 12.1 dB (4×). The input resistance is reduced by an internal bias resistor of 6 kΩ in parallel with the source resistance connected to the LI-x pin, with the LG-x pin ac grounded. Use Equation 5 to calculate the required R_{FB} for a desired R_{IN}, even for higher values of R_{IN}.

$$R_{IN} = \frac{(R_{FB1} + 20\,\Omega) \,||\, (R_{FB2} + 20\,\Omega) + 30\,\Omega}{(1 + A/2)} \,||\, 6\,\text{k}\Omega \quad (5)$$

For example, to set R_{IN} to 200 Ω with a single-ended LNA gain of 12.1 dB (4×), the value of R_{FB} from Equation 4 must be 950 Ω, while the switch for R_{FB2} is open. If the more accurate equation (Equation 5) is used to calculate R_{IN}, the value is then 194 Ω instead of 200 Ω, resulting in a gain error of less than 0.27 dB. Some factors, such as the presence of a dynamic source resistance, may influence the absolute gain accuracy more significantly. At higher frequencies, the input capacitance of the LNA must be considered. The user must determine the level of matching accuracy and adjust R_{FB} accordingly.

R_{FB} is the resulting impedance of the R_{FB1} and R_{FB2} combination (see Figure 33). Using Register 0x02C in the SPI memory map, the AD9670 can be programmed for four impedance matching options: three active terminations and one unterminated option. Table 8 shows an example of how to select R_{FB1} and R_{FB2} for 66 Ω, 100 Ω, and 200 Ω input impedances for LNA gain = 21.6 dB (12×).

Table 8. Active Termination Example for LNA Gain = 21.6 dB, R_{FB1} = 650 Ω, and R_{FB2} = 1350 Ω

Reg. 0x02C Value	R_S (Ω)	LO-x Switch	LOSW-x Switch	R_{FB} (Ω)	R_{IN} (Ω)[1]
00 (default)	100	On	Off	R_{FB1}	100
01	50	On	On	R_{FB1} || R_{FB2}	66
10	200	Off	On	R_{FB2}	200
11	N/A[2]	Off	Off	∞	∞

[1] See Equation 4.
[2] N/A means not applicable.

The bandwidth (BW) of the LNA is greater than 80 MHz. Ultimately, the BW of the LNA limits the accuracy of the synthesized R_{IN}. For R_{IN} = R_S up to about 200 Ω, the best match is between 100 kHz and 10 MHz, where the lower frequency limit is determined by the size of the ac coupling capacitors, and the upper limit is determined by the LNA BW. Furthermore, the input capacitance and R_S limit the BW at higher frequencies. Figure 34 shows R_{IN} vs. frequency for various values of R_{FB}.

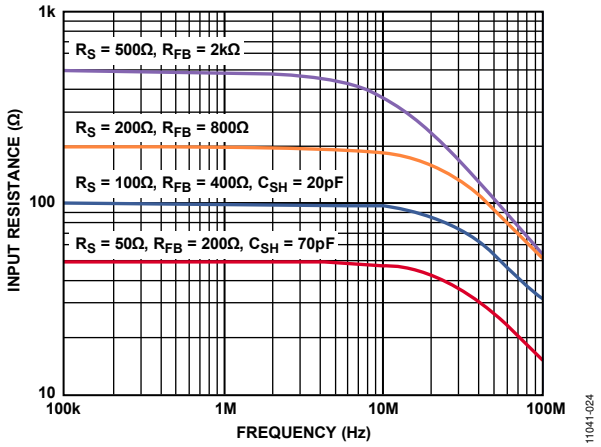

Figure 34. R_{IN} vs. Frequency for Various Values of R_{FB} (Effects of R_{SH} and C_{SH} Are Also Shown)

However, as seen for larger R_{IN} values, parasitic capacitance starts rolling off the signal BW before the LNA produces peaking. C_{SH} further degrades the match; therefore, do not use C_{SH} for values of R_{IN} that are greater than 100 Ω.

Table 9 lists the recommended values for R_{FB} and C_{SH} in terms of R_{IN}. C_{FB} is needed in series with R_{FB} because the dc levels at the LO-x pin and the LI-x pin are unequal.

Table 9. Active Termination External Component Values

LNA Gain (dB)	R_{IN} (Ω)	R_{FB} (Ω)	Minimum C_{SH} (pF)
15.6	50	150	90
17.9	50	200	70
21.6	50	300	50
15.6	100	350	30
17.9	100	450	20
21.6	100	650	10
15.6	200	750	Not applicable
17.9	200	950	Not applicable
21.6	200	1350	Not applicable

LNA Noise

The short-circuit noise voltage (input referred noise) is an important limit on system performance. The short-circuit noise voltage for the LNA is 0.78 nV/√Hz at a gain of 21.6 dB, including the VGA noise at a VGA postamplifier gain of 27 dB. These measurements, taken without a feedback resistor, provide the basis for calculating the input noise and noise figure (NF) performance. Figure 35 and Figure 36 are simulations of noise figure vs. R_S results with different input configurations and an input referred noise voltage of 2.5 nV/√Hz for the VGA. Unterminated ($R_{FB} = \infty$) operation exhibits the lowest equivalent input noise and noise figure. Figure 36 shows the noise figure vs. source resistance rising at low R_S—where the LNA voltage noise is large compared to the source noise—and at high R_S due to the noise contribution from R_{FB}. The lowest NF is achieved when R_S matches R_{IN}.

Figure 35 shows the relative noise figure performance. With an LNA gain of 21.6 dB, the input impedance is swept with R_S to preserve the match at each point. The noise figures for a source impedance of 50 Ω are 7 dB, 4 dB, and 2.5 dB for the shunt termination, active termination, and unterminated configurations, respectively. The noise figures for 200 Ω are 4.5 dB, 1.7 dB, and 1 dB, respectively.

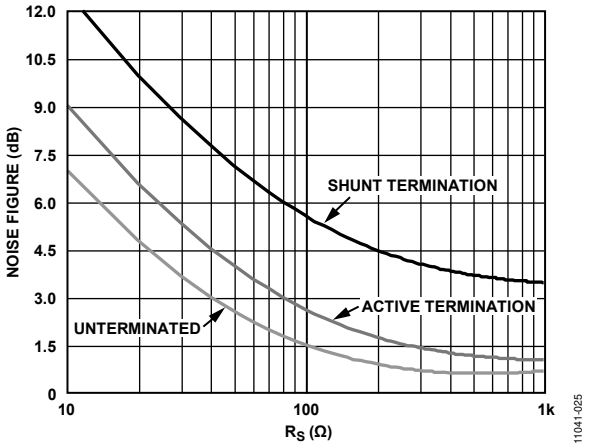

Figure 35. Noise Figure vs. R_S for Shunt Termination, Active Termination Matched, and Unterminated Inputs, V_{GAIN} = 1.6 V

Figure 36 shows the noise figure as it relates to R_S for various values of R_{IN}, which is helpful for design purposes.

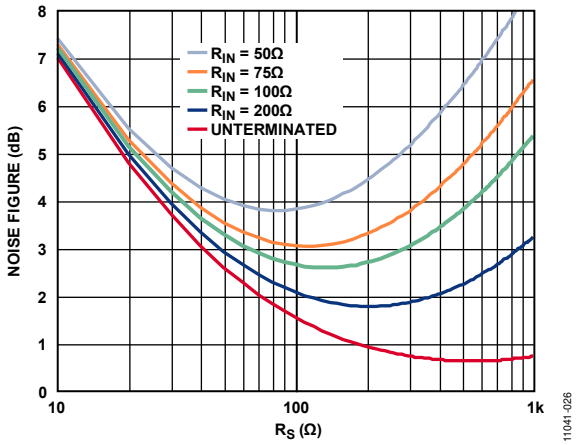

Figure 36. Noise Figure vs. R_S for Various Fixed Values of R_{IN}, Active Termination Matched Inputs, V_{GAIN} = 1.6 V

CLNA Connection

Attach a 1 nF capacitor from CLNA (Ball B7) to AVDD2.

DC Offset Correction/High-Pass Filter

The AD9670 LNA architecture is designed to correct for dc offset voltages that can develop on the external C_S capacitor due to leakage of the T/R switch during ultrasound transmit cycles. The dc offset correction, as shown in Figure 37, provides a feedback mechanism to the LG-x input of the LNA to correct for this dc voltage.

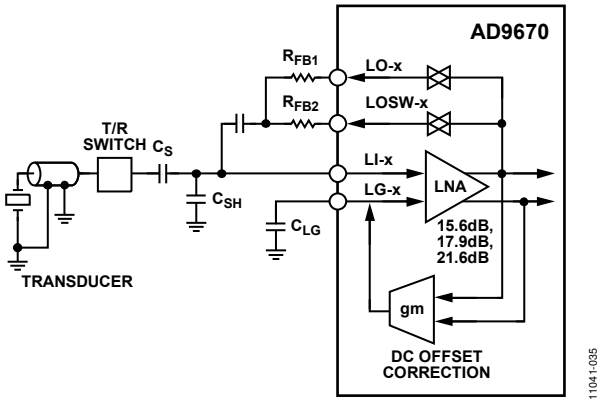

Figure 37. Simplified LNA Input Configuration

The feedback acts as high-pass filter providing dynamic correction of the dc offset. The cutoff frequency of the high-pass filter response is dependent on the value of the C_{LG} capacitor, the gain of the LNA (LNA_{GAIN}), and the transconductance (g_m) of the feedback transconductance amplifier. The g_m value is programmed in Register 0x120, Bits[4:3]. C_S must be equal to C_{LG} for proper operation.

Table 10. High-Pass Filter Cutoff Frequency, f_{HP}, for C_{LG} = 10 nF

Reg. 0x120, Bits[4:3]	g_m (mS)	LNA_{GAIN} = 15.6 dB (kHz)	LNA_{GAIN} = 17.9 dB (kHz)	LNA_{GAIN} = 21.6 dB (kHz)
00 (default)	0.5	41	55	83
01	1.0	83	110	167
10	1.5	133	178	267
11	2.0	167	220	330

For other values of C_{LG}, determine the high-pass filter cutoff frequency by scaling the values from Table 10 or calculating based on C_{LG}, LNA_{GAIN}, and g_m, as shown in Equation 6.

$$f_{HP}(C_{LG}) = \frac{1}{2\times\pi} \times LNA_{GAIN} \times \frac{g_m}{C_{LG}} = f_{HP}\text{ (see Table 10)} \times \frac{10\text{ nF}}{C_{LG}} \quad (6)$$

Variable Gain Amplifier (VGA)

The differential X-AMP VGA provides precise input attenuation and interpolation. It has a low input referred noise of 2.5 nV/√Hz and excellent gain linearity. The VGA is driven by a fully differential input signal from the LNA. The X-AMP architecture produces a linear in dB gain law conformance and low distortion levels—deviating by only ±0.5 dB or less from the ideal. The gain slope is monotonic with respect to the control voltage and is stable with variations in process, temperature, and supply. The resulting total gain range is 45 dB, which allows range loss at the endpoints. The X-AMP inputs are part of a PGA that completes the VGA. The PGA in the VGA is programmable to a gain of 21 dB, 24 dB, 27 dB, or 30 dB. This allows the optimization of channel gain for different imaging modes in the ultrasound system. The VGA bandwidth is greater than 100 MHz. The input stage is designed to ensure excellent frequency response uniformity across the gain setting. For TGC mode, this uniformity minimizes time delay variation across the gain range.

Gain Control

The analog gain control interface, GAIN±, is a differential input. V_{GAIN} varies the gain of all VGAs through the interpolator by selecting the appropriate input stages connected to the input attenuator. The nominal V_{GAIN} range is 14 dB/V from −1.6 V to +1.6 V, with the best gain linearity from approximately −1.44 V to +1.44 V, where the error is typically less than ±0.5 dB. For V_{GAIN} voltages of greater than +1.44 V and less than −1.44 V, the error increases. The value of GAIN± can exceed the supply voltage by 1 V without gain foldover.

Gain control response time is less than 750 ns to settle within 10% of the final value for a change from minimum to maximum gain.

The differential input pins, GAIN+ and GAIN−, can be interfaced as shown in Figure 38. DC couple the GAIN+ and GAIN− pins, and drive them to accommodate a 3.2 V full-scale input.

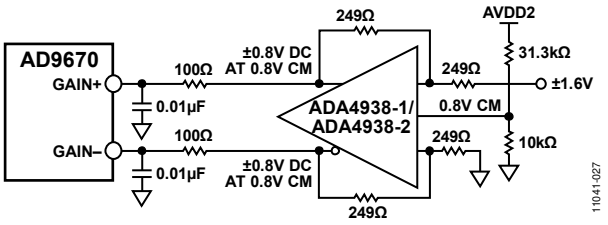

Figure 38. Differential GAIN± Pin Configuration

Disable the analog gain control and digitally control the attenuator using SPI Register 0x011, Bits[7:4]. The control range is 45 dB, and the step size is 3.5 dB.

VGA Noise

In a typical application, a VGA compresses a wide dynamic range input signal to within the input span of an ADC. The input referred noise of the LNA limits the minimum resolvable input signal, whereas the output referred noise, which depends primarily on the VGA, limits the maximum instantaneous dynamic range that can be processed at any one particular gain control voltage. This latter limit is set in accordance with the total noise floor of the ADC.

The output referred noise is a flat 40 nV/√Hz (postamplifier gain = 24 dB) over most of the gain range because it is dominated by the fixed output referred noise of the VGA. At the high end of the gain control range, the noise of the LNA and of the source prevail. The input referred noise reaches its minimum value near the maximum gain control voltage, where the input referred contribution of the VGA is miniscule.

At lower gains, the input referred noise and, therefore, the noise figure, increases as the gain decreases. The instantaneous dynamic range of the system is not lost, however, because the input capacity increases as the input referred noise increases. The contribution of the ADC noise floor has the same dependence. The important relationship is the magnitude of the VGA output noise floor relative to that of the ADC.

Gain control noise is a concern in very low noise applications. Thermal noise in the gain control interface can modulate the channel gain. The resulting noise is proportional to the output signal level and is usually evident only when a large signal is present. Take care to minimize noise impinging at the GAIN± inputs. Use an external RC filter to remove V_{GAIN} source noise. The filter bandwidth must be sufficient to accommodate the desired control bandwidth and attenuate unwanted switching noise from the external DACs used to drive the gain control.

The AD9670 can bypass the GAIN± inputs and control the gain of the attenuator digitally (see the Gain Control section). This mode removes any external noise contributions when active gain control is not needed.

Antialiasing Filter

The filter that the signal reaches prior to the ADC is used to reject dc signals and to band limit the signal for antialiasing. The antialiasing filter is a combination of a single-pole high-pass filter and a second-order low-pass filter. The high-pass filter can be configured at a ratio of the low-pass filter cutoff. This is selectable through Register 0x02B.

The filter uses on-chip tuning to trim the capacitors and, in turn, to set the desired low-pass cutoff frequency and reduce variations. The default −3 dB low-pass filter cutoff is 1/3, 1/4.5, or 1/6 of the ADC sample clock rate. The cutoff can be scaled to 0.75, 0.8, 0.9, 1.0, 1.13, 1.25, or 1.45 times this frequency through Register 0x00F. The cutoff tolerance (±10%) is maintained from 8 MHz to 18 MHz for low band mode and 13.5 MHz to 30 MHz for high band mode. Table 11 and Table 12 calculate the valid SPI-selectable low-pass filter settings and expected cutoff frequencies for the low band and high band mode at the minimum sample frequency and the maximum sample frequency in each speed mode.