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14-Bit, 1.25 GSPS/1 GSPS/820 MSPS/500 MSPS JESD204B, Dual Analog-to-Digital Converter

Data Sheet **AD9680**

FEATURES

- JESD204B (Subclass 1) coded serial digital outputs
- 1.65 W total power per channel at 1 GSPS (default settings)
- SFDR at 1 GSPS = 85 dBFS at 340 MHz, 80 dBFS at 1 GHz
- SNR at 1 GSPS = 65.3 dBFS at 340 MHz (A_{IN} = −1.0 dBFS),
  - 60.5 dBFS at 1 GHz (A_{IN} = −1.0 dBFS)
- ENOB = 10.8 bits at 10 MHz
- DNL = ±0.5 LSB
- INL = ±2.5 LSB
- Noise density = −154 dBFS/Hz at 1 GSPS
- 1.25 V, 2.5 V, and 3.3 V dc supply operation
- No missing codes
- Internal ADC voltage reference
- Flexible input range: 1.46 V p-p to 1.94 V p-p
  - AD9680-1250: 1.58 V p-p nominal
  - AD9680-1000 and AD9680-820: 1.70 V p-p nominal
  - AD9680-500: 1.46 V p-p to 2.06 V p-p (2.06 V p-p nominal)
- Programmable termination impedance
  - 400 Ω, 200 Ω, 100 Ω, and 50 Ω differential
- 2 GHz usable analog input full power bandwidth
- 95 dB channel isolation/crosstalk
- Amplitude detect bits for efficient AGC implementation
- 2 integrated wideband digital processors per channel
  - 12-bit NCO, up to 4 half-band filters
- Differential clock input
- Integer clock divide by 1, 2, 4, or 8
- Flexible JESD204B lane configurations
- Small signal dither

APPLICATIONS

- Communications
- Diversity multiband, multimode digital receivers
  - 3G/4G, TD-SCDMA, W-CDMA, GSM, LTE
- General-purpose software radios
- Ultrawideband satellite receivers
- Instrumentation
- Radars
- Signals intelligence (SIGINT)
- DOCSIS 3.0 CMTS upstream receive paths
- HFC digital reverse path receivers

FUNCTIONAL BLOCK DIAGRAM

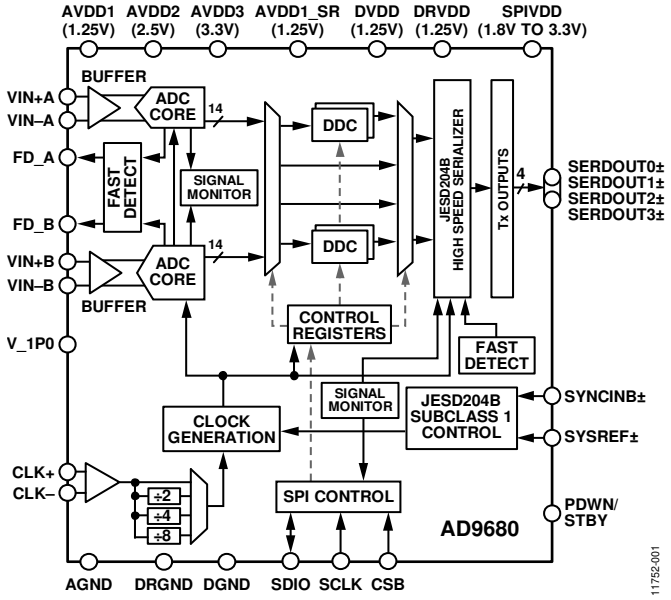

Figure 1.

PRODUCT HIGHLIGHTS

1. Wide full power bandwidth supports IF sampling of signals up to 2 GHz.
2. Buffered inputs with programmable input termination eases filter design and implementation.
3. Four integrated wideband decimation filters and numerically controlled oscillator (NCO) blocks supporting multiband receivers.
4. Flexible serial port interface (SPI) controls various product features and functions to meet specific system requirements.
5. Programmable fast overrange detection.
6. 9 mm × 9 mm, 64-lead LFCSP.

Rev. C
Document Feedback

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AD9680* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD-FMCDAQ2-EBZ Evaluation Board
- AD9680/AD9234/AD9690 Evaluation Board
- ADA4961 & AD9680 Analog Signal Chain Evaluation and AD9528 Converter Synchronization

DOCUMENTATION

Application Notes

- AN-835: Understanding High Speed ADC Testing and Evaluation

Data Sheet

- AD9680: 14-Bit, 1 GSPS/820 MSPS/500 MSPS JESD204B, Dual Analog-to-Digital Converter Data Sheet

TOOLS AND SIMULATIONS

- AD9680 Delphi Models
- Visual Analog
- AD9680 / AD6674 IBIS Model
- AD9680 AMI Model
- AD9680 S-Parameters

REFERENCE MATERIALS

Informational

- JESD204 Serial Interface

Press

- Analog Devices Introduces High-Performance RF ICs for Multi-band Base Stations and Microwave Point-to-Point Radios
- Analog Devices Unveils New Class of Data Converters That Set 14-bit, GSPS Performance Standard

Technical Articles

- Clocking Wideband GSPS JESD204B ADCs
- Digital Signal Process in IF RF Data Converters
- MS-2660: Understanding Spurious-Free Dynamic Range in Wideband GSPS ADCs
- MS-2672: JESD204B Subclasses - Part 1: An Introduction to JESD204B Subclasses and Deterministic Latency
- MS-2677: JESD204B Subclasses - Part 2: Subclass 1 vs. Subclass 2 System Considerations
- MS-2708: GSPS Data Converters to the Rescue for Electronics Surveillance and Warfare Systems
- MS-2714: Understanding Layers in the JESD204B Specificaton: A High Speed ADC Perspective, Part 1
- MS-2735: Maximizing the Dynamic Range of Software-Defined Radio
- Powering GSPS or RF Sampling ADCs: Switcher vs LDO

DESIGN RESOURCES

- AD9680 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9680 EngineerZone Discussions.

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5/14—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9680 is a dual, 14-bit, 1.25 GSPS/1 GSPS/820 MSPS/500 MSPS analog-to-digital converter (ADC). The device has an on-chip buffer and sample-and-hold circuit designed for low power, small size, and ease of use. This device is designed for sampling wide bandwidth analog signals of up to 2 GHz. The AD9680 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

The analog input and clock signals are differential inputs. Each ADC data output is internally connected to two digital down-converters (DDCs). Each DDC consists of up to five cascaded signal processing stages: a 12-bit frequency translator (NCO), and four half-band decimation filters. The DDCs are bypassed by default.

In addition to the DDC blocks, the AD9680 has several functions that simplify the automatic gain control (AGC) function in the communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

Users can configure the Subclass 1 JESD204B-based high speed serialized output in a variety of one-, two-, or four-lane configurations, depending on the DDC configuration and the acceptable lane rate of the receiving logic device. Multiple device synchronization is supported through the SYSREF± and SYNCINB± input pins.

The AD9680 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using a 1.8 V to 3.3 V capable, 3-wire SPI.

The AD9680 is available in a Pb-free, 64-lead LFCSP and is specified over the −40°C to +85°C industrial temperature range. This product is protected by a U.S. patent.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate for each speed grade, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 1.

		AD9680-500			AD9680-820			AD9680-1000			AD9680-1250			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	14			14			14			14			Bits
ACCURACY														
No Missing Codes	Full	Guaranteed			Guaranteed			Guaranteed			Guaranteed			
Offset Error	Full	−0.3	0	+0.3	−0.3	0	+0.3	−0.31	0	+0.31	−0.31	0	+0.31	% FSR
Offset Matching	Full		0	0.3		0	0.23		0	0.23		0	0.3	% FSR
Gain Error	Full	−6	0	+6	−6	0	+6	−6	0	+6	−6	0	+6	% FSR
Gain Matching	Full		1	5.1		1	5.5		1	4.5		1	4.5	% FSR
Differential Nonlinearity (DNL)	Full	−0.6	±0.5	+0.7	−0.7	±0.5	+0.8	−0.7	±0.5	+0.8	−0.8	±0.5	+0.8	LSB
Integral Nonlinearity (INL)	Full	−4.5	±2.5	+5.0	−3.3	±2.5	+4.3	−5.7	±2.5	+6.9	−6	±3	+6	LSB
TEMPERATURE DRIFT														
Offset Error	Full		−3			−10			−12			−15		ppm/°C
Gain Error	Full		±25			±54			±13.8			92		ppm/°C
INTERNAL VOLTAGE REFERENCE														
Voltage	Full		1.0			1.0			1.0			1.0		V
INPUT-REFERRED NOISE														
V_{REF} = 1.0 V	25°C		2.06			2.46			2.63			3.45		LSB rms
ANALOG INPUTS														
Differential Input Voltage Range (Programmable)	Full	1.46	2.06	2.06	1.46	1.70	1.94	1.46	1.70	1.94	1.46	1.58	1.94	V p-p
Common-Mode Voltage (V_{CM})	25°C		2.05			2.05			2.05			2.05		V
Differential Input Capacitance[1]	25°C		1.5			1.5			1.5			1.5		pF
Analog Input Full Power Bandwidth	25°C		2			2			2			2		GHz
POWER SUPPLY														
AVDD1	Full	1.22	1.25	1.28	1.22	1.25	1.28	1.22	1.25	1.28	1.22	1.25	1.28	V
AVDD2	Full	2.44	2.50	2.56	2.44	2.50	2.56	2.44	2.50	2.56	2.44	2.50	2.56	V
AVDD3	Full	3.2	3.3	3.4	3.2	3.3	3.4	3.2	3.3	3.4	3.2	3.3	3.4	V
AVDD1_SR	Full	1.22	1.25	1.28	1.22	1.25	1.28	1.22	1.25	1.28	1.22	1.25	1.28	V
DVDD	Full	1.22	1.25	1.28	1.22	1.25	1.28	1.22	1.25	1.28	1.22	1.25	1.28	V
DRVDD	Full	1.22	1.25	1.28	1.22	1.25	1.28	1.22	1.25	1.28	1.22	1.25	1.28	V
SPIVDD	Full	1.7	1.8	3.4	1.7	1.8	3.4	1.7	1.8	3.4	1.7	1.8	3.4	V
I_{AVDD1}	Full		435	467		605	660		685	720		785	880	mA
I_{AVDD2}	Full		395	463		490	545		595	680		675	780	mA
I_{AVDD3}	Full		87	101		125	140		125	142		125	142	mA
I_{AVDD1_SR}	Full		15	22		15	18		16	18		17	20	mA
I_{DVDD}[2]	Full		145	152		205	246		208	269		250	325	mA
I_{DRVDD}[1]	Full		190	237		200	240		200	225		220	300	mA
I_{DRVDD} (L = 2 Mode)	25°C		140			N/A[3]			N/A[3]			N/A[3]		mA
I_{SPIVDD}	Full		5	6		5	6		5	6		5	6	mA

Parameter	Temp	AD9680-500 Min	AD9680-500 Typ	AD9680-500 Max	AD9680-820 Min	AD9680-820 Typ	AD9680-820 Max	AD9680-1000 Min	AD9680-1000 Typ	AD9680-1000 Max	AD9680-1250 Min	AD9680-1250 Typ	AD9680-1250 Max	Unit
POWER CONSUMPTION														
Total Power Dissipation (Including Output Drivers)[2]	Full		2.2			2.9			3.3			3.7		W
Total Power Dissipation (L = 2 Mode)	25°C		2.1			N/A[3]			N/A[3]			N/A[3]		W
Power-Down Dissipation	Full		700			820			835			1030		mW
Standby[4]	Full		1.2			1.3			1.4			1.66		W

[1] All lanes running. Power dissipation on DRVDD changes with lane rate and number of lanes used.
[2] Default mode. No DDCs used. L = 4, M = 2, F = 1.
[3] N/A means not applicable. At the maximum sample rate, it is not applicable to use L = 2 mode on the JESD204B output interface because this exceeds the maximum lane rate of 12.5 Gbps. L = 2 mode is supported when the equation ((M × N´ × (10/8) × f_{OUT})/L) results in a line rate that is ≤12.5 Gbps. f_{OUT} is the output sample rate and is denoted by f_S/DCM, where DCM is the decimation ratio.
[4] Can be controlled by the SPI.

AC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate for each speed grade, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter[1]	Temp	AD9680-500 Min	AD9680-500 Typ	AD9680-500 Max	AD9680-820 Min	AD9680-820 Typ	AD9680-820 Max	AD9680-1000 Min	AD9680-1000 Typ	AD9680-1000 Max	AD9680-1250 Min	AD9680-1250 Typ	AD9680-1250 Max	Unit
ANALOG INPUT FULL SCALE	Full		2.06			1.7			1.7			1.58		V p-p
NOISE DENSITY[2]	Full		−153			−153			−154			−151.5		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)[3]														
f_{IN} = 10 MHz	25°C		69.2			67.2			67.2			63.6		dBFS
f_{IN} = 170 MHz	Full	67.8	69.0		65.6	67.0		65.1	66.6		61.5	63.2		dBFS
f_{IN} = 340 MHz	25°C		68.6			66.5			65.3			62.8		dBFS
f_{IN} = 450 MHz	25°C		68.0			65.1			64.0			62.2		dBFS
f_{IN} = 765 MHz	25°C		64.4			64.0			61.5			61.1		dBFS
f_{IN} = 985 MHz	25°C		63.8			63.4			60.5			59.2		dBFS
f_{IN} = 1950 MHz	25°C		60.5			59.7			57.0			55.5		dBFS
SNR AND DISTORTION RATIO (SINAD)[3]														
f_{IN} = 10 MHz	25°C		69.0			67.1			67.1			63.5		dBFS
f_{IN} = 170 MHz	Full	67.6	68.8		65.2	66.8		65.0	66.4		61.4	62.8		dBFS
f_{IN} = 340 MHz	25°C		68.4			66.3			65.2			62.6		dBFS
f_{IN} = 450 MHz	25°C		67.9			64.7			63.8			61.8		dBFS
f_{IN} = 765 MHz	25°C		64.2			63.5			62.1			60.8		dBFS
f_{IN} = 985 MHz	25°C		63.6			62.7			61.1			58.2		dBFS
f_{IN} = 1950 MHz	25°C		60.3			58.7			56.0			51.5		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)														
f_{IN} = 10 MHz	25°C		11.2			10.9			10.8			10.3		Bits
f_{IN} = 170 MHz	Full	10.9	11.1		10.5	10.8		10.5	10.7		9.9	10.1		Bits
f_{IN} = 340 MHz	25°C		11.1			10.7			10.5			10.1		Bits
f_{IN} = 450 MHz	25°C		11.0			10.5			10.3			10.0		Bits
f_{IN} = 765 MHz	25°C		10.4			10.3			10.0			9.8		Bits
f_{IN} = 985 MHz	25°C		10.3			10.1			9.8			9.4		Bits
f_{IN} = 1950 MHz	25°C		9.7			9.5			9.0			8.3		Bits

Parameter[1]	Temp	AD9680-500 Min	AD9680-500 Typ	AD9680-500 Max	AD9680-820 Min	AD9680-820 Typ	AD9680-820 Max	AD9680-1000 Min	AD9680-1000 Typ	AD9680-1000 Max	AD9680-1250 Min	AD9680-1250 Typ	AD9680-1250 Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)[3]														
f_{IN} = 10 MHz	25°C		83			91			88			84		dBFS
f_{IN} = 170 MHz	Full	80	88		75	83		75	85		74	77		dBFS
f_{IN} = 340 MHz	25°C		83			81			85			78		dBFS
f_{IN} = 450 MHz	25°C		81			78			82			76		dBFS
f_{IN} = 765 MHz	25°C		80			78			82			77		dBFS
f_{IN} = 985 MHz	25°C		75			74			80			71		dBFS
f_{IN} = 1950 MHz	25°C		70			70			68			61		dBFS
WORST HARMONIC, SECOND OR THIRD[3]														
f_{IN} = 10 MHz	25°C		−83			−91			−88			−84		dBFS
f_{IN} = 170 MHz	Full		−88	−80		−83	−75		−85	−75		−77	−74	dBFS
f_{IN} = 340 MHz	25°C		−83			−81			−85			−78		dBFS
f_{IN} = 450 MHz	25°C		−81			−78			−82			−76		dBFS
f_{IN} = 765 MHz	25°C		−80			−78			−82			−77		dBFS
f_{IN} = 985 MHz	25°C		−75			−74			−80			−71		dBFS
f_{IN} = 1950 MHz	25°C		−70			−70			−68			−61		dBFS
WORST OTHER, EXCLUDING SECOND OR THIRD HARMONIC[3]														
f_{IN} = 10 MHz	25°C		−95			−97			−95			−87		dBFS
f_{IN} = 170 MHz	Full		−95	−82		−93	−80		−94	−81		−79	−74	dBFS
f_{IN} = 340 MHz	25°C		−93			−91			−88			−81		dBFS
f_{IN} = 450 MHz	25°C		−93			−90			−86			−79		dBFS
f_{IN} = 765 MHz	25°C		−88			−83			−81			−79		dBFS
f_{IN} = 985 MHz	25°C		−89			−84			−82			−77		dBFS
f_{IN} = 1950 MHz	25°C		−84			−74			−75			−69		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD), A_{IN1} AND A_{IN2} = −7 dBFS														
f_{IN1} = 185 MHz, f_{IN2} = 188 MHz	25°C		−88			−90			−87			−82		dBFS
f_{IN1} = 338 MHz, f_{IN2} = 341 MHz	25°C		−88			−87			−88			−78[4]		dBFS
CROSSTALK[5]	25°C		95			95			95			95		dB
FULL POWER BANDWIDTH[6]	25°C		2			2			2			2		GHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Noise density is measured at a low analog input frequency (30 MHz).
[3] See Table 10 for the recommended settings for full-scale voltage and buffer current settings.
[4] Measurement taken with 449 MHz and 452 MHz inputs for two-tone.
[5] Crosstalk is measured at 170 MHz with a −1.0 dBFS analog input on one channel and no input on the adjacent channel.
[6] Measured with the circuit shown in Figure 115.

DIGITAL SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate for each speed grade, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage	Full	600	1200	1800	mV p-p
Input Common-Mode Voltage	Full		0.85		V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance	Full			2.5	pF
SYSREF INPUTS (SYSREF+, SYSREF−)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage	Full	400	1200	1800	mV p-p
Input Common-Mode Voltage	Full	0.6	0.85	2.0	V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance (Differential)	Full			2.5	pF
LOGIC INPUTS (SDI, SCLK, CSB, PDWN/STBY)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage	Full	0.8 × SPIVDD			V
Logic 0 Voltage	Full	0		0.5	V
Input Resistance	Full		30		kΩ
LOGIC OUTPUT (SDIO)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage (I_{OH} = 800 µA)	Full	0.8 × SPIVDD			V
Logic 0 Voltage (I_{OL} = 50 µA)	Full	0		0.5	V
SYNCIN INPUT (SYNCINB+/SYNCINB−)					
Logic Compliance	Full		LVDS/LVPECL/CMOS		
Differential Input Voltage	Full	400	1200	1800	mV p-p
Input Common-Mode Voltage	Full	0.6	0.85	2.0	V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance	Full			2.5	pF
LOGIC OUTPUTS (FD_A, FD_B)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage	Full	0.8 × SPIVDD			V
Logic 0 Voltage	Full	0		0.5	V
Input Resistance	Full		30		kΩ
DIGITAL OUTPUTS (SERDOUTx±, x = 0 TO 3)					
Logic Compliance	Full		CML		
Differential Output Voltage	Full	360		770	mV p-p
Output Common-Mode Voltage (V_{CM})					
AC-Coupled	25°C	0		1.8	V
Short-Circuit Current (I_{DSHORT})	25°C	−100		+100	mA
Differential Return Loss (RL_{DIFF})[1]	25°C	8			dB
Common-Mode Return Loss (RL_{CM})[1]	25°C	6			dB
Differential Termination Impedance	Full	80	100	120	Ω

[1] Differential and common-mode return loss are measured from 100 MHz to 0.75 × baud rate.

SWITCHING SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate for each speed grade, A_{IN} = −1.0 dBFS, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 4.

		AD9680-500			AD9680-820			AD9680-1000			AD9680-1250			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK														
Clock Rate (at CLK+/CLK− Pins)	Full	0.3		4	0.3		4	0.3		4	0.3		4	GHz
Maximum Sample Rate[1]	Full	500			820			1000			1250			MSPS
Minimum Sample Rate[2]	Full	300			300			300			300			MSPS
Clock Pulse Width High	Full	1000			609.7			500			400			ps
Clock Pulse Width Low	Full	1000			609.7			500			400			ps
OUTPUT PARAMETERS														
Unit Interval (UI)[3]	Full	80	200		80	121.95		80	100		80	80		ps
Rise Time (t_R) (20% to 80% into 100 Ω Load)	25°C	24	32		24	32		24	32		24	32		ps
Fall Time (t_F) (20% to 80% into 100 Ω Load)	25°C	24	32		24	32		24	32		24	32		ps
PLL Lock Time	25°C		2			2			2			2		ms
Data Rate per Channel (NRZ)[4]	25°C	3.125	5	12.5	3.125	8.2	12.5	3.125	10	12.5	3.1215	12.5	12.5	Gbps
LATENCY[5]														
Pipeline Latency	Full		55			55			55			55		Clock cycles
Fast Detect Latency	Full			28			28			28			28	Clock cycles
Wake-Up Time[6]														
Standby	25°C		1			1			1			1		ms
Power-Down	25°C			4			4			4			4	ms
APERTURE														
Aperture Delay (t_A)	Full		530			530			530			530		ps
Aperture Uncertainty (Jitter, t_J)	Full		55			55			55			55		f_S rms
Out-of-Range Recovery Time	Full		1			1			1			1		Clock cycles

[1] The maximum sample rate is the clock rate after the divider.
[2] The minimum sample rate operates at 300 MSPS with L = 2 or L = 1.
[3] Baud rate = 1/UI. A subset of this range can be supported.
[4] Default L = 4. This number can be changed based on the sample rate and decimation ratio.
[5] No DDCs used. L = 4, M = 2, F = 1.
[6] Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLK+ to SYSREF+ TIMING REQUIREMENTS	See Figure 3				
t_{SU_SR}	Device clock to SYSREF+ setup time		117		ps
t_{H_SR}	Device clock to SYSREF+ hold time		−96		ps
SPI TIMING REQUIREMENTS	See Figure 4				
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK must be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK must be in a logic low state	10			ns
t_{ACCESS}	Maximum time delay between falling edge of SCLK and output data valid for a read operation		6	10	ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 4)	10			ns

Timing Diagrams

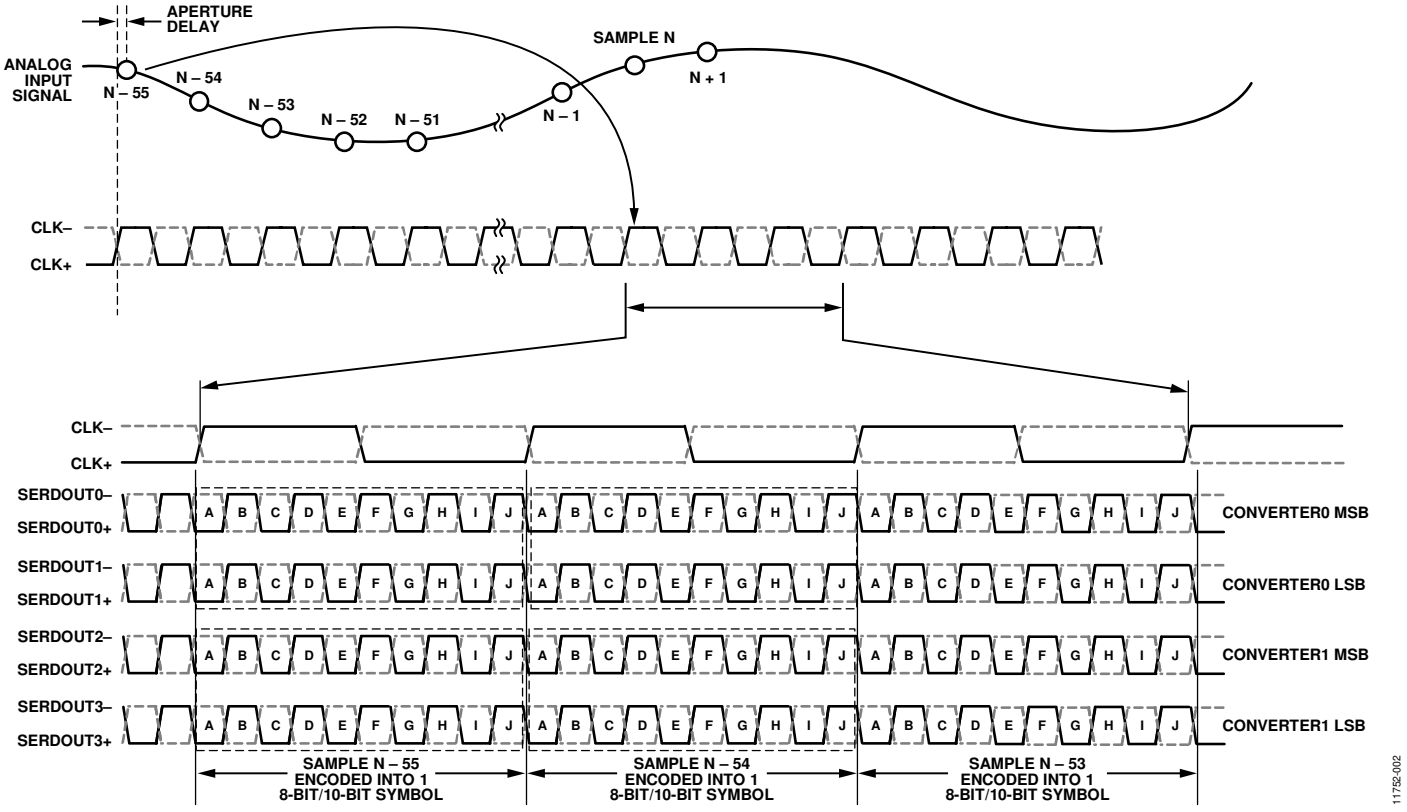


Figure 2. Data Output Timing (Full Bandwidth Mode; L = 4; M = 2; F = 1)

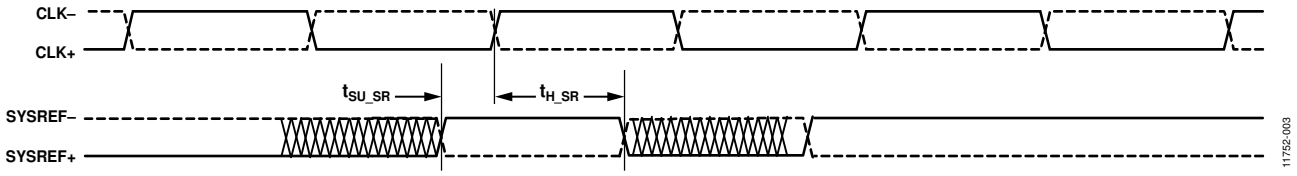


Figure 3. SYSREF± Setup and Hold Timing

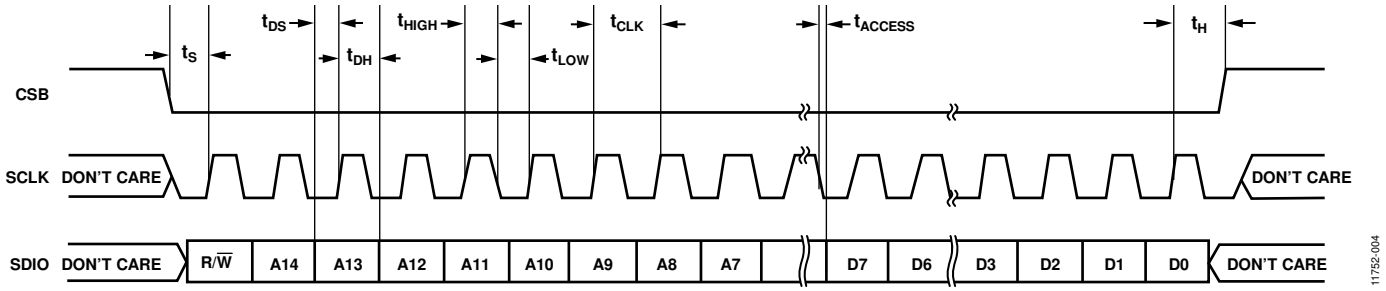


Figure 4. Serial Port Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD1 to AGND	1.32 V
AVDD1_SR to AGND	1.32 V
AVDD2 to AGND	2.75 V
AVDD3 to AGND	3.63 V
DVDD to DGND	1.32 V
DRVDD to DRGND	1.32 V
SPIVDD to AGND	3.63 V
AGND to DRGND	−0.3 V to +0.3 V
VIN±x to AGND	3.2 V
SCLK, SDIO, CSB to AGND	−0.3 V to SPIVDD + 0.3 V
PDWN/STBY to AGND	−0.3 V to SPIVDD + 0.3 V
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−40°C to +115°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Typical θ_{JA}, θ_{JB}, and θ_{JC} are specified vs. the number of printed circuit board (PCB) layers in different airflow velocities (in m/sec). Airflow increases heat dissipation effectively reducing θ_{JA} and θ_{JB}. In addition, metal in direct contact with the package leads and exposed pad from metal traces, through holes, ground, and power planes, reduces θ_{JA}. Thermal performance for actual applications requires careful inspection of the conditions in an application. The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 6.

Table 7. Thermal Resistance Values

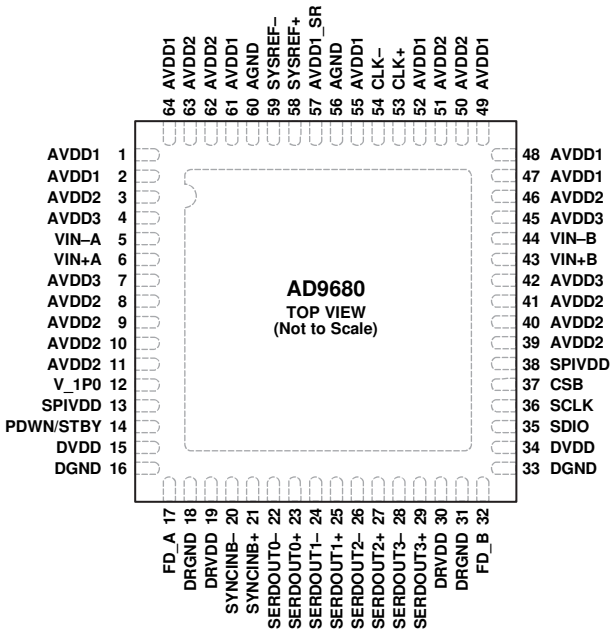
PCB Type	Airflow Velocity (m/sec)	θ_{JA}	Ψ_{JB}	θ_{JC_TOP}	θ_{JC_BOT}	Unit
JEDEC 2s2p Board	0.0	17.8[1, 2]	6.3[1, 3]	4.7[1, 4]	1.2[1, 4]	°C/W
	1.0	15.6[1, 2]	5.9[1, 3]	N/A[5]		°C/W
	2.5	15.0[1, 2]	5.7[1, 3]	N/A[5]		°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2s2p test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per JEDEC JESD51-8 (still air).
[4] Per MIL-STD 883, Method 1012.1.
[5] N/A means not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE GROUND REFENCE FOR AVDDx. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

11752-005

Figure 5. Pin Configuration (Top View)

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
Power Supplies			
0	EPAD	Ground	Exposed Pad. The exposed thermal pad on the bottom of the package provides the ground reference for AVDDx. This exposed pad must be connected to ground for proper operation.
1, 2, 47, 48, 49, 52, 55, 61, 64	AVDD1	Supply	Analog Power Supply (1.25 V Nominal).
3, 8, 9, 10, 11, 39, 40, 41, 46, 50, 51, 62, 63	AVDD2	Supply	Analog Power Supply (2.5 V Nominal).
4, 7, 42, 45	AVDD3	Supply	Analog Power Supply (3.3 V Nominal).
13, 38	SPIVDD	Supply	Digital Power Supply for SPI (1.8 V to 3.3 V).
15, 34	DVDD	Supply	Digital Power Supply (1.25 V Nominal).
16, 33	DGND	Ground	Ground Reference for DVDD.
18, 31	DRGND	Ground	Ground Reference for DRVDD.
19, 30	DRVDD	Supply	Digital Driver Power Supply (1.25 V Nominal).
56, 60	AGND[1]	Ground	Ground Reference for SYSREF±.
57	AVDD1_SR[1]	Supply	Analog Power Supply for SYSREF± (1.25 V Nominal).
Analog			
5, 6	VIN–A, VIN+A	Input	ADC A Analog Input Complement/True.
12	V_1P0	Input/DNC	1.0 V Reference Voltage Input/Do Not Connect. This pin is configurable through the SPI as a no connect or an input. Do not connect this pin if using the internal reference. Requires a 1.0 V reference voltage input if using an external voltage reference source.
44, 43	VIN–B, VIN+B	Input	ADC B Analog Input Complement/True.
53, 54	CLK+, CLK–	Input	Clock Input True/Complement.
CMOS Outputs			
17, 32	FD_A, FD_B	Output	Fast Detect Outputs for Channel A and Channel B.

Pin No.	Mnemonic	Type	Description
Digital Inputs			
20, 21	SYNCINB−, SYNCINB+	Input	Active Low JESD204B LVDS Sync Input True/Complement.
58, 59	SYSREF+, SYSREF−	Input	Active High JESD204B LVDS System Reference Input True/Complement.
Data Outputs			
22, 23	SERDOUT0−, SERDOUT0+	Output	Lane 0 Output Data Complement/True.
24, 25	SERDOUT1−, SERDOUT1+	Output	Lane 1 Output Data Complement/True.
26, 27	SERDOUT2−, SERDOUT2+	Output	Lane 2 Output Data Complement/True.
28, 29	SERDOUT3−, SERDOUT3+	Output	Lane 3 Output Data Complement/True.
Device Under Test (DUT) Controls			
14	PDWN/STBY	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby. Requires an external 10 kΩ pull-down resistor.
35	SDIO	Input/Output	SPI Serial Data Input/Output.
36	SCLK	Input	SPI Serial Clock.
37	CSB	Input	SPI Chip Select (Active Low).

[1] To ensure proper ADC operation, connect AVDD1_SR and AGND separately from the AVDD1 and EPAD connection. For more information, see the Applications Information section.

TYPICAL PERFORMANCE CHARACTERISTICS

AD9680-1250

AVDD1 = 1.25 V, AVDD1_SR = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, 1.58 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, default SPI settings, clock divider = 2, T_A = 25°C, 128k FFT sample, unless otherwise noted. See Table 10 for recommended settings.

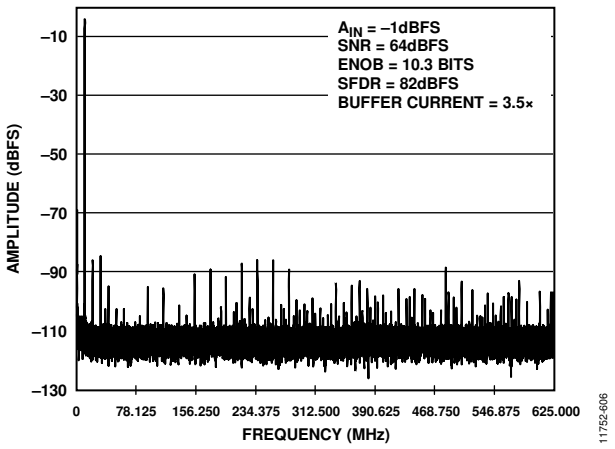


Figure 6. Single-Tone FFT with f_{IN} = 10.3 MHz

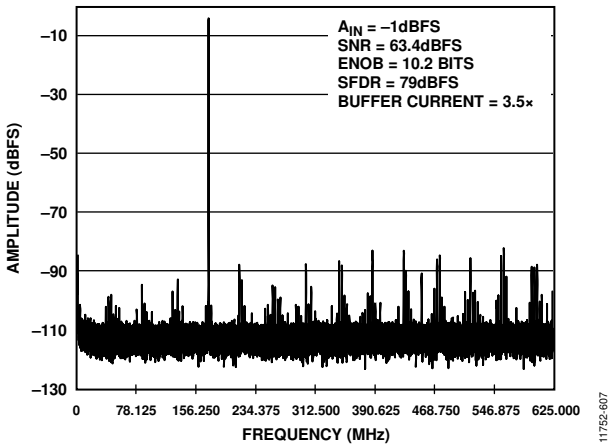


Figure 7. Single-Tone FFT with f_{IN} = 170.3 MHz

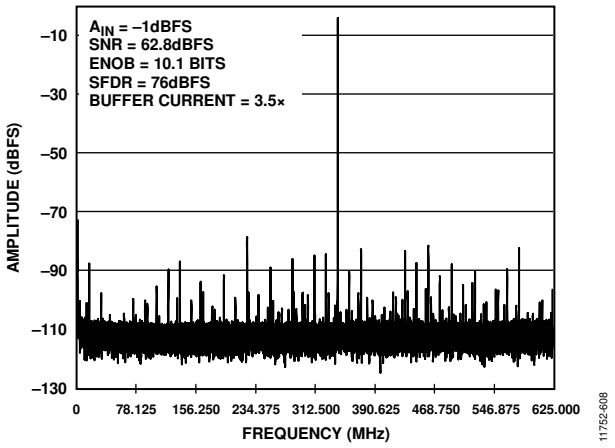


Figure 8. Single-Tone FFT with f_{IN} = 340.3 MHz

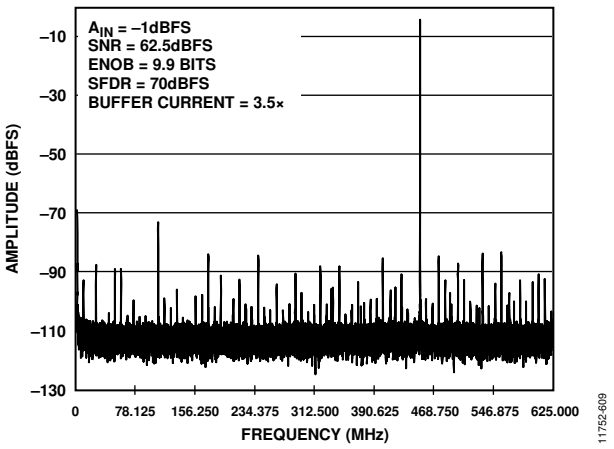


Figure 9. Single-Tone FFT with f_{IN} = 450.3 MHz

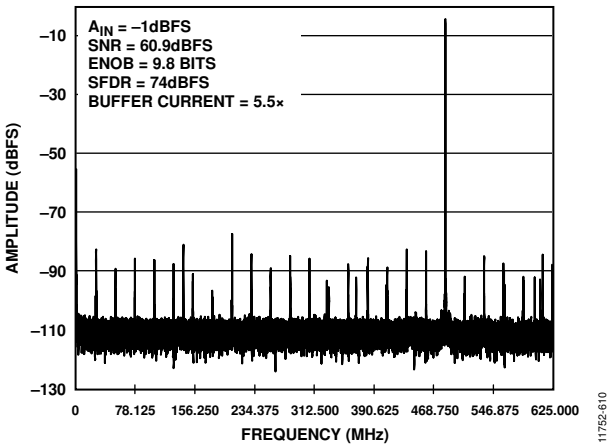


Figure 10. Single-Tone FFT with f_{IN} = 765.3 MHz

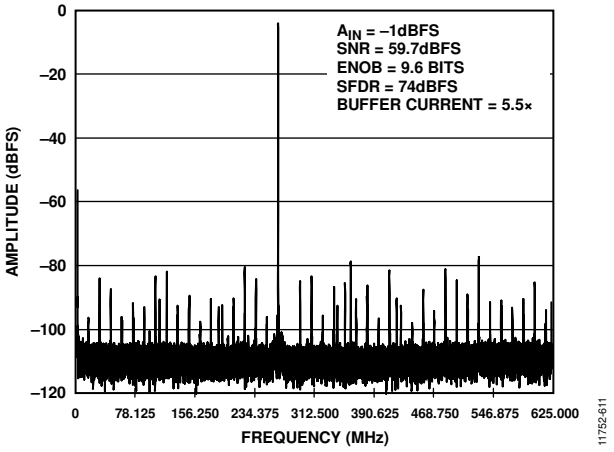


Figure 11. Single-Tone FFT with f_{IN} = 985.3 MHz

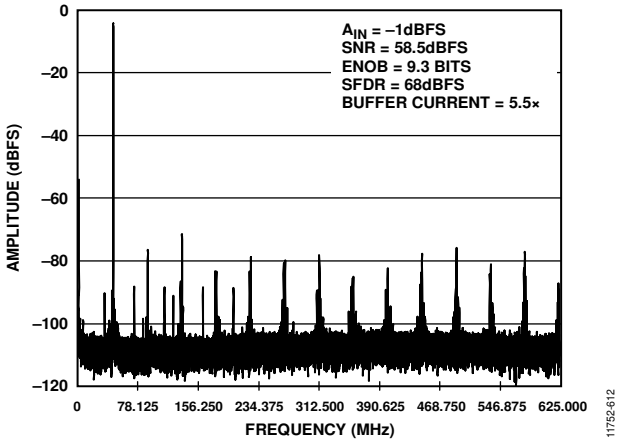


Figure 12. Single-Tone FFT with f_{IN} = 1205.3 MHz

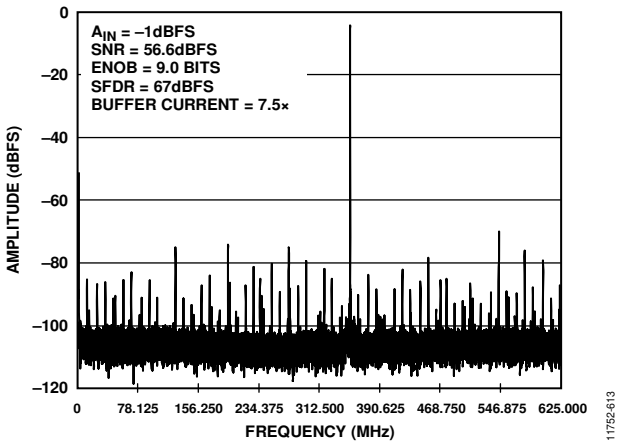


Figure 13. Single-Tone FFT with f_{IN} = 1602.3 MHz

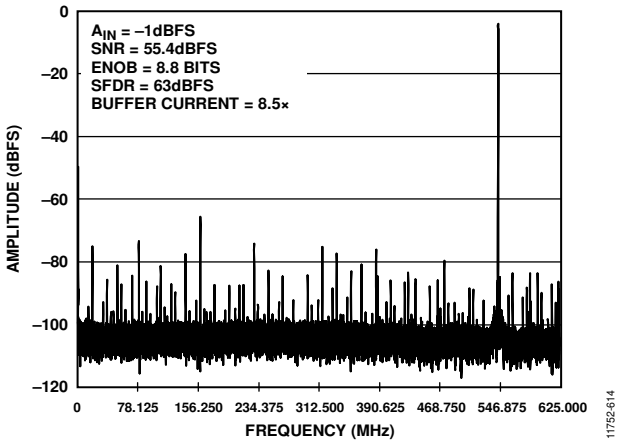


Figure 14. Single-Tone FFT with f_{IN} = 1954.3 MHz

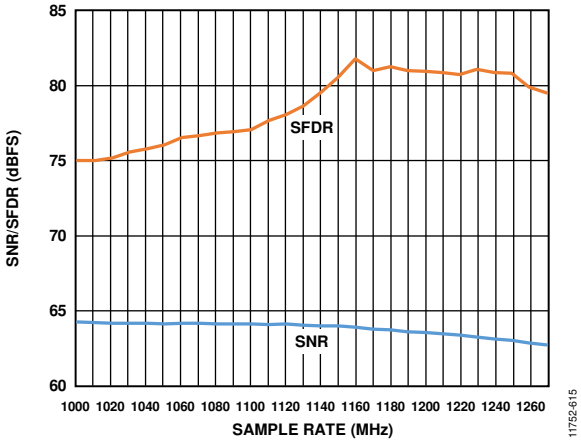


Figure 15. SNR/SFDR vs. f_S, f_{IN} = 170.3 MHz; Buffer Control 1 (0x018) = 3.5×

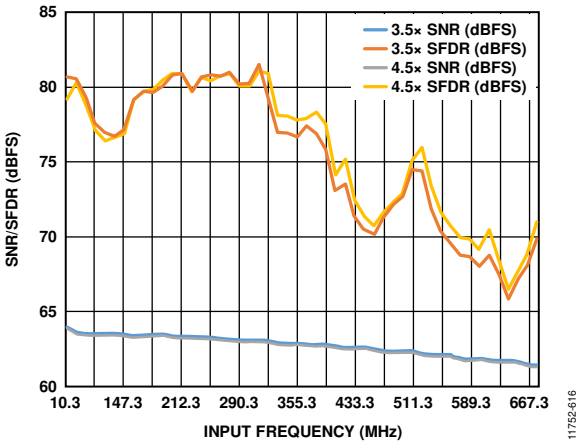


Figure 16. SNR/SFDR vs. f_{IN}; f_{IN} < 700 MHz; Buffer Control 1 (0x018) = 3.5× and 4.5×

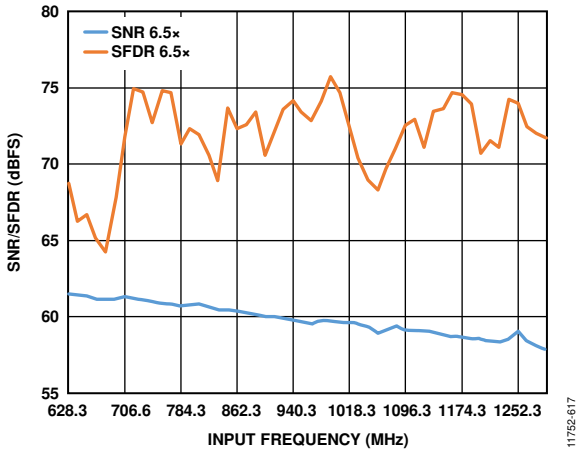


Figure 17. SNR/SFDR vs. f_{IN}; 650 MHz < f_{IN} < 1.3 GHz; Buffer Control 1 (0x018) = 6.5×

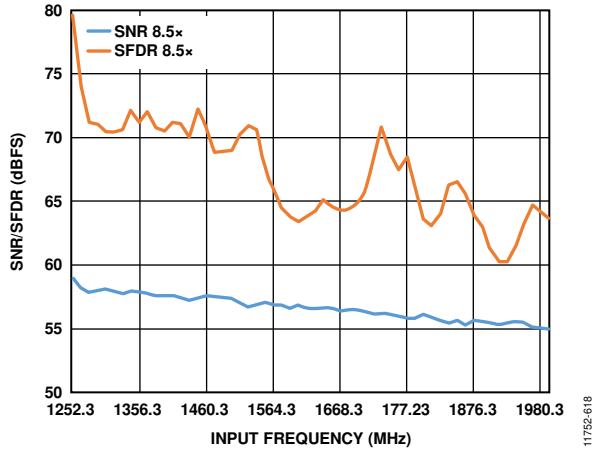


Figure 18. SNR/SFDR vs. f_{IN}; 1.3 GHz < f_{IN} < 2GHz; Buffer Control 1 (0x018) = 8.5×

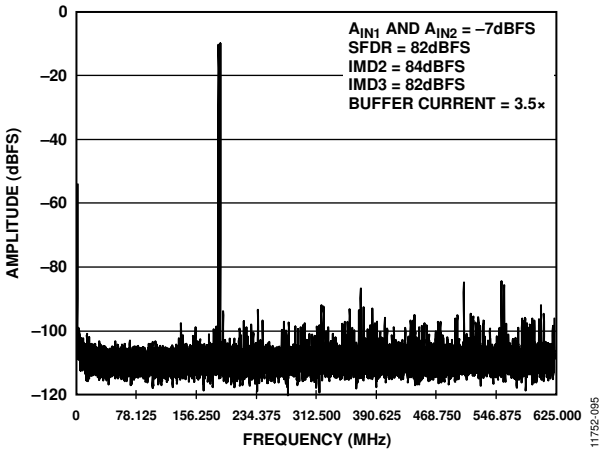


Figure 19. Two-Tone FFT; f_{IN1} = 184 MHz, f_{IN2} = 187 MHz

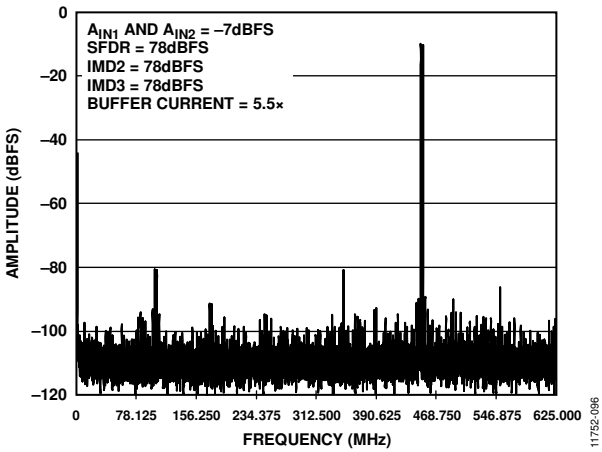


Figure 20. Two-Tone FFT; f_{IN1} = 449 MHz, f_{IN2} = 452 MHz

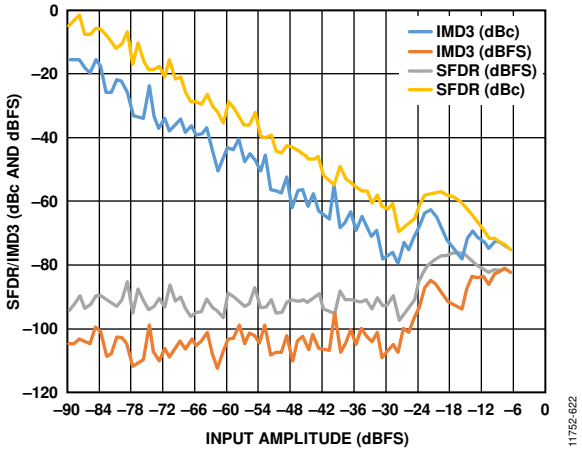


Figure 21. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184 MHz and f_{IN2} = 187 MHz

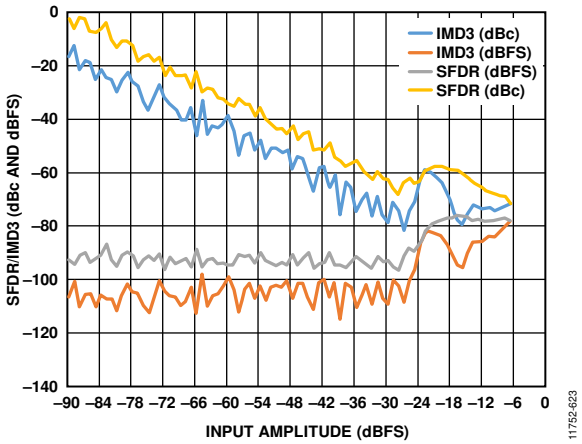


Figure 22. Two-Tone IMD3/SFDR vs. Input Amplitude (A_{IN}) with f_{IN1} = 449 MHz and f_{IN2} = 452 MHz

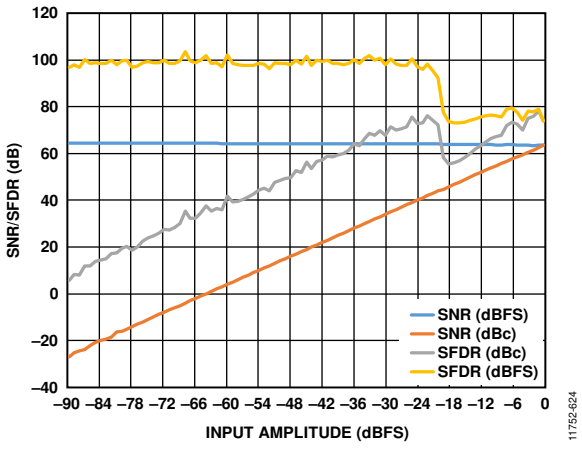


Figure 23. SNR/SFDR vs. Analog Input Level, f_{IN} = 170.3 MHz

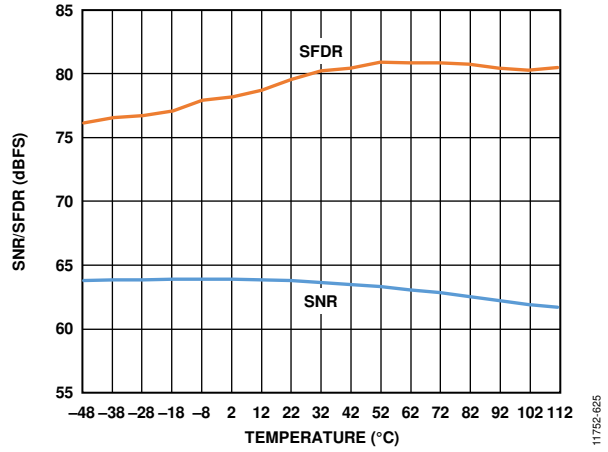


Figure 24. SNR/SFDR vs. Temperature, f_{IN} = 170.3 MHz

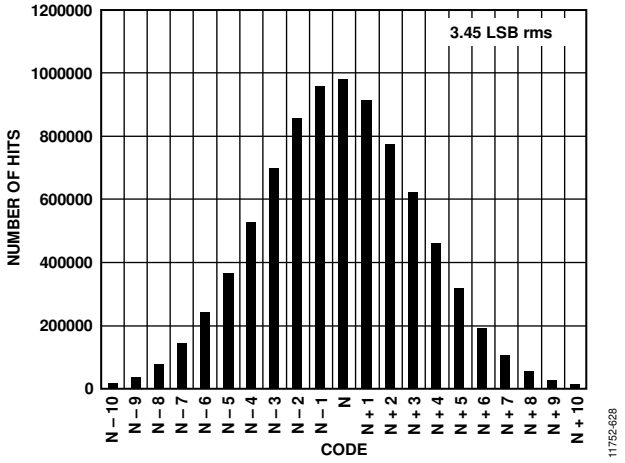


Figure 27. Input-Referred Noise Histogram

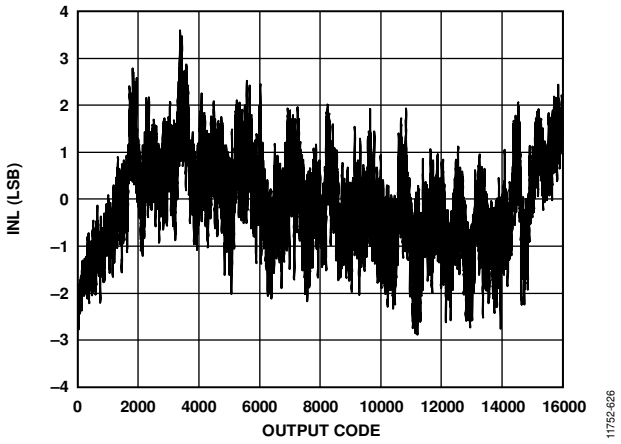


Figure 25. INL, f_{IN} = 10.3 MHz

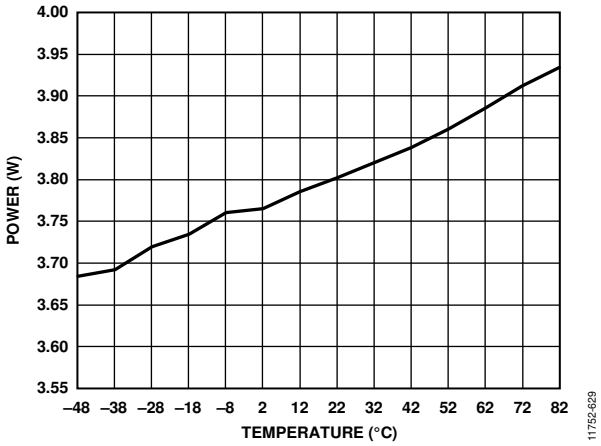


Figure 28. Power Dissipation vs. Temperature

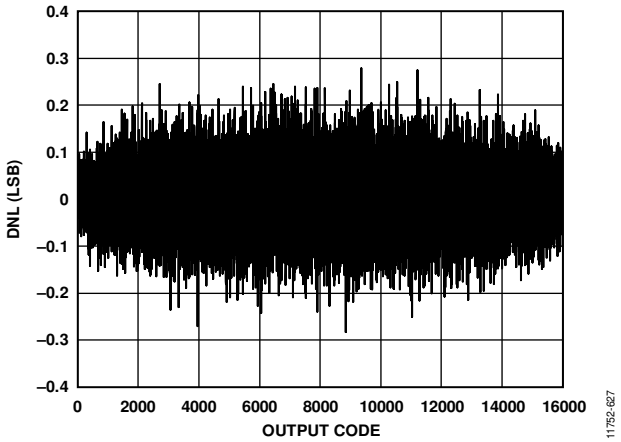


Figure 26. DNL, f_{IN} = 15 MHz

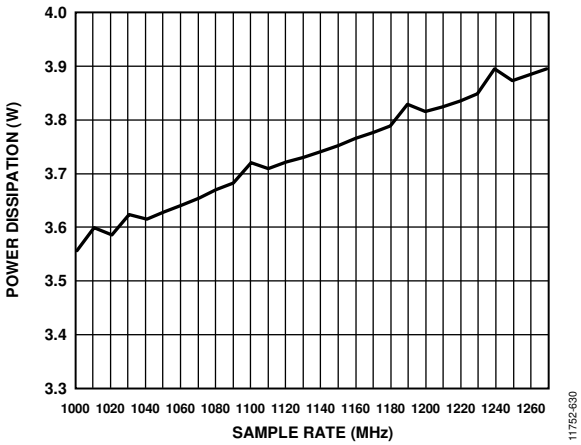


Figure 29. Power Dissipation vs. f_S

AD9680-1000

AVDD1 = 1.25 V, AVDD1_SR = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, 1.7 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, default SPI settings, clock divider = 2, T_A = 25°C, 128k FFT sample, unless otherwise noted. See Table 10 for recommended settings.

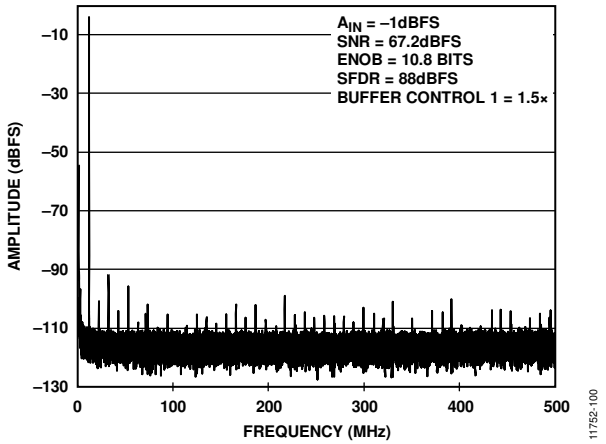


Figure 30. Single-Tone FFT with f_{IN} = 10.3 MHz

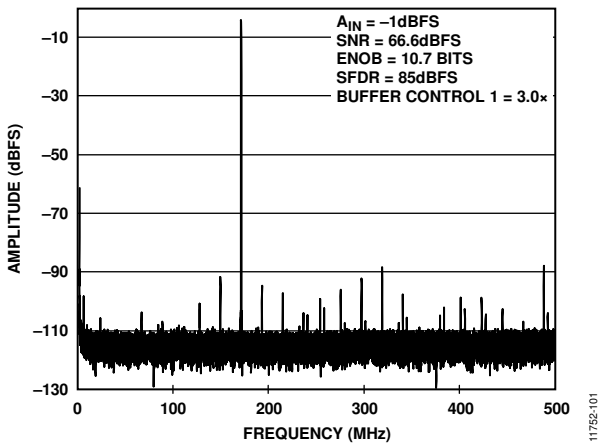


Figure 31. Single-Tone FFT with f_{IN} = 170.3 MHz

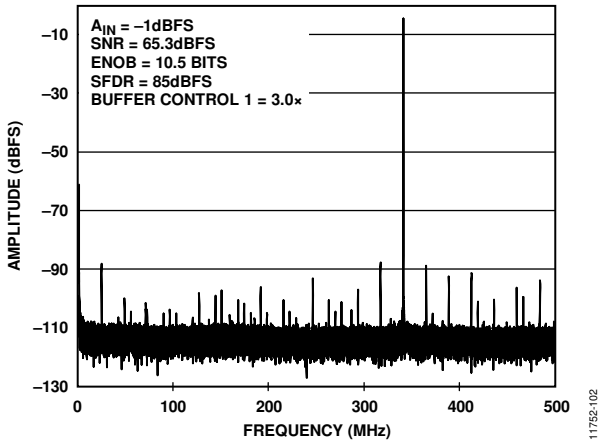


Figure 32. Single-Tone FFT with f_{IN} = 340.3 MHz

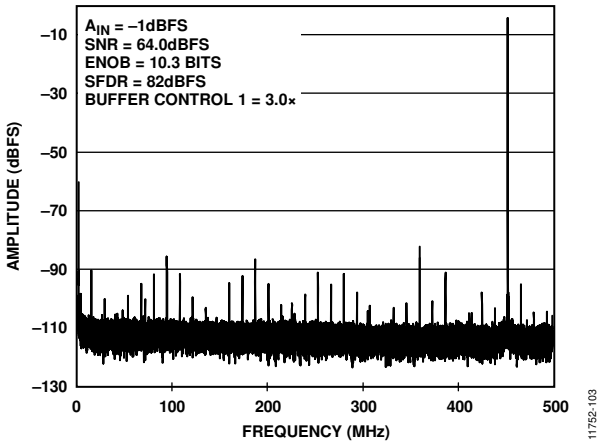


Figure 33. Single-Tone FFT with f_{IN} = 450.3 MHz

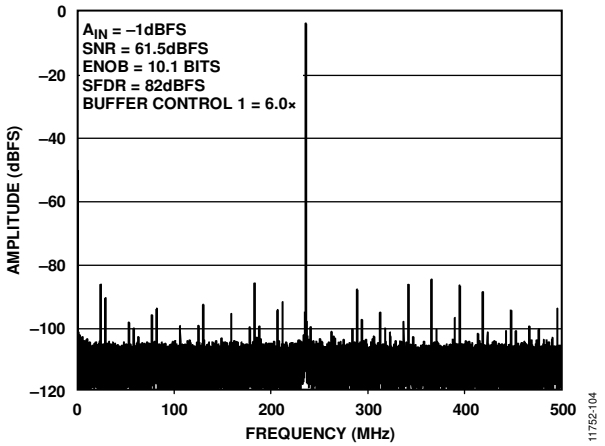


Figure 34. Single-Tone FFT with f_{IN} = 765.3 MHz

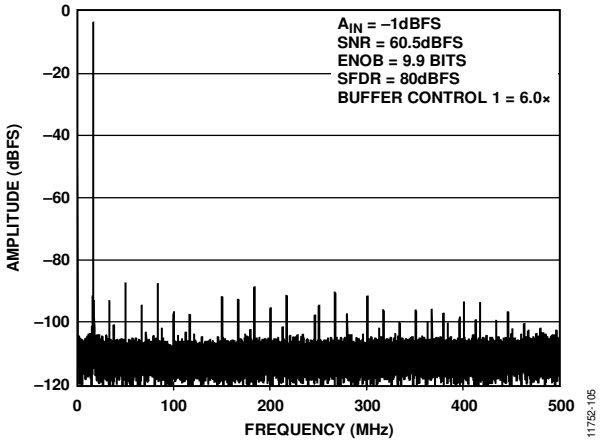


Figure 35. Single-Tone FFT with f_{IN} = 985.3 MHz

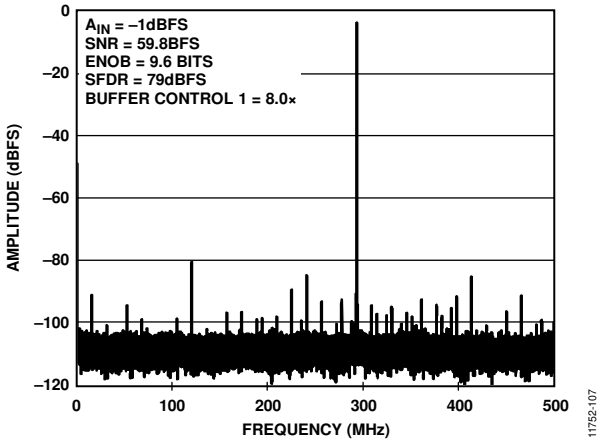


Figure 36. Single-Tone FFT with f_{IN} = 1293.3 MHz

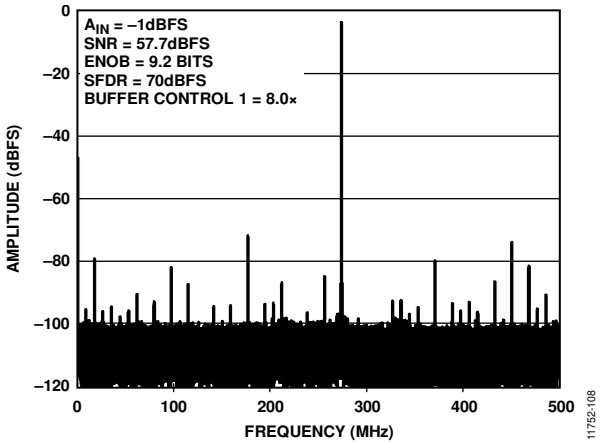


Figure 37. Single-Tone FFT with f_{IN} = 1725.3 MHz

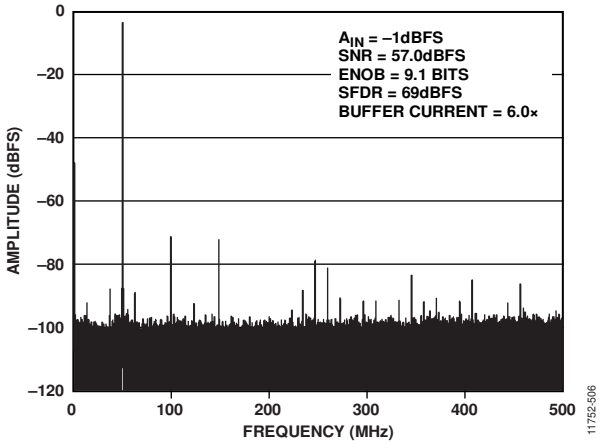


Figure 38. Single-Tone FFT with f_{IN} = 1950.3 MHz

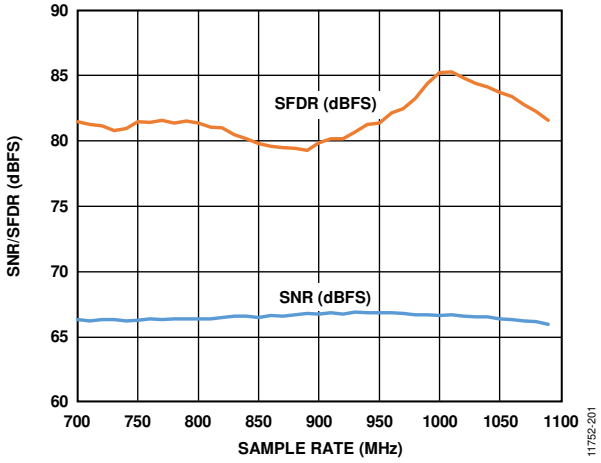


Figure 39. SNR/SFDR vs. f_S, f_{IN} = 170.3 MHz; Buffer Control 1 (0x018) = 3.0×

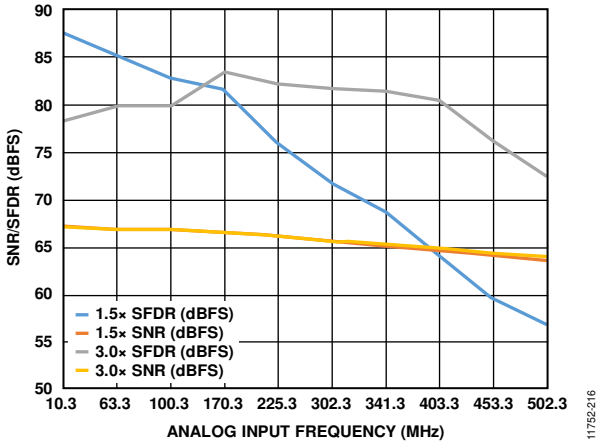


Figure 40. SNR/SFDR vs. f_{IN}; f_{IN} < 500 MHz; Buffer Control 1 (0x018) = 1.5× and 3.0×

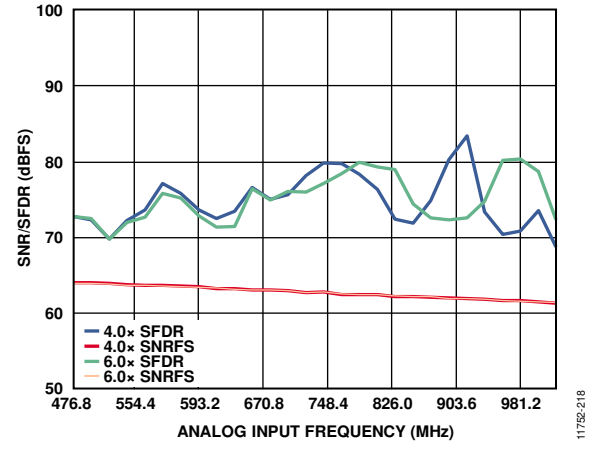


Figure 41. SNR/SFDR vs. f_{IN}; 500 MHz < f_{IN} < 1 GHz; Buffer Control 1 (0x018) = 4.0× and 6.0×

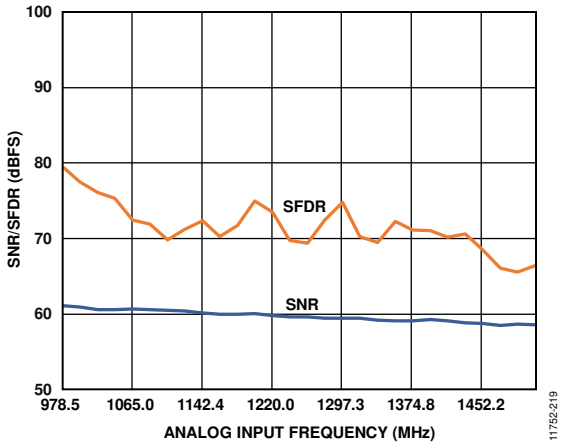


Figure 42. SNR/SFDR vs. f_{IN}; 1 GHz < f_{IN} < 1.5 GHz; Buffer Control 1 (0x018) = 6.0×

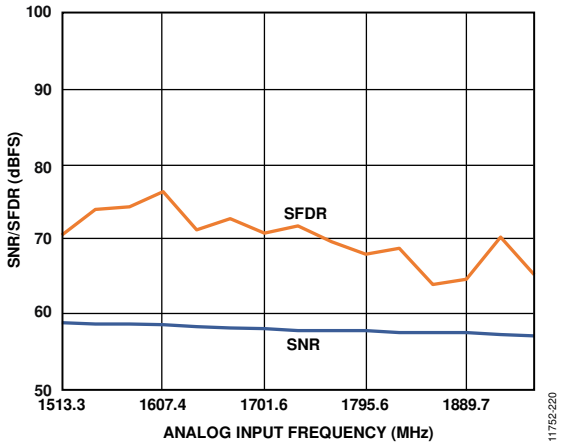


Figure 43. SNR/SFDR vs. f_{IN}; 1.5 GHz < f_{IN} < 2 GHz; Buffer Control 1 (0x018) = 7.5×

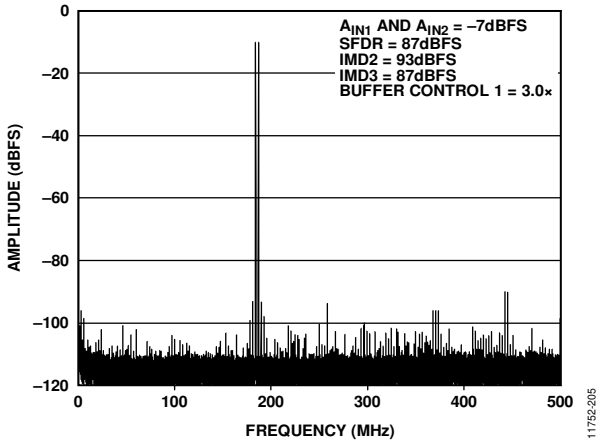


Figure 44. Two-Tone FFT; f_{IN1} = 184 MHz, f_{IN2} = 187 MHz

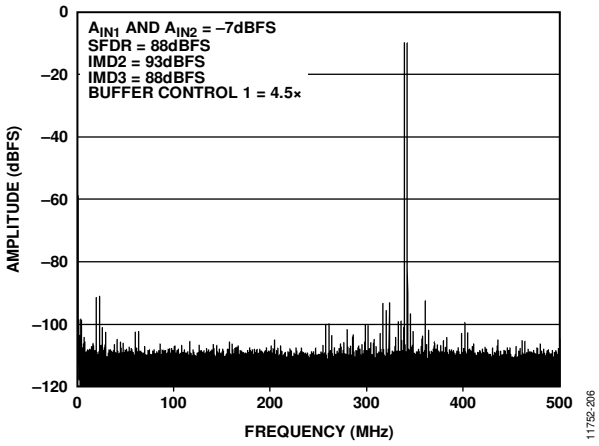


Figure 45. Two-Tone FFT; f_{IN1} = 338 MHz, f_{IN2} = 341 MHz

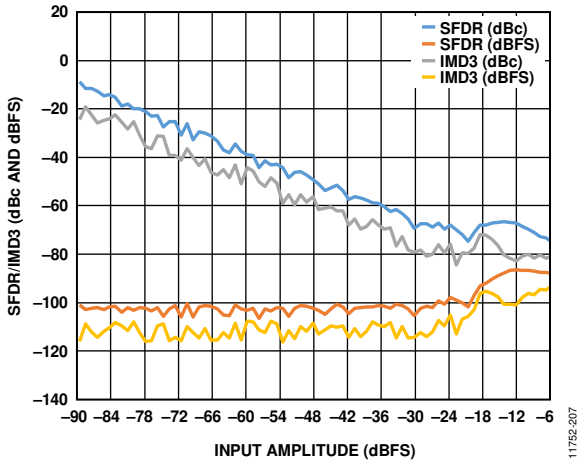


Figure 46. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184 MHz and f_{IN2} = 187 MHz

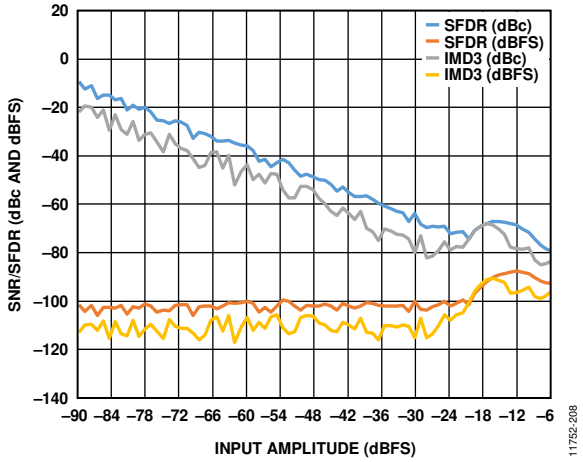


Figure 47. Two-Tone IMD3/SFDR vs. Input Amplitude (A_{IN}) with f_{IN1} = 338 MHz and f_{IN2} = 341 MHz

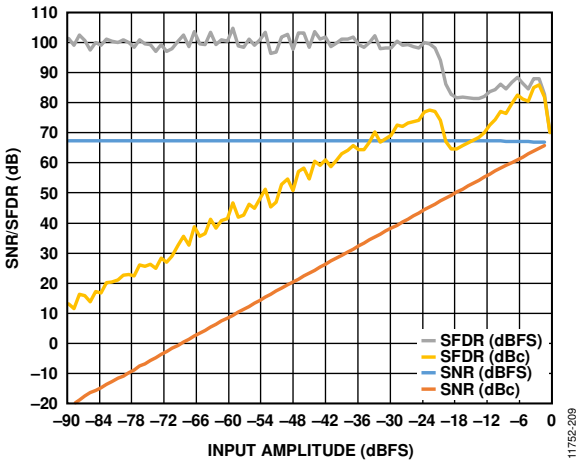


Figure 48. SNR/SFDR vs. Analog Input Level, f_{IN} = 170.3 MHz

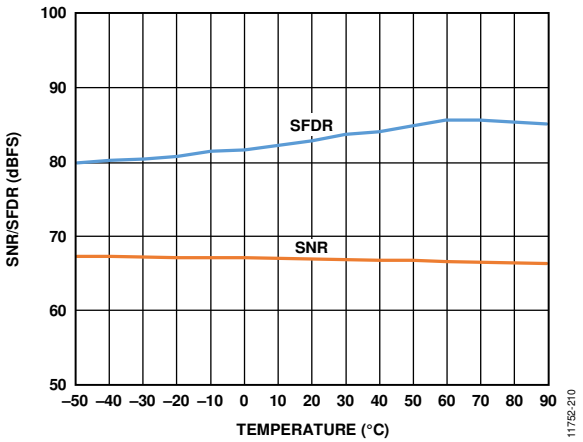


Figure 49. SNR/SFDR vs. Temperature, f_{IN} = 170.3 MHz

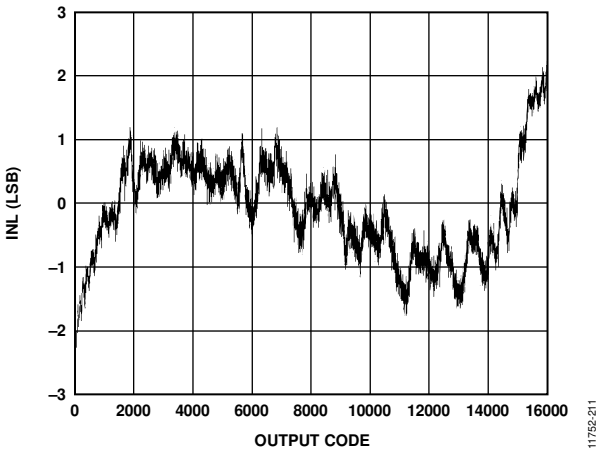


Figure 50. INL, f_{IN} = 10.3 MHz

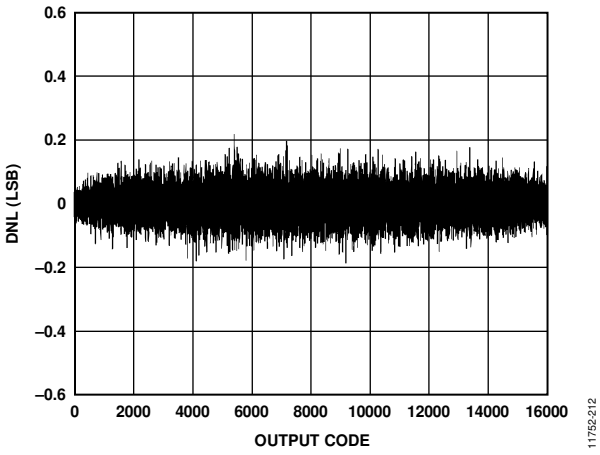


Figure 51. DNL, f_{IN} = 15 MHz

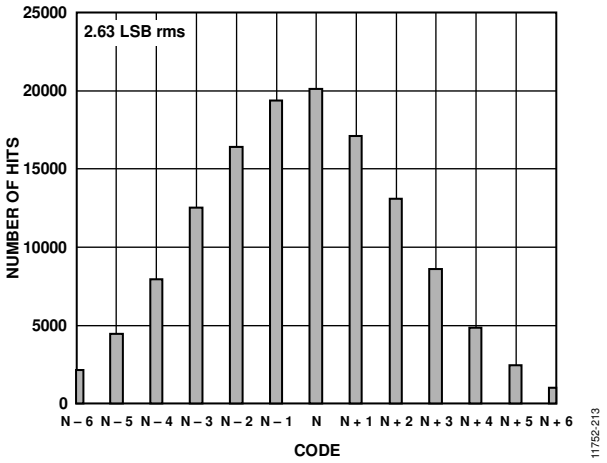


Figure 52. Input-Referred Noise Histogram

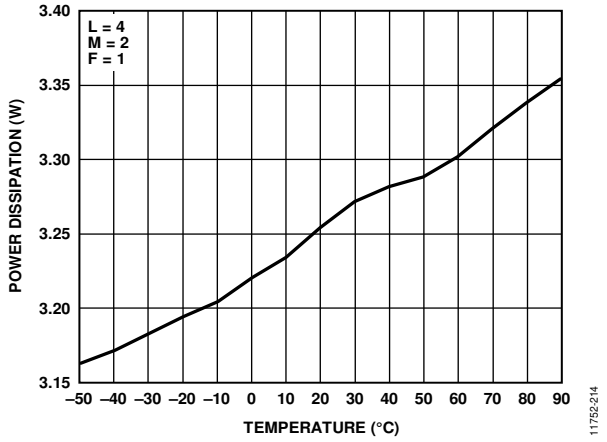


Figure 53. Power Dissipation vs. Temperature

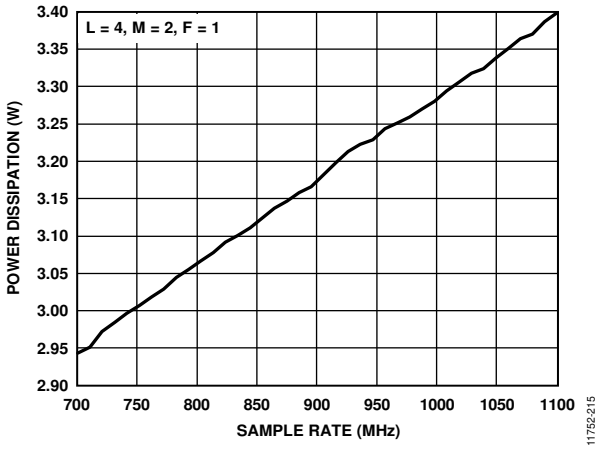


Figure 54. Power Dissipation vs. f_S