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Octal, 14-Bit, 125 MSPS, Serial LVDS, 1.8 V Analog-to-Digital Converter

Data Sheet **AD9681**

FEATURES

- Low power
  - 8 ADC channels integrated into 1 package
  - 110 mW per channel at 125 MSPS with scalable power options
- SNR: 74 dBFS (to Nyquist); SFDR: 90 dBc (to Nyquist)
- DNL: ±0.8 LSB (typical); INL: ±1.2 LSB (typical)
- Crosstalk, worst adjacent channel, 70 MHz, −1 dBFS: −83 dB typical
- Serial LVDS (ANSI-644, default)
  - Low power, reduced signal option (similar to IEEE 1596.3)
- Data and frame clock outputs
- 650 MHz full power analog bandwidth
- 2 V p-p input voltage range
- 1.8 V supply operation
- Serial port control
  - Flexible bit orientation
  - Built-in and custom digital test pattern generation
  - Programmable clock and data alignment
  - Power-down and standby modes

APPLICATIONS

- Medical imaging
- Communications receivers
- Multichannel data acquisition

GENERAL DESCRIPTION

The AD9681 is an octal, 14-bit, 125 MSPS analog-to-digital converter (ADC) with an on-chip sample-and-hold circuit that is designed for low cost, low power, small size, and ease of use. The device operates at a conversion rate of up to 125 MSPS and is optimized for outstanding dynamic performance and low power in applications where a small package size is critical.

The ADC requires a single 1.8 V power supply and an LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The AD9681 automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. Data clock outputs (DCO±1, DCO±2) for capturing data on the output and frame clock outputs (FCO±1, FCO±2) for signaling a new output byte are provided. Individual channel power-down is supported, and the device typically consumes less than 2 mW when all channels are disabled.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

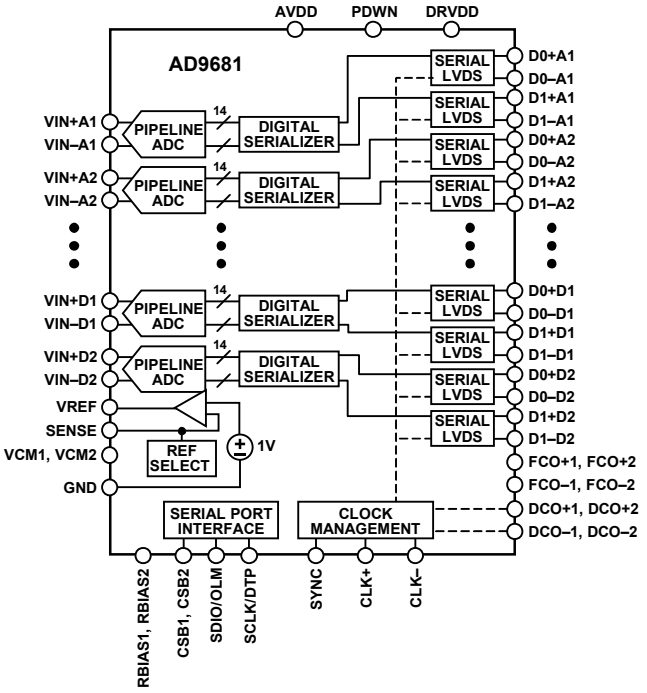

Figure 1.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

The AD9681 is available in an RoHS-compliant, 144-ball CSP-BGA. It is specified over the industrial temperature range of −40°C to +85°C. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Small Footprint. Eight ADCs are contained in a small, 10 mm × 10 mm package.
2. Low Power. The device dissipates 110 mW per channel at 125 MSPS with scalable power options.
3. Ease of Use. Data clock outputs (DCO±1, DCO±2) operate at frequencies of up to 500 MHz and support double data rate (DDR) operation.
4. User Flexibility. SPI control offers a wide range of flexible features to meet specific system requirements.

Rev. C

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AD9681* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9681 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9681: Octal, 14-Bit, 125 MSPS, Serial LVDS, 1.8 V Analog-to-Digital Converter Data Sheet

User Guides

- Evaluating the AD9681 Analog-to-Digital Converter

TOOLS AND SIMULATIONS

- AD9681 ADISimADC model
- AD9681 Input Impedance

REFERENCE MATERIALS

Press

- Low-Power 14-bit A/D Converters Enable High-Performance, Multi-Channel Data Acquisition in Compact Package

DESIGN RESOURCES

- AD9681 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9681 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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FUNCTIONAL BLOCK DIAGRAM

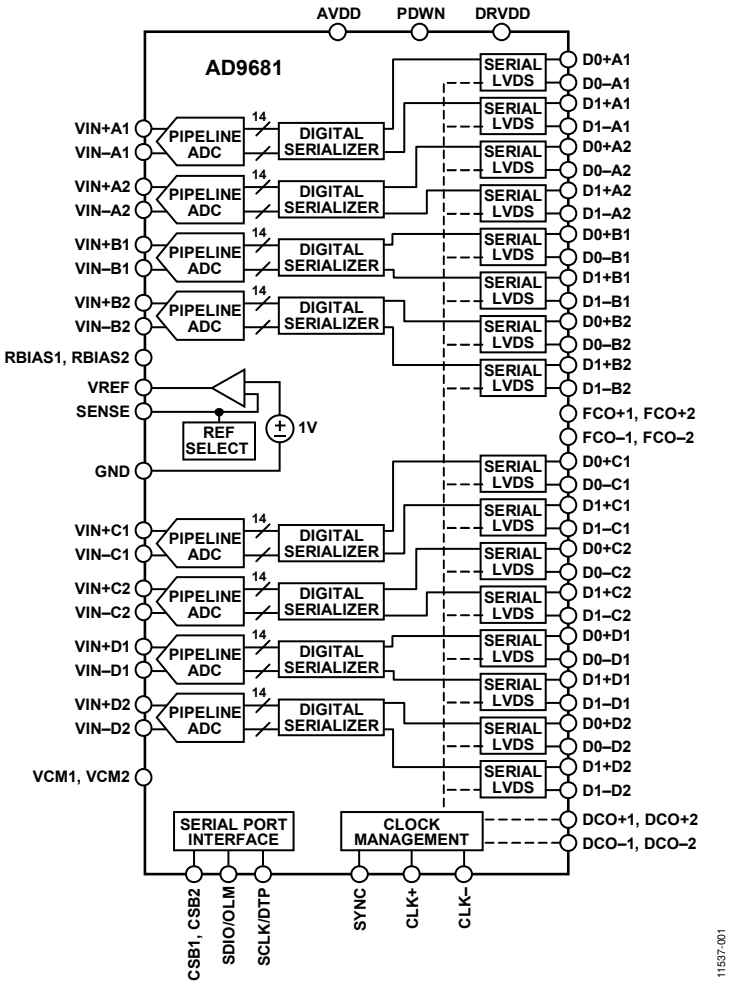

Figure 2.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, A_{IN} = −1.0 dBFS, unless otherwise noted.

Table 1.

Parameter[1]	Temp	Min	Typ	Max	Unit
RESOLUTION		14			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	−0.23	+0.21	+0.62	% FSR
Offset Matching	Full	0	0.24	0.7	% FSR
Gain Error	Full	−8.0	−3.1	+1.7	% FSR
Gain Matching	Full	0	1.8	6.0	% FSR
Differential Nonlinearity (DNL)	Full	−0.92	±0.8	+1.75	LSB
Integral Nonlinearity (INL)	Full	−4.0	±1.2	+4.0	LSB
TEMPERATURE DRIFT					
Offset Error	Full		−4		ppm/°C
Gain Error	Full		38		ppm/°C
INTERNAL VOLTAGE REFERENCE					
Output Voltage (1 V Mode)	Full	0.98	1.0	1.02	V
Load Regulation at 1.0 mA (V_{REF} = 1 V)	25°C		3		mV
Input Resistance	Full		7.5		kΩ
INPUT-REFERRED NOISE					
V_{REF} = 1.0 V	25°C		0.99		LSB rms
ANALOG INPUTS					
Differential Input Voltage (V_{REF} = 1 V)	Full		2		V p-p
Common-Mode Voltage	Full	0.5	0.9	1.3	V
Differential Input Resistance	Full		5.2		kΩ
Differential Input Capacitance	Full		3.5		pF
POWER SUPPLY					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
I_{AVDD}	Full		368	423	mA
I_{DRVDD} (ANSI-644 Mode)	Full		120	126	mA
I_{DRVDD} (Reduced Range Mode)	25°C		90		mA
TOTAL POWER CONSUMPTION					
Total Power Dissipation (Eight Channels, Including Output Drivers ANSI-644 Mode)	Full		879	988	mW
Total Power Dissipation (Eight Channels, Including Output Drivers Reduced Range Mode)	25°C		825		mW
Power-Down Dissipation	25°C		2		mW
Standby Dissipation[2]	25°C		485		mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for information about how these tests were completed.
[2] Controlled via the SPI.

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, A_{IN} = −1.0 dBFS, unless otherwise noted.

Table 2.

Parameter[1]	Temp	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 9.7 MHz	25°C		74.8		dBFS
f_{IN} = 19.7 MHz	25°C		74.7		dBFS
f_{IN} = 69.5 MHz	Full	72.6	73.9		dBFS
f_{IN} = 139.5 MHz	25°C		71.5		dBFS
f_{IN} = 201 MHz	25°C		69.6		dBFS
f_{IN} = 301 MHz	25°C		66.6		dBFS
SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)					
f_{IN} = 9.7 MHz	25°C		74.7		dBFS
f_{IN} = 19.7 MHz	25°C		74.7		dBFS
f_{IN} = 69.5 MHz	Full	72.3	73.8		dBFS
f_{IN} = 139.5 MHz	25°C		71.4		dBFS
f_{IN} = 201 MHz	25°C		69.3		dBFS
f_{IN} = 301 MHz	25°C		65.8		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 9.7 MHz	25°C		12.1		Bits
f_{IN} = 19.7 MHz	25°C		12.1		Bits
f_{IN} = 69.5 MHz	Full	11.7	12.0		Bits
f_{IN} = 139.5 MHz	25°C		11.6		Bits
f_{IN} = 201 MHz	25°C		11.2		Bits
f_{IN} = 301 MHz	25°C		10.6		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 9.7 MHz	25°C		94		dBc
f_{IN} = 19.7 MHz	25°C		94		dBc
f_{IN} = 69.5 MHz	Full	81	90		dBc
f_{IN} = 139.5 MHz	25°C		87		dBc
f_{IN} = 201 MHz	25°C		83		dBc
f_{IN} = 301 MHz	25°C		73		dBc
WORST HARMONIC (SECOND OR THIRD)					
f_{IN} = 9.7 MHz	25°C		−94		dBc
f_{IN} = 19.7 MHz	25°C		−94		dBc
f_{IN} = 69.5 MHz	Full		−90	−81	dBc
f_{IN} = 139.5 MHz	25°C		−87		dBc
f_{IN} = 201 MHz	25°C		−83		dBc
f_{IN} = 301 MHz	25°C		−73		dBc
WORST OTHER (EXCLUDING SECOND OR THIRD)					
f_{IN} = 9.7 MHz	25°C		−98		dBc
f_{IN} = 19.7 MHz	25°C		−94		dBc
f_{IN} = 69.5 MHz	Full		−96	−84	dBc
f_{IN} = 139.5 MHz	25°C		−90		dBc
f_{IN} = 201 MHz	25°C		−85		dBc
f_{IN} = 301 MHz	25°C		−75		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)—AIN1 AND AIN2 = −7.0 dBFS					
f_{IN1} = 70 MHz, f_{IN2} = 72.5 MHz	25°C		94		dBc
CROSSTALK, WORST ADJACENT CHANNEL[2]	25°C		−83		dB
Crosstalk, Worst Adjacent Channel Overrange Condition[3]	25°C		−79		dB
ANALOG INPUT BANDWIDTH, FULL POWER	25°C		650		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Crosstalk is measured at 70 MHz, with −1.0 dBFS analog input on one channel and no input on the adjacent channel.
[3] Overrange condition is defined as 3 dB above input full scale.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, A_{IN} = −1.0 dBFS, unless otherwise noted.

Table 3.

Parameter[1]	Temp	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	0.2		3.6	V p-p
Input Voltage Range	Full	GND − 0.2		AVDD + 0.2	V
Input Common-Mode Voltage	Full		0.9		V
Input Resistance (Differential)	25°C		15		kΩ
Input Capacitance	25°C		4		pF
LOGIC INPUTS (PDWN, SYNC, SCLK)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		2		pF
LOGIC INPUTS (CSB1, CSB2)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		2		pF
LOGIC INPUT (SDIO)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		5		pF
LOGIC OUTPUT (SDIO)[3]					
Logic 1 Voltage (I_{OH} = 800 µA)	Full		1.79		V
Logic 0 Voltage (I_{OL} = 50 µA)	Full			0.05	V
DIGITAL OUTPUTS (D0±xx, D1±xx), ANSI-644					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	290	345	400	mV
Output Offset Voltage (V_{OS})	Full	1.15	1.25	1.35	V
Output Coding (Default)			Twos complement		
DIGITAL OUTPUTS (D0±xx, D1±xx), LOW POWER, REDUCED SIGNAL OPTION					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	160	200	230	mV
Output Offset Voltage (V_{OS})	Full	1.15	1.25	1.35	V
Output Coding (Default)			Twos complement		

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Specified for LVDS and LVPECL only.
[3] Specified for 13 SDIO/OLM pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, A_{IN} = −1.0 dBFS, unless otherwise noted.

Table 4.

Parameter[1, 2]	Symbol	Temp	Min	Typ	Max	Unit
CLOCK[3]						
Input Clock Rate		Full	10		1000	MHz
Conversion Rate[4]		Full	10		125	MSPS
Clock Pulse Width High	t_{EH}	Full		4.00		ns
Clock Pulse Width Low	t_{EL}	Full		4.00		ns
OUTPUT PARAMETERS[3]						
Propagation Delay	t_{PD}	Full	1.5	2.3	3.1	ns
Rise Time (20% to 80%)	t_R	Full		300		ps
Fall Time (20% to 80%)	t_F	Full		300		ps
FCO±1, FCO±2 Propagation Delay	t_{FCO}	Full	1.5	2.3	3.1	ns
DCO±1, DCO±2 Propagation Delay[5]	t_{CPD}	Full		t_{FCO} + (t_{SAMPLE}/16)		ns
DCO±1, DCO±2 to Data Delay[5]	t_{DATA}	Full	(t_{SAMPLE}/16) − 300	(t_{SAMPLE}/16)	(t_{SAMPLE}/16) + 300	ps
DCO±1, DCO±2 to FCO±1, FCO±2 Delay[5]	t_{FRAME}	Full	(t_{SAMPLE}/16) − 300	(t_{SAMPLE}/16)	(t_{SAMPLE}/16) + 300	ps
Lane Delay	t_{LD}			90		ps
Data to Data Skew	$t_{DATA-MAX} - t_{DATA-MIN}$	Full		±50	±200	ps
Wake-Up Time (Standby)		25°C		250		ns
Wake-Up Time (Power-Down)[6]		25°C		375		µs
Pipeline Latency		Full		16		Clock cycles
APERTURE						
Aperture Delay	t_A	25°C		1		ns
Aperture Uncertainty (Jitter)	t_J	25°C		135		fs rms
Out-of-Range Recovery Time		25°C		1		Clock cycles

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Measured on standard FR-4 material.
[3] Adjustable using the SPI. The conversion rate is the clock rate after the divider.
[4] The maximum conversion rate is based on two-lane output mode. See the Digital Outputs and Timing section for the maximum conversion rate in one-lane output mode.
[5] t_{SAMPLE}/16 is based on the number of bits in two LVDS data lanes. $t_{SAMPLE} = 1/f_{SAMPLE}$.
[6] Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Description	Limit	Unit
SYNC TIMING REQUIREMENTS			
t_{SSYNC}	SYNC to rising edge of CLK+ setup time	1.2	ns min
t_{HSYNC}	SYNC to rising edge of CLK+ hold time	−0.2	ns min
SPI TIMING REQUIREMENTS	See Figure 53		
t_{DS}	Setup time between the data and the rising edge of SCLK	2	ns min
t_{DH}	Hold time between the data and the rising edge of SCLK	2	ns min
t_{CLK}	Period of the SCLK	40	ns min
t_S	Setup time between CSB1/CSB2 and SCLK	2	ns min
t_H	Hold time between CSB1/CSB2 and SCLK	2	ns min
t_{HIGH}	SCLK pulse width high	10	ns min
t_{LOW}	SCLK pulse width low	10	ns min
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 53)	10	ns min
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 53)	10	ns min

Timing Diagrams

Refer to the Memory Map Register Descriptions section and Table 21 for SPI register setting of output modes.

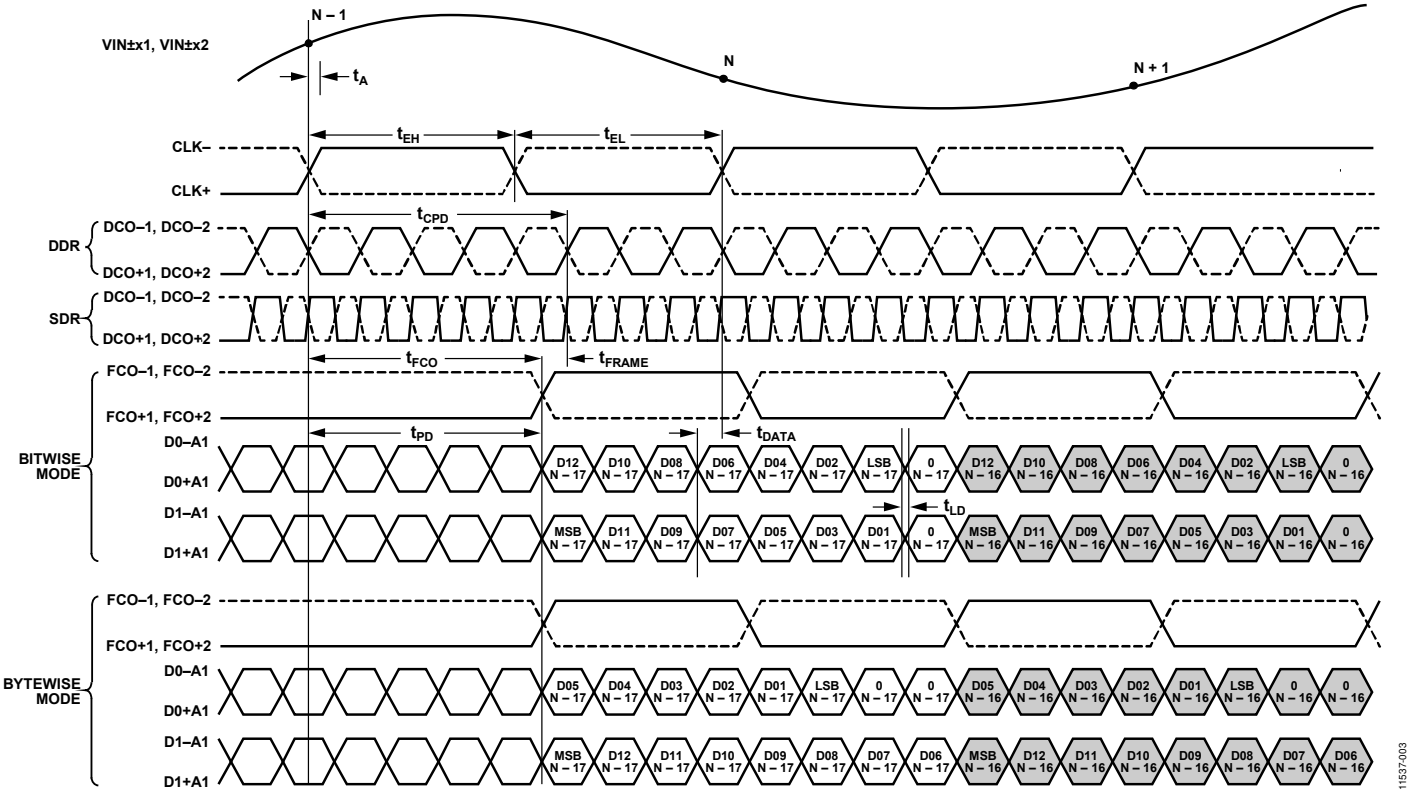

Figure 3. 16-Bit DDR/SDR, Two-Lane, 1× Frame Mode (Default)

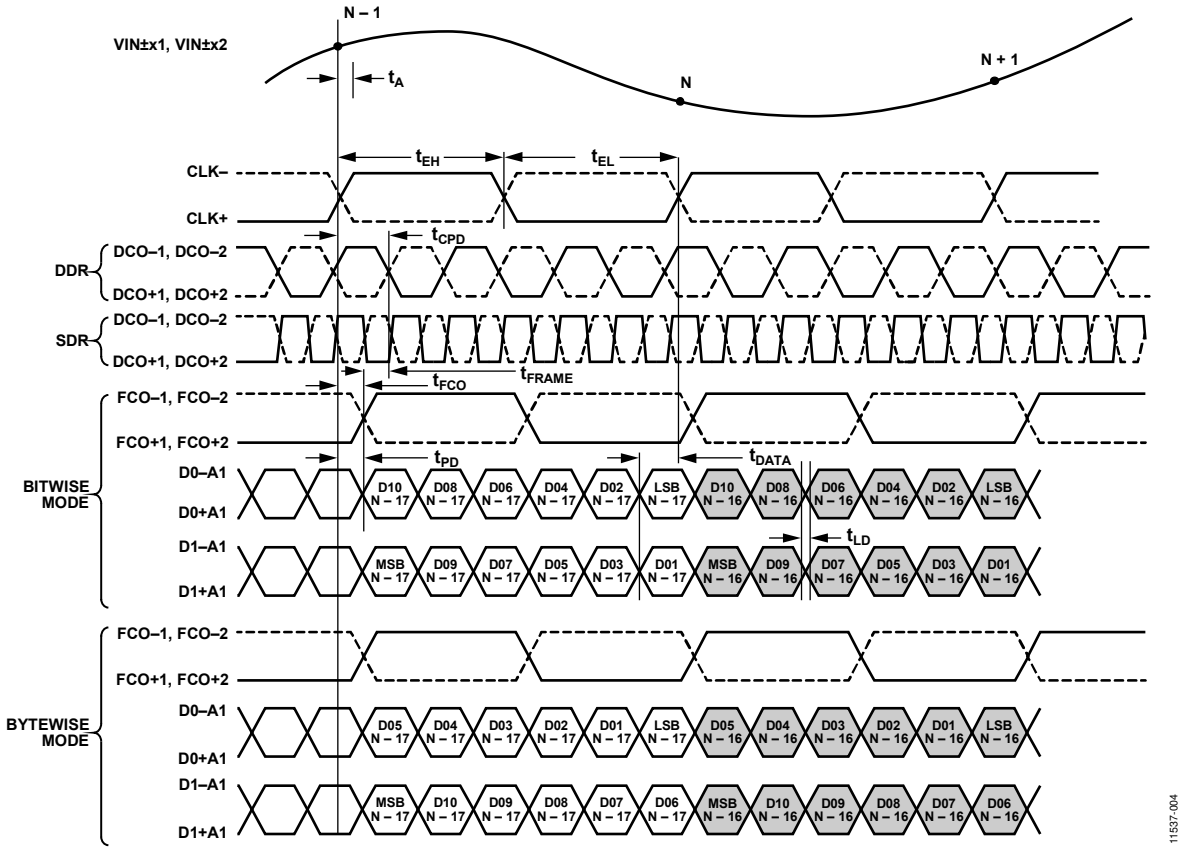

Figure 4. 12-Bit DDR/SDR, Two-Lane, 1× Frame Mode

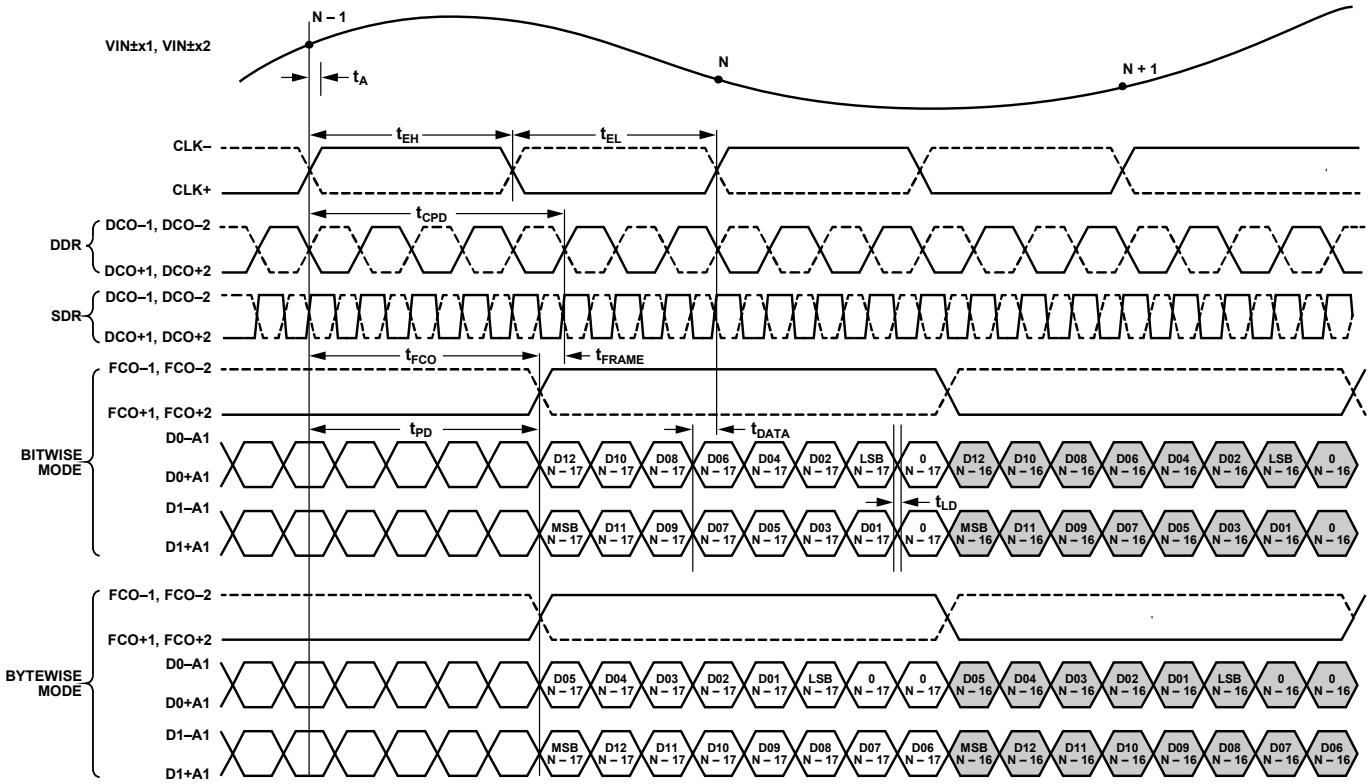

Figure 5. 16-Bit DDR/SDR, Two-Lane, 2× Frame Mode

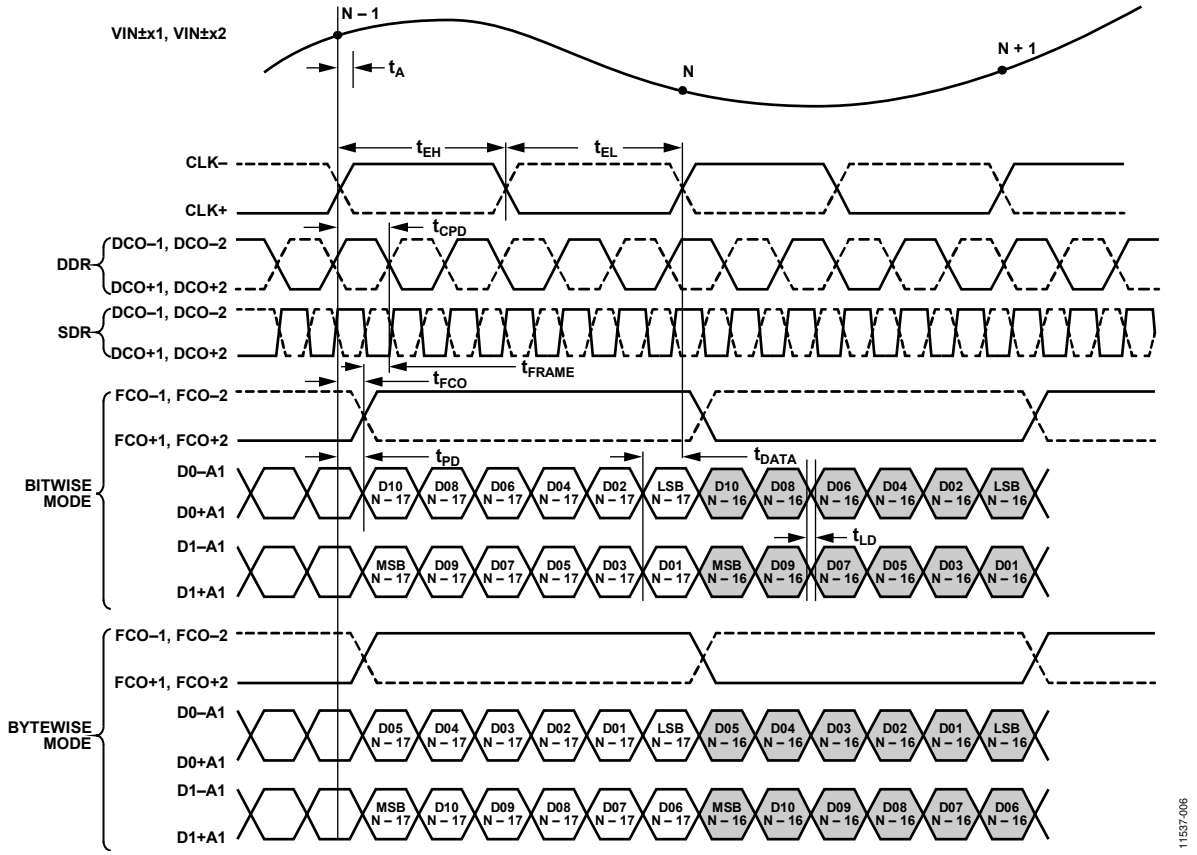

Figure 6. 12-Bit DDR/SDR, Two-Lane, 2× Frame Mode

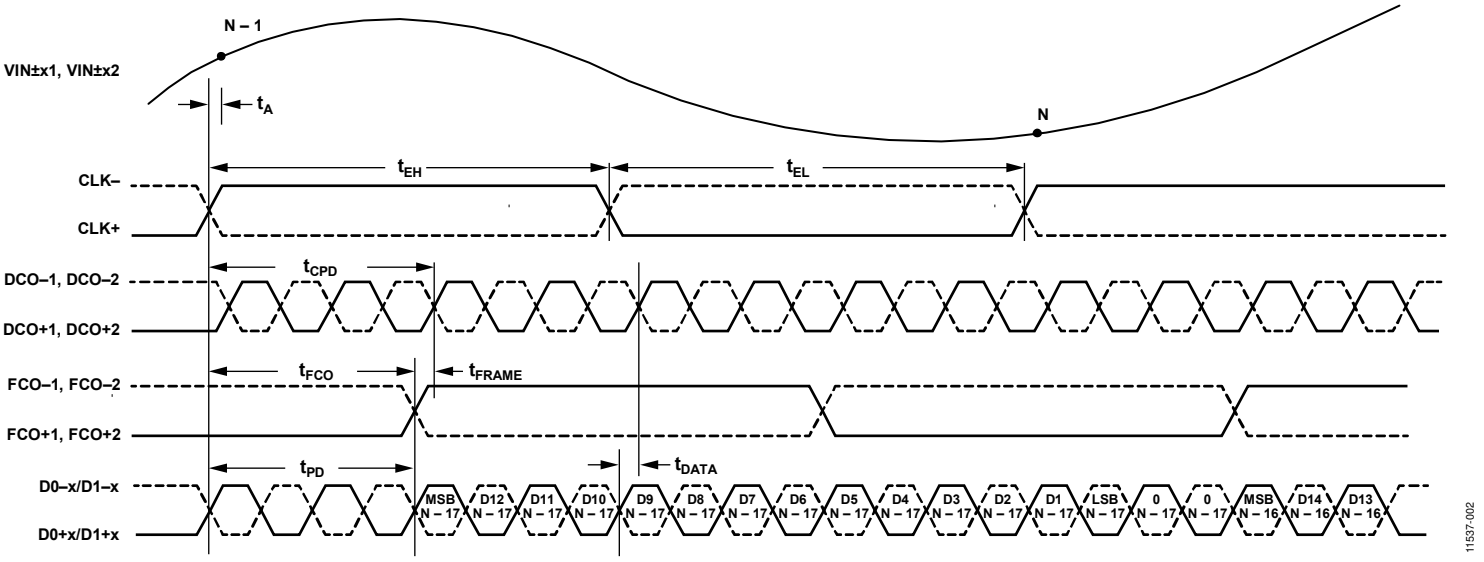

Figure 7. Wordwise DDR, One-Lane, 1× Frame, 16-Bit Output Mode (See Table 8 for One-Lane Channel Assignments)

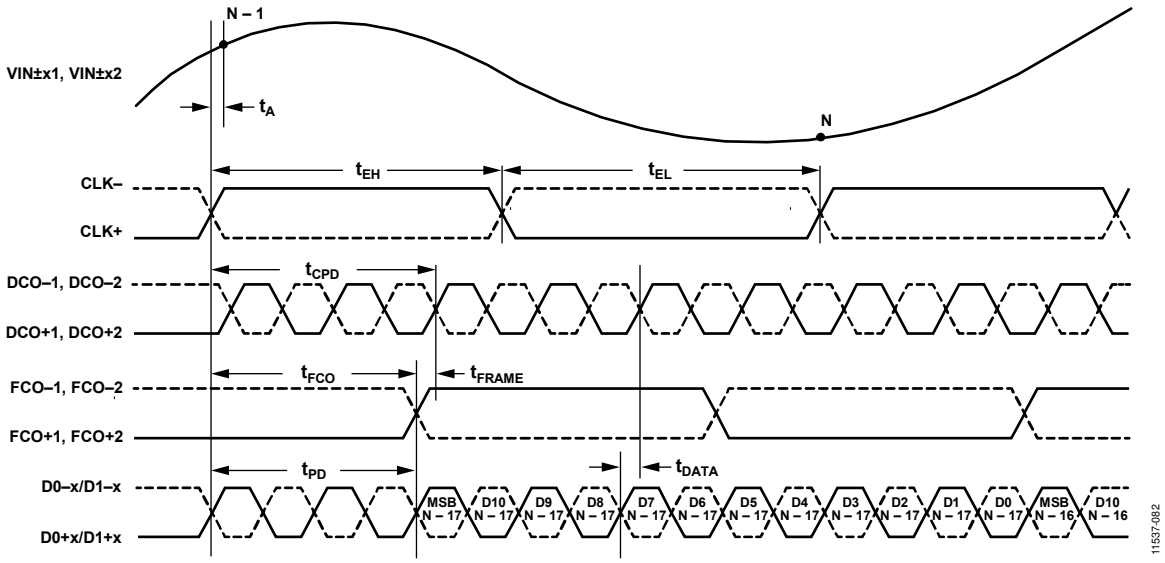

Figure 8. Wordwise DDR, One-Lane, 1× Frame, 12-Bit Output Mode (See Table 8 for One-Lane Channel Assignments)

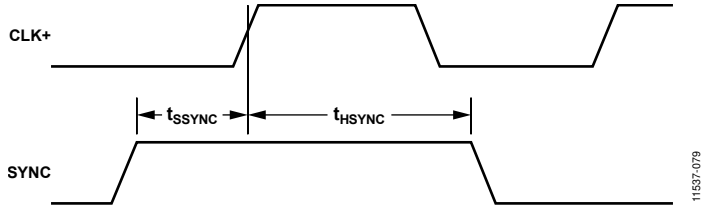

Figure 9. SYNC Input Timing Requirements

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD to GND	−0.3 V to +2.0 V
DRVDD to GND	−0.3 V to +2.0 V
Digital Outputs (D0±xx, D1±xx, DCO±1, DCO±2, FCO±1, FCO±2) to GND	−0.3 V to +2.0 V
CLK+, CLK− to GND	−0.3 V to +2.0 V
VIN±x1, VIN±x2 to GND	−0.3 V to +2.0 V
SCLK/DTP, SDIO/OLM, CSB1, CSB2 to GND	−0.3 V to +2.0 V
SYNC, PDWN to GND	−0.3 V to +2.0 V
RBIAS1, RBIAS2 to GND	−0.3 V to +2.0 V
VREF, VCM1, VCM2, SENSE to GND	−0.3 V to +2.0 V
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. Airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces θ_{JA}.

Table 7. Thermal Resistance (Simulated)

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	Ψ_{JT}[1, 2]	Unit
144-Ball, 10 mm × 10 mm CSP-BGA	0	30.2	0.13	°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

AD9681
TOP VIEW
(Not to Scale)

	1	2	3	4	5	6	7	8	9	10	11	12
A	VIN–D1	VIN+D1	NC	VIN–C2	NC	VIN–C1	NC	NC	VIN–B2	NC	VIN+B1	VIN–B1
B	NC	NC	NC	VIN+C2	NC	VIN+C1	NC	NC	VIN+B2	NC	NC	NC
C	VIN–D2	VIN+D2	SYNC	VCM1	VCM2	VREF	SENSE	RBIAS1	RBIAS2	GND	VIN+A2	VIN–A2
D	GND	GND	GND	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	GND	NC	NC
E	CLK–	CLK+	GND	AVDD	GND	GND	GND	GND	AVDD	CSB1	VIN+A1	VIN–A1
F	GND	GND	GND	AVDD	GND	GND	GND	GND	AVDD	CSB2	SDIO/OLM	SCLK/DTP
G	D1–D2	D1+D2	GND	AVDD	GND	GND	GND	GND	AVDD	PDWN	D0+A1	D0–A1
H	D0–D2	D0+D2	GND	AVDD	GND	GND	GND	GND	AVDD	GND	D1+A1	D1–A1
J	D1–D1	D1+D1	GND	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	GND	D0+A2	D0–A2
K	D0–D1	D0+D1	DRVDD	DRVDD	GND	GND	GND	GND	DRVDD	DRVDD	D1+A2	D1–A2
L	D1–C2	D1+C2	D1+C1	D0+C1	FCO+1	DCO+1	DCO+2	FCO+2	D1+B2	D0+B2	D0+B1	D0–B1
M	D0–C2	D0+C2	D1–C1	D0–C1	FCO–1	DCO–1	DCO–2	FCO–2	D1–B2	D0–B2	D1+B1	D1–B1

NOTES
1. NC = NO CONNECT. THESE PINS ARE NOT ELECTRICALLY CONNECTED TO THE DEVICE. HOWEVER, CONNECT THESE PINS TO BOARD GROUND WHERE POSSIBLE.

11537-009

Figure 10. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
A3, A5, A7, A8, A10, B1 to B3, B5, B7, B8, B10 to B12, D11, D12	NC	No Connect. These pins are not electrically connected to the device. However, connect these pins to board ground where possible.
C10, D1 to D3, D10, E3, E5 to E8, F1 to F3, F5 to F8, G3, G5 to G8, H3, H5 to H8, H10, J3, J10, K5 to K8	GND	Ground.
D4 to D9, E4, E9, F4, F9, G4, G9, H4, H9, J4 to J9	AVDD	1.8 V Analog Supply.
K3, K4, K9, K10	DRVDD	1.8 V Digital Output Driver Supply.
E1, E2	CLK–, CLK+	Input Clock Complement, Input Clock True.
G12, G11	D0−A1, D0+A1	Channel A Lane 0 Bank 1 Digital Output Complement, Lane 0 Bank 1 Digital Output True (Default Two-Lane Mode) or Disabled (One-Lane Mode).
H12, H11	D1−A1, D1+A1	Channel A Lane 1 Bank 1 Digital Output Complement, Lane 1 Bank 1 Digital Output True (Default Two-Lane Mode) or Disabled (One-Lane Mode).

Pin No.	Mnemonic	Description
J12, J11	D0−A2, D0+A2	Channel A Lane 0 Bank 2 Digital Output Complement, Lane 0 Bank 2 Digital Output True (Default Two-Lane Mode) or Disabled (One-Lane Mode).
K12, K11	D1−A2, D1+A2	Channel A Lane 1 Bank 2 Digital Output Complement, Lane 1 Bank 2 Digital Output True (Default Two-Lane Mode) or Disabled (One-Lane Mode).
L12, L11	D0−B1, D0+B1	Channel B Lane 0 Bank 1 Digital Output Complement, Lane 0 Bank 1 Digital Output True (Default Two-Lane Mode) or Channel A Bank 1 Digital Output Complement, Digital Output True (One-Lane Mode).
M12, M11	D1−B1, D1+B1	Channel B Lane 1 Bank 1 Digital Output Complement, Lane 1 Bank 1 Digital Output True (Default Two-Lane Mode) or Channel B Bank 1 Digital Output Complement, Digital Output True (One-Lane Mode).
M10, L10	D0−B2, D0+B2	Channel B Lane 0 Bank 2 Digital Output Complement, Lane 0 Bank 2 Digital Output True (Default Two-Lane Mode). Channel A Bank 2 Digital Output Complement, Digital Output True (One-Lane Mode).
M9, L9	D1−B2, D1+B2	Channel B Lane 1 Bank 2 Digital Output Complement, Lane 1 Bank 2 Digital Output True (Default Two-Lane Mode) or Channel B Bank 2 Digital Output Complement, Digital Output True (One-Lane Mode).
M4, L4	D0−C1, D0+C1	Channel C Lane 0 Bank 1 Digital Output Complement, Lane 0 Bank 1 Digital Output True (Default Two-Lane Mode) or Channel C Bank 1 Digital Output Complement, Digital Output True (One-Lane Mode).
M3, L3	D1−C1, D1+C1	Channel C Lane 1 Bank 1 Digital Output Complement, Lane 1 Bank 1 Digital Output True (Default Two-Lane Mode) or Channel D Bank 1 Digital Output Complement, Digital Output True (One-Lane Mode).
M1, M2	D0−C2, D0+C2	Channel C Lane 0 Bank 2 Digital Output Complement, Lane 0 Bank 2 Digital Output True (Default Two-Lane Mode) or Channel C Bank 2 Digital Output Complement, Digital Output True (One-Lane Mode).
L1, L2	D1−C2, D1+C2	Channel C Lane 1 Bank 2 Digital Output Complement, Lane 1 Bank 2 Digital Output True (Default Two-Lane Mode) or Channel D Bank 2 Digital Output Complement, Digital Output True (One-Lane Mode).
K1, K2	D0−D1, D0+D1	Channel D Lane 0 Bank 1 Digital Output Complement, Lane 0 Bank 1 Digital Output True (Default Two-Lane Mode) or Disabled (One-Lane Mode).
J1, J2	D1−D1, D1+D1	Channel D Lane 1 Bank 1 Digital Output Complement, Lane 1 Bank 1 Digital Output True (Default Two-Lane Mode) or Disabled (One-Lane Mode).
H1, H2	D0−D2, D0+D2	Channel D Lane 0 Bank 2 Digital Output Complement, Lane 0 Bank 2 Digital Output True (Default Two-Lane Mode) or Disabled (One-Lane Mode).
G1, G2	D1−D2, D1+D2	Channel D Lane 1 Bank 2 Digital Output Complement, Lane 1 Bank 2 Digital Output True (Default Two-Lane Mode) or Disabled (One-Lane Mode).
M6, L6; M7, L7	DCO−1, DCO+1; DCO−2, DCO+2	Data Clock Digital Output Complement, Data Clock Digital Output True. DCO±1 is used to capture D0±x1/D1±x1 digital output data, and DCO±2 is used to capture D0±x2/D1±x2 digital output data.
M5, L5; M8, L8	FCO−1, FCO+1; FCO−2, FCO+2	Frame Clock Digital Output Complement, Frame Clock Digital Output True. FCO±1 frames D0±x1/D1±x1 digital output data, and FCO±2 frames D0±x2/D1±x2 digital output data.
F12	SCLK/DTP	Serial Clock/Digital Test Pattern.
F11	SDIO/OLM	Serial Data Input/Output/Output Lane Mode.
E10, F10	CSB1, CSB2	Chip Select Bar. CSB1 enables/disables the SPI for four channels in Bank 1; CSB2 enables/ disables the SPI for four channels in Bank 2.
G10	PDWN	Power-Down.
E12, E11	VIN−A1, VIN+A1	Analog Input Complement, Analog Input True.
C12, C11	VIN−A2, VIN+A2	Analog Input Complement, Analog Input True.
A12, A11	VIN−B1, VIN+B1	Analog Input Complement, Analog Input True.
A9, B9	VIN−B2, VIN+B2	Analog Input Complement, Analog Input True.
A6, B6	VIN−C1, VIN+C1	Analog Input Complement, Analog Input True.

Pin No.	Mnemonic	Description
A4, B4	VIN−C2, VIN+C2	Analog Input Complement, Analog Input True.
A1, A2	VIN−D1, VIN+D1	Analog Input Complement, Analog Input True.
C1, C2	VIN−D2, VIN+D2	Analog Input Complement, Analog Input True.
C8, C9	RBIAS1, RBIAS2	Sets analog current bias. Connect each RBIASx pin to a 10 kΩ (1% tolerance) resistor to ground.
C7	SENSE	Reference Mode Selection.
C6	VREF	Voltage Reference Input/Output.
C4, C5	VCM1, VCM2	Analog Output Voltage at Midsupply. Sets the common mode of the analog inputs, external to the ADC, as shown in Figure 38 and Figure 39.
C3	SYNC	Digital Input; Synchronizing Input to Clock Divider. This pin is internally pulled to ground by a 30 kΩ resistor.

TYPICAL PERFORMANCE CHARACTERISTICS

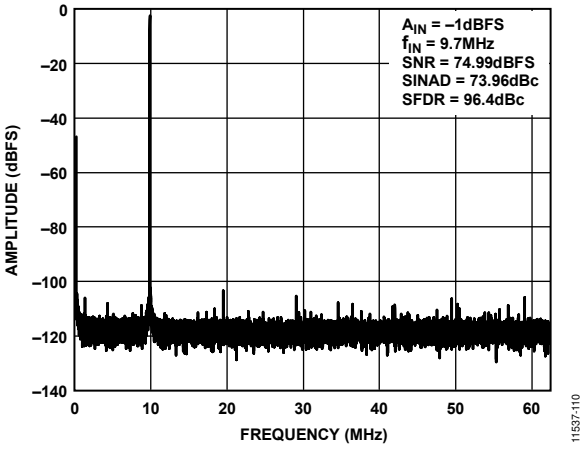

Figure 11. Single-Tone 32k FFT with f_{IN} = 9.7 MHz; f_{SAMPLE} = 125 MSPS

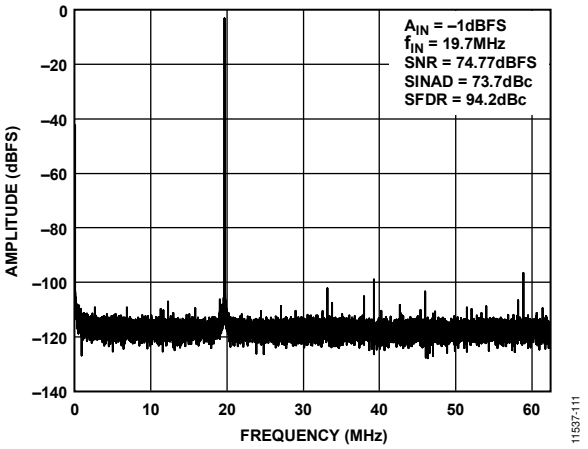

Figure 12. Single-Tone 32k FFT with f_{IN} = 19.7 MHz; f_{SAMPLE} = 125 MSPS

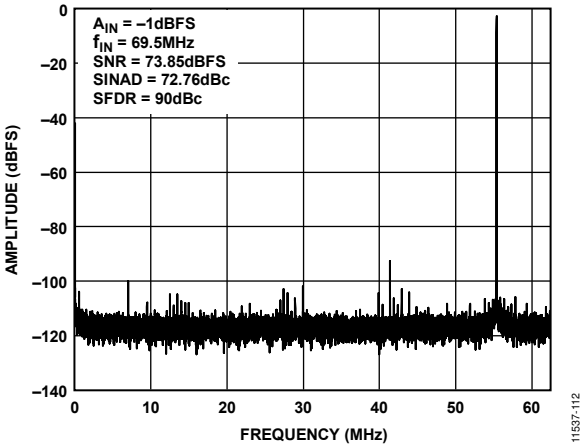

Figure 13. Single-Tone 32k FFT with f_{IN} = 69.5 MHz; f_{SAMPLE} = 125 MSPS

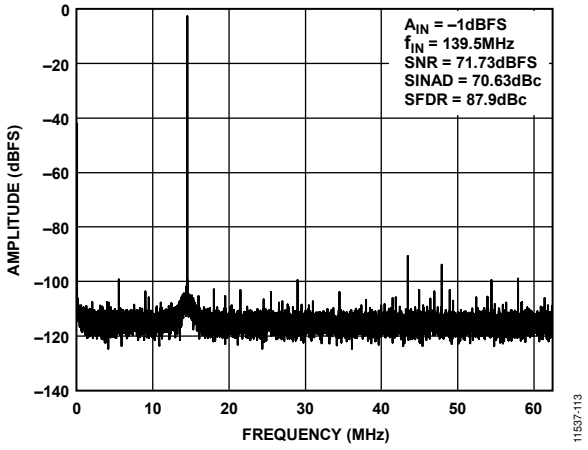

Figure 14. Single-Tone 32k FFT with f_{IN} = 139.5 MHz; f_{SAMPLE} = 125 MSPS

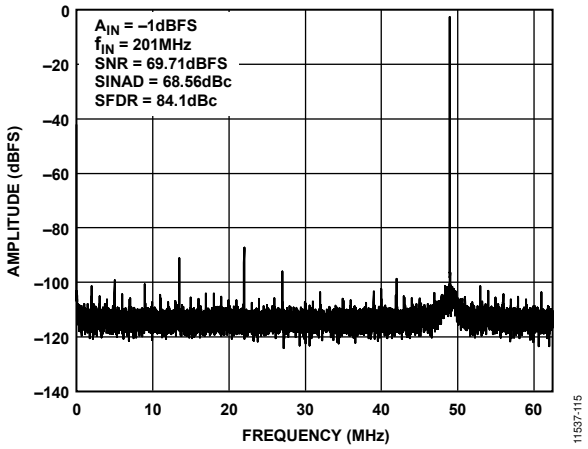

Figure 15. Single-Tone 32k FFT with f_{IN} = 201 MHz; f_{SAMPLE} = 125 MSPS

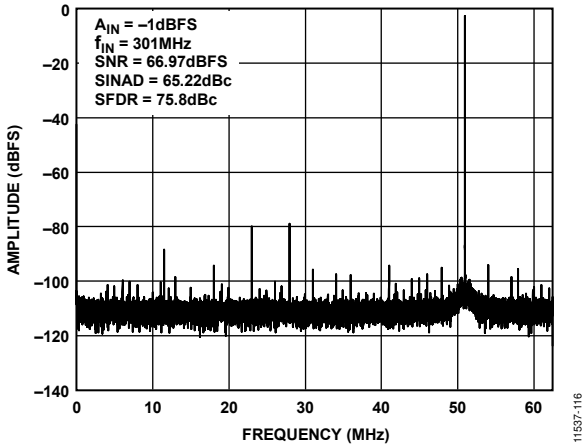

Figure 16. Single-Tone 32k FFT with f_{IN} = 301 MHz; f_{SAMPLE} = 125 MSPS

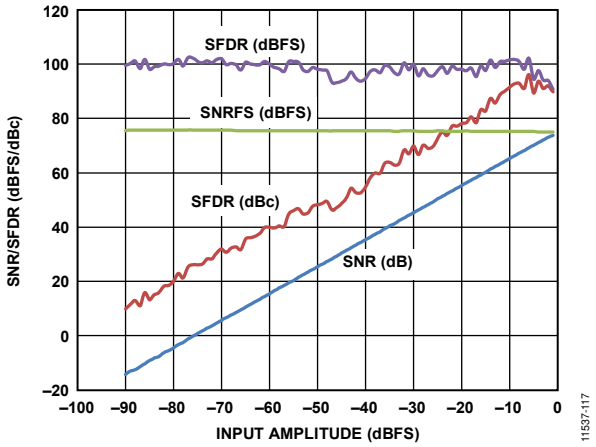

Figure 17. SNR/SFDR vs. Input Amplitude (A_{IN}); f_{IN} = 9.7 MHz; f_{SAMPLE} = 125 MSPS

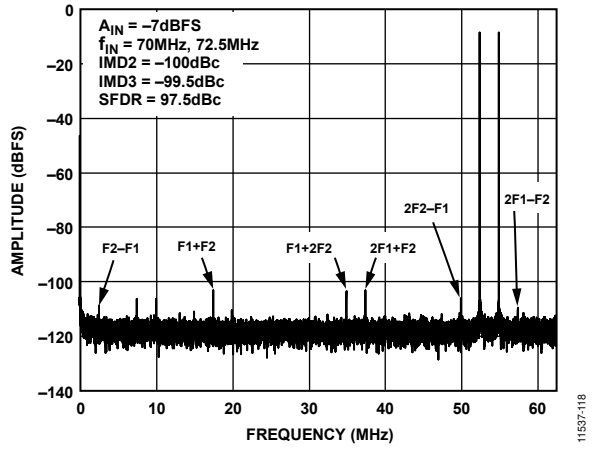

Figure 18. Two-Tone 32k FFT with f_{IN1} = 70.5 MHz and f_{IN2} = 72.5 MHz; f_{SAMPLE} = 125 MSPS

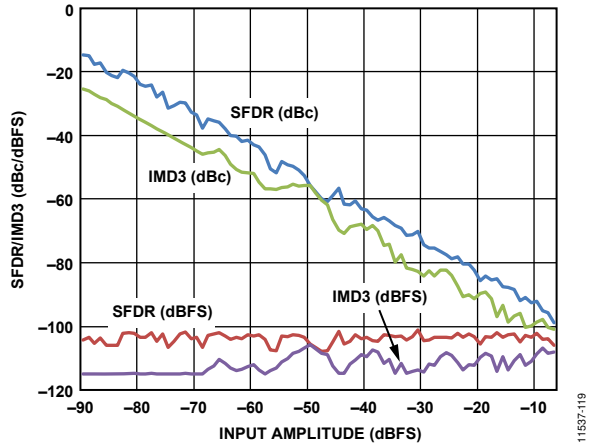

Figure 19. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 70.0 MHz and f_{IN2} = 72.5 MHz; f_{SAMPLE} = 125 MSPS

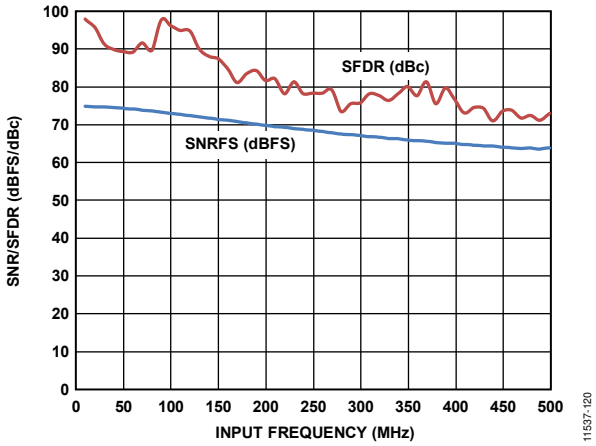

Figure 20. SNR/SFDR vs. f_{IN}; f_{SAMPLE} = 125 MSPS

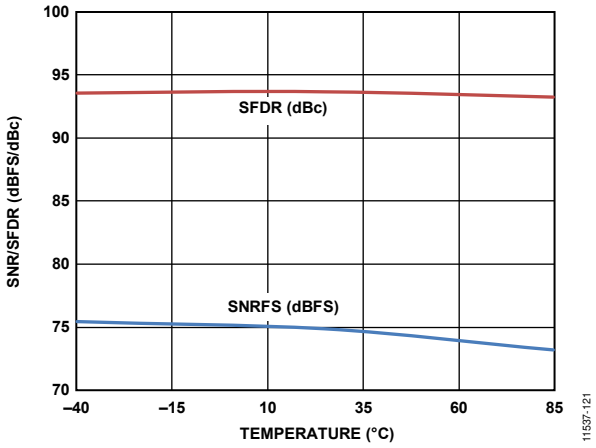

Figure 21. SNR/SFDR vs. Temperature; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS

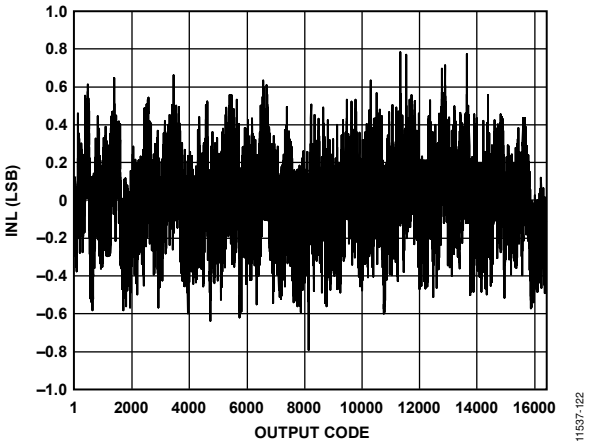

Figure 22. INL; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS

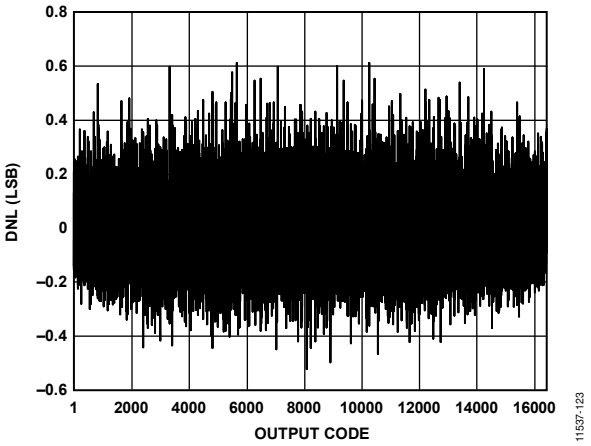

Figure 23. DNL; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS

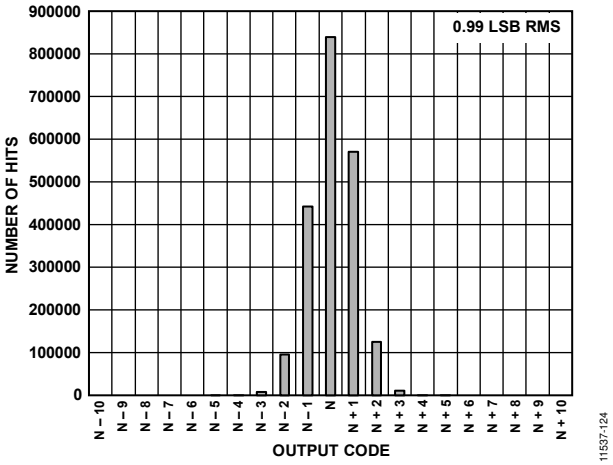

Figure 24. Input Referred Noise Histogram; f_{SAMPLE} = 125 MSPS

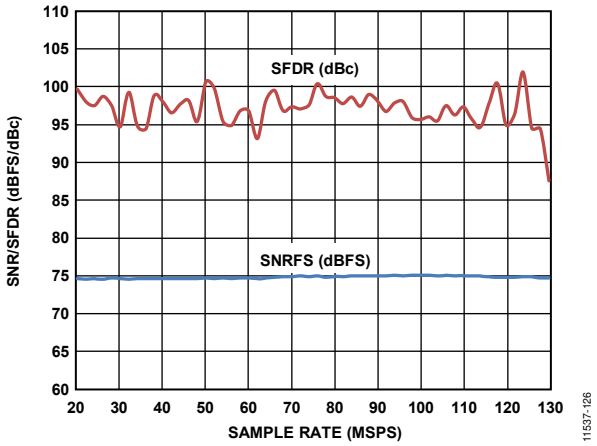

Figure 25. SNR/SFDR vs. Sample Rate; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS

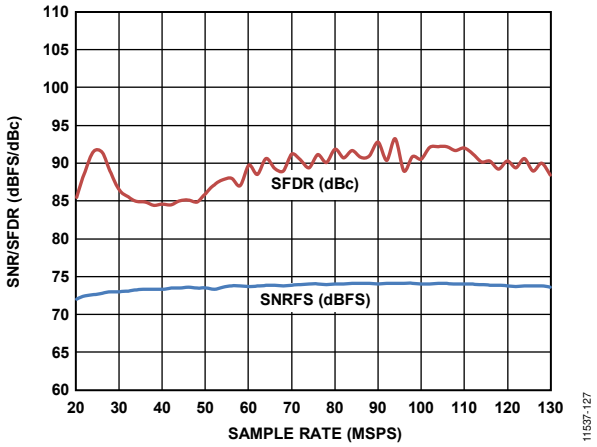

Figure 26. SNR/SFDR vs. Sample Rate; f_{IN} = 70 MHz, f_{SAMPLE} = 125 MSPS

EQUIVALENT CIRCUITS

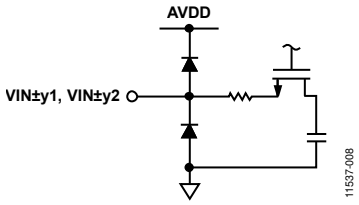

Figure 27. Equivalent Analog Input Circuit

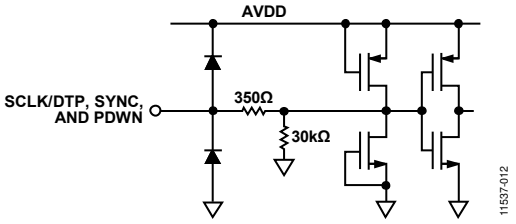

Figure 31. Equivalent SCLK/DTP, SYNC, and PDWN Input Circuit

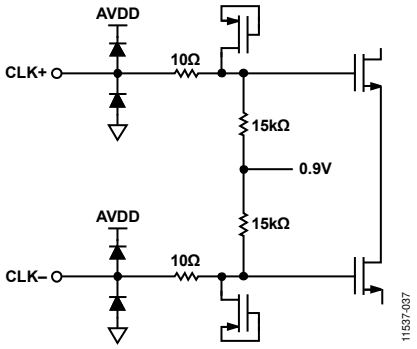

Figure 28. Equivalent Clock Input Circuit

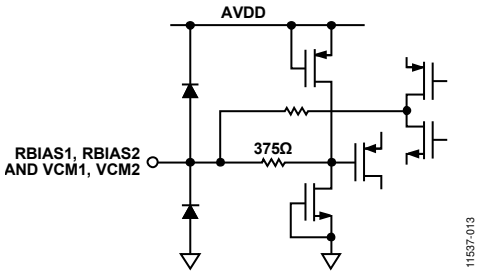

Figure 32. Equivalent RBIASx and VCMx Circuit

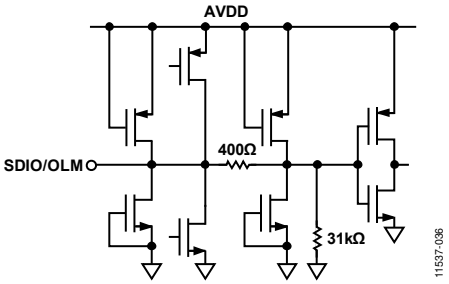

Figure 29. Equivalent SDIO/OLM Input Circuit

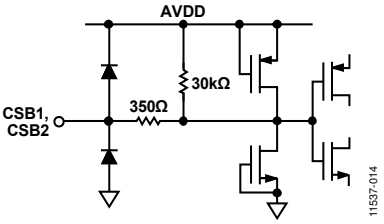

Figure 33. Equivalent CSBx Input Circuit

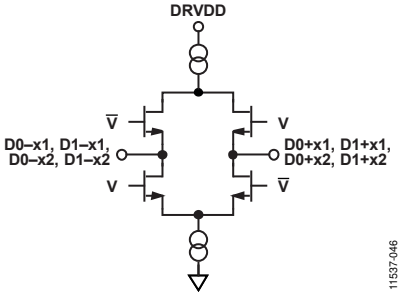

Figure 30. Equivalent Digital Output Circuit

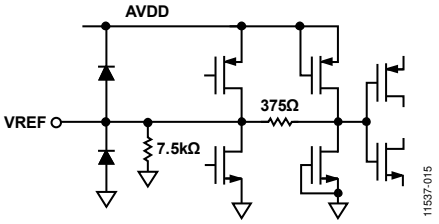

Figure 34. Equivalent VREF Circuit

THEORY OF OPERATION

The AD9681 is a multistage, pipelined ADC. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The serializer transmits this converted data in a 16-bit output. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The data is then serialized and aligned to the frame and data clocks.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9681 is a differential switched capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. By using an input common-mode voltage of midsupply, users can minimize signal dependent errors and achieve optimum performance.

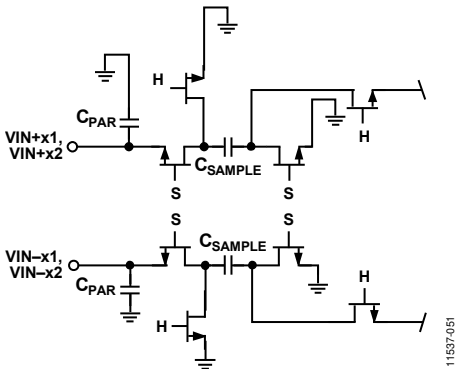

Figure 35. Switched Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample mode and hold mode (see Figure 35). When the input circuit is switched to sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor, in series with each input, can help reduce the peak transient current injected from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and, therefore, achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Place either a differential capacitor or two single-ended capacitors on the inputs to provide a matching passive network. This configuration ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-742 Application Note, *Frequency Domain Response of Switched-Capacitor ADCs*; the AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*; and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005) for more information. In general, the precise values vary, depending on the application.

Input Common Mode

The analog inputs of the AD9681 are not internally dc biased. Therefore, in ac-coupled applications, the user must provide this bias externally. For optimum performance, set the device so that V_{CM} = AVDD/2. However, the device can function over a wider range with reasonable performance, as shown in Figure 36.

An on-chip, common-mode voltage reference is included in the design and is available at the VCMx pin. Decouple the VCMx pin to ground using a 0.1 µF capacitor, as described in the Applications Information section.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9681, the largest available input span is 2 V p-p.

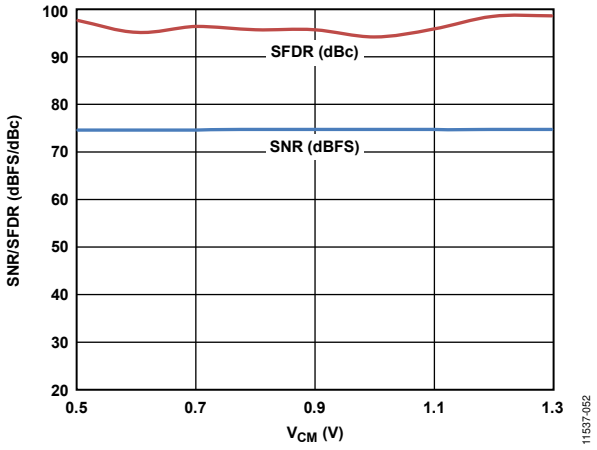

Figure 36. SNR/SFDR vs. Common-Mode Voltage; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS

Differential Input Configurations

There are several ways to drive the AD9681, either actively or passively. However, optimum performance is achieved by driving the analog inputs differentially. Using a differential double balun configuration to drive the AD9681 provides excellent performance and a flexible interface to the ADC (see Figure 38) for baseband applications. Similarly, differential transformer coupling also provides excellent performance (see Figure 39). Because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9681, use of these passive configurations is recommended wherever possible.

Regardless of the configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

It is recommended that the AD9681 inputs not be driven single-ended.

VOLTAGE REFERENCE

A stable and accurate 1.0 V voltage reference is built into the AD9681. Configure VREF using either the internal 1.0 V reference or an externally applied 1.0 V reference voltage. The various reference modes are summarized in the Internal Reference Connection section and the External Reference Operation section. Bypass the VREF pin to ground externally, using a low ESR, 1.0 µF capacitor in parallel with a low ESR, 0.1 µF ceramic capacitor.

Internal Reference Connection

A comparator within the AD9681 detects the potential at the SENSE pin and configures the reference into two possible modes, which are summarized in Table 9. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 37), setting VREF to 1.0 V.

Table 9. Reference Configuration Summary

Selected Mode	SENSE Voltage (V)	Resulting VREF (V)	Resulting Differential Span (V p-p)
Fixed Internal Reference	GND to 0.2	1.0 internal	2.0
Fixed External Reference	AVDD	1.0 applied to external VREF pin	2.0

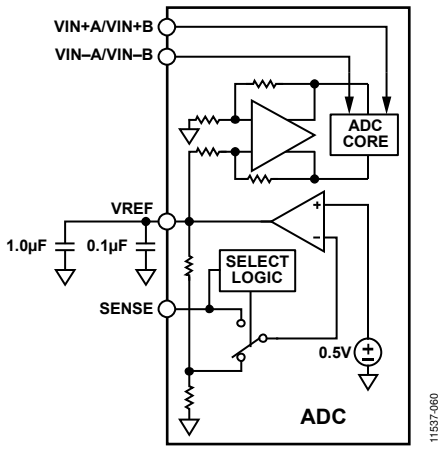

Figure 37. Internal Reference Configuration

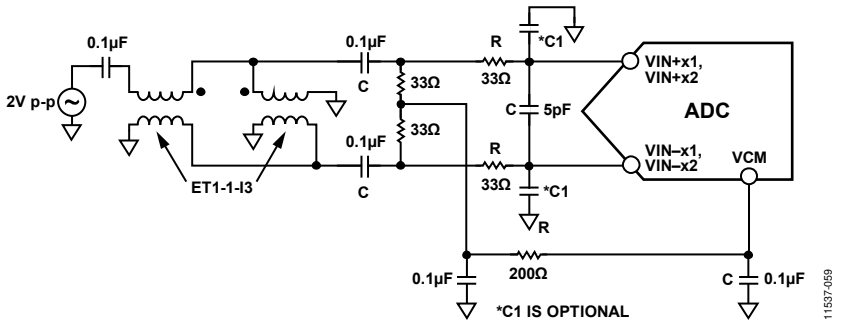

Figure 38. Differential Double Balun Input Configuration for Baseband Applications

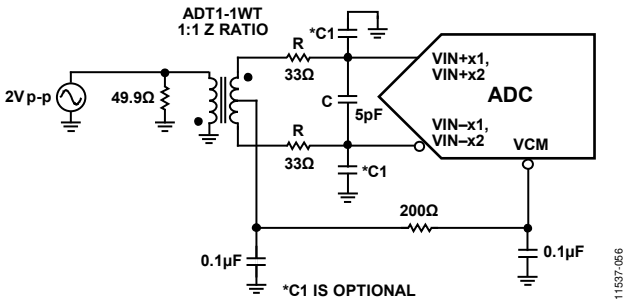

Figure 39. Differential Transformer Coupled Configuration for Baseband Applications

If the internal reference of the AD9681 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 40 shows how the internal reference voltage is affected by loading.

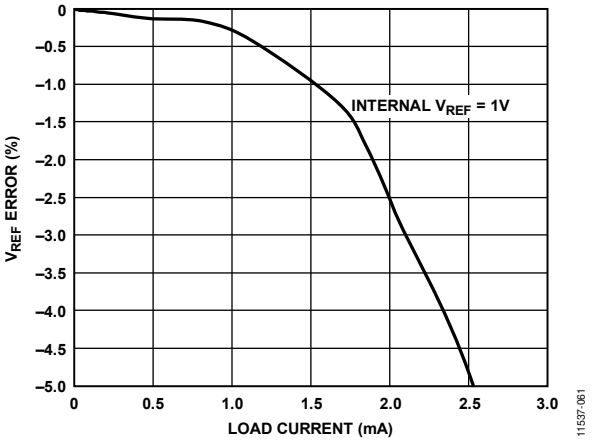

Figure 40. V_{REF} Error vs. Load Current

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 41 shows the typical drift characteristics of the internal reference in 1.0 V mode.

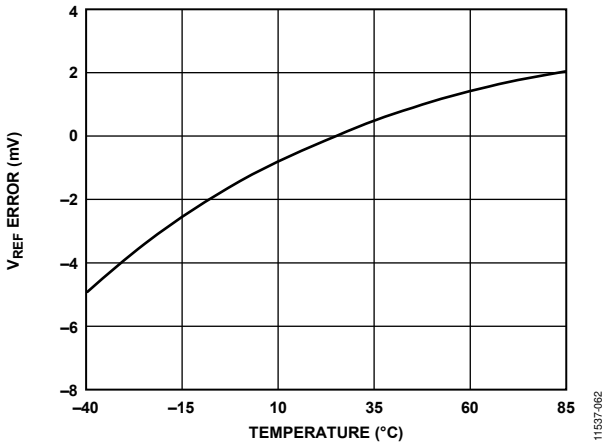

Figure 41. Typical V_{REF} Drift

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7.5 kΩ load (see Figure 34). The internal buffer generates the positive and negative full-scale references for the ADC core. Therefore, limit the external reference to a maximum of 1.0 V.

Do not leave the SENSE pin floating.

CLOCK INPUT CONSIDERATIONS

For optimum performance, clock the AD9681 sample clock inputs, CLK+ and CLK–, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK– pins via a transformer or capacitors. These pins are biased internally (see Figure 28) and require no external bias.

Clock Input Options

The AD9681 has a flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of the utmost concern, as described in the Jitter Considerations section.

Figure 42 and Figure 43 show two preferred methods for clocking the AD9681 (at clock rates of up to 1 GHz prior to the internal clock divider). A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF transformer or an RF balun.

The RF balun configuration is recommended for clock frequencies from 125 MHz to 1 GHz, and the RF transformer is recommended for clock frequencies from 10 MHz to 200 MHz. The antiparallel Schottky diodes across the transformer/balun secondary winding limit clock excursions into the AD9681 to approximately 0.8 V p-p differential.

This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9681 while preserving the fast rise and fall times of the signal that are critical to achieving a low jitter performance. However, the diode capacitance comes into play at frequencies above 500 MHz. Take care when choosing the appropriate signal limiting diode.

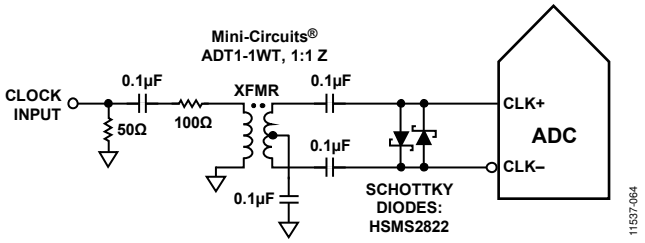

Figure 42. Transformer Coupled Differential Clock (Up to 200 MHz)

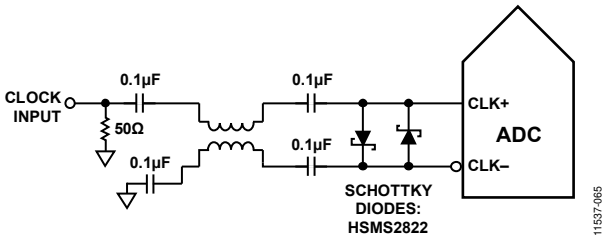

Figure 43. Balun Coupled Differential Clock (Up to 1 GHz)

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 44. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516-4/AD9517-4 clock drivers, noted by AD951x in Figure 44, offer excellent jitter performance.

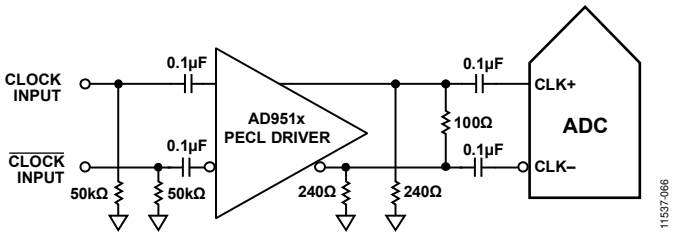

Figure 44. Differential PECL Sample Clock (Up to 1 GHz)

A third option is to ac couple a differential LVDS signal to the sample clock input pins, as shown in Figure 45. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516-4/AD9517-4 clock drivers, noted by AD951x in Figure 45 and Figure 46, offer excellent jitter performance.

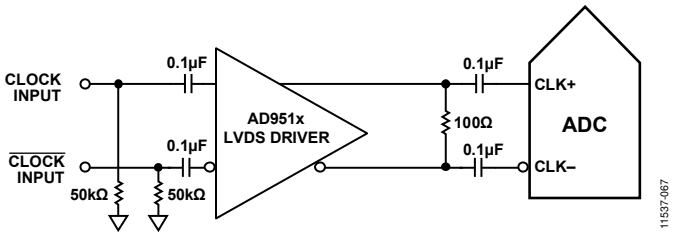

Figure 45. Differential LVDS Sample Clock (Up to 1 GHz)

In some applications, it may be acceptable to drive the sample clock inputs with a single-ended 1.8 V CMOS signal. In such applications, drive the CLK+ pin directly from a CMOS gate, and bypass the CLK− pin to ground with a 0.1 µF capacitor (see Figure 46).

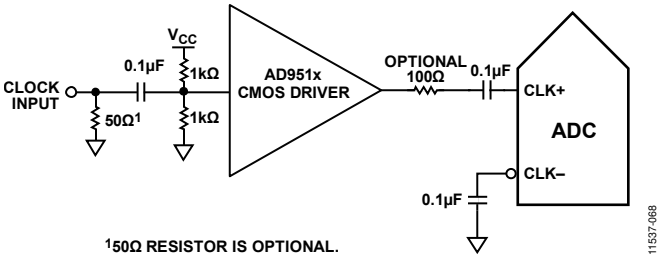

Figure 46. Single-Ended 1.8 V CMOS Input Clock (Up to 200 MHz)

Input Clock Divider

The AD9681 contains an input clock divider with the ability to divide the input clock by integer values from 1 to 8.

The AD9681 clock divider can be synchronized using the external SYNC input. Bit 0 and Bit 1 of Register 0x109 allow the clock divider to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written. A valid SYNC causes the clock divider to reset to its initial state. This synchronization feature allows the clock dividers of multiple devices to be aligned to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9681 contains a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD9681. Noise and distortion performance are nearly flat for a wide range of duty cycles with the DCS turned on.

Jitter on the rising edge of the input is still of concern and is not easily reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates of less than 20 MHz, nominally. The loop has a time constant associated with it that must be considered in applications in which the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) that is due only to aperture jitter (t_J) is expressed by

$$SNR\ Degradation = 20 \log_{10}\left(\frac{1}{2\pi \times f_A \times t_J}\right)$$

In this equation, the rms aperture jitter represents the root sum square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 47).

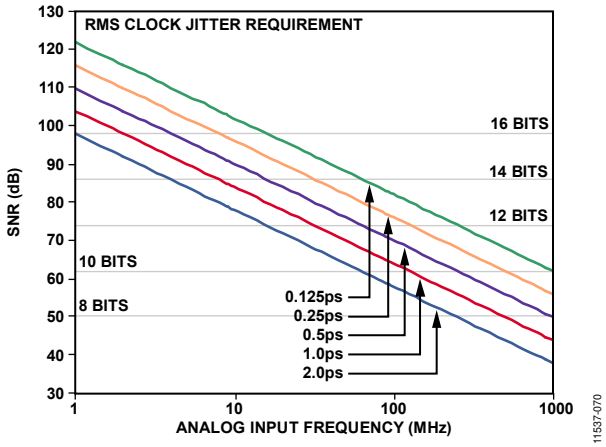

Figure 47. Ideal SNR vs. Input Frequency and Jitter

Treat the clock input as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9681. Separate the clock driver power supplies from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal controlled oscillators are excellent clock sources. If another type of source generates the clock (by gating, dividing, or another method), ensure that it is retimed by the original clock at the last step.

See the AN-501 Application Note, *Aperture Uncertainty and ADC System Performance*, and the AN-756 Application Note, *Sampled Systems and the Effects of Clock Phase Noise and Jitter*, for more in depth information about jitter performance as it relates to ADCs.

POWER DISSIPATION AND POWER-DOWN MODE

As shown in Figure 48, the power dissipated by the AD9681 is proportional to its sample rate and can be set to one of several power saving modes using Register 0x100, Bits[2:0].

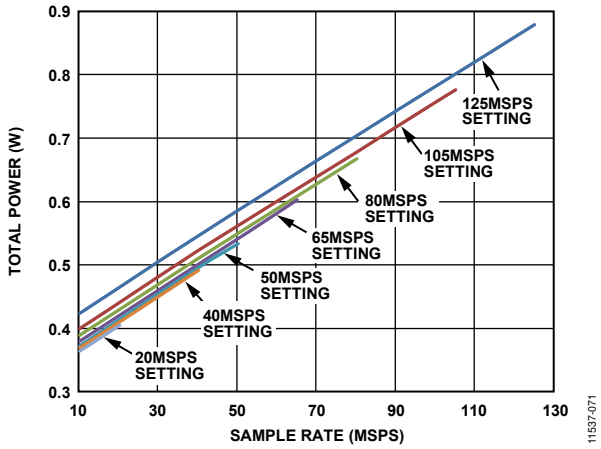

Figure 48. Total Power vs. f_{SAMPLE} for f_{IN} = 9.7 MHz

The AD9681 is placed in power-down mode either by the SPI port or by asserting the PDWN pin high. In this state, the ADC typically dissipates 2 mW. During power-down, the output drivers are placed in a high impedance state. Asserting the PDWN pin low returns the AD9681 to its normal operating mode. Note that PDWN is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. The internal capacitors are discharged when the device enters power-down mode and then must be recharged when returning to normal operation. As a result, wake-up time is related to the time spent in power-down mode, and shorter power-down cycles result in proportionally shorter wake-up times. When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the Memory Map section for more details on using these features.