Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

14-Bit, 500 MSPS LVDS, Dual Analog-to-Digital Converter

Data Sheet **AD9684**

FEATURES

- Parallel LVDS (DDR) outputs
- 1.1 W total power per channel at 500 MSPS (default settings)
- SFDR = 85 dBFS at 170 MHz f_{IN} (500 MSPS)
- SNR = 68.6 dBFS at 170 MHz f_{IN} (500 MSPS)
- ENOB = 10.9 bits at 170 MHz f_{IN}
- DNL = ±0.5 LSB
- INL = ±2.5 LSB
- Noise density = −153 dBFS/Hz at 500 MSPS
- 1.25 V, 2.50 V, and 3.3 V supply operation
- No missing codes
- Internal analog-to-digital converter (ADC) voltage reference
- Flexible input range and termination impedance
  - 1.46 V p-p to 2.06 V p-p (2.06 V p-p nominal)
  - 400 Ω, 200 Ω, 100 Ω, and 50 Ω differential
- SYNC± input allows multichip synchronization
- DDR LVDS (ANSI-644 levels) outputs
- 2 GHz usable analog input full power bandwidth
- >96 dB channel isolation/crosstalk
- Amplitude detect bits for efficient AGC implementation
- Two integrated wideband digital processors per channel
  - 12-bit numerically controlled oscillator (NCO)
  - 3 cascaded half-band filters
- Differential clock inputs
  - Serial port control
  - Integer clock divide by 2, 4, or 8
- Small signal dither

APPLICATIONS

- Communications
- Diversity multiband, multimode digital receivers
  - 3G/4G, TD-SCDMA, W-CDMA, MC-GSM, LTE
- General-purpose software radios
- Ultrawideband satellite receiver
- Instrumentation (spectrum analyzers, network analyzers, integrated RF test solutions)
- Radar
- Digital oscilloscopes
- High speed data acquisition systems
- DOCSIS CMTS upstream receiver paths
- HFC digital reverse path receivers

FUNCTIONAL BLOCK DIAGRAM

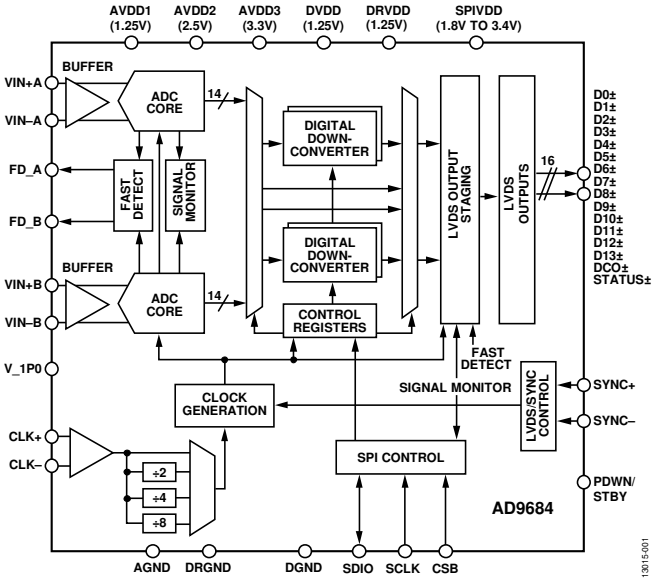


Figure 1.

GENERAL DESCRIPTION

The AD9684 is a dual, 14-bit, 500 MSPS ADC. The device has an on-chip buffer and a sample-and-hold circuit designed for low power, small size, and ease of use. This product is designed for sampling wide bandwidth analog signals. The AD9684 is optimized for wide input bandwidth, a high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth buffered inputs, supporting a variety of user selectable input ranges. An integrated voltage reference eases design considerations. Each ADC data output is internally connected to an optional decimate by 2 block.

The analog input and clock signals are differential inputs. Each ADC data output is internally connected to two digital downconverters (DDCs). Each DDC consists of four cascaded signal processing stages: a 12-bit frequency translator (NCO), and three half-band decimation filters supporting a divide by factor of two, four, and eight.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

5/15—Revision 0: Initial Version

The AD9684 has several functions that simplify the automatic gain control (AGC) function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly reduce the system gain to avoid an overrange condition at the ADC input. In addition to the fast detect outputs, the AD9684 also offers signal monitoring capability. The signal monitoring block provides additional information about the signal that the ADC digitized.

The dual ADC output data is routed directly to the one external, 14-bit LVDS output port, supporting double data rate (DDR) formatting. An external data clock and status bit are offered for data capture flexibility.

The LVDS outputs have several configurations, depending on the acceptable rate of the receiving logic device and the sampling rate of the ADC. Multiple device synchronization is supported through the SYNC± input pins.

The AD9684 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using a 1.8 V to 3.4 V capable 3-wire serial port interface (SPI).

The AD9684 is available in a Pb-free, 196-ball ball grid array (BGA) and is specified over the −40°C to +85°C industrial temperature range. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Wide full power bandwidth supports intermediate frequency (IF) sampling of signals up to 2 GHz.
2. Buffered inputs with programmable input termination ease filter design and implementation.
3. Four integrated wideband decimation filters and NCO blocks supporting multiband receivers.
4. Flexible SPI controls various product features and functions to meet specific system requirements.
5. Programmable fast overrange detection and signal monitoring.
6. SYNC± input allows synchronization of multiple devices.
7. 12 mm × 12 mm, 196-ball BGA_ED.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate (500 MSPS), 1.7 V p-p full-scale differential input, 1.0 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Temperature	Min	Typ	Max	Unit
RESOLUTION	Full	14			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	−0.3	0	+0.3	% FSR
Offset Matching	Full		0	+0.3	% FSR
Gain Error	Full	−6.5	0	+6.5	% FSR
Gain Matching	Full		0	+5.0	% FSR
Differential Nonlinearity (DNL)	Full	−0.6	±0.5	+0.7	LSB
Integral Nonlinearity (INL)	Full	−4.5	±2.5	+5.0	LSB
TEMPERATURE DRIFT					
Offset Error	25°C		±3		ppm/°C
Gain Error	25°C		−39		ppm/°C
INTERNAL VOLTAGE REFERENCE	Full		1.0		V
INPUT-REFERRED NOISE					
V_{REF} = 1.0 V	25°C		2.63		LSB rms
ANALOG INPUTS					
Differential Input Voltage Range (Programmable)	Full	1.46	2.06	2.06	V p-p
Common-Mode Voltage (V_{CM})	25°C		2.05		V
Differential Input Capacitance[1]	25°C		1.5		pF
Analog Input Full Power Bandwidth	25°C		2		GHz
POWER SUPPLY					
AVDD1	Full	1.22	1.25	1.28	V
AVDD2	Full	2.44	2.50	2.56	V
AVDD3	Full	3.2	3.3	3.4	V
DVDD	Full	1.22	1.25	1.28	V
DRVDD	Full	1.22	1.25	1.28	V
SPIVDD	Full	1.22	1.8	3.4	V
I_{AVDD1}	Full		448	503	mA
I_{AVDD2}	Full		396	455	mA
I_{AVDD3}	Full		103	124	mA
I_{DVDD}	Full		108	127	mA
I_{DRVDD}	Full		106	119	mA
I_{SPIVDD}	Full		2	6	mA
POWER CONSUMPTION					
Total Power Dissipation[2]	Full		2.2		W
Power-Down Dissipation	Full		710		mW
Standby	Full		1.0		W

[1] Differential capacitance is measured between the VIN+x and VIN−x pins (x = A or B).
[2] Parallel interleaved LVDS mode. The power dissipation on DRVDD changes with the output data mode used.

AC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate (500 MSPS), 1.7 V p-p full-scale differential input, 1.0 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
ANALOG INPUT FULL SCALE	Full		2.06		V p-p
NOISE DENSITY[2]	Full		−153		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)[3]					
f_{IN} = 10 MHz	25°C		69.2		dBFS
f_{IN} = 170 MHz	Full	67.5	68.6		dBFS
f_{IN} = 340 MHz	25°C		68.4		dBFS
f_{IN} = 450 MHz	25°C		68.0		dBFS
f_{IN} = 765 MHz	25°C		64.4		dBFS
f_{IN} = 985 MHz	25°C		63.8		dBFS
f_{IN} = 1950 MHz	25°C		60.5		dBFS
SIGNAL-TO-NOISE RATIO AND DISTORTION RATIO (SINAD)[3]					
f_{IN} = 10 MHz	25°C		68.7		dBFS
f_{IN} = 170 MHz	Full	67	68.5		dBFS
f_{IN} = 340 MHz	25°C		67.6		dBFS
f_{IN} = 450 MHz	25°C		67.2		dBFS
f_{IN} = 765 MHz	25°C		63.8		dBFS
f_{IN} = 985 MHz	25°C		62.5		dBFS
f_{IN} = 1950 MHz	25°C		58.3		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 10 MHz	25°C		11.1		Bits
f_{IN} = 170 MHz	Full	10.8	10.9		Bits
f_{IN} = 340 MHz	25°C		10.8		Bits
f_{IN} = 450 MHz	25°C		10.8		Bits
f_{IN} = 765 MHz	25°C		10.3		Bits
f_{IN} = 985 MHz	25°C		10.1		Bits
f_{IN} = 1950 MHz	25°C		9.5		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)[3]					
f_{IN} = 10 MHz	25°C		83		dBFS
f_{IN} = 170 MHz	Full	76	85		dBFS
f_{IN} = 340 MHz	25°C		82		dBFS
f_{IN} = 450 MHz	25°C		86		dBFS
f_{IN} = 765 MHz	25°C		81		dBFS
f_{IN} = 985 MHz	25°C		76		dBFS
f_{IN} = 1950 MHz	25°C		69		dBFS
WORST HARMONIC, SECOND OR THIRD[3]					
f_{IN} = 10 MHz	25°C		−83		dBFS
f_{IN} = 170 MHz	Full		−85	−76	dBFS
f_{IN} = 340 MHz	25°C		−82		dBFS
f_{IN} = 450 MHz	25°C		−86		dBFS
f_{IN} = 765 MHz	25°C		−81		dBFS
f_{IN} = 985 MHz	25°C		−76		dBFS
f_{IN} = 1950 MHz	25°C		−69		dBFS

Parameter[1]	Temperature	Min	Typ	Max	Unit
WORST OTHER, EXCLUDING SECOND OR THIRD HARMONIC[3]					
f_{IN} = 10 MHz	25°C		−93		dBFS
f_{IN} = 170 MHz	Full		−92	−76	dBFS
f_{IN} = 340 MHz	25°C		−90		dBFS
f_{IN} = 450 MHz	25°C		−92		dBFS
f_{IN} = 765 MHz	25°C		−89		dBFS
f_{IN} = 985 MHz	25°C		−89		dBFS
f_{IN} = 1950 MHz	25°C		−85		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD), A_{IN1} AND A_{IN2} = −7 dBFS					
f_{IN1} = 185 MHz, f_{IN2} = 188 MHz	25°C		−88		dBFS
f_{IN1} = 338 MHz, f_{IN2} = 341 MHz	25°C		−87		dBFS
CROSSTALK[4]	25°C		96		dB
FULL POWER BANDWIDTH	25°C		2		GHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Noise density is measured at a low analog input frequency (30 MHz).
[3] See Table 9 for the recommended settings for full-scale voltage and buffer current control.
[4] Crosstalk is measured at 170 MHz with a −1.0 dBFS analog input on one channel and no input on the adjacent channel.

DIGITAL SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate (500 MSPS), 1.7 V p-p full-scale differential input, 1.0 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage	Full	600	1200	1800	mV p-p
Input Common-Mode Voltage	Full		0.85		V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance	Full			2.5	pF
SYNC INPUTS (SYNC+, SYNC−)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage	Full	400	1200	1800	mV p-p
Input Common-Mode Voltage	Full	0.6	0.85	2.0	V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance (Differential)	Full			2.5	pF
LOGIC INPUTS (SDIO, SCLK, CSB, PDWN/STBY)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage	Full		0.8 × SPIVDD		V
Logic 0 Voltage	Full	0	0.2 × SPIVDD		V
Input Resistance	Full		30		kΩ
LOGIC OUTPUT (SDIO)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage (I_{OH} = 800 µA)	Full		0.8 × SPIVDD		V
Logic 0 Voltage (I_{OL} = 50 µA)	Full		0.2 × SPIVDD		V
LOGIC OUTPUTS (FD_A, FD_B)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage	Full	0.8	SPIVDD		V
Logic 0 Voltage	Full	0	0		V
Input Resistance	Full		30		kΩ

Parameter	Temperature	Min	Typ	Max	Unit
DIGITAL OUTPUTS (Dx±,[1] DCO±, STATUS±)					
Logic Compliance	Full		LVDS		
Differential Output Voltage	Full	230		430	mV p-p
Output Common-Mode Voltage (V_{CM})					
AC-Coupled	25°C	0		1.8	V
Short-Circuit Current (I_{DSHORT})	25°C	−100		+100	mA
Differential Return Loss (RL_{DIFF})[2]	25°C	8			dB
Common-Mode Return Loss (RL_{CM}) [2]	25°C	6			dB
Differential Termination Impedance	Full	80	100	120	Ω

[1] Where x = 0 to 13.
[2] Differential and common-mode return loss is measured from 100 MHz to 0.75 MHz × baud rate.

SWITCHING SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, 1.7 V p-p full-scale differential input, 1.0 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK					
Clock Rate (at CLK+/CLK− Pins)	Full	0.25		4	GHz
Maximum Sample Rate[1]	Full	500			MSPS
Minimum Sample Rate[2]	Full	250			MSPS
Clock Pulse Width					
High	Full	1000			ps
Low	Full	1000			ps
LVDS DATA OUTPUT PARAMETERS					
Data Propagation Delay (t_{PD})[3]	Full		2.225		ns
DCO± Propagation Delay (t_{DCO})[3]	Full		2.2		ns
DCO± to Data Skew					
Rising Edge Data (t_{SKEWR})[3]	Full	−150	−25	+100	ps
Falling Edge Data (t_{SKEWF})[3]	Full	850	1.025	1100	ps
STATUS± Propagation Delay (t_{STATUS})[4]	Full		2.2		ns
DCO± to STATUS± Skew (t_{FRAME})[4]	Full	−150	−25	+100	ps
Data Propagation Delay (t_{PD})[3]	Full		2.225		ns
DCO± Propagation Delay (t_{DCO})[3]	Full		2.2		ns
LATENCY[5]					
Pipeline Latency	Full		35		Clock cycles
Fast Detect Latency	Full			28	Clock cycles
HB1 Filter Latency[3]	Full		50		Clock cycles
HB1 + HB2 Filter Latency[3]	Full		101		Clock cycles
HB1 + HB2 + HB3 Filter Latency[3]	Full		217		Clock cycles
HB1 + HB2 + HB3 + HB4 Filter Latency[3]	Full		433		Clock cycles
Fast Detect Latency	Full		28		Clock cycles
Wake-Up Time[6]					
Standby	25°C		1		ms
Power-Down	25°C			4	ms

Parameter	Temperature	Min	Typ	Max	Unit
APERTURE					
Aperture Delay (t_A)	Full		530		ps
Aperture Uncertainty (Jitter, t_j)	Full		55		fs rms
Out of Range Recovery Time	Full		1		Clock Cycles

[1] The maximum sample rate is the clock rate after the divider.
[2] The minimum sample rate operates at 300 MSPS.
[3] This specification is valid for parallel interleaved, channel multiplexed, and byte mode output modes.
[4] This specification is valid for byte mode output mode only.
[5] No DDCs used.
[6] Wake-up time is defined as the time required to return to normal operation from power-down mode or standby mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Description	Min	Typ	Max	Unit
CLK± to SYNC± TIMING REQUIREMENTS	See Figure 2				
t_{SU_SR}	Device clock to SYNC± setup time		117		ps
t_{H_SR}	Device clock to SYNC± hold time		−96		ps
SPI TIMING REQUIREMENTS	See Figure 3				
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK must be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK must be in a logic low state	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 3)	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 3)	10			ns

Timing Diagrams

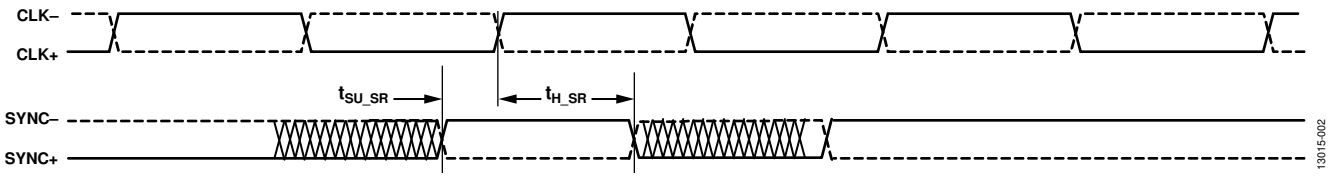


Figure 2. SYNC± Setup and Hold Timing

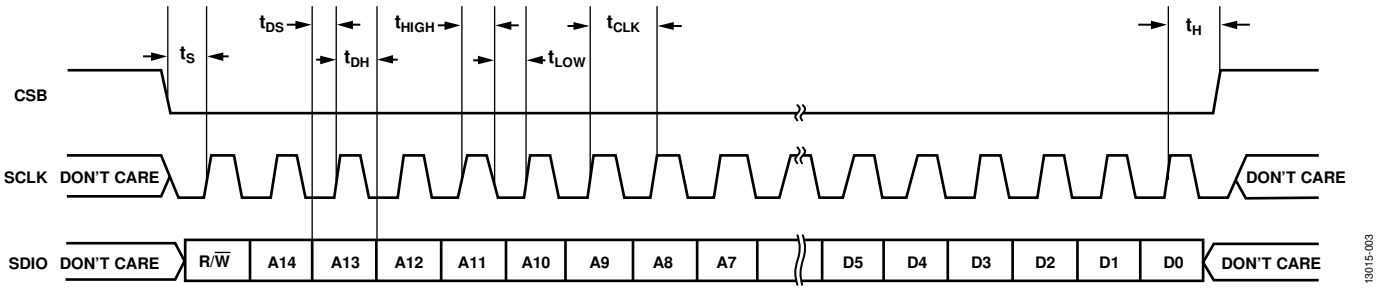


Figure 3. Serial Port Interface Timing Diagram

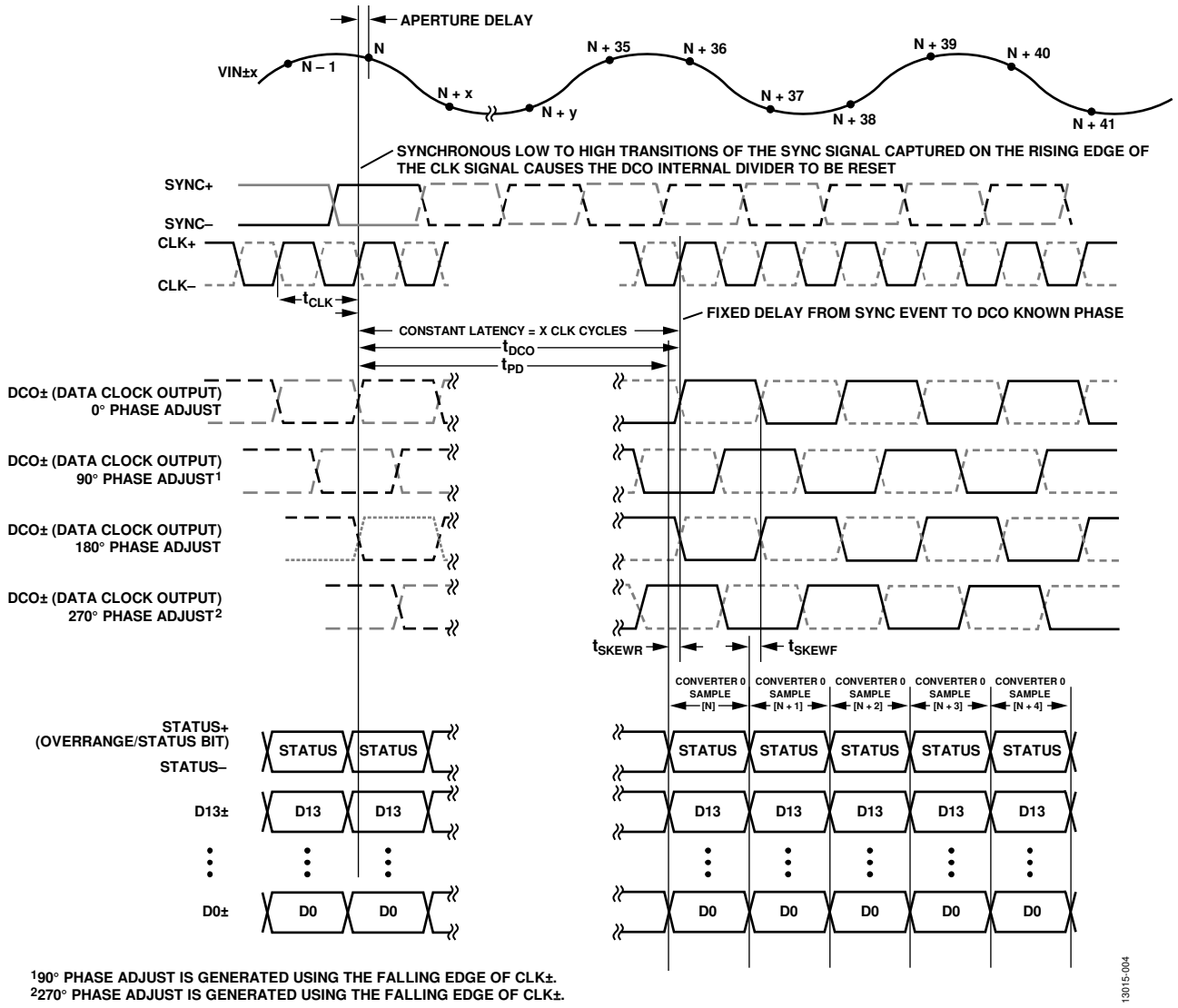


Figure 4. Parallel Interleaved Mode—One Converter, ≤14-Bit Data

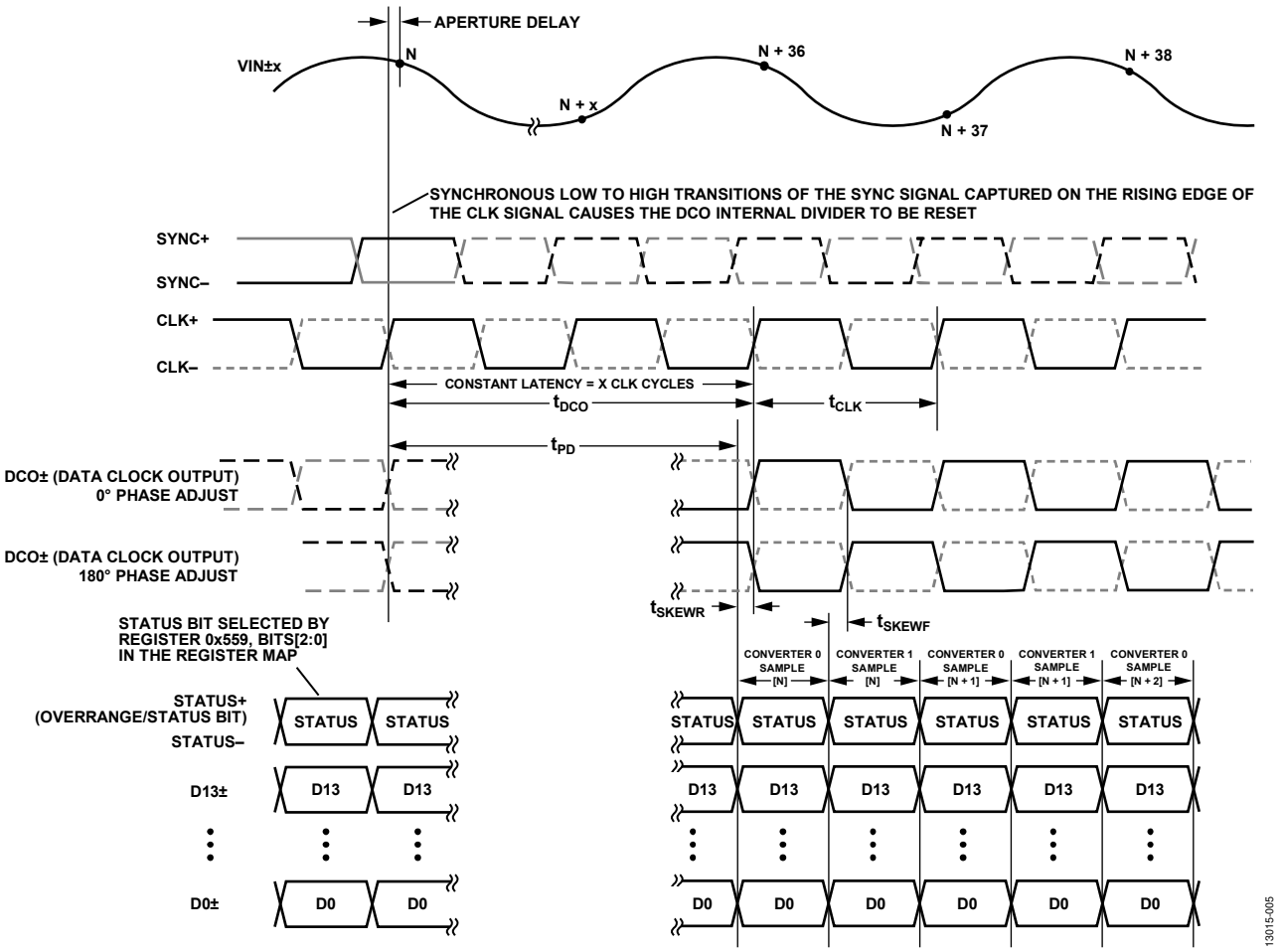


Figure 5. Parallel Interleaved Mode—Two Converters, ≤14-Bit Data, Output Sample Rate < 625 MSPS

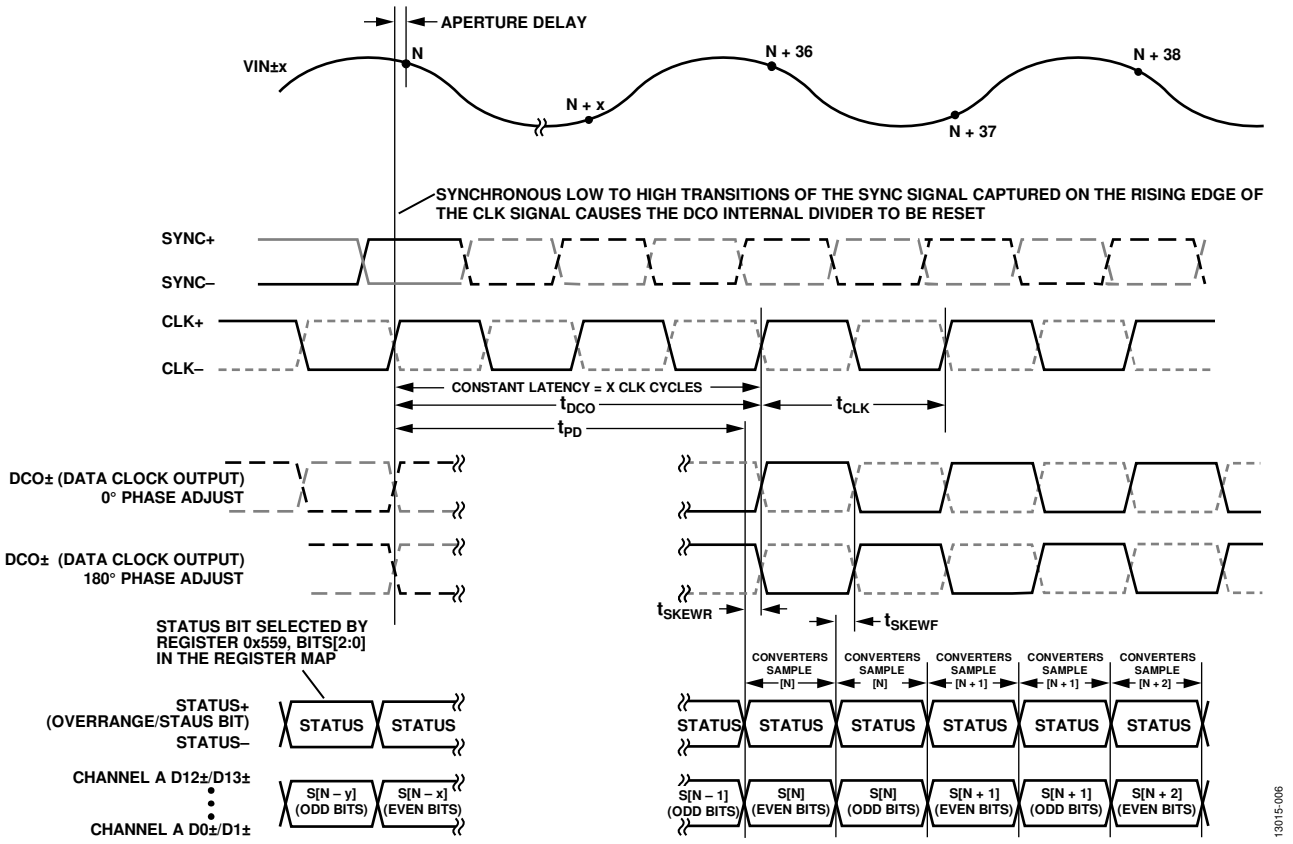


Figure 6. Channel Multiplexed (Even/Odd) Mode—One Converter, ≤14-Bit Data

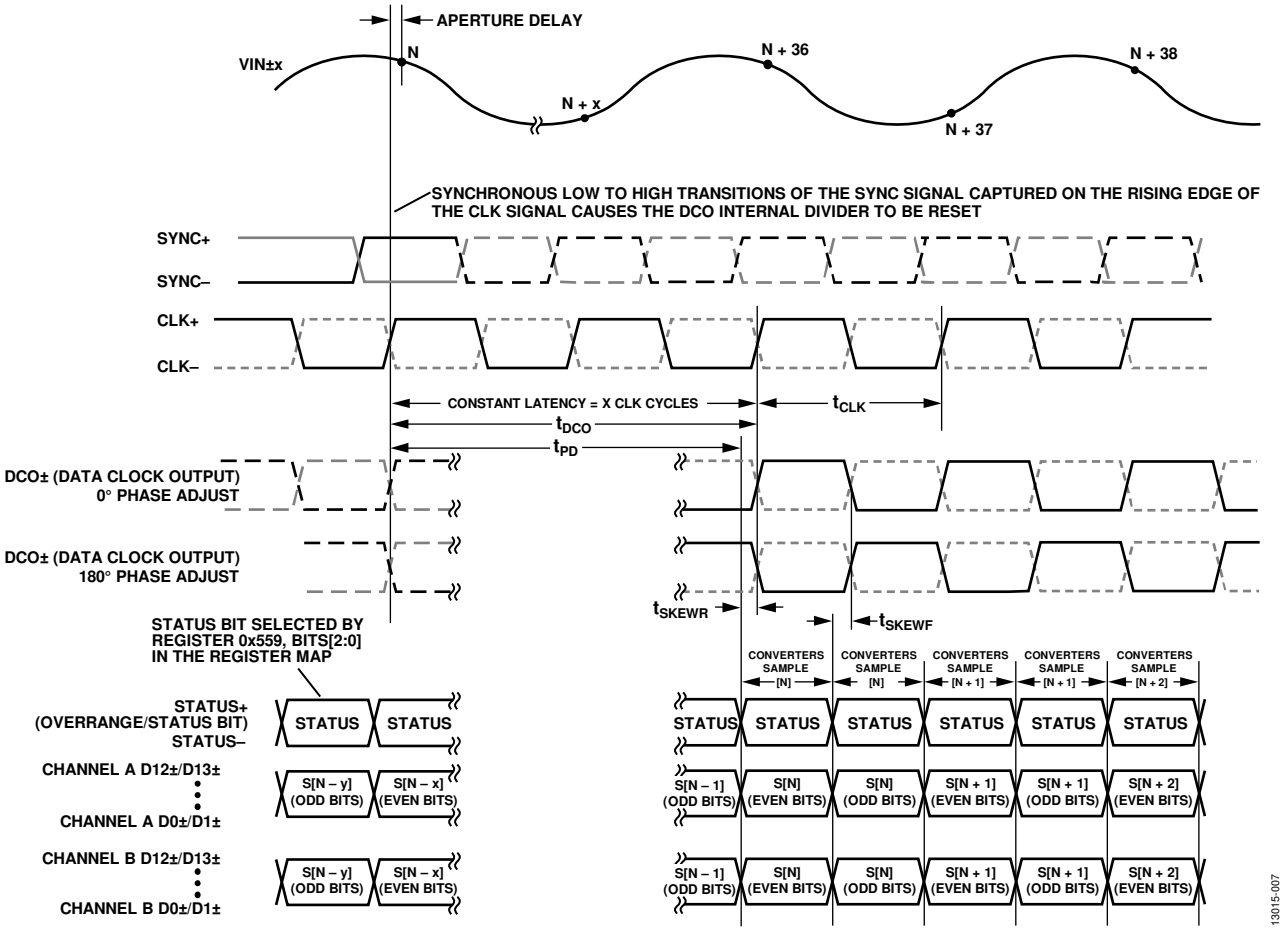
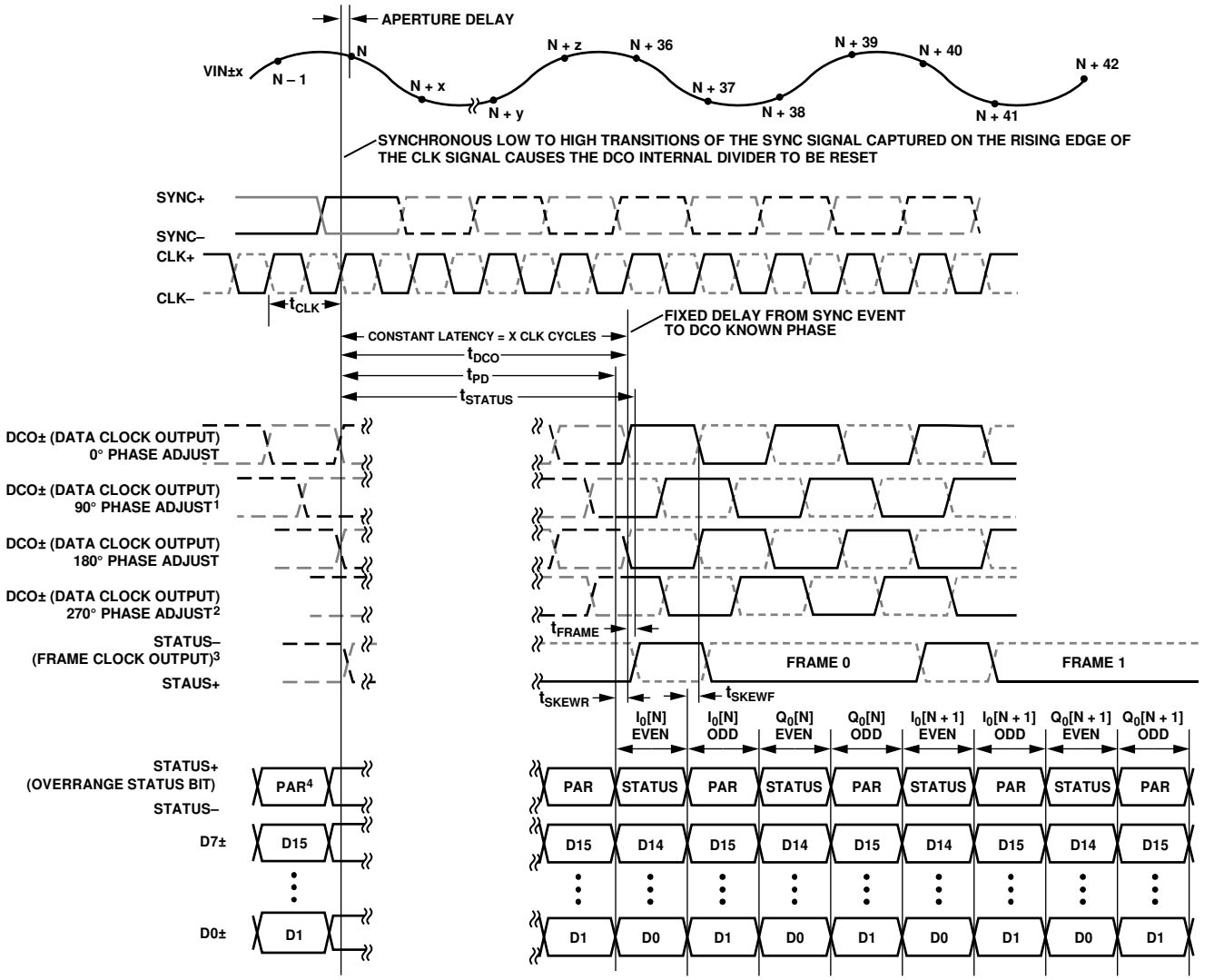
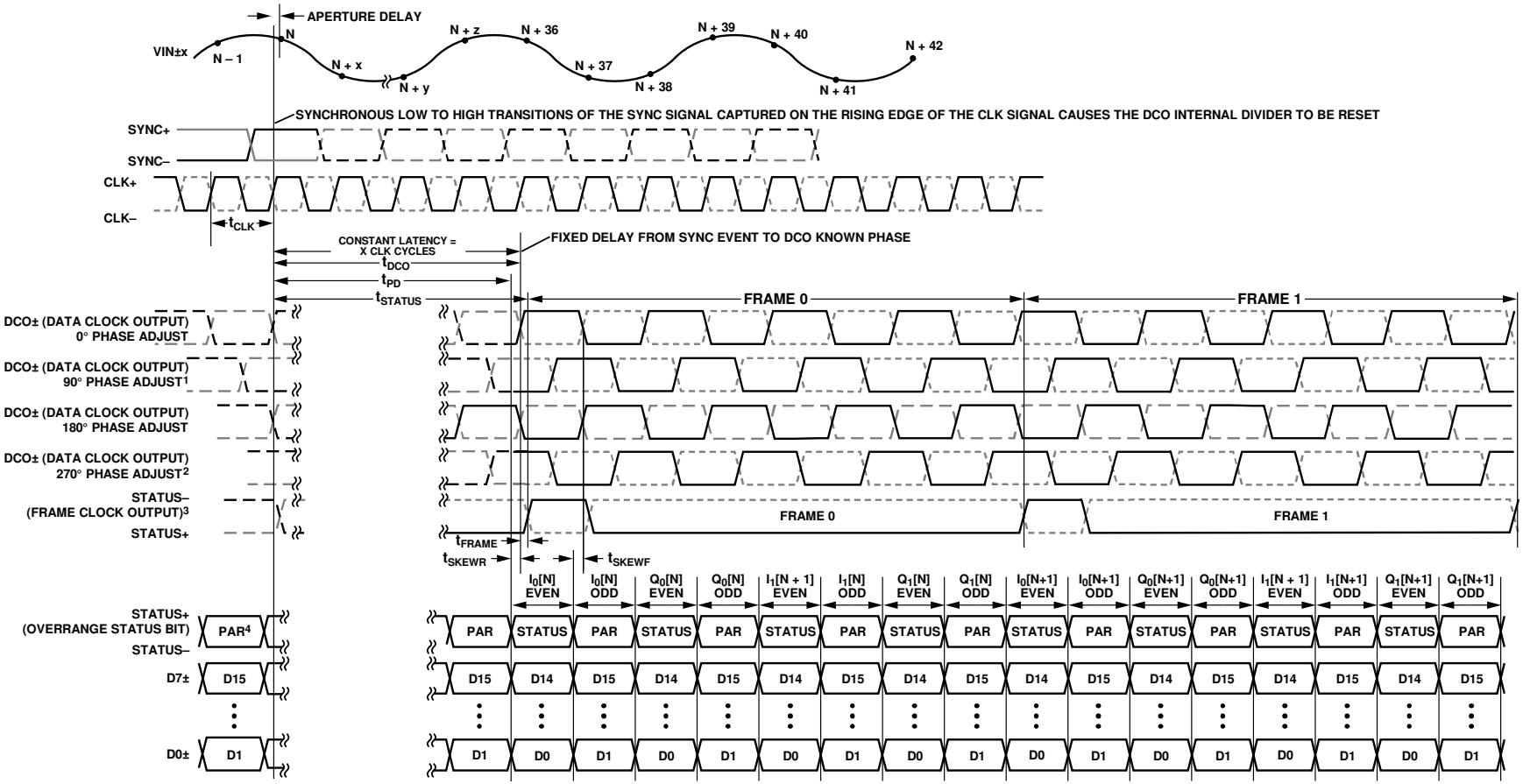


Figure 7. Channel Multiplexed (Even/Odd) Mode—Two Converters, ≤14-Bit Data, Output Sample Rate < 625 MSPS



1 90° PHASE ADJUST IS GENERATED USING THE FALLING EDGE OF CLK±.
2 270° PHASE ADJUST IS GENERATED USING THE FALLING EDGE OF CLK±.
3 FRAME CLOCK OUTPUT SUPPORTS 3 MODES OF OPERATION:
1) ENABLED (ALWAYS ON).
2) DISABLED (ALWAYS OFF).
3) GAPPED PERIODIC (CONDITIONALLY ENABLED BASED ON PSEUDO-RANDOM BIT).
4 STATUS BIT SELECTED BY REGISTER 0x559, BITS[2:0] IN THE REGISTER MAP.

Figure 8. LVDS Byte Mode—Two Virtual Converters, One DDC, I/Q Data Decimate by 4



1090° PHASE ADJUST IS GENERATED USING THE FALLING EDGE OF CLK±.
2270° PHASE ADJUST IS GENERATED USING THE FALLING EDGE OF CLK±.
3FRAME CLOCK OUTPUT SUPPORTS 3 MODES OF OPERATION:
1) ENABLED (ALWAYS ON).
2) DISABLED (ALWAYS OFF).
3) GAPPED PERIODIC (CONDITIONALLY ENABLED BASED ON PSEUDO-RANDOM BIT).
4STATUS BIT SELECTED BY REGISTER 0x559, BITS[2:0] IN THE REGISTER MAP.

13015-010

Figure 9. LVDS Byte Mode—Four Virtual Converters, Two DDCs, ≤16-Bit Data, I/Q Data Decimate by 8

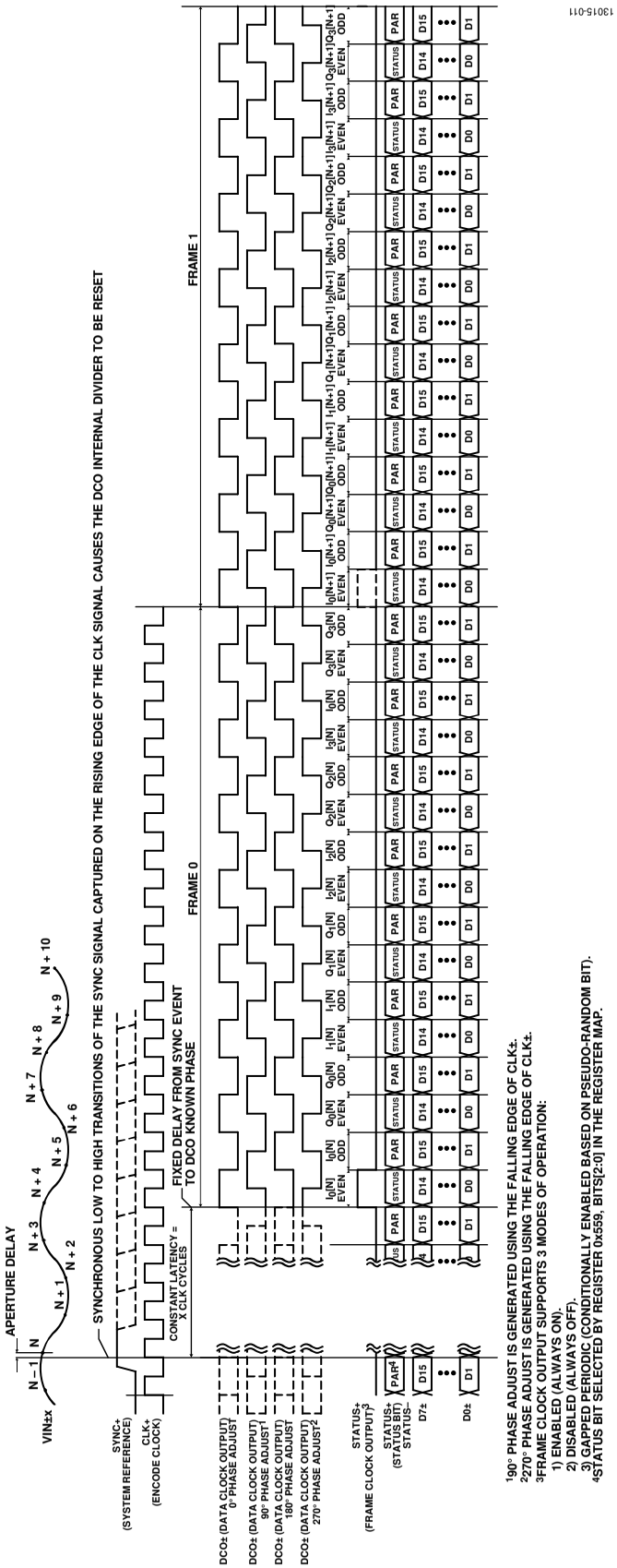


Figure 10. LVDS Byte Mode—Eight Virtual Converters, Four DDCs, ≤16-Bit Data, I/Q Data Decimate by 16

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD1 to AGND	1.32 V
AVDD2 to AGND	2.75 V
AVDD3 to AGND	3.63 V
DVDD to DGND	1.32 V
DRVDD to DRGND	1.32 V
SPIVDD to AGND	3.63 V
AGND to DRGND	−0.3 V to +0.3 V
VIN±x to AGND	3.2 V
SCLK, SDIO, CSB to AGND	−0.3 V to SPIVDD + 0.3 V
VIN±x Maximum Swing	4.3 V p-p
PDWN/STBY to AGND	−0.3 V to SPIVDD + 0.3 V
Environmental	
Operating Temperature Range (T_{CASE})	−40°C to +85°C
Maximum Junction Temperature	125°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Typical θ_{JA}, θ_{JB}, and θ_{JC} are specified vs. the number of printed circuit board (PCB) layers in different airflow velocities (in m/sec). Airflow increases heat dissipation effectively reducing θ_{JA} and θ_{JB}. The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 7.

Table 7. Simulated Thermal Data

PCB Type	Airflow Velocity (m/sec)	θ_{JA}	θ_{JB}	θ_{JC_TOP}	θ_{JC_BOT}	Unit
JEDEC 2s2p Board	0.0	17.8[1,2]	6.3[1,3]	4.7[1,5]	1.2[1,5]	°C/W
	1.0	15.6[1,2]	5.9[1,3]	N/A[4]	N/A[4]	°C/W
	2.5	15.0[1,2]	5.7[1,3]	N/A[4]	N/A[4]	°C/W
10-Layer PCB	0.0	13.8	4.6	4.7	1.2	°C/W
	1.0	12.7	4.6	N/A[4]	N/A[4]	°C/W
	2.5	12.0	4.6	N/A[4]	N/A[4]	°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2s2p test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per JEDEC JESD51-8 (still air).
[4] N/A means not applicable.
[5] Per MIL-STD 883, Method 1012.1.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

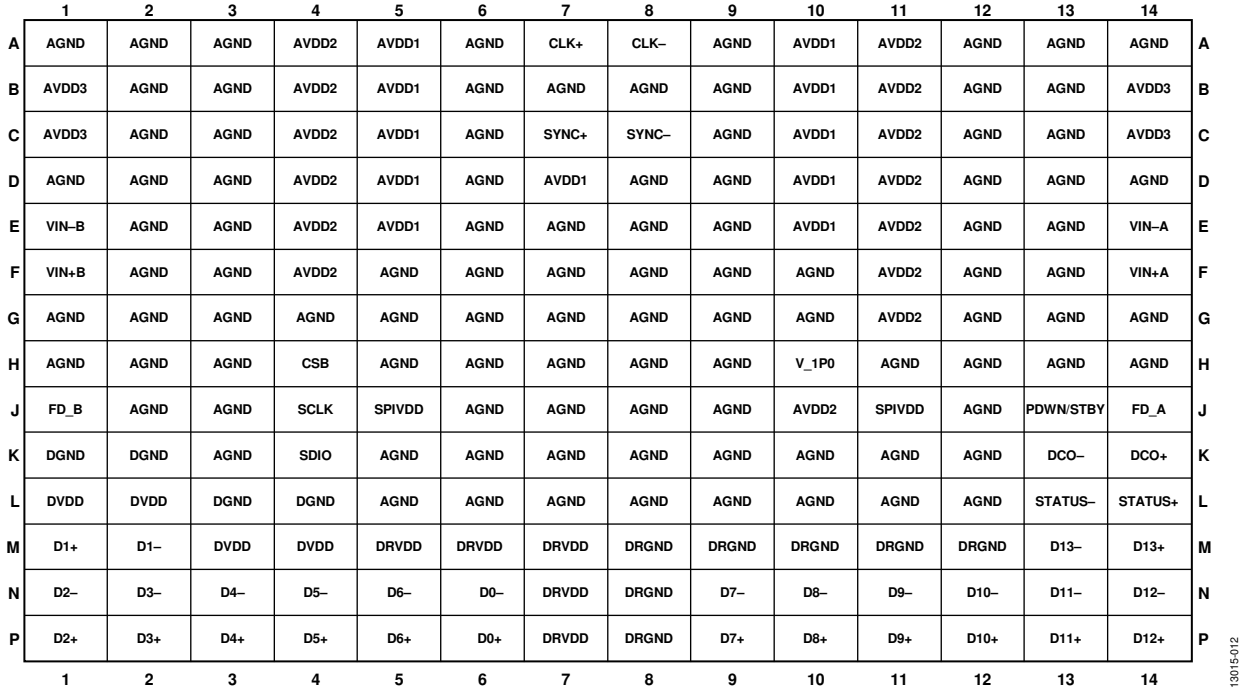


Figure 11. Pin Configuration (Top View)

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
Power Supplies			
A5, A10, B5, B10, C5, C10, D5, D7, D10, E5, E10	AVDD1	Supply	Analog Power Supply (1.25 V Nominal).
A4, A11, B4, B11, C4, C11, D4, D11, E4, E11, F4, F11, G11, J10	AVDD2	Supply	Analog Power Supply (2.50 V Nominal).
B1, B14, C1, C14	AVDD3	Supply	Analog Power Supply (3.3 V Nominal)
L1, L2, M3, M4	DVDD	Supply	Digital Power Supply (1.25 V Nominal).
M5, M6, M7, N7, P7	DRVDD	Supply	Digital Driver Power Supply (1.25 V Nominal).
J5, J11	SPIVDD	Supply	Digital Power Supply for SPI (1.8 V to 3.4 V).
K1, K2, L3, L4	DGND	Ground	Ground Reference for DVDD.
M8 to M12, N8, P8	DRGND	Ground	Ground Reference for DRVDD.
A1, A2, A3, A6, A9, A12, A13, A14, B2, B3, B6, B7, B8, B9, B12, B13, C2, C3, C6, C9, C12, C13, D1, D2, D3, D6, D8, D9, D12, D13, D14, E2, E3, E6 to E9, E12, E13, F2, F3, F5 to F10, F12, F13, G1 to G10, G12, G13, G14, H1, H2, H3, H5 to H9, H11 to H14, J2, J3, J6 to J9, J12, K3, K5 to K12, L5 to L12	AGND	Ground	Ground Reference for AVDD.
Analog			
E14, F14	VIN–A, VIN+A	Input	ADC A Analog Input Complement/True.
E1, F1	VIN–B, VIN+B	Input	ADC B Analog Input Complement/True.
H10	V_1P0	Input/DNC	1.0 V Reference Voltage Input/Do Not Connect. This pin is configurable through the SPI as a no connect or as an input. Do not connect this pin if using the internal reference. This pin requires a 1.0 V reference voltage input if using an external voltage reference source.
A7, A8	CLK+, CLK–	Input	Clock Input True/Complement.

Pin No.	Mnemonic	Type	Description
CMOS Outputs			
J14, J1	FD_A, FD_B	Output	Fast Detect Outputs for Channel A and Channel B.
Digital Inputs			
C7, C8	SYNC+, SYNC−	Input	Active High LVDS SYNC Input—True/Complement.
Data Outputs			
N6, P6	D0−, D0+	Output	LVDS Lane 0 Output Data—Complement/True.
M1, M2	D1+, D1−	Output	LVDS Lane 1 Output Data—True/Complement.
N1, P1	D2−, D2+	Output	LVDS Lane 2 Output Data—Complement/True.
N2, P2	D3−, D3+	Output	LVDS Lane 3 Output Data—Complement/True.
N3, P3	D4−, D4+	Output	LVDS Lane 4 Output Data—Complement/True.
N4, P4	D5−, D5+	Output	LVDS Lane 5 Output Data—Complement/True.
N5, P5	D6−, D6+	Output	LVDS Lane 6 Output Data—Complement/True.
N9, P9	D7−, D7+	Output	LVDS Lane 7 Output Data—Complement/True.
N10, P10	D8−, D8+	Output	LVDS Lane 8 Output Data—Complement/True.
N11, P11	D9−, D9+	Output	LVDS Lane 9 Output Data—Complement/True.
N12, P12	D10−, D10+	Output	LVDS Lane 10 Output Data—Complement/True.
N13, P13	D11−, D11+	Output	LVDS Lane 11 Output Data—Complement/True.
N14, P14	D12−, D12+	Output	LVDS Lane 12 Output Data—Complement/True.
M13, M14	D13−, D13+	Output	LVDS Lane 13 Output Data—Complement/True.
L13, L14	STATUS−, STATUS+	Output	LVDS Status Output Data—Complement/True.
K13, K14	DCO−, DCO+	Output	LVDS Digital Clock Output Data—Complement/True.
SPI Controls			
K4	SDIO	Input/output	SPI Serial Data Input/Output.
J4	SCLK	Input	SPI Serial Clock.
H4	CSB	Input	SPI Chip Select (Active Low).
J13	PDWN/STBY	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 1.2 V, AVDD2= 2.5 V, AVDD3 = 3.3 V, DVDD = 1.2 V, DRVDD = 1.2 V, SPIVDD = 1.8 V, sampling rate = 500 MHz, 1.6 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, default SPI settings, T_A = 25°C, 256k FFT sample, unless otherwise noted.

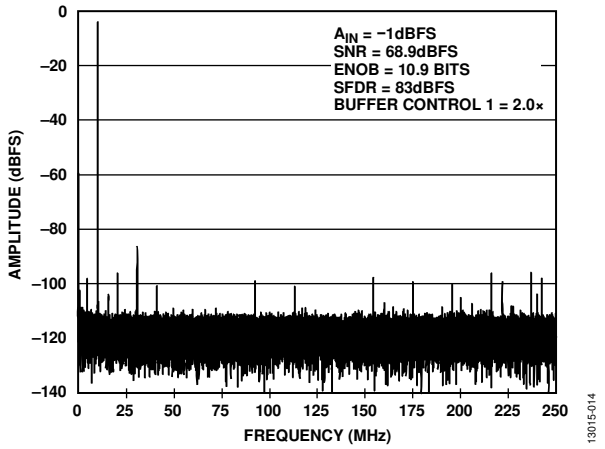


Figure 12. Single Tone FFT with f_{IN} = 10.3 MHz

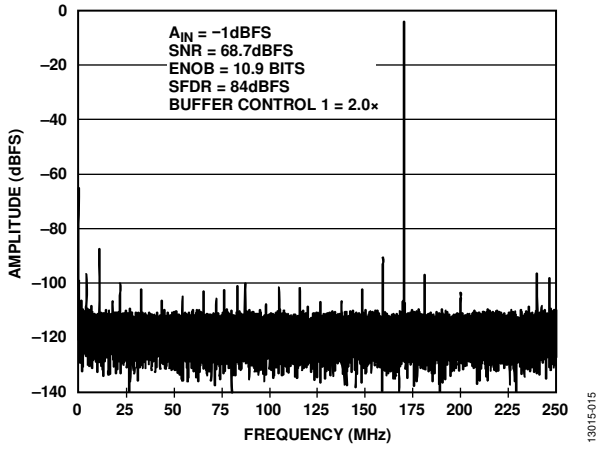


Figure 13. Single Tone FFT with f_{IN} = 170.3 MHz

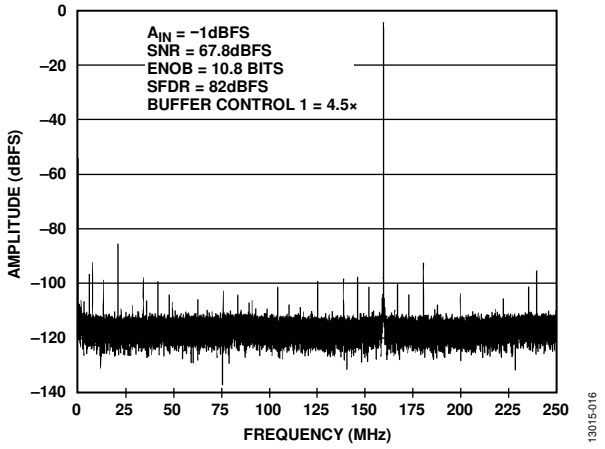


Figure 14. Single Tone FFT with f_{IN} = 340.3 MHz

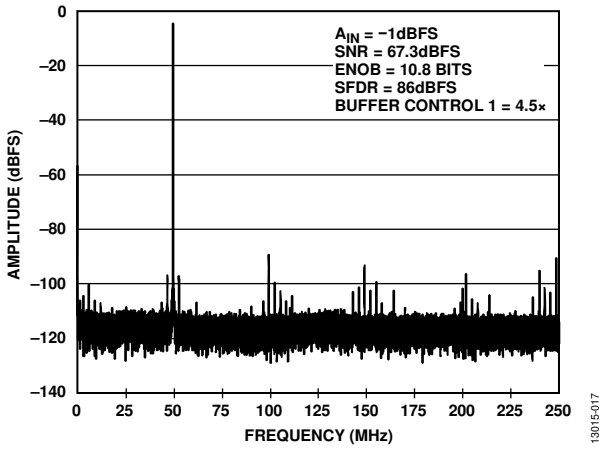


Figure 15. Single Tone FFT with f_{IN} = 450.3 MHz

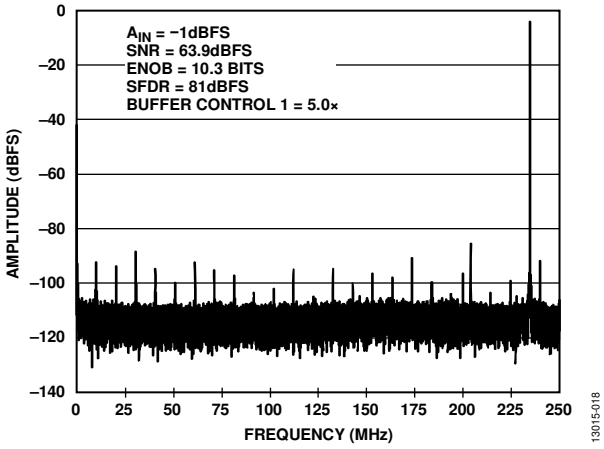


Figure 16. Single Tone FFT with f_{IN} = 765.3 MHz

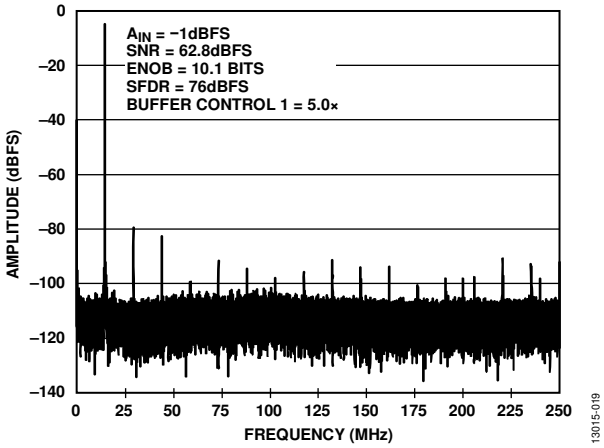


Figure 17. Single-Tone FFT with f_{IN} = 985.3 MHz

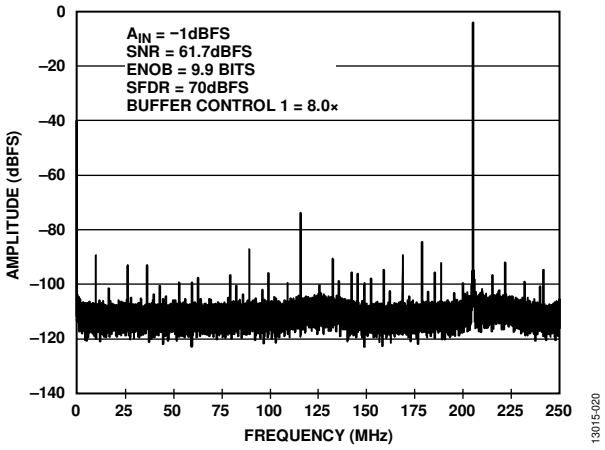


Figure 18. Single Tone FFT with f_{IN} = 1205.3 MHz

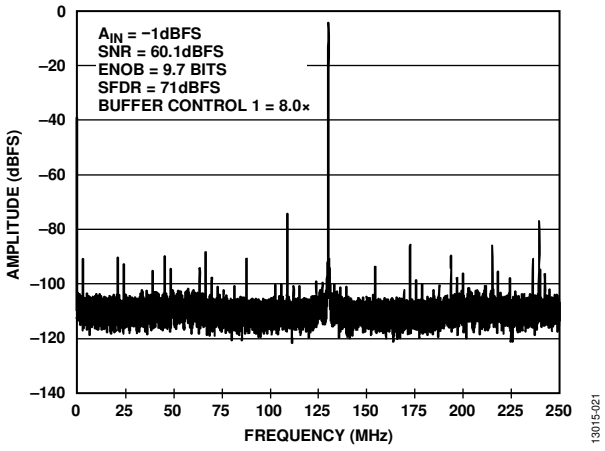


Figure 19. Single Tone FFT with f_{IN} = 1630.3 MHz

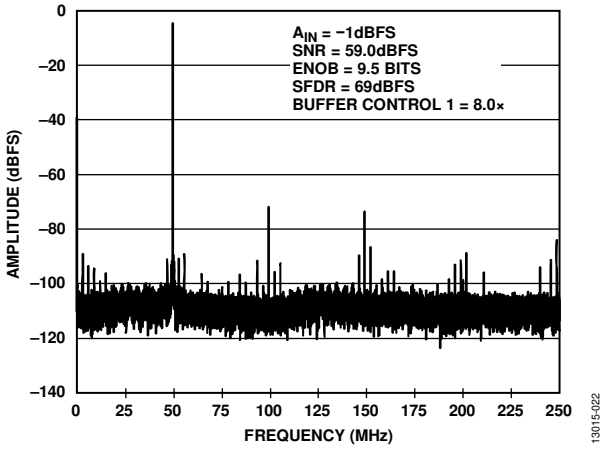


Figure 20. Single Tone FFT with f_{IN} = 985.3 MHz

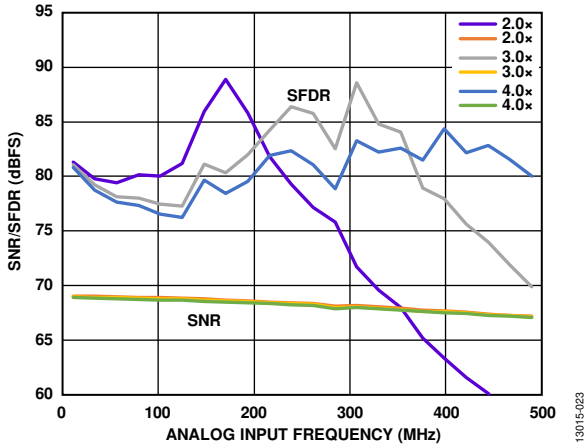


Figure 21. SNR/SFDR vs. Analog Input Frequency (f_{IN}); f_{IN} < 500 MHz; Buffer Control 1 Setting = 2.0×, 3.0×, and 4.0×

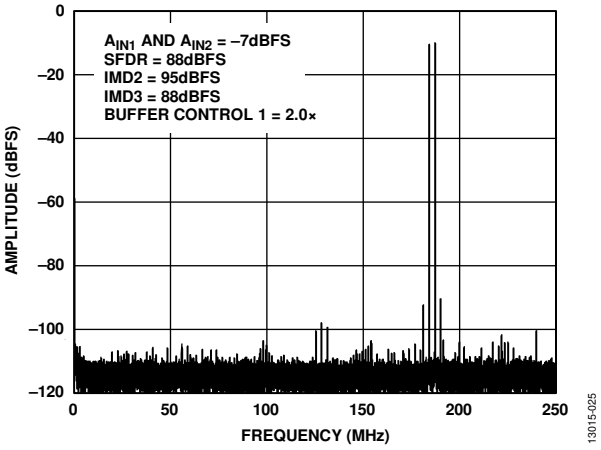


Figure 22. Two-Tone FFT with f_{IN1} = 184 MHz and f_{IN2} = 187 MHz

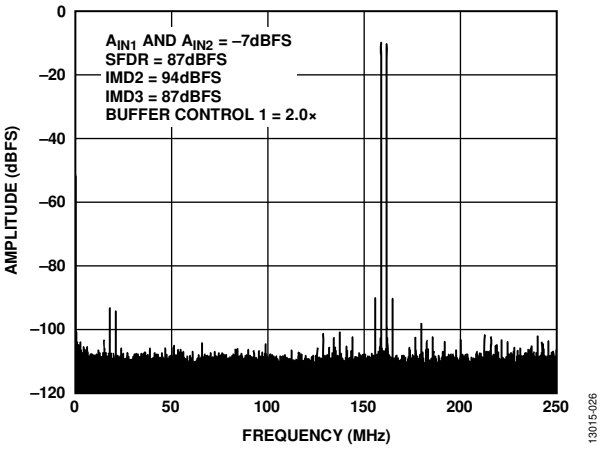


Figure 23. Two-Tone FFT; f_{IN1} = 338 MHz, f_{IN2} = 341 MHz

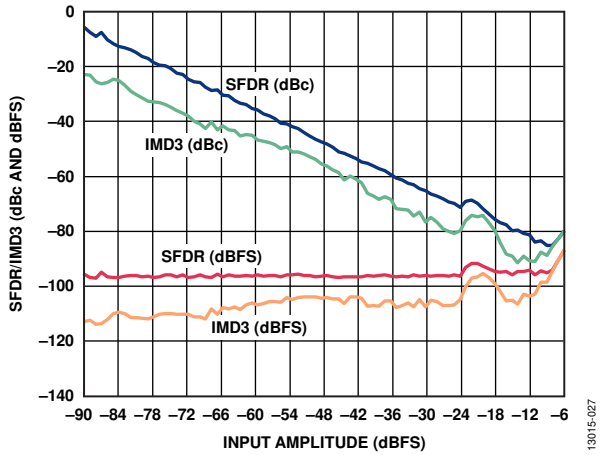


Figure 24. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184 MHz and f_{IN2} = 187 MHz

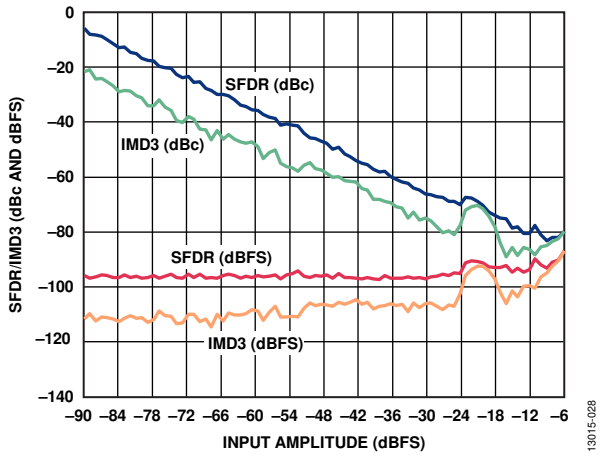


Figure 25. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 338 MHz and f_{IN2} = 341 MHz

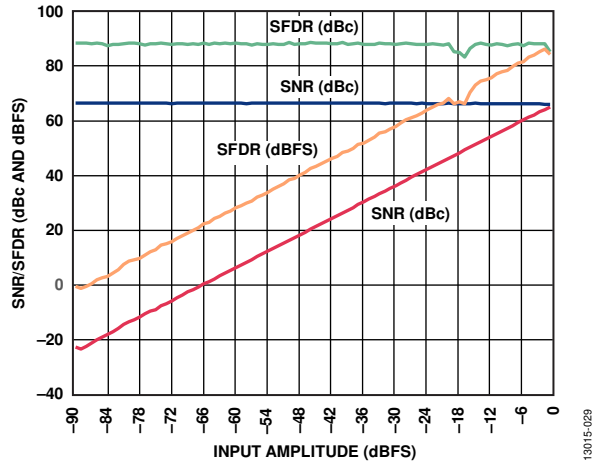


Figure 26. SNR/SFDR vs. Input Amplitude, f_{IN} = 170.3 MHz

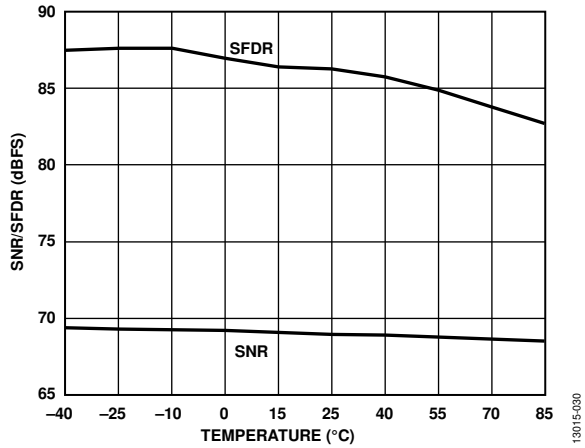


Figure 27. SNR/SFDR vs. Temperature, f_{IN} = 170.3 MHz

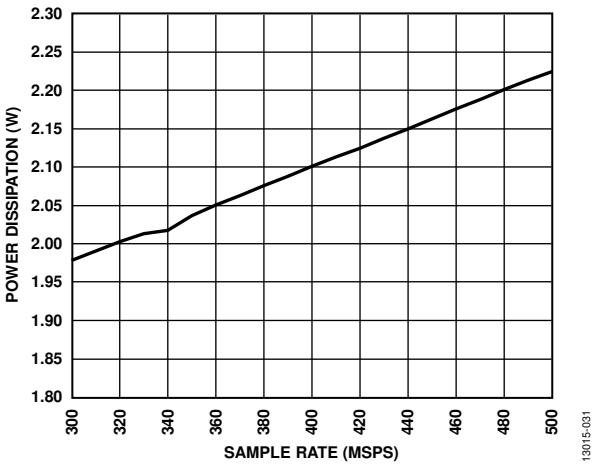


Figure 28. Power Dissipation vs. Sample Rate (f_S) (Default SPI)

EQUIVALENT CIRCUITS

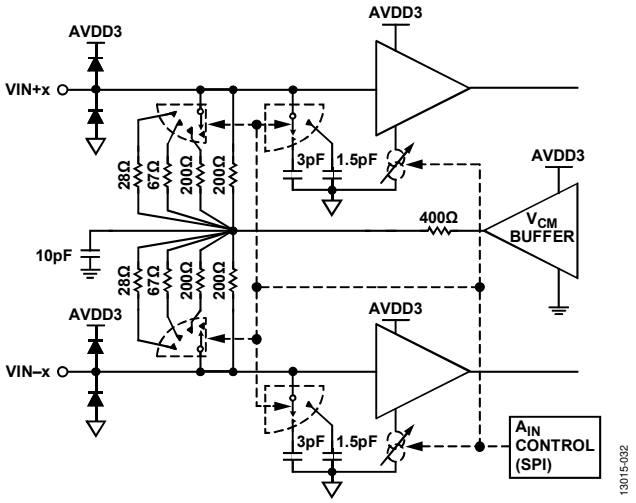


Figure 29. Analog Inputs

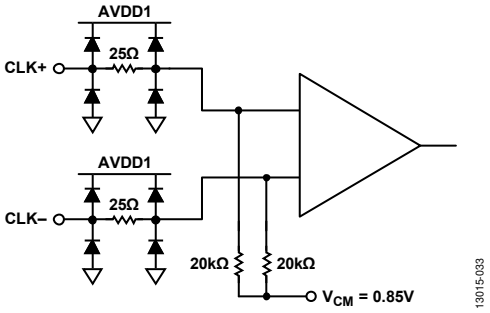


Figure 30. Clock Inputs

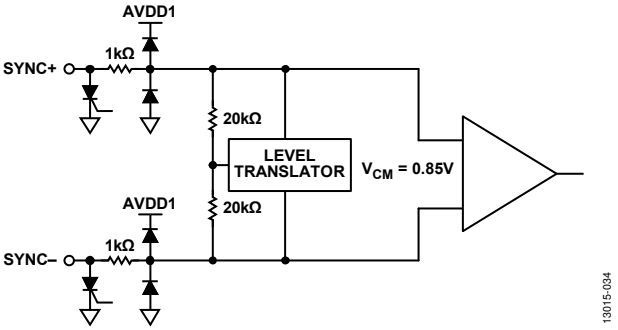


Figure 31. SYNC± Inputs

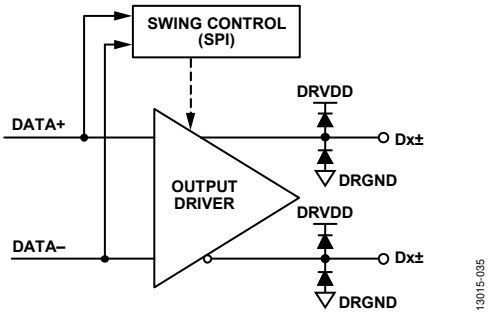


Figure 32. LVDS Digital Outputs, STATUS±, DCO±

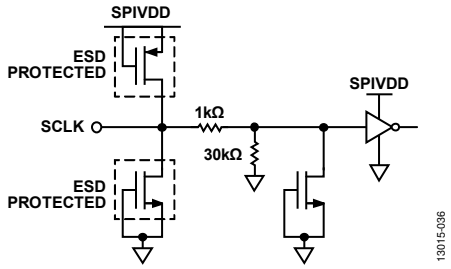


Figure 33. SCLK Inputs

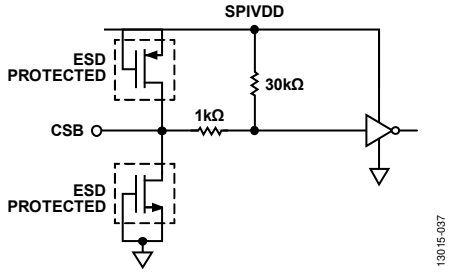


Figure 34. CSB Input

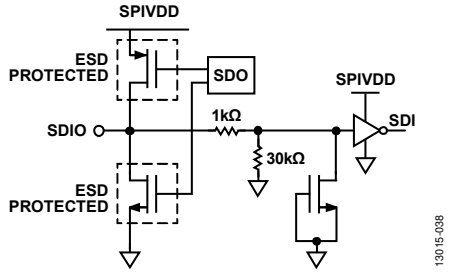


Figure 35. SDIO

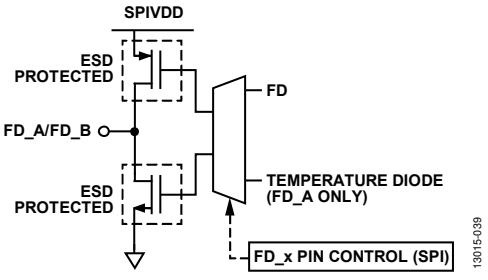


Figure 36. FD_A/FD_B Outputs

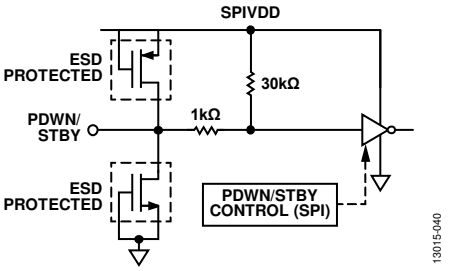


Figure 37. PDWN/STBY Input

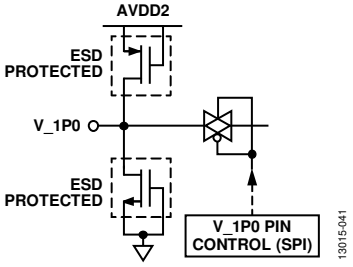


Figure 38. V_1P0 Input/Output

THEORY OF OPERATION

The AD9684 has two analog input channels and 14 LVDS output lane pairs. The ADC is designed to sample wide bandwidth analog signals of up to 2 GHz. The AD9684 is optimized for wide input bandwidth, a high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs that support a variety of user selectable input ranges. An integrated voltage reference eases design considerations.

The AD9684 has several functions that simplify the AGC function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly reduce the system gain to avoid an overrange condition at the ADC input.

The LVDS outputs can be configured depending on the decimation ratio. Multiple device synchronization is supported through the SYNC± input pins.

ADC ARCHITECTURE

The architecture of the AD9684 consists of an input buffered pipelined ADC. The input buffer provides a termination impedance to the analog input signal. This termination impedance can be changed using the SPI to meet the termination needs of the driver/amplifier. The default termination value is set to 400 Ω. The input buffer is optimized for high linearity, low noise, and low power.

The input buffer provides a linear high input impedance (for ease of drive) and reduces kickback from the ADC. The buffer is optimized for high linearity, low noise, and low power. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample, whereas the remaining stages operate with the preceding samples. Sampling occurs on the rising edge of the clock.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9684 is a differential buffer. The internal common-mode voltage of the buffer is 2.05 V. The clock signal alternately switches the input circuit between sample mode and hold mode. When the input circuit is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor, in series with each input, helps reduce the peak transient current injected from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and, thus, achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Place either a differential capacitor or two single-ended capacitors on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input, which limits unwanted broadband noise. For more information, see the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005). In general, the precise values depend on the application.

For best dynamic performance, the source impedances driving VIN+x and VIN−x must be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates a differential reference that defines the span of the ADC core.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9684, the available span is 2.06 V p-p differential.

Differential Input Configurations

There are several ways to drive the AD9684, either actively or passively. However, optimum performance is achieved by driving the analog input differentially.

For applications in which SNR and SFDR are key parameters, differential transformer coupling is the recommended input configuration because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9684.

For low to midrange frequencies, a double balun or double transformer network is recommended for optimum performance of the AD9684 (see Figure 39). For higher frequencies in the second and third Nyquist zones, it is better to remove some of the front-end passive components to ensure wideband operation (see Figure 40).

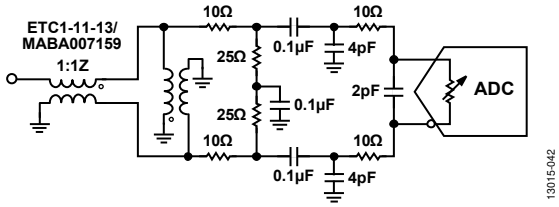


Figure 39. Differential Transformer-Coupled Configuration for First and Second Nyquist Frequencies

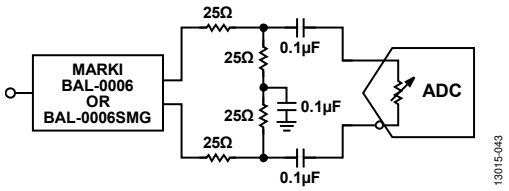


Figure 40. Differential Transformer-Coupled Configuration for Second and Third Nyquist Frequencies

Input Common Mode

The analog inputs of the AD9684 are internally biased to the common mode as shown in Figure 41. The common-mode buffer has a limited range in that the performance suffers greatly if the common-mode voltage drops by more than 100 mV. Therefore, in dc-coupled applications, set the common-mode voltage to 2.05 V ± 100 mV to ensure proper ADC operation.

Analog Input Controls and SFDR Optimization

The AD9684 offers flexible controls for the analog inputs, such as input termination and buffer current. All of the available controls are shown in Figure 41.

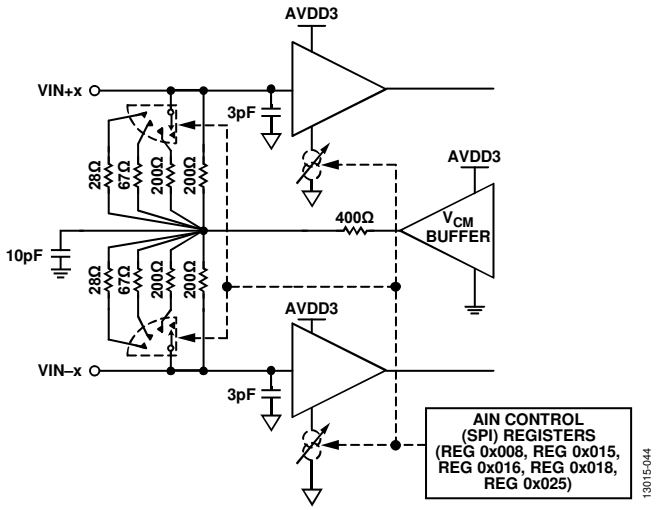


Figure 41. Analog Input Controls (Should the AIN

Using Register 0x018, the buffer currents on each channel can be scaled to optimize the SFDR over various input frequencies and bandwidths of interest. As the input buffer currents are set, the amount of current required by the AVDD3 supply changes. For a complete list of buffer current settings, see Table 29.

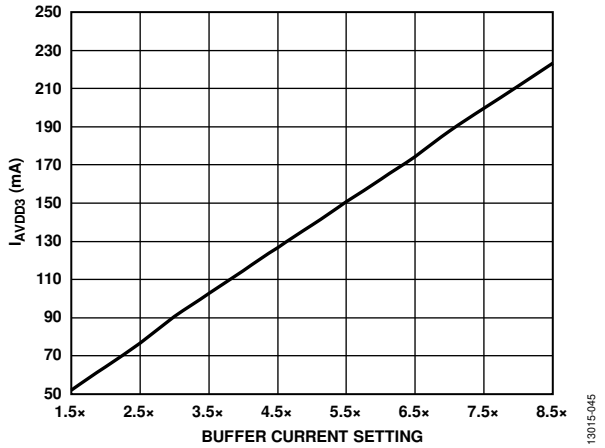


Figure 42. AVDD3 Power (I_{AVDD3}) vs. Buffer Current Control Setting in Register 0x018

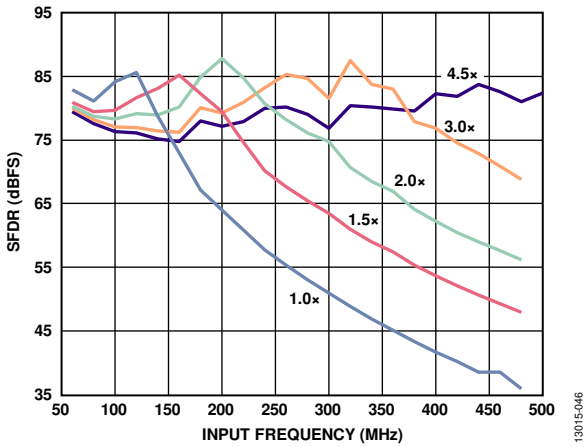


Figure 43. Buffer Current Sweeps (SFDR vs. Input Frequency and I_{BUFF}), 10 MHz < f_{IN} < 500 MHz

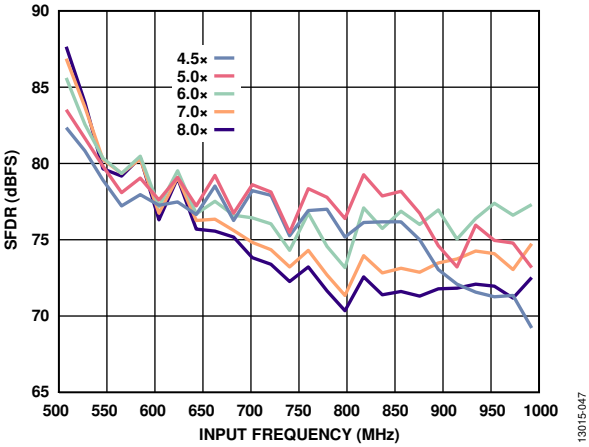


Figure 44. Buffer Current Sweeps (SFDR vs. Input Frequency and I_{BUFF}), 500 MHz < f_{IN} < 1000 MHz

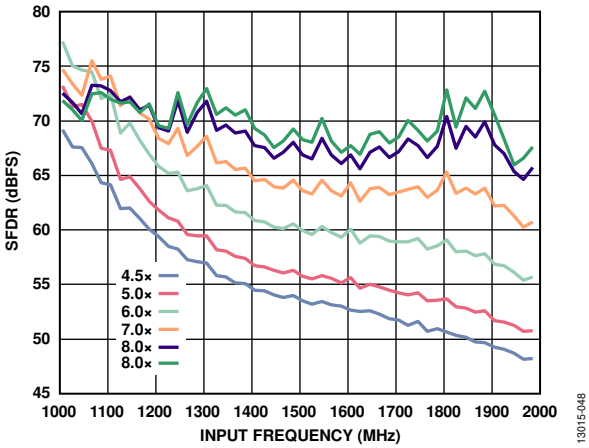


Figure 45. Buffer Current Sweeps (SFDR vs. Input Frequency and I_{BUFF}), 1 GHz < f_{IN} < 2 GHz, Front-End Network Shown in Figure 40

Figure 43, Figure 44, and Figure 45 show how the SFDR can be optimized using the buffer current setting in Register 0x018 for different Nyquist zones. At frequencies greater than 1 GHz, it is better to run the ADC at input amplitudes less than −1 dBFS (−3 dBFS, for example). This greatly improves the linearity of the converted signal without sacrificing SNR performance.