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14-Bit, 2.0 GSPS/2.6 GSPS, JESD204B, Dual Analog-to-Digital Converter

Data Sheet **AD9689**

FEATURES

- JESD204B (Subclass 1) coded serial digital outputs
  - Support for lane rates up to 16 Gbps per lane
- Noise density
  - −152 dBFS/Hz at 2.56 GSPS at full-scale voltage = 1.7 V p-p
  - −154 dBFS/Hz at 2.56 GSPS at full-scale voltage = 2.0 V p-p
  - −154.2 dBFS/Hz at 2.0 GSPS at full-scale voltage = 1.7 V p-p
  - −155.3 dBFS/Hz at 2.0 GSPS at full-scale voltage = 2.0 V p-p
- 1.55 W total power per channel at 2.56 GSPS (default settings)
- SFDR at 2.56 GSPS encode
  - 73 dBFS at 1.8 GHz A_{IN} at −2.0 dBFS
  - 59 dBFS at 5.53 GHz A_{IN} at −2.0 dBFS
    - full-scale voltage = 1.1 V p-p
- SNR at 2.56 GSPS encode
  - 59.7 dBFS at 1.8 GHz A_{IN} at −2.0 dBFS
  - 53.0 dBFS at 5.53 GHz A_{IN} at −2.0 dBFS
    - full-scale voltage = 1.1 V p-p
- SFDR at 2.0 GSPS encode
  - 78 dBFS at 900 MHz A_{IN} at −2.0 dBFS
  - 62 dBFS at 5.53 GHz A_{IN} at −2.0 dBFS
    - full-scale voltage = 1.1 V p-p
- SNR at 2.0 GSPS encode
  - 62.7 dBFS at 900 MHz A_{IN} at −2.0 dBFS
  - 53.1 dBFS at 5.5 GHz A_{IN} at −2.0 dBFS
    - full-scale voltage = 1.1 V p-p
- 0.975 V, 1.9 V, and 2.5 V dc supply operation
- 9 GHz analog input full power bandwidth (−3 dB)
- Amplitude detect bits for efficient AGC implementation
- Programmable FIR filters for analog channel loss equalization
- 2 integrated, wideband digital processors per channel
  - 48-bit NCO
  - Programmable decimation rates
- Phase coherent NCO switching
  - Up to 4 channels available
- Serial port control
  - Supports 100 MHz SPI writes and 50 MHz SPI reads
  - Integer clock with divide by 2 and divide by 4 options
  - Flexible JESD204B lane configurations
- On-chip dither

APPLICATIONS

- Diversity multiband and multimode digital receivers
- 3G/4G, TD-SCDMA, W-CDMA, and GSM, LTE, LTE-A
- Electronic test and measurement systems
- Phased array radar and electronic warfare
- DOCSIS 3.0 CMTS upstream receive paths
- HFC digital reverse path receivers

FUNCTIONAL BLOCK DIAGRAM

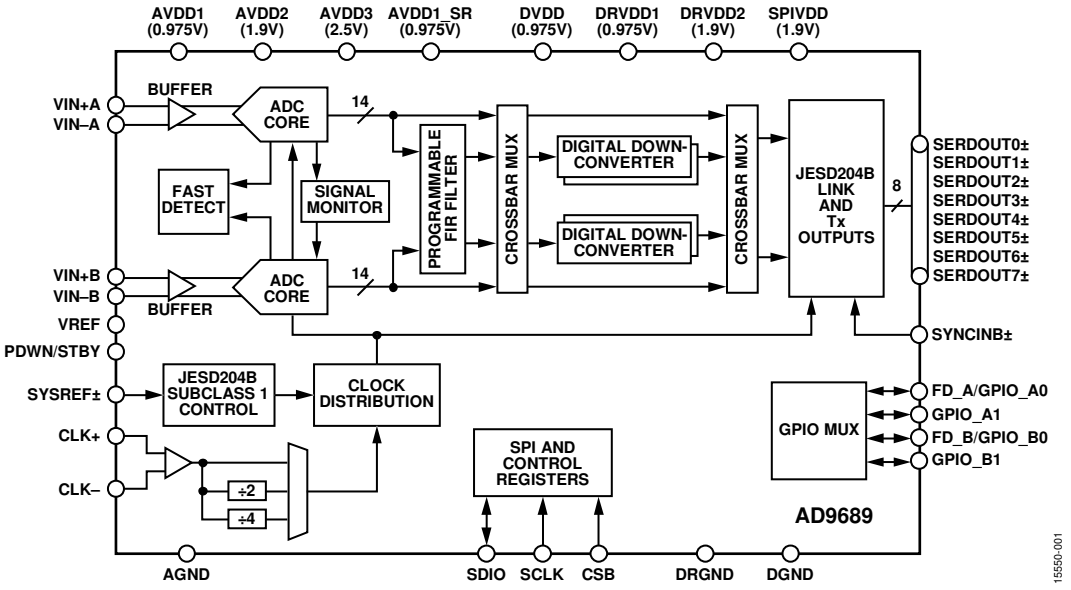

Figure 1.

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TABLE OF CONTENTS

REVISION HISTORY

10/2017—Rev. 0 to Rev. A

Added 2.0 GSPS..... Throughout
Changes to Features Section 1
Changes to Product Highlights Section 4
Changes to Table 1 5
Changes to Table 2 6
Changes to Table 4 9
Added 2.0 GSPS Section and Figure 6 to Figure 11; Renumbered Sequentially.....16
Added Figure 12 to Figure 17 17
Added Figure 18 to Figure 23 18
Added Figure 24 through Figure 29.....19
Added Figure 30 through Figure 35.....20
Added 2.6 GSPS Section.....21
Change to Figure 41 21
Change to Figure 45 22
Changes to Figure 52 and Figure 53 23
Changes to Figure 54, Figure 55, Figure 56, Figure 58, and Figure 59 24
Changes to Figure 60 and Figure 61 25
Changes to Figure 67 Caption 26
Changes to Table 10 30
Changes to Figure 87 32
Changes to Figure 96 Caption 35
Changes to Programming Instructions Section.....42
Added Table 28; Renumbered Sequentially.....67
Changes to Table 29 Title 67
Changes to De-Emphasis Section 74
Changes to Figure 142 82
Changes to Reading the Memory Map Register Table Section.....97
Changes to Address 0x0006, Table 46 98
Changes to Address 0x010A, Table 47 99
Changes to Table 50 105
Changes to Table 51 117
Changes to Power Supply Recommendations Section, Figure 157, and Figure 158 132
Changes to Ordering Guide.....134

9/2017—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9689 is a dual, 14-bit, 2.0 GSPS/2.6 GSPS analog-to-digital converter (ADC). The device has an on-chip buffer and a sample-and-hold circuit designed for low power, small size, and ease of use. This product is designed to support communications applications capable of direct sampling wide bandwidth analog signals of up to 5 GHz. The −3 dB bandwidth of the ADC input is 9 GHz. The AD9689 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. The analog input and clock signals are differential inputs. The ADC data outputs are internally connected to four digital downconverters (DDCs) through a crossbar mux. Each DDC consists of multiple cascaded signal processing stages: a 48-bit frequency translator (numerically controlled oscillator (NCO)), and decimation rates. The NCO has the option to select preset bands over the general-purpose input/output (GPIO) pins, which enables the selection of up to three bands. Operation of the AD9689 between the DDC modes is selectable via SPI-programmable profiles.

In addition to the DDC blocks, the AD9689 has several functions that simplify the automatic gain control (AGC) function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect control bits in Register 0x0245 of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input. In addition to the fast detect outputs, the AD9689 also offers signal monitoring capability. The signal monitoring block provides additional information about the signal being digitized by the ADC.

The user can configure the Subclasss 1 JESD204B-based high speed serialized output in a variety of one-lane, two-lane, four-lane, and eight-lane configurations, depending on the DDC configuration and the acceptable lane rate of the receiving logic device. Multidevice synchronization is supported through the SYSREF± and SYNCINB± input pins.

The AD9689 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using a 3-wire serial port interface (SPI).

The AD9689 is available in a Pb-free, 196-ball BGA, specified over the −40°C to +85°C ambient temperature range. This product is protected by a U.S. patent.

Note that throughout this data sheet, multifunction pins, such as FD_A/GPIO_A0, are referred to either by the entire pin name or by a single function of the pin, for example, FD_A, when only that function is relevant.

PRODUCT HIGHLIGHTS

1. Wide, input −3 dB bandwidth of 9 GHz supports direct radio frequency (RF) sampling of signals up to about 5 GHz.
2. Four integrated, wideband decimation filters and NCO blocks supporting multiband receivers.
3. Fast NCO switching enabled through the GPIO pins.
4. SPI controls various product features and functions to meet specific system requirements.
5. Programmable fast overrange detection and signal monitoring.
6. On-chip temperature diode for system thermal management.
7. 12 mm × 12 mm, 196-ball BGA.
8. Pin, package, feature, and memory map compatible with the AD9208 14-bit, 3.0 GSPS, JESD204B dual ADC.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.9 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.9 V, SPIVDD = 1.9 V, sampling rate = 2.0 GHz/2.56 GHz, clock divider = 2, 1.7 V p-p full-scale differential input, input amplitude (A_{IN}) = −2.0 dBFS, L = 8, M = 2, F = 1, −10°C ≤ T_J ≤ +120°C,[1] unless otherwise noted. Typical specifications represent performance at T_J = 70°C (T_A = 25°C).

Table 1.

	2.0 GSPS			2.6 GSPS			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	14			14			Bits
ACCURACY							
No Missing Codes		Guaranteed			Guaranteed		
Offset Error					0		%FSR
Offset Matching		0			0		%FSR
Gain Error	−2.9	±1	+1.8	−4.9	±1	+5.6	%FSR
Gain Matching		±0.2			±0.2		%FSR
Differential Nonlinearity (DNL)	−0.62	±0.4	+0.79	−0.65	±0.4	+0.75	LSB
Integral Nonlinearity (INL)	−9.9	±2	+8.1	−16	±6	+13	LSB
TEMPERATURE DRIFT							
Offset Error		±7.7			±3.7		ppm/°C
Gain Error		15			58		ppm/°C
INTERNAL VOLTAGE REFERENCE		0.5			0.5		V
INPUT REFERRED NOISE		3.8			4.6		LSB rms
ANALOG INPUTS							
Differential Input Voltage Range	1.1	1.7	2.0	1.1	1.7	2.0	V p-p
Common-Mode Voltage (V_{CM})		1.4			1.4		V
Differential Input Capacitance		0.35			0.35		pF
−3 dB Bandwidth		9			9		GHz
POWER SUPPLY							
AVDD1	0.95	0.975	1.0	0.95	0.975	1.0	V
AVDD2	1.85	1.9	1.95	1.85	1.9	1.95	V
AVDD3	2.44	2.5	2.56	2.44	2.5	2.56	V
AVDD1_SR	0.95	0.975	1.0	0.95	0.975	1.0	V
DVDD	0.95	0.975	1.0	0.95	0.975	1.0	V
DRVDD1	0.95	0.975	1.0	0.95	0.975	1.0	V
DRVDD2	1.85	1.9	1.95	1.85	1.9	1.95	V
SPIVDD	1.85	1.9	1.95	1.85	1.9	1.95	V
I_{AVDD1}		455	605		590	693	mA
I_{AVDD2}		585	670		810	882	mA
I_{AVDD3}		65	72		65	73	mA
I_{AVDD1_SR}		25	41		25	43	mA
I_{DVDD}		340	800		405	833	mA
I_{DRVDD1} [2]		320	432		390	500	mA
I_{DRVDD2}		25	30		25	30	mA
I_{SPIVDD}		1	5		1	5	mA

POWER CONSUMPTION			
Total Power Dissipation (Including Output Drivers)[3]	2.45	3.1	W
Power-Down Dissipation	265	300	mW
Standby[4]	1.3	1.5	W

[1] The junction temperature (T_J) range of −10°C to +120°C translates to an ambient temperature (T_A) range of −40°C to +85°C.
[2] All lanes running. Power dissipation on DRVDDx changes with lane rate and number of lanes used.
[3] Default mode. No DDCs used.
[4] Can be controlled by the SPI.

AC SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.9 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.9 V, SPIVDD = 1.9 V, sampling rate = 2.0 GHz/2.56 GHz, clock divider = 2, 1.7 V p-p full-scale differential input, input amplitude (A_{IN}) = −2.0 dBFS, default SPI settings, −10°C ≤ T_J ≤ +120°C,[1] unless otherwise noted. Typical specifications represent performance at T_J = 70°C (T_A = 25°C).

Table 2.

	2.0 GSPS			2.6 GSPS			
Parameter[2]	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
NOISE DENSITY[3]							
Full Scale = 1.7 V p-p		−154.2			−152		dBFS/Hz
Full Scale = 2.0 V p-p		−155.3			−154		dBFS/Hz
CODE ERROR RATE (CER)							
AVDD1 = 0.975 V		7×10^{-15}			9×10^{-9}		Errors
AVDD1 = 1.0 V		3×10^{-15}			4.5×10^{-10}		Errors
SIGNAL-TO-NOISE RATIO (SNR)							
f_{IN} = 155 MHz		63.7			61.3		dBFS
f_{IN} = 155 MHz (Full Scale = 2.0 V p-p)		65.0			62.5		dBFS
f_{IN} = 750 MHz		63.1			61.0		dBFS
f_{IN} = 900 MHz	60.2	62.7			60.9		dBFS
f_{IN} = 1800 MHz		60.9		56.0	59.7		dBFS
f_{IN} = 2100 MHz		59.9			59.3		dBFS
f_{IN} = 3300 MHz		58.3			58.0		dBFS
f_{IN} = 4350 MHz (Full Scale = 1.1 V p-p)		54.4			54.0		dBFS
f_{IN} = 5530 MHz (Full Scale = 1.1 V p-p)		53.1			53.0		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)							
f_{IN} = 155 MHz		63.5			61.2		dBFS
f_{IN} = 155 MHz (Full Scale = 2.0 V p-p)		64.7			62.4		dBFS
f_{IN} = 750 MHz		62.8			60.7		dBFS
f_{IN} = 900 MHz	59.6	62.5			60.5		dBFS
f_{IN} = 1800 MHz		60.8		52.4	59.4		dBFS
f_{IN} = 2100 MHz		59.7			59.1		dBFS
f_{IN} = 3300 MHz		55.3			56.6		dBFS
f_{IN} = 4350 MHz (Full Scale = 1.1 V p-p)		53.2			51.0		dBFS
f_{IN} = 5530 MHz (Full Scale = 1.1 V p-p)		52.3			49.5		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)							
f_{IN} = 155 MHz		10.3			9.9		Bits
f_{IN} = 155 MHz (Full Scale = 2.0 V p-p)		10.5			10.1		Bits
f_{IN} = 750 MHz		10.1			9.8		Bits
f_{IN} = 900 MHz	9.6	10.1			9.8		Bits
f_{IN} = 1800 MHz		9.8		8.4	9.6		Bits
f_{IN} = 2100 MHz		9.6			9.5		Bits
f_{IN} = 3300 MHz		8.9			9.1		Bits
f_{IN} = 4350 MHz (Full Scale = 1.1 V p-p)		8.6			8.2		Bits
f_{IN} = 5530 MHz (Full Scale = 1.1 V p-p)		8.4			7.9		Bits

Parameter[2]	2.0 GSPS Min	2.0 GSPS Typ	2.0 GSPS Max	2.6 GSPS Min	2.6 GSPS Typ	2.6 GSPS Max	Unit
SPURIOUS FREE DYNAMIC RANGE (SFDR), SECOND OR THIRD HARMONIC[4, 5]							
f_{IN} = 155 MHz		77			78		dBFS
f_{IN} = 155 MHz (Full Scale = 2.0 V p-p)		77			78		dBFS
f_{IN} = 750 MHz		77			73		dBFS
f_{IN} = 900 MHz	66	78			74		dBFS
f_{IN} = 1800 MHz		76		58	73		dBFS
f_{IN} = 2100 MHz		76			73		dBFS
f_{IN} = 3300 MHz		60			64		dBFS
f_{IN} = 4350 MHz (Full Scale = 1.1 V p-p)		61			60		dBFS
f_{IN} = 5530 MHz (Full Scale = 1.1 V p-p)		62			59		dBFS
WORST OTHER, EXCLUDING SECOND OR THIRD HARMONIC							
f_{IN} = 155 MHz		−99			−96		dBFS
f_{IN} = 155 MHz (Full Scale = 2.0 V p-p)		−95			−98		dBFS
f_{IN} = 750 MHz		−100			−97		dBFS
f_{IN} = 900 MHz		−94	−80		−96		dBFS
f_{IN} = 1800 MHz		−91			−88	−74	dBFS
f_{IN} = 2100 MHz		−86			−94		dBFS
f_{IN} = 3300 MHz		−85			−85		dBFS
f_{IN} = 4350 MHz (Full Scale = 1.1 V p-p)		−83			−84		dBFS
f_{IN} = 5530 MHz (Full Scale = 1.1 V p-p)		−82			−82		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD), A_{IN1} AND A_{IN2} = −8.0 dBFS							
f_{IN1} = 1841 MHz, f_{IN2} = 1846 MHz		−72			−72		dBFS
f_{IN1} = 2137 MHz, f_{IN2} = 2142 MHz		−74			−76		dBFS
CROSSTALK[6]		>90			>90		dB
ANALOG INPUT BANDWIDTH, FULL POWER[7]		5			5		GHz

[1] The junction temperature (T_J) range of −10°C to +120°C translates to an ambient temperature (T_A) range of −40°C to +85°C.
[2] See AN-835 for definitions and for details on how these tests were completed.
[3] Noise density is measured at a low analog input frequency (30 MHz).
[4] The input configuration component values are found in Table 9. Refer to Table 10 for the recommended buffer settings.
[5] Figure 79 shows the differential transformer coupled configuration. Figure 80 is the input network configuration for frequencies > 5 GHz.
[6] Crosstalk is measured at 950 MHz with a −2.0 dBFS analog input on one channel, and no input on the adjacent channel.
[7] Full power bandwidth is the bandwidth of operation in which proper ADC performance can be achieved.

DIGITAL SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.9 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.9 V, SPIVDD = 1.9 V, −10°C ≤ T_J ≤ +120°C,[1] unless otherwise noted. Typical specifications represent performance at T_J = 70°C (T_A = 25°C).

Table 3.

Parameter	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)				
Logic Compliance		LVDS/LVPECL		
Differential Input Voltage	300	800	1800	mV p-p
Input Common-Mode Voltage		0.675		V
Input Resistance (Differential)		106		Ω
Input Capacitance		0.9		pF
Differential Input Return Loss at 2.6 GHz[2]		9.4		dB
SYSTEM REFERENCE (SYSREF) INPUTS (SYSREF+, SYSREF−)				
Logic Compliance		LVDS/LVPECL		
Differential Input Voltage	400	800	1800	mV p-p
Input Common-Mode Voltage		0.675	2.0	V
Input Resistance (Differential)		18		kΩ
Input Capacitance (Differential)		1		pF
LOGIC INPUTS (SDIO, SCLK, CSB, PDWN/STBY, FD_A/GPIO_A0, FD_B/GPIO_B0, GPIO_A1, GPIO_B1)				
Logic Compliance		CMOS		
Logic 1 Voltage	0.65 × SPIVDD			V
Logic 0 Voltage	0		0.35 × SPIVDD	V
Input Resistance		30		kΩ
LOGIC OUTPUTS (SDIO, FD_A, FD_B)				
Logic Compliance		CMOS		
Logic 1 Voltage (I_{OH} = 4 mA)	SPIVDD − 0.45V			V
Logic 0 Voltage (I_{OL} = 4 mA)	0		0.45	V
SYNCHRONIZATION INPUT (SYNCINB+/SYNCINB−)				
Logic Compliance		LVDS/LVPECL		
Differential Input Voltage	400	800	1800	mV p-p
Input Common-Mode Voltage		0.675	2.0	V
Input Resistance (Differential)		18		kΩ
Input Capacitance		1		pF
SYNCINB+ INPUT				
Logic Compliance		CMOS		
Logic 1 Voltage	0.9 × DRVDD1		2 × DRVDD1	V
Logic 0 Voltage			0.1 × DRVDD1	V
Input Resistance		2.6		kΩ
DIGITAL OUTPUTS (SERDOUTx±, x = 0 TO 7)				
Logic Compliance		SST		
Differential Output Voltage	360	560	770	mV p-p
Differential Termination Impedance	80	100	120	Ω

[1] The junction temperature (T_J) range of −10°C to +120°C translates to an ambient temperature (T_A) range of −40°C to +85°C.
[2] Reference impedance = 100 Ω.

SWITCHING SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.9 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.9 V, SPIVDD = 1.9 V, default SPI settings, −10°C ≤ T_J ≤ +120°C,[1] unless otherwise noted. Typical specifications represent performance at T_J = 70°C (T_A = 25°C).

Table 4.

	2.0 GSPS			2.6 GSPS			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK							
Clock Rate at CLK+/CLK− Pins			6			6	GHz
Sample Rate[2]	1200	2000	2100	1900	2600	2700	MSPS
Clock Pulse Width High	238.096			185.185			ps
Clock Pulse Width Low	238.096			185.185			ps
OUTPUT PARAMETERS							
Unit Interval (UI)[3]	62.5	66.67	592.6	62.5	66.67	592.6	ps
Rise Time (t_R) (20% to 80% into 100 Ω Load)		26			26		ps
Fall Time (t_F) (20% to 80% into 100 Ω Load)		26			26		ps
Phase-Locked Loop (PLL) Lock Time		5			5		ms
Data Rate per Channel (Nonreturn to Zero)[4]	1.6875	13	16	1.6875	13	16	Gbps
LATENCY[5]							
Pipeline Latency[6]		75			75		Clock cycles
Fast Detect Latency		26			26		Clock cycles
NCO Channel Selection to Output			8			8	Clock cycles
WAKE-UP TIME							
Standby		400			400		µs
Power-Down		15			15		ms
APERTURE							
Delay (t_A)		250			250		ps
Uncertainty (Jitter, t_J)		55			55		fs rms
Out of Range Recovery Time		1			1		Clock cycles

[1] The junction temperature (T_J) range of −10°C to +120°C translates to an ambient temperature (T_A) range of −40°C to +85°C.
[2] The maximum sample rate is the clock rate after the divider.
[3] Baud rate = 1/UI. A subset of this range can be supported.
[4] Default L = 8. This number can be changed based on the sample rate and decimation ratio.
[5] No DDCs used. L = 8, M = 2, and F = 1.
[6] Refer to the Latency section for more details.

TIMING SPECIFICATIONS

Table 5.

Parameter	Description	Min	Typ	Max	Unit
CLK+ to SYSREF+ TIMING REQUIREMENTS					
t_{SU_SR}	Device clock to SYSREF+ setup time		−65		ps
t_{H_SR}	Device clock to SYSREF+ hold time		95		ps
SPI TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK} for SPI Reads	Period of the SCLK	20			ns
t_{CLK} for SPI Writes	Period of the SCLK	10			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH} for SPI Reads	Minimum period that SCLK must be in a logic high state	8			ns
t_{HIGH} for SPI Writes	Minimum period that SCLK must be in a logic high state	4			ns
t_{LOW} for SPI Reads	Minimum period that SCLK must be in a logic low state	8			ns
t_{LOW} for SPI Writes	Minimum period that SCLK must be in a logic low state	4			ns
t_{ACCESS}	Maximum time delay between the falling edge of SCLK and output data valid for a read operation		5	8	ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input, relative to the SCLK rising edge (not shown in Figure 4)	2			ns

Timing Diagrams

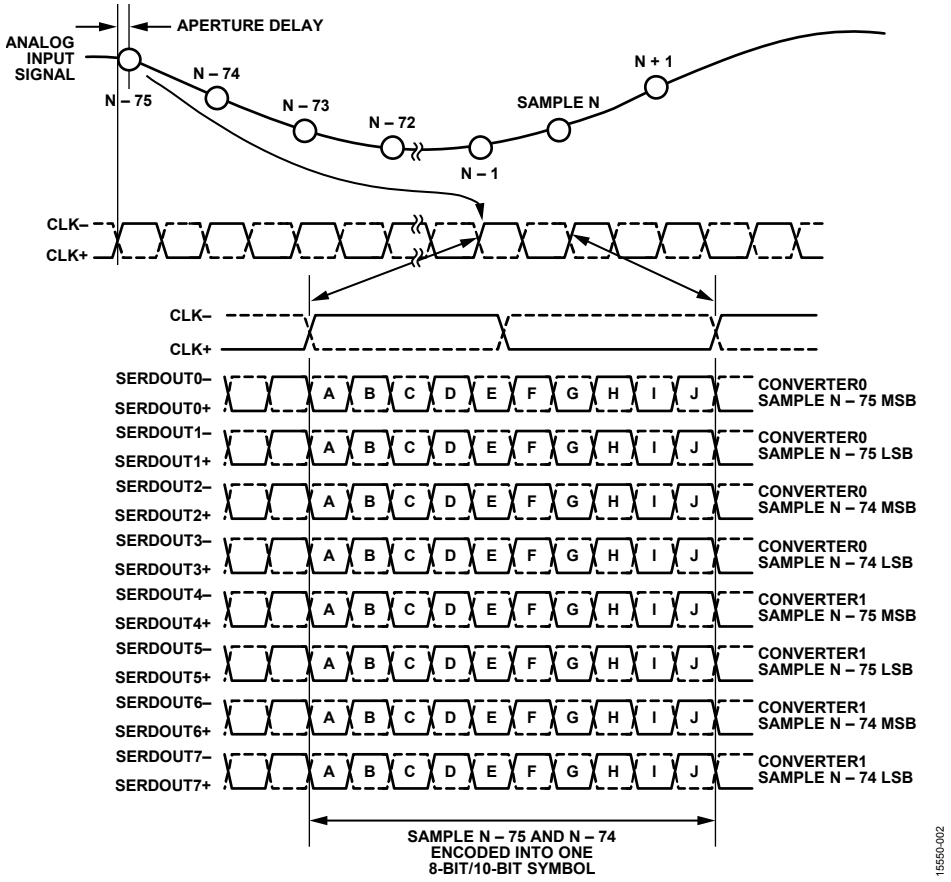

Figure 2. Data Output Timing Diagram

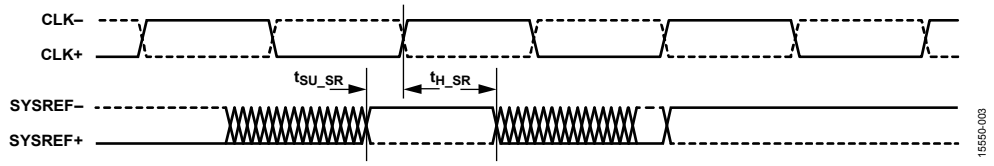

Figure 3. CLK+ to SYSREF+ Setup and Hold Timing Diagram

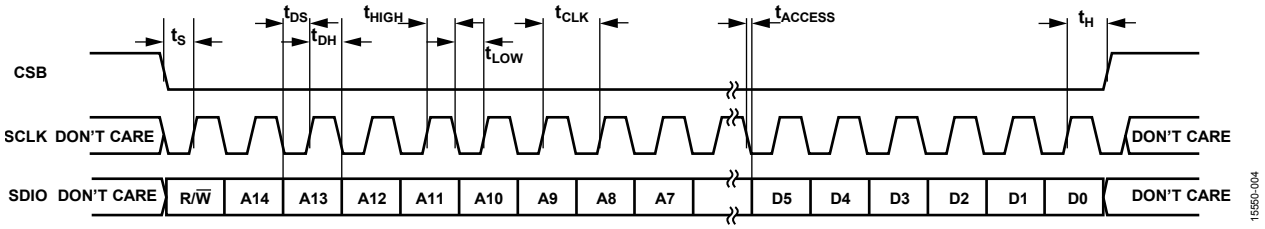

Figure 4. SPI Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD1 to AGND	1.05 V
AVDD1_SR to AGND	1.05 V
AVDD2 to AGND	2.0 V
AVDD3 to AGND	2.70 V
DVDD to DGND	1.05 V
DRVDD1 to DRGND	1.05 V
DRVDD2 to DRGND	2.0 V
SPIVDD to DGND	2.0 V
AGND to DRGND	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
DGND to DRGND	−0.3 V to +0.3 V
VIN±x to AGND	AGND − 0.3 V to AVDD3 + 0.3 V
CLK± to AGND	AGND − 0.3 V to AVDD1 + 0.3 V
SCLK, SDIO, CSB to DGND	DGND − 0.3 V to SPIVDD + 0.3 V
PDWN/STBY to DGND	DGND − 0.3 V to SPIVDD + 0.3 V
SYSREF± to AGND	2.5 V
SYNCINB± to DRGND	2.5 V
Junction Temperature Range (T_J)	−40°C to +125°C
Storage Temperature Range, Ambient (T_A)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required. θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC_TOP}	Ψ_{JB}	Unit
BP-196-4[1]	16.26	1.4	5.44	°C/W

[1] Test Condition 1: Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with 190 thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	AVDD2	AVDD2	AVDD1	AVDD1[1]	AVDD1[1]	AGND[1]	CLK+	CLK–	AGND[1]	AVDD1[1]	AVDD1[1]	AVDD1	AVDD2	AVDD2
B	AVDD2	AVDD2	AVDD1	AVDD1[1]	AGND	AGND[1]	AGND[1]	AGND[1]	AGND[1]	AGND	AVDD1[1]	AVDD1	AVDD2	AVDD2
C	AVDD2	AVDD2	AVDD1	AGND	AGND	AGND[1]	AGND[1]	AGND[1]	AGND[1]	AGND	AGND	AVDD1	AVDD2	AVDD2
D	AVDD3	AGND	AGND	AGND	AGND	AGND	AGND[1]	AGND[1]	AGND	AGND	AGND	AGND	AGND	AVDD3
E	VIN–B	AGND	AGND	AGND	AGND	AGND[2]	AVDD1_SR	AGND[2]	AGND	AGND	AGND	AGND	AGND	VIN–A
F	VIN+B	AGND	AGND	AGND	AGND	AGND	SYSREF+	SYSREF–	AGND	AGND	AGND	AGND	AGND	VIN+A
G	AVDD3	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AVDD3
H	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	VREF	AGND	AGND	AGND	AGND
J	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND
K	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]
L	DGND	GPIO_B1	SPIVDD	FD_B/ GPIO_B0	CSB	SCLK	SDIO	PDWN/ STBY	FD_A/ GPIO_A0	SPIVDD	GPIO_A1	DGND	DGND	DGND
M	DGND	DGND	DRGND	DRGND	DRVDD1	DRVDD1	DRVDD1	DRVDD1	DRGND	DRGND	DRVDD1	DRGND	DRVDD2	DVDD
N	DVDD	DVDD	DRGND	SERDOUT7+	SERDOUT6+	SERDOUT5+	SERDOUT4+	SERDOUT3+	SERDOUT2+	SERDOUT1+	SERDOUT0+	DRGND	SYNCINB+	DVDD
P	DVDD	DVDD	DRGND	SERDOUT7–	SERDOUT6–	SERDOUT5–	SERDOUT4–	SERDOUT3–	SERDOUT2–	SERDOUT1–	SERDOUT0–	DRGND	SYNCINB–	DVDD

[1]DENOTES CLOCK DOMAIN.
[2]DENOTES SYSREF± DOMAIN.
[3]DENOTES ISOLATION DOMAIN.

15550-005

Figure 5. Pin Configuration (Top View)

Table 8. Pin Function Descriptions[1]

Pin No.	Mnemonic	Type	Description
Power Supplies			
A3, A12, B3, B12, C3, C12	AVDD1	Power	Analog Power Supply (0.975 V Nominal).
A4, A5, A10, A11, B4, B11	AVDD1[2]	Power	Analog Power Supply for the Clock Domain (0.975 V Nominal).
A1, A2, A13, A14, B1, B2, B13, B14, C1, C2, C13, C14	AVDD2	Power	Analog Power Supply (1.9 V Nominal).
D1, D14, G1, G14	AVDD3	Power	Analog Power Supply (2.5 V Nominal).
E7	AVDD1_SR	Power	Analog Power Supply for SYSREF± (0.975 V Nominal).
L3, L10	SPIVDD	Power	Digital Power Supply for SPI (1.9 V Nominal).
M14, N1, N2, N14, P1, P2, P14	DVDD	Power	Digital Power Supply (0.975 V Nominal).
M5 to M8, M11	DRVDD1	Power	Digital Driver Power Supply (0.975 V Nominal).
M13	DRVDD2	Power	Digital Driver Power Supply (1.9 V Nominal).
B5, B10, C4, C5, C10, C11, D2 to D6, D9 to D13, E2 to E5, E9 to E13, F2 to F6, F9 to F13, G2 to G13, H1 to H9, H11 to H14, J1 to J14	AGND	Ground	Analog Ground. These pins connect to the analog ground plane.
A6, A9, B6 to B9, C6 to C9, D7, D8	AGND[2]	Ground	Ground Reference for the Clock Domain.
E6, E8	AGND[3]	Ground	Ground Reference for SYSREF±.
K1 to K14	AGND[4]	Ground	Isolation Ground.
L1, L12 to L14, M1, M2	DGND	Ground	Digital Control Ground Supply. These pins connect to the digital ground plane.
M3, M4, M9, M10, M12, N3, N12, P3, P12	DRGND	Ground	Digital Driver Ground Supply. These pins connect to the digital driver ground plane.
Analog			
E1, F1	VIN−B, VIN+B	Input	ADC B Analog Input Complement/True.
E14, F14	VIN−A, VIN+A	Input	ADC A Analog Input Complement/True.
A7, A8	CLK+, CLK−	Input	Clock Input True/Complement.
H10	VREF	Input/output/ do not connect (DNC)	0.50 V Reference Voltage Input/Do Not Connect. This pin is configurable through the SPI as a no connect or an input. Do not connect this pin if using the internal reference. This pin requires a 0.50 V reference voltage input if using an external voltage reference source.
CMOS Inputs/Outputs			
L2	GPIO_B1	Input/output	GPIO B1.
L4	FD_B/GPIO_B0	Input/output	Fast Detect Outputs for Channel B/GPIO B0.
L9	FD_A/GPIO_A0	Input/output	Fast Detect Outputs for Channel A/GPIO A0.
L11	GPIO_A1	Input/output	GPIO A1.
Digital Inputs			
F7, F8	SYSREF+, SYSREF−	Input	Active High JESD204B LVDS System Reference Input True/Complement.
N13	SYNCINB+	Input	Active Low JESD204B LVDS/CMOS Sync Input True.
P13	SYNCINB−	Input	Active Low JESD204B LVDS Sync Input Complement.
Data Outputs			
N4, P4	SERDOUT7+, SERDOUT7−	Output	Lane 7 Output Data True/Complement.
N5, P5	SERDOUT6+, SERDOUT6−	Output	Lane 6 Output Data True/Complement.
N6, P6	SERDOUT5+, SERDOUT5−	Output	Lane 5 Output Data True/Complement.
N7, P7	SERDOUT4+, SERDOUT4−	Output	Lane 4 Output Data True/Complement.
N8, P8	SERDOUT3+, SERDOUT3−	Output	Lane 3 Output Data True/Complement.
N9, P9	SERDOUT2+, SERDOUT2−	Output	Lane 2 Output Data True/Complement.
N10, P10	SERDOUT1+, SERDOUT1−	Output	Lane 1 Output Data True/Complement.
N11, P11	SERDOUT0+, SERDOUT0−	Output	Lane 0 Output Data True/Complement.

Pin No.	Mnemonic	Type	Description
Digital Controls			
L5	CSB	Input	SPI Chip Select (Active Low).
L6	SCLK	Input	SPI Serial Clock.
L7	SDIO	Input/output	SPI Serial Data Input/Output.
L8	PDWN/STBY	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby.

[1] See the Theory of Operation section and the Applications Information section for more information on isolating the planes for optimal performance.
[2] Denotes clock domain.
[3] Denotes SYSREF± domain.
[4] Denotes isolation domain.

TYPICAL PERFORMANCE CHARACTERISTICS

2.0 GSPS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.9 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.9 V, SPIVDD = 1.9 V, sampling rate = 2.0 GHz, clock divider = 2, 1.7 V p-p full-scale differential input, input amplitude (A_{IN}) = −2.0 dBFS, T_J = 70°C (T_A = 25°C), 128k fast Fourier transform (FFT) sample, unless otherwise noted. See Table 10 for the recommended settings.

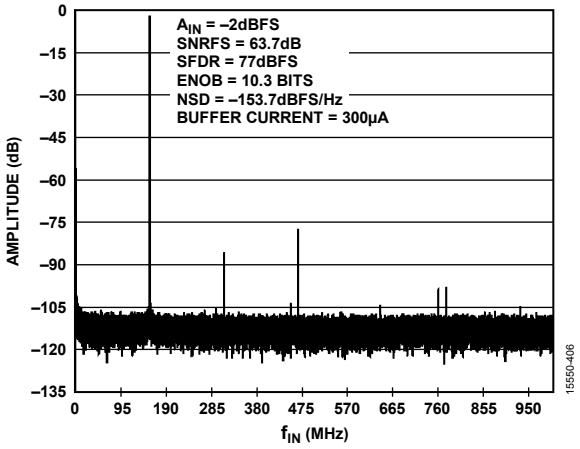

Figure 6. Single-Tone FFT at f_{IN} = 155 MHz

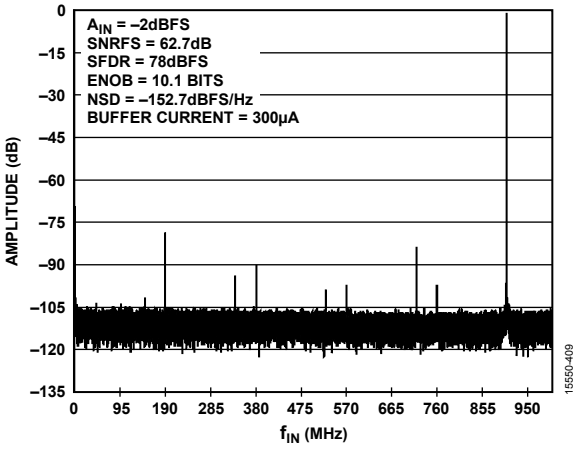

Figure 9. Single-Tone FFT at f_{IN} = 905 MHz

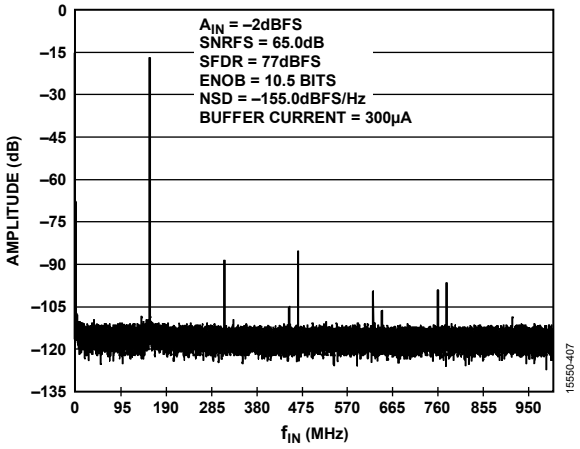

Figure 7. Single-Tone FFT at f_{IN} = 155 MHz, Full-Scale Voltage = 2.04 V p-p

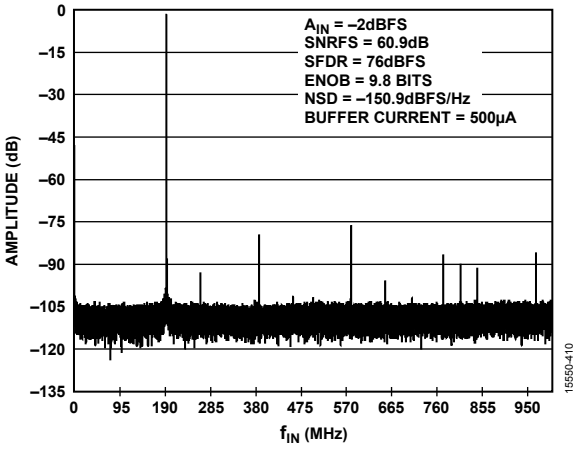

Figure 10. Single-Tone FFT at f_{IN} = 1807 MHz

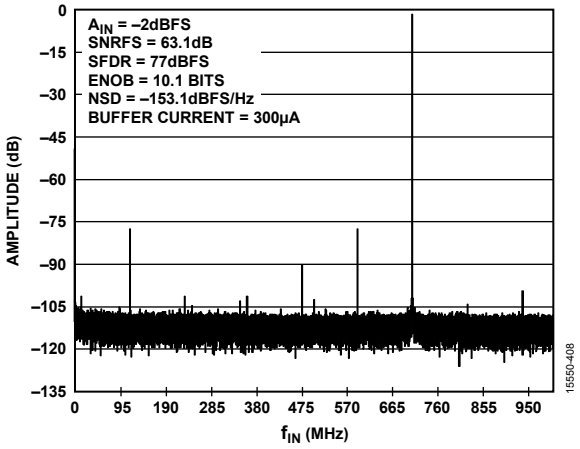

Figure 8. Single-Tone FFT at f_{IN} = 750 MHz

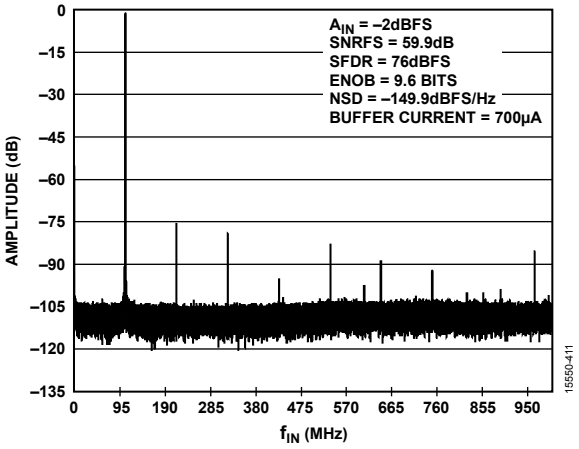

Figure 11. Single-Tone FFT at f_{IN} = 2100 MHz

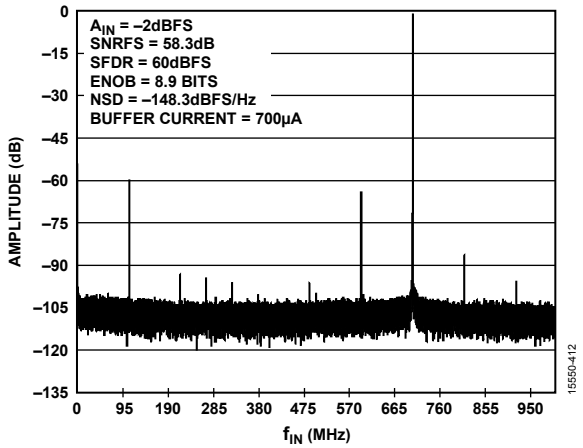

Figure 12. Single-Tone FFT at f_{IN} = 3300 MHz

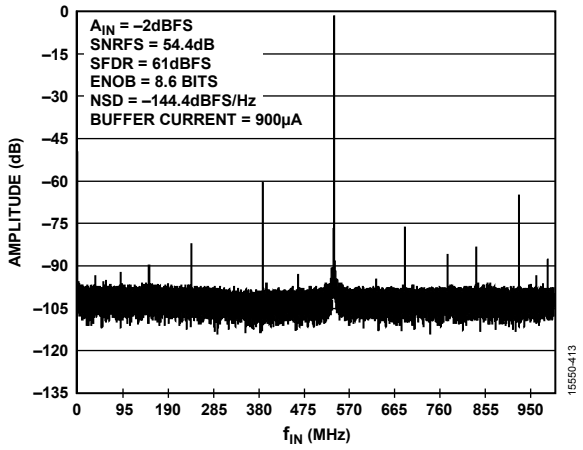

Figure 13. Single-Tone FFT at f_{IN} = 4350 MHz; Full-Scale Voltage = 1.1 V p-p

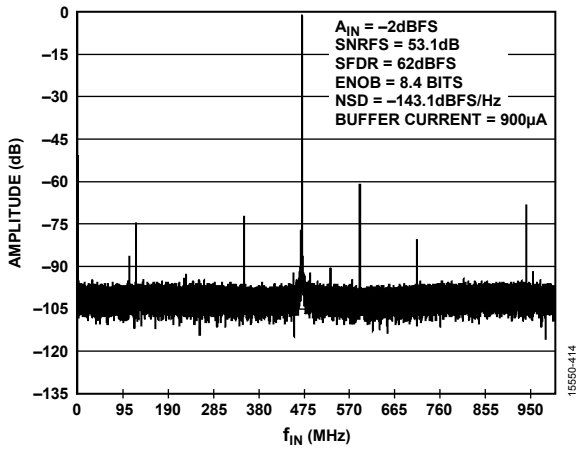

Figure 14. Single-Tone FFT at f_{IN} = 5400 MHz; Full-Scale Voltage = 1.1 V p-p

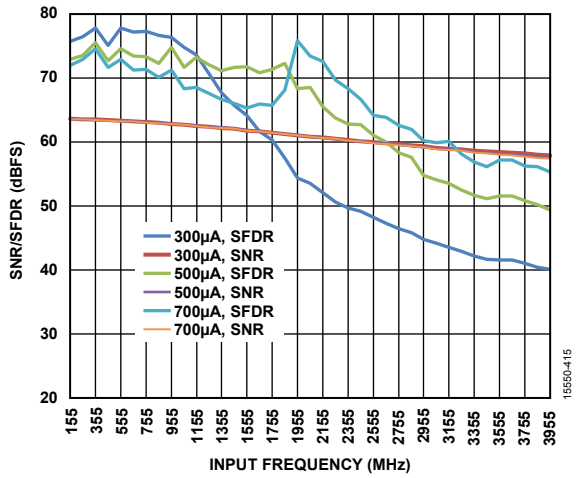

Figure 15. SNR/SFDR vs. Input Frequency (f_{IN}) for Various Buffer Currents

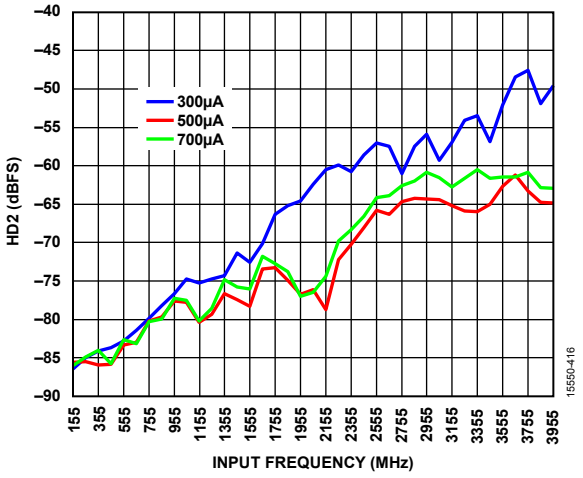

Figure 16. HD2 vs. Input Frequency (f_{IN}) for Various Buffer Currents

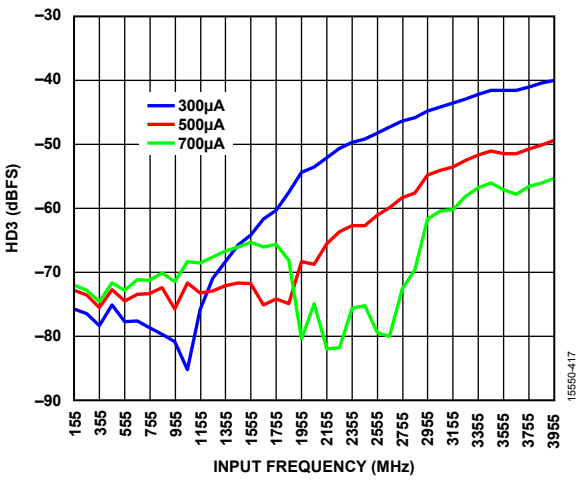

Figure 17. HD3 vs. Input Frequency (f_{IN}) for Various Buffer Currents

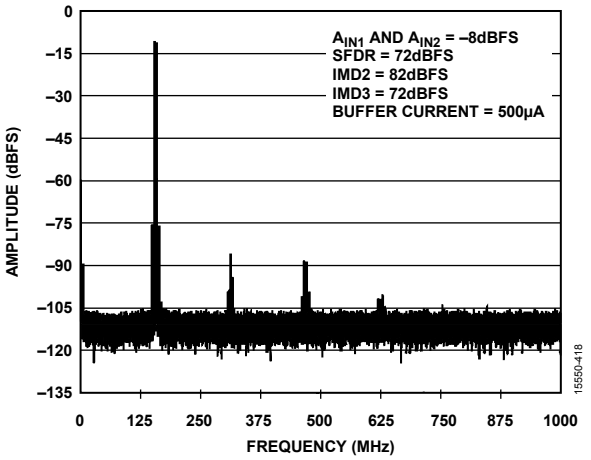

Figure 18. Two-Tone FFT; f_{IN1} = 1841 MHz, f_{IN2} = 1846 MHz; A_{IN1} and A_{IN2} = –8 dBFS

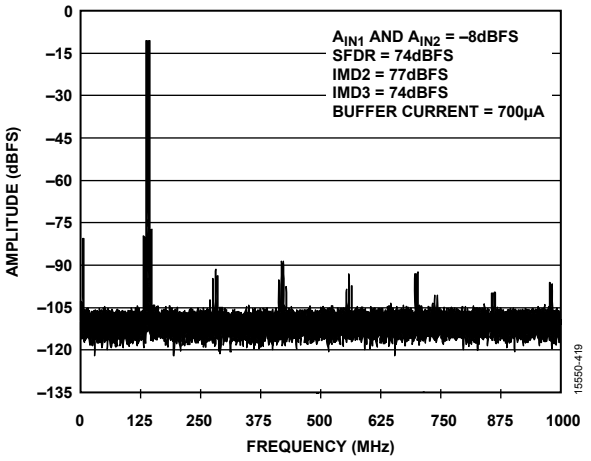

Figure 19. Two-Tone FFT; f_{IN1} = 2137 MHz, f_{IN2} = 2142 MHz; A_{IN1} and A_{IN2} = –8 dBFS

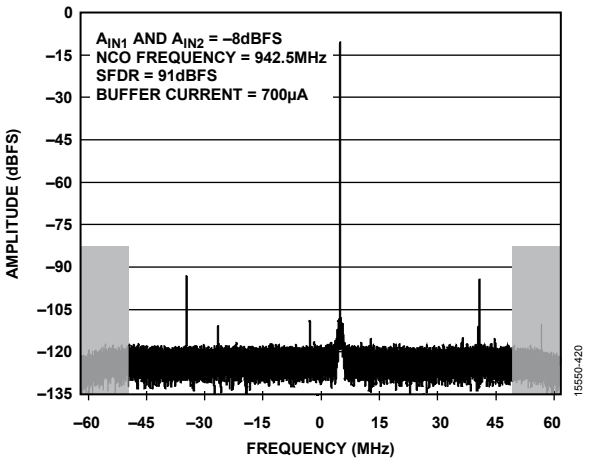

Figure 20. Two-Tone FFT; f_{IN1} = 947.5 MHz, f_{IN2} = 1855.5 MHz f_{CLK} = 1.96608 GHz; Decimation Ratio = 16, NCO Frequency = 942.5 MHz

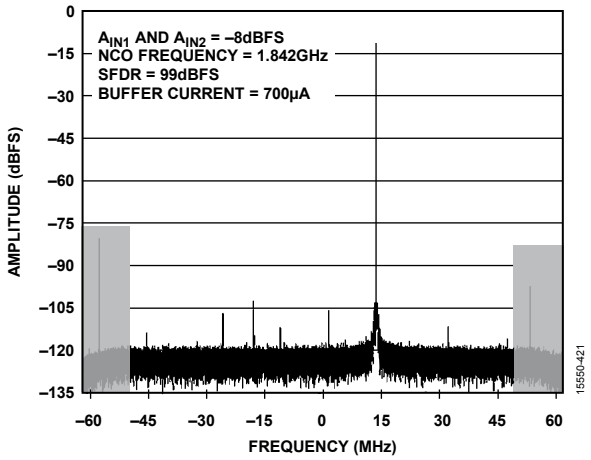

Figure 21. Two-Tone FFT; f_{IN1} = 947.5 MHz, f_{IN2} = 1855.5 MHz f_{CLK} = 1.96608 GHz; Decimation Ratio = 16, NCO Frequency = 1842.5 MHz

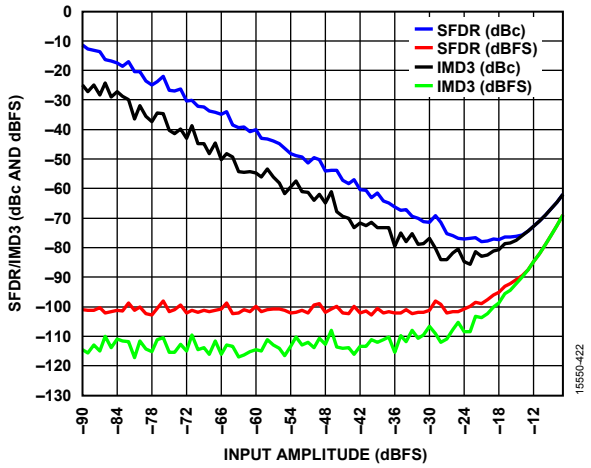

Figure 22. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 1841.5 MHz, f_{IN2} = 1846.5 MHz

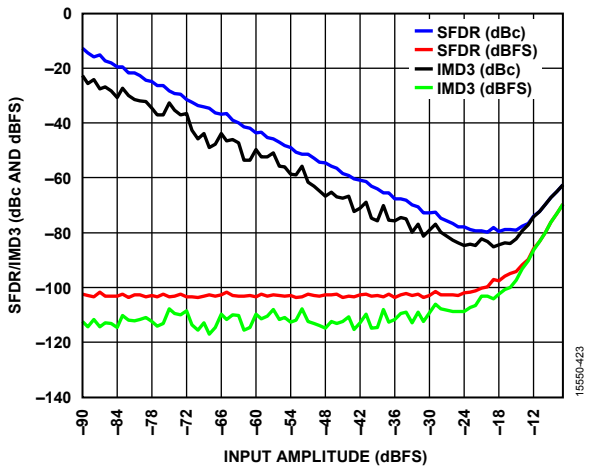

Figure 23. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 2137.5 MHz, f_{IN2} = 2142.5 MHz

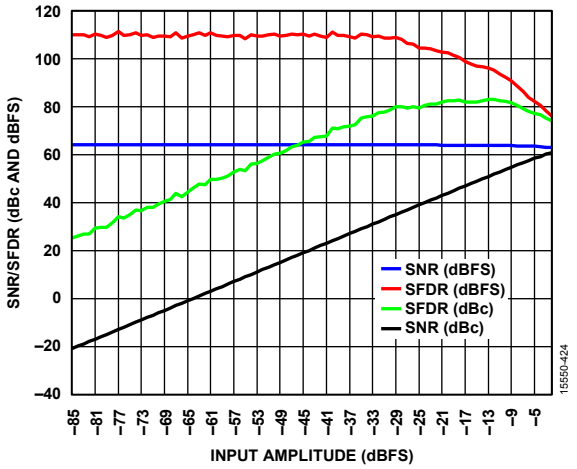

Figure 24. SNR/SFDR vs. Input Amplitude (A_{IN}), f_{IN} = 900 MHz

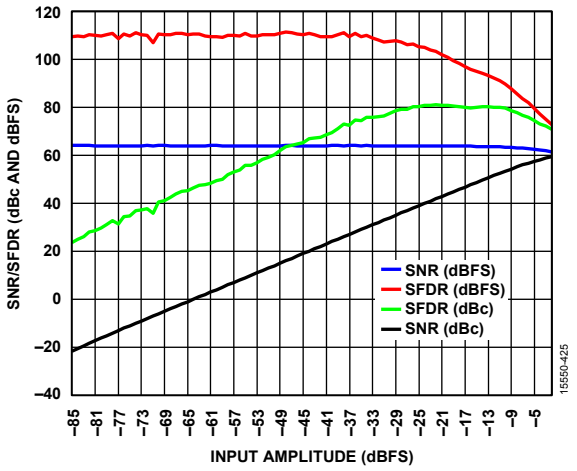

Figure 25. SNR/SFDR vs. Input Amplitude (A_{IN}), f_{IN} = 1800 MHz

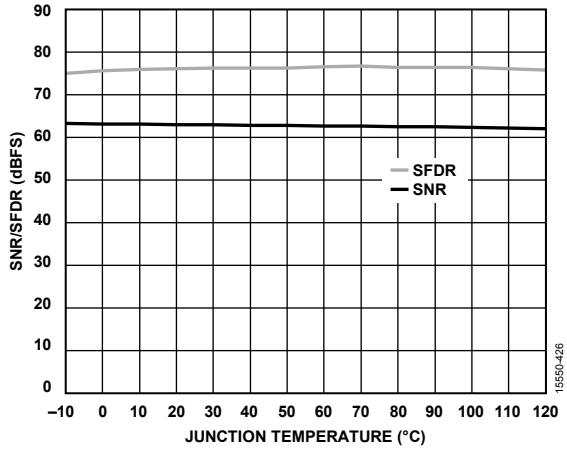

Figure 26. SNR/SFDR vs. Junction Temperature (T_J), f_{IN} = 900 MHz

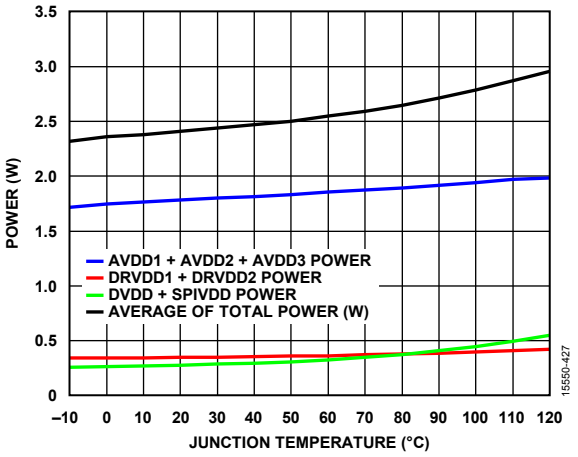

Figure 27. Power vs. Junction Temperature (T_J), f_{IN} = 900 MHz

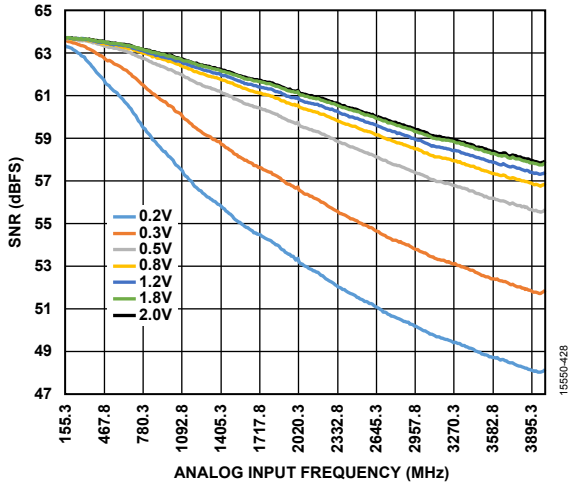

Figure 28. SNR vs. Analog Input Frequency (f_{IN}) for Various Clock Amplitude in Differential Peak-to-Peak Voltages

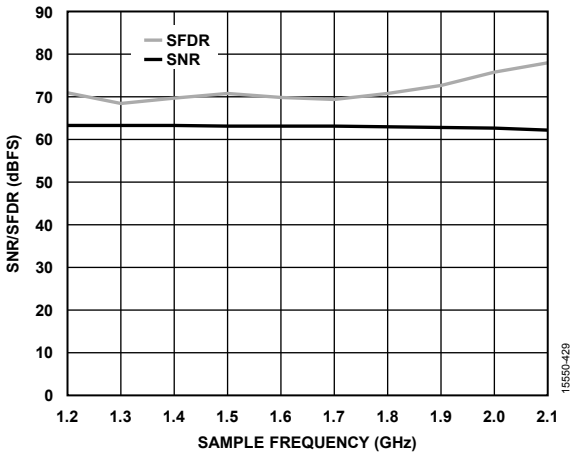

Figure 29. SNR/SFDR vs. Sample Frequency (f_S), f_{IN} = 900 MHz

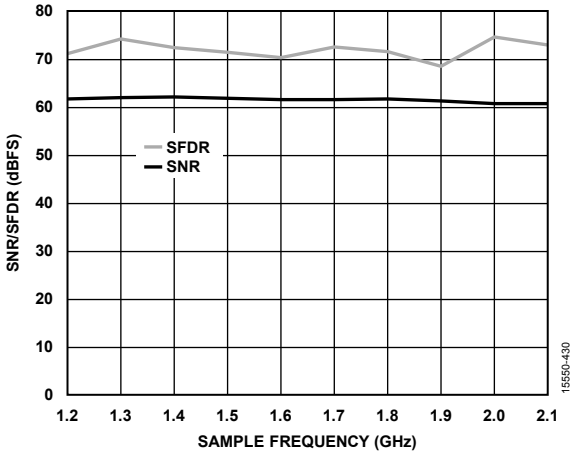

Figure 30. SNR/SFDR vs. Sample Frequency (f_S), f_{IN} = 1.8 GHz

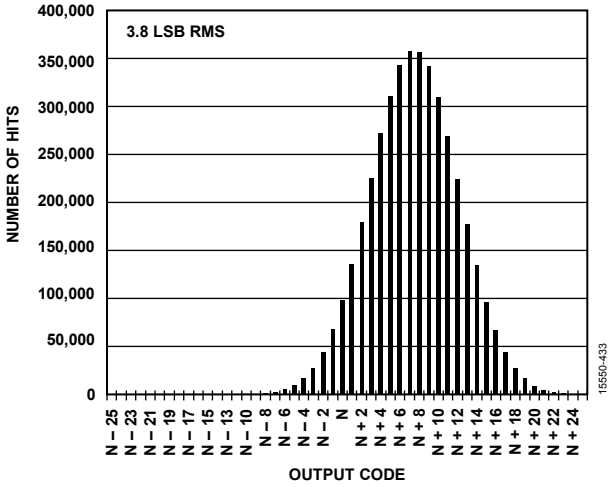

Figure 33. Input Referred Noise Histogram

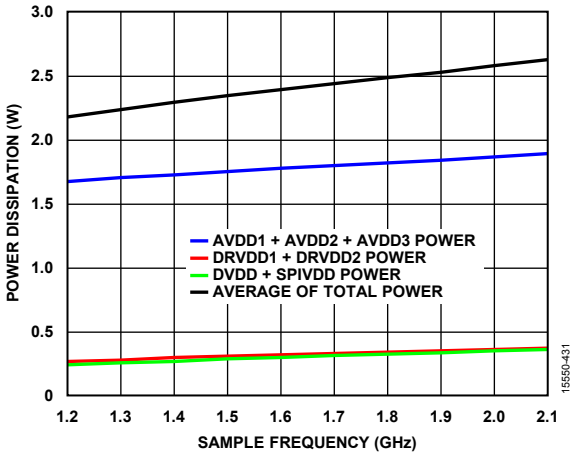

Figure 31. Power Dissipation vs. Sample Frequency (f_S), f_{IN} = 1.8 GHz

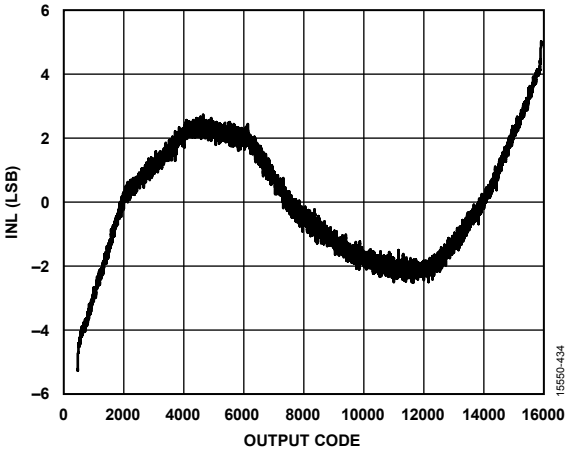

Figure 34. INL, f_{IN} = 155 MHz

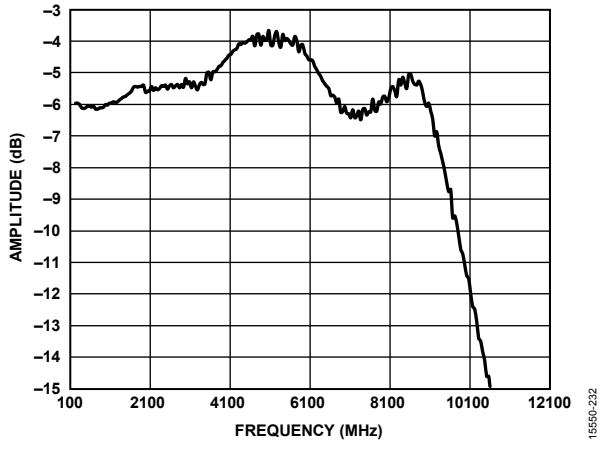

Figure 32. Input Bandwidth (See Figure 80 for the Input Configuration)

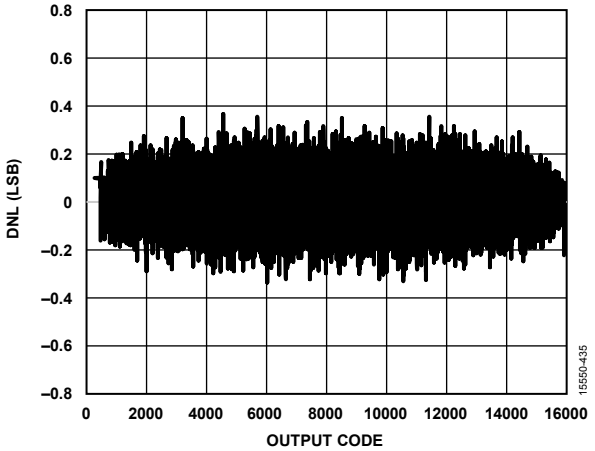

Figure 35. DNL, f_{IN} = 155 MHz

2.6 GSPS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.9 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.9 V, SPIVDD = 1.9 V, sampling rate = 2.56 GHz, clock divider = 2, 1.7 V p-p full-scale differential input, input amplitude (A_{IN}) = −2.0 dBFS, T_J = 70°C (T_A = 25°C), 128 k FFT sample, unless otherwise noted. See Table 10 for the recommended settings.

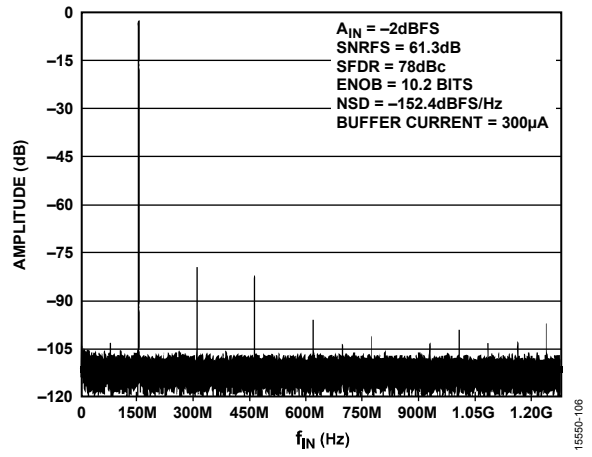

Figure 36. Single-Tone FFT at f_{IN} = 155 MHz

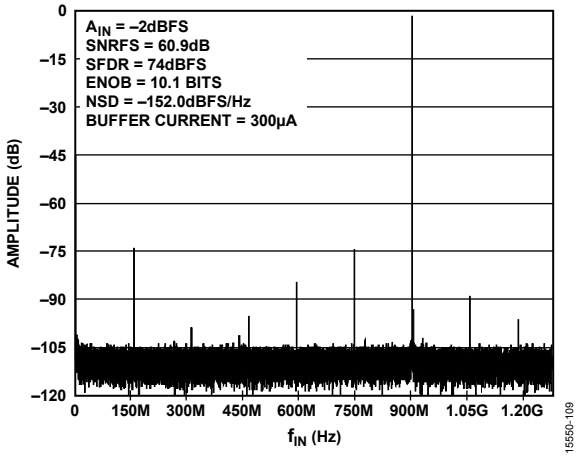

Figure 39. Single-Tone FFT at f_{IN} = 905 MHz

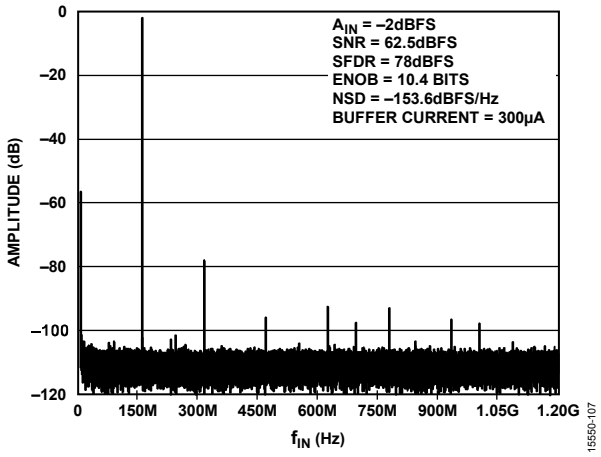

Figure 37. Single-Tone FFT at f_{IN} = 155 MHz, Full-Scale Voltage = 2.04 V p-p

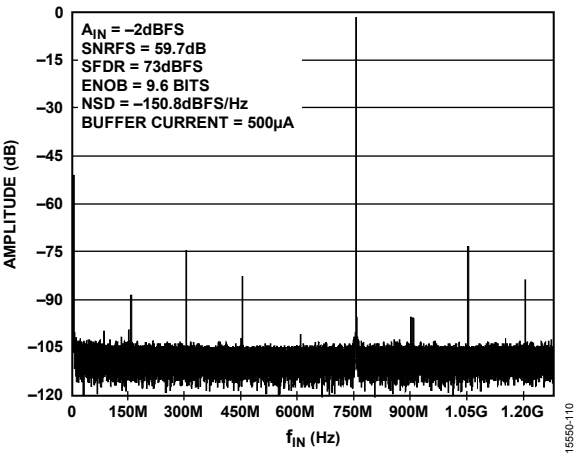

Figure 40. Single-Tone FFT at f_{IN} = 1807 MHz

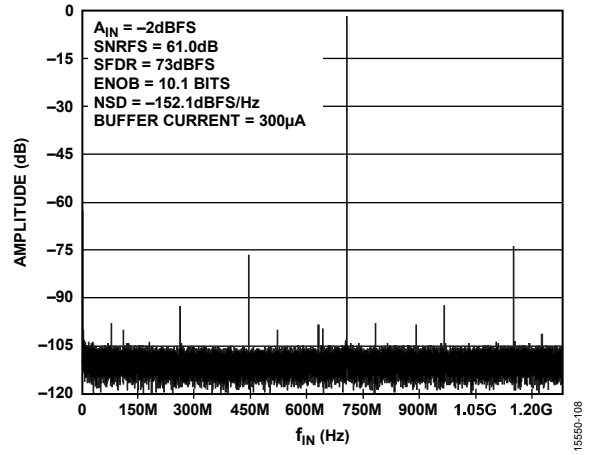

Figure 38. Single-Tone FFT at f_{IN} = 750 MHz

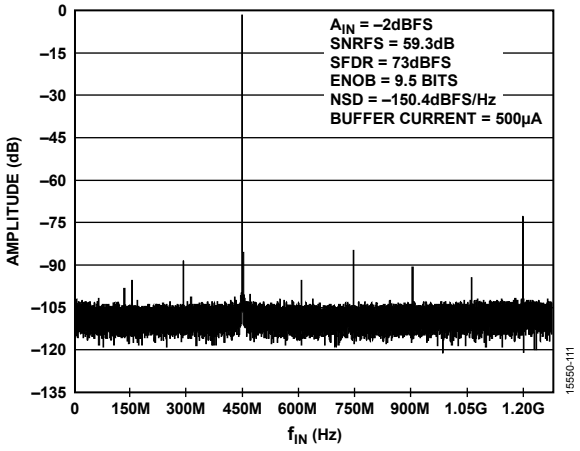

Figure 41. Single-Tone FFT at f_{IN} = 2100 MHz

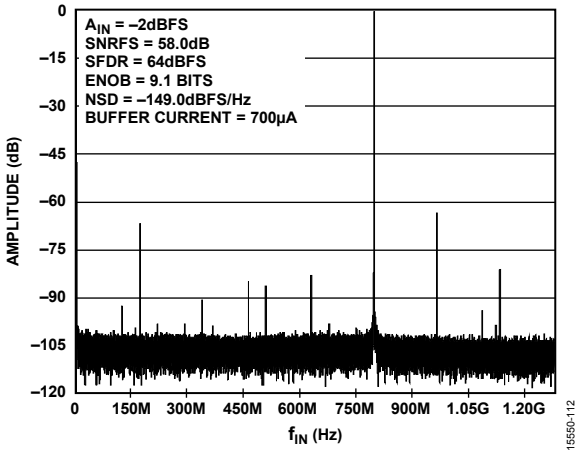

Figure 42. Single-Tone FFT at f_{IN} = 3300 MHz

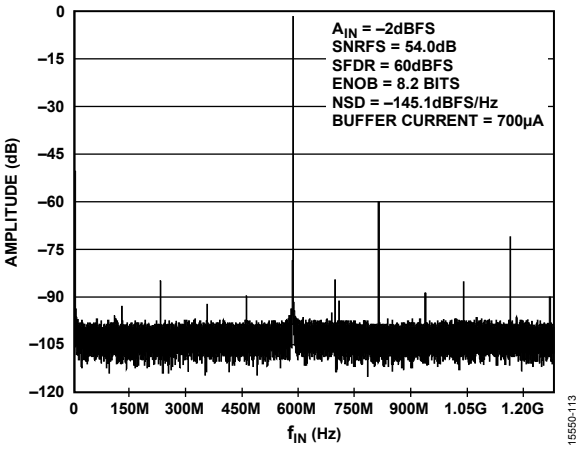

Figure 43. Single-Tone FFT at f_{IN} = 4350 MHz; Full-Scale Voltage = 1.1 V p-p

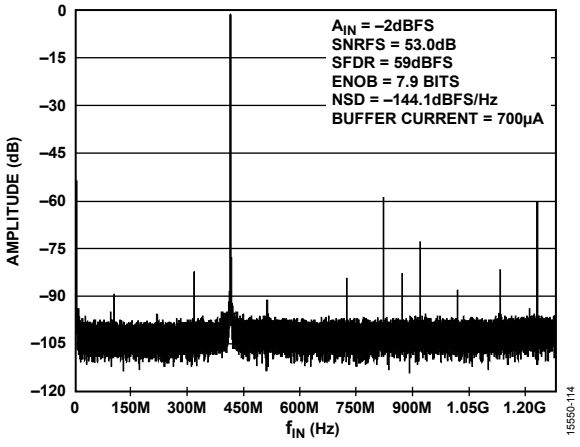

Figure 44. Single-Tone FFT at f_{IN} = 5400 MHz; Full-Scale Voltage = 1.1 V p-p

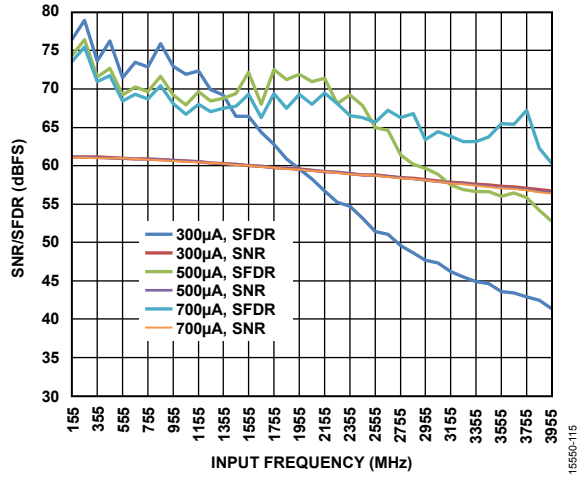

Figure 45. SNR/SFDR vs. Input Frequency (f_{IN}) for Various Buffer Currents

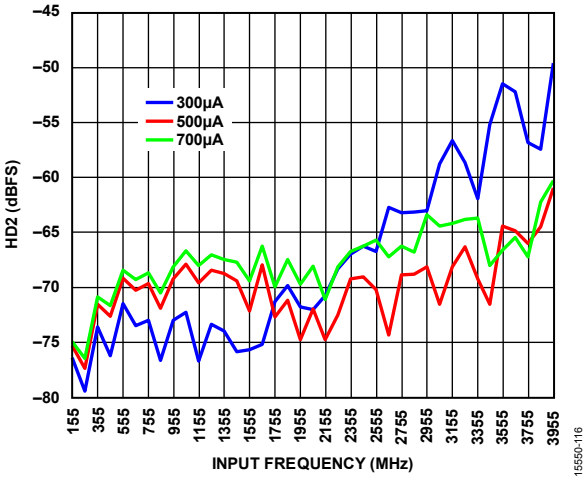

Figure 46. Second Harmonics (HD2) vs. Input Frequency (f_{IN}) for Various Buffer Currents

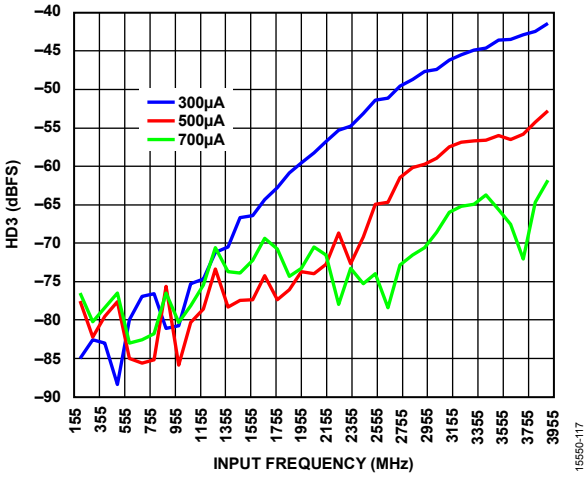

Figure 47. Third Harmonics (HD3) vs. Input Frequency (f_{IN}) for Various Buffer Currents

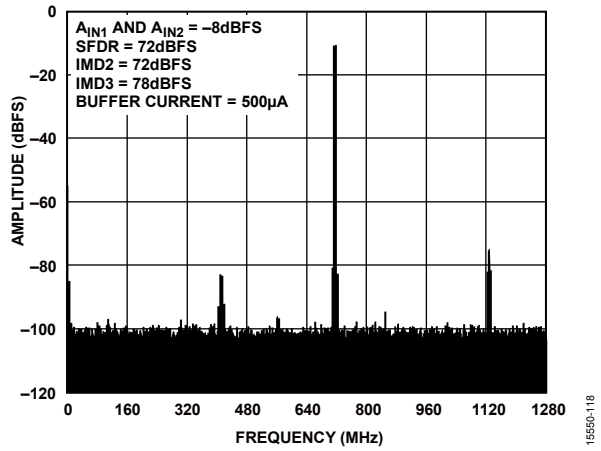

Figure 48. Two-Tone FFT; f_{IN1} = 1841 MHz, f_{IN2} = 1846 MHz; A_{IN1} and A_{IN2} = –8 dBFS

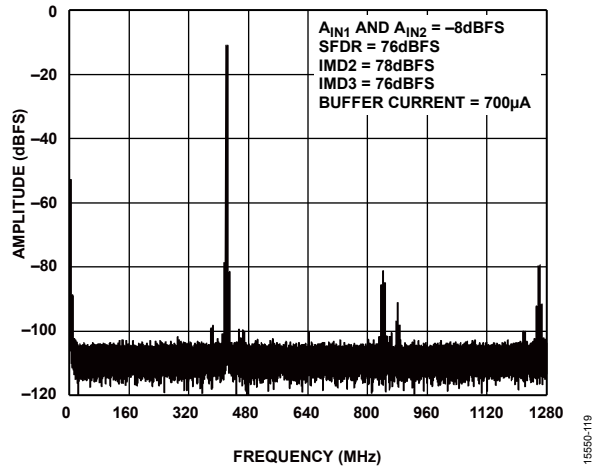

Figure 49. Two-Tone FFT; f_{IN1} = 2137 MHz, f_{IN2} = 2142 MHz; A_{IN1} and A_{IN2} = –8 dBFS

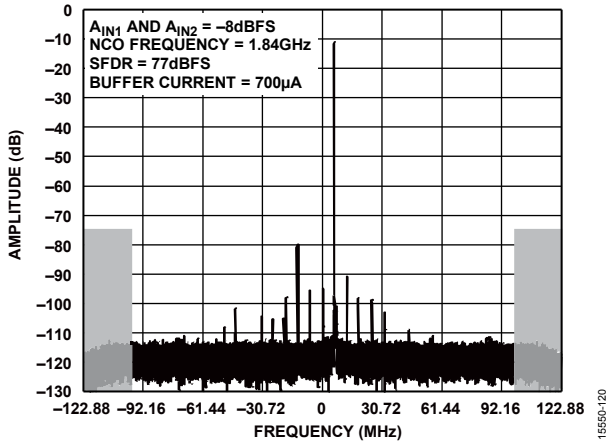

Figure 50. Two-Tone FFT; f_{IN1} = 1846.5 MHz, f_{IN2} = 2142.5 MHz f_{CLK} = 2.4576 GHz; Decimation Ratio = 10, NCO Frequency = 1840 MHz

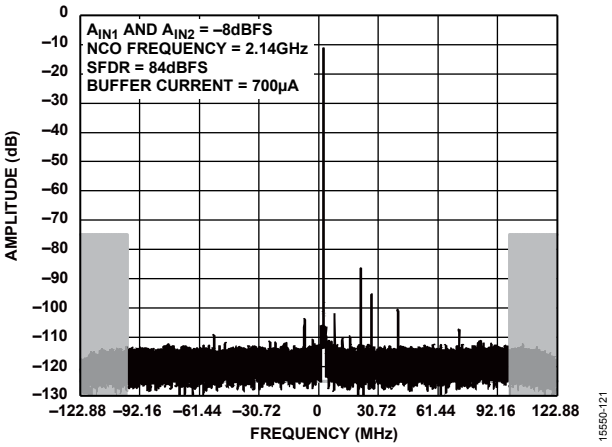

Figure 51. Two-Tone FFT; f_{IN1} = 1846.5 MHz, f_{IN2} = 2142.5 MHz f_{CLK} = 2.4576 GHz; Decimation Ratio = 10, NCO Frequency = 2140 MHz

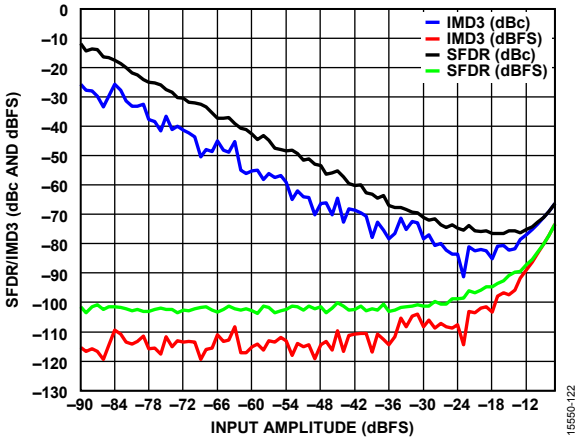

Figure 52. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 1841.5 MHz, f_{IN2} = 1846.5 MHz

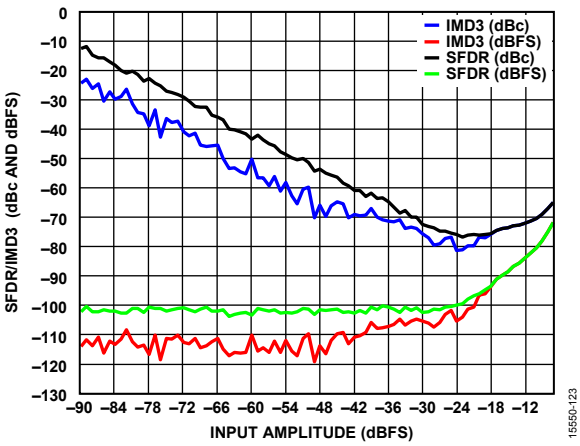

Figure 53. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 2137.5 MHz, f_{IN2} = 2142.5 MHz

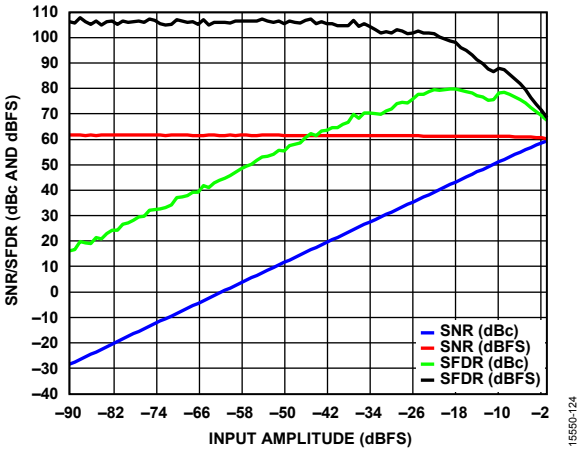

Figure 54. SNR/SFDR vs. Input Amplitude (A_{IN}), f_{IN} = 900 MHz

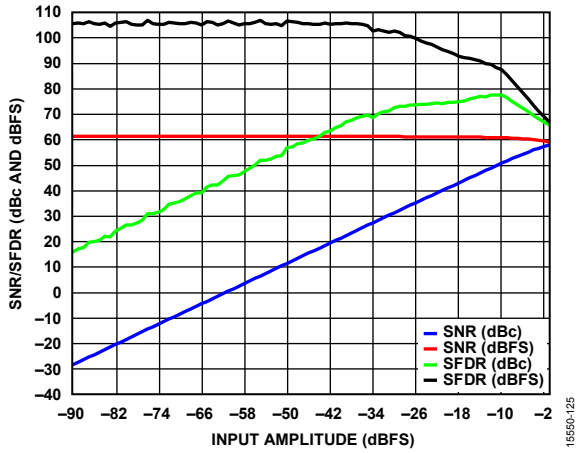

Figure 55. SNR/SFDR vs. Input Amplitude (A_{IN}), f_{IN} = 1800 MHz

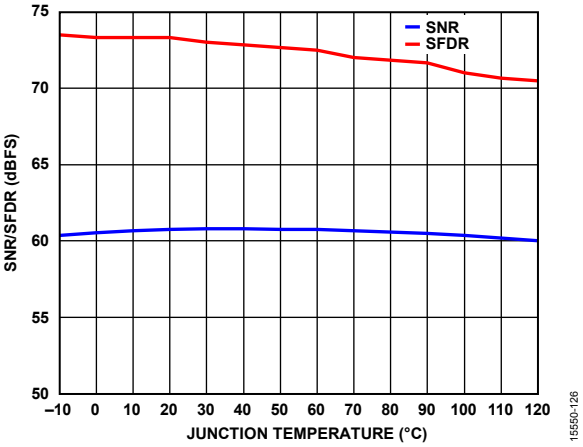

Figure 56. SNR/SFDR vs. Junction Temperature (T_J), f_{IN} = 900 MHz

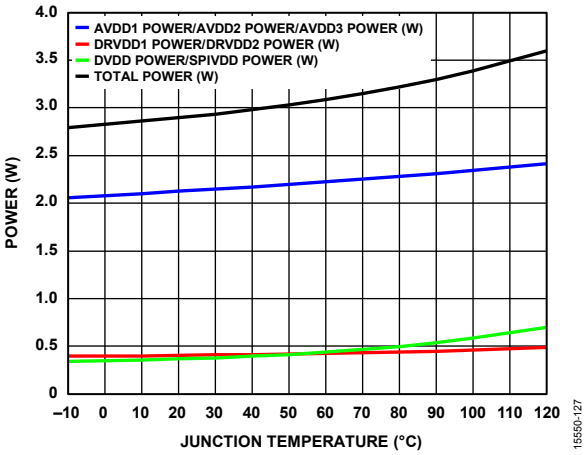

Figure 57. Power vs. Junction Temperature (T_J), f_{IN} = 900 MHz

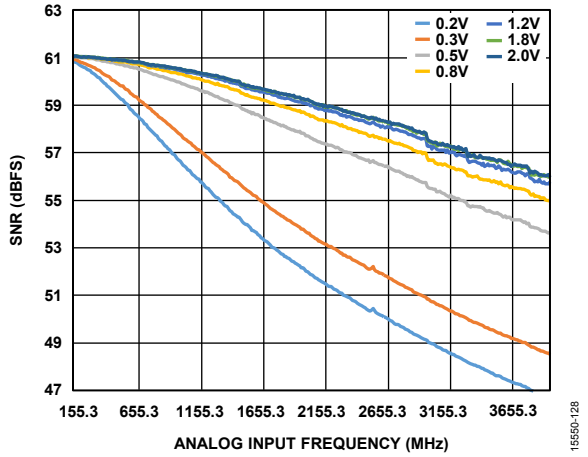

Figure 58. SNR vs. Analog Input Frequency (f_{IN}) for Various Clock Amplitude in Differential Peak-to-Peak Voltages

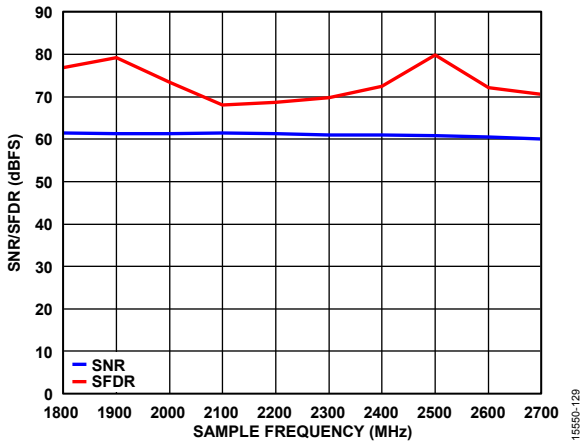

Figure 59. SNR/SFDR vs. Sample Frequency (f_S), f_{IN} = 900 MHz

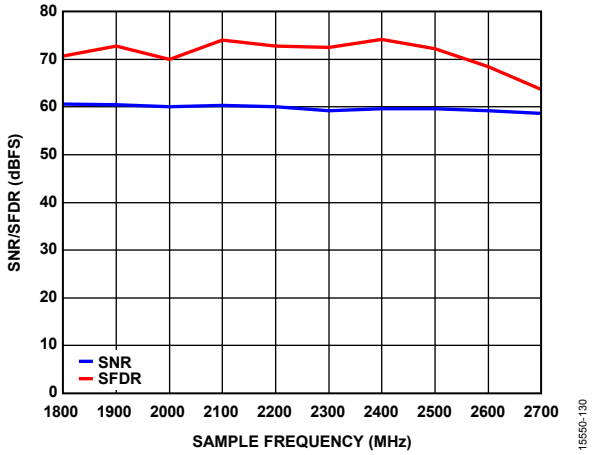

Figure 60. SNR/SFDR vs. Sample Frequency (f_S), f_{IN} = 1.8 GHz

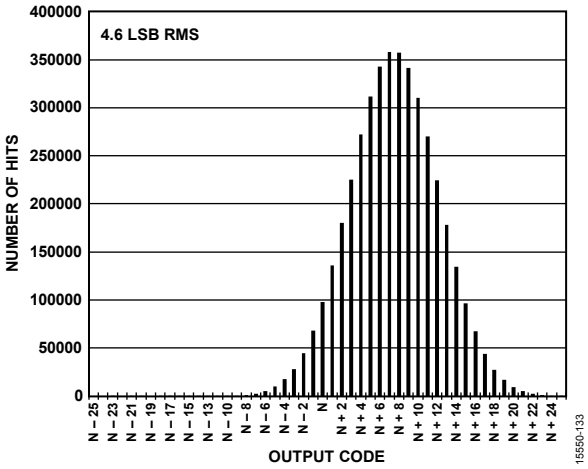

Figure 63. Input Referred Noise Histogram

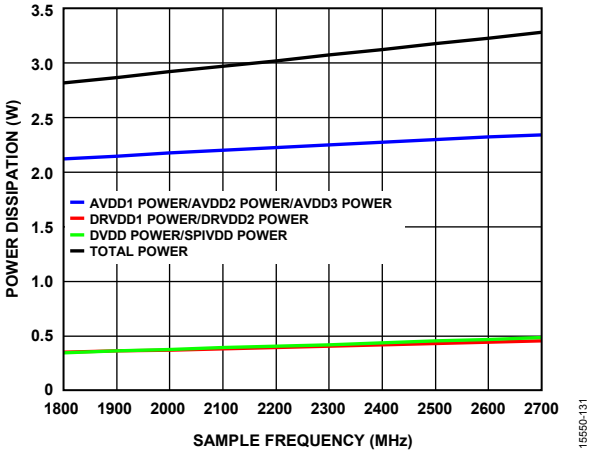

Figure 61. Power Dissipation vs. Sample Frequency (f_S), f_{IN} = 1.8 GHz

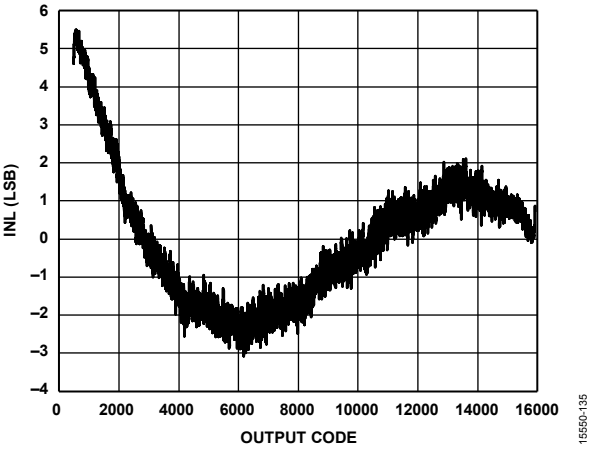

Figure 64. INL, f_{IN} = 155 MHz

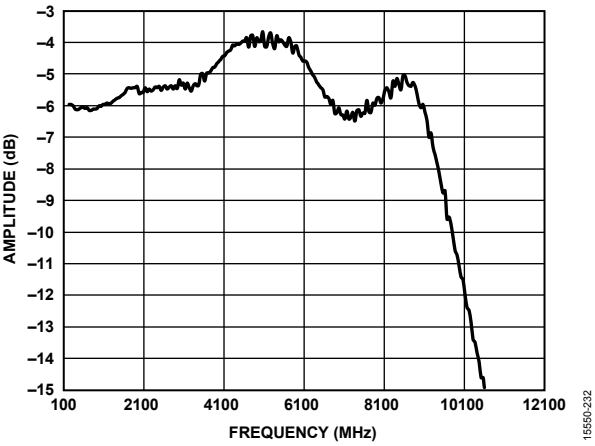

Figure 62. Input Bandwidth (See Figure 80 for the Input Configuration)

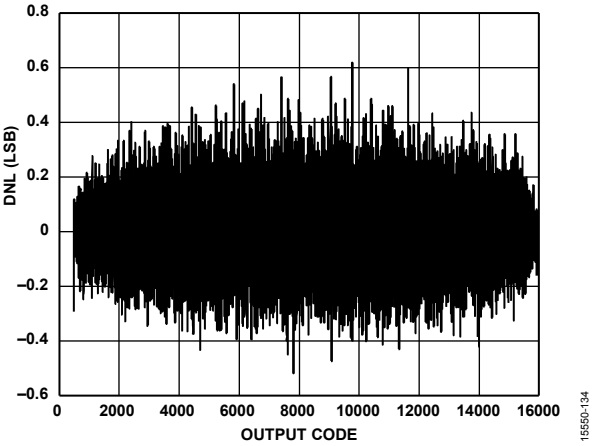

Figure 65. DNL, f_{IN} = 155 MHz