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14-Bit, 1.25 GSPS JESD204B, Dual Analog-to-Digital Converter

Data Sheet **AD9691**

FEATURES

- JESD204B (Subclass 1) coded serial digital outputs
- 1.9 W total power per channel (default settings)
- SFDR = 77 dBFS at 340 MHz
- SNR = 63.4 dBFS at 340 MHz (A_{IN} = −1.0 dBFS)
- Noise density = −152.6 dBFS/Hz
- 1.25 V, 2.50 V, and 3.3 V dc supply operation
- No missing codes
- 1.58 V p-p differential full scale input voltage
- Flexible termination impedance
  - 400 Ω, 200 Ω, 100 Ω, and 50 Ω differential
- 1.5 GHz usable analog input full power bandwidth
- 95 dB channel isolation/crosstalk
- Amplitude detection bits for efficient AGC implementation
- 2 integrated wideband digital processors per channel
  - 12-bit NCO, up to 4 cascaded half-band filters
- Integer clock divide by 1, 2, 4, or 8
- Flexible JESD204B lane configurations
- Timestamp feature
- Small signal dither

APPLICATIONS

- Communications (wideband receivers and digital predistortion)
- Instrumentation (spectrum analyzers, network analyzers, integrated RF test solutions)
- DOCSIS 3.x CMTS upstream receive paths
- High speed data acquisition systems

FUNCTIONAL BLOCK DIAGRAM

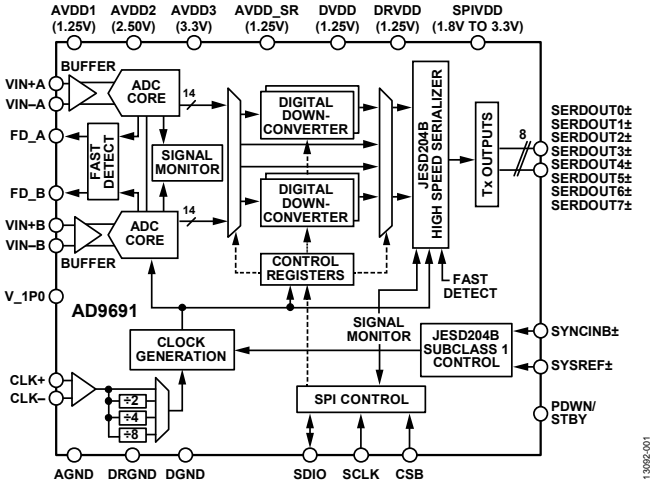

Figure 1.

GENERAL DESCRIPTION

The AD9691 is a dual, 14-bit, 1.25 GSPS analog-to-digital converter (ADC). The device has an on-chip buffer and sample-and-hold circuit designed for low power, small size, and ease of use. The device is designed for sampling wide bandwidth analog signals of up to 1.5 GHz.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

Each ADC data output is internally connected to two digital downconverters (DDCs). Each DDC consists of four cascaded signal processing stages: a 12-bit frequency translator (NCO) and four half-band decimation filters.

In addition to the DDC blocks, the AD9691 has a programmable threshold detector that allows monitoring of the incoming signal power using the fast detect output bits of the ADC. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

Users can configure the Subclass 1 JESD204B-based high speed serialized output in a variety of one-, two-, four- or eight-lane configurations, depending on the DDC configuration and the acceptable lane rate of the receiving logic device. Multiple device synchronization is supported through the SYSREF± input pins.

The AD9691 is available in a Pb-free, 88-lead LFCSP and is specified over the −40°C to +85°C industrial temperature range. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Low power consumption analog core, 14-bit, 1.25 GSPS dual ADC with 1.9 W per channel.
2. Wide full power bandwidth supports intermediate frequency (IF) sampling of signals up to 1.5 GHz.
3. Buffered inputs with programmable input termination eases filter design and implementation.
4. Flexible serial port interface (SPI) controls various product features and functions to meet specific system requirements.
5. Programmable fast overrange detection.
6. 12 mm × 12 mm, 88-lead LFCSP.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 Technical Support

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AD9691* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Data Sheet

- AD9691: 14-Bit, 1.25 GSPS JESD204B, Dual Analog-to-Digital Converter Data Sheet

DESIGN RESOURCES

- AD9691 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9691 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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REVISION HISTORY

7/15—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.50 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate (1250 MSPS), 1.58 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Temperature	Min	Typ	Max	Unit
RESOLUTION	Full	14			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	−0.31	0	+0.31	% FSR
Offset Matching	Full		0	0.3	% FSR
Gain Error	Full	−6	0	+6	% FSR
Gain Matching	Full		1	3.9	% FSR
Differential Nonlinearity (DNL)	Full	−0.8	±0.5	+0.8	LSB
Integral Nonlinearity (INL)	Full	−6.5	±2.6	+6.5	LSB
TEMPERATURE DRIFT					
Offset Error	25°C		−26		ppm/°C
Gain Error	25°C		±9.8		ppm/°C
INTERNAL VOLTAGE REFERENCE					
Voltage	Full		1.0		V
INPUT REFERRED NOISE					
V_{REF} = 1.0 V	25°C		3.53		LSB rms
ANALOG INPUTS					
Differential Input Voltage Range	Full		1.58		V p-p
Common-Mode Voltage (V_{CM})	25°C		2.05		V
Differential Input Capacitance	25°C		1.5		pF
Analog Input Full Power Bandwidth	25°C		2		GHz
POWER SUPPLY					
AVDD1	Full	1.22	1.25	1.28	V
AVDD2	Full	2.44	2.50	2.56	V
AVDD3	Full	3.2	3.3	3.4	V
AVDD1_SR	Full	1.22	1.25	1.28	V
DVDD	Full	1.22	1.25	1.28	V
DRVDD	Full	1.22	1.25	1.28	V
SPIVDD	Full	1.7	1.8	3.4	V
I_{AVDD1}	Full		800	840	mA
I_{AVDD2}	Full		670	770	mA
I_{AVDD3}	Full		125	140	mA
I_{AVDD1_SR}	Full		15	18	mA
I_{DVDD}[1]	Full		250	290	mA
I_{DRVDD}[2]	Full		310	380	mA
I_{SPIVDD}	Full		5	6	mA
POWER CONSUMPTION					
Total Power Dissipation (Including Output Drivers)[1]	Full		3.8		W
Power-Down Dissipation	Full		0.9		mW
Standby[3]	Full		1.5		W

[1] Default mode. No DDCs used. L = 8, M = 2, and F = 1.
[2] All lanes running. Power dissipation on DRVDD changes with the lane rate and number of lanes used.
[3] Standby mode can be controlled by the SPI.

AC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.50 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate (1250 MSPS), 1.58 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
ANALOG INPUT FULL SCALE	Full		1.58		V p-p
NOISE DENSITY[2]	Full		−152.6		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)[3]					
f_{IN} = 10 MHz	25°C		64.6		dBFS
f_{IN} = 170 MHz	Full	60.8	64.2		dBFS
f_{IN} = 340 MHz	25°C		63.4		dBFS
f_{IN} = 450 MHz	25°C		62.9		dBFS
f_{IN} = 750 MHz	25°C		61.7		dBFS
f_{IN} = 985 MHz	25°C		59.7		dBFS
f_{IN} = 1205 MHz	25°C		58.3		dBFS
f_{IN} = 1600 MHz	25°C		56.5		dBFS
f_{IN} = 1950 MHz	25°C		55.1		dBFS
SNR AND DISTORTION RATIO (SINAD)[3]					
f_{IN} = 10 MHz	25°C		64.5		dBFS
f_{IN} = 170 MHz	Full	60.5	64.0		dBFS
f_{IN} = 340 MHz	25°C		63.0		dBFS
f_{IN} = 450 MHz	25°C		62.3		dBFS
f_{IN} = 750 MHz	25°C		61.3		dBFS
f_{IN} = 985 MHz	25°C		59.4		dBFS
f_{IN} = 1205 MHz	25°C		57.5		dBFS
f_{IN} = 1600 MHz	25°C		55.8		dBFS
f_{IN} = 1950 MHz	25°C		54.7		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 10 MHz	25°C		10.4		Bits
f_{IN} = 170 MHz	Full	9.7	10.3		Bits
f_{IN} = 340 MHz	25°C		10.2		Bits
f_{IN} = 450 MHz	25°C		10.1		Bits
f_{IN} = 750 MHz	25°C		9.9		Bits
f_{IN} = 985 MHz	25°C		9.6		Bits
f_{IN} = 1205 MHz	25°C		9.2		Bits
f_{IN} = 1600 MHz	25°C		9.0		Bits
f_{IN} = 1950 MHz	25°C		8.8		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)[3]					
f_{IN} = 10 MHz	25°C		87		dBFS
f_{IN} = 170 MHz	Full	72	79		dBFS
f_{IN} = 340 MHz	25°C		77		dBFS
f_{IN} = 450 MHz	25°C		72		dBFS
f_{IN} = 750 MHz	25°C		73		dBFS
f_{IN} = 985 MHz	25°C		72		dBFS
f_{IN} = 1205 MHz	25°C		66		dBFS
f_{IN} = 1600 MHz	25°C		66		dBFS
f_{IN} = 1950 MHz	25°C		69		dBFS

Parameter[1]	Temperature	Min	Typ	Max	Unit
WORST HARMONIC, SECOND OR THIRD[3]					
f_{IN} = 10 MHz	25°C		−87		dBFS
f_{IN} = 170 MHz	Full		−84	−72	dBFS
f_{IN} = 340 MHz	25°C		−77		dBFS
f_{IN} = 450 MHz	25°C		−72		dBFS
f_{IN} = 750 MHz	25°C		−73		dBFS
f_{IN} = 985 MHz	25°C		−72		dBFS
f_{IN} = 1205 MHz	25°C		−66		dBFS
f_{IN} = 1600 MHz	25°C		−66		dBFS
f_{IN} = 1950 MHz	25°C		−69		dBFS
WORST OTHER, EXCLUDING SECOND OR THIRD HARMONIC[3]					
f_{IN} = 10 MHz	25°C		−93		dBFS
f_{IN} = 170 MHz	Full		−81	−76	dBFS
f_{IN} = 340 MHz	25°C		−79		dBFS
f_{IN} = 450 MHz	25°C		−81		dBFS
f_{IN} = 750 MHz	25°C		−77		dBFS
f_{IN} = 985 MHz	25°C		−76		dBFS
f_{IN} = 1205 MHz	25°C		−72		dBFS
f_{IN} = 1600 MHz	25°C		−72		dBFS
f_{IN} = 1950 MHz	25°C		−73		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD), A_{IN1} AND A_{IN2} = −7 dBFS					
f_{IN1} = 185 MHz, f_{IN2} = 188 MHz, Buffer Current Setting = 3.5×	25°C		82		dBFS
f_{IN1} = 449 MHz, f_{IN2} = 452 MHz, Buffer Current Setting = 6.5×	25°C		78		dBFS
CHANNEL ISOLATION/CROSSTALK[4]	25°C		95		dB
FULL POWER BANDWIDTH[5]	25°C		1.5		GHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Noise density is measured at a low analog input frequency (30 MHz).
[3] See Table 10 for the recommended settings for full-scale voltage and buffer current control.
[4] Crosstalk is measured at 170 MHz with a −1.0 dBFS analog input on one channel and no input on the adjacent channel.
[5] Measured with the circuit shown in Figure 41.

DIGITAL SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.50 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate (1250 MSPS), 1.58 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage	Full	600	1200	1800	mV p-p
Input Common-Mode Voltage	Full		0.85		V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance	Full			2.5	pF
SYSTEM REFERENCE INPUTS (SYSREF+, SYSREF−)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage	Full	400	1200	1800	mV p-p
Input Common-Mode Voltage	Full	0.6	0.85	2.0	V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance (Differential)	Full			2.5	pF

Parameter	Temperature	Min	Typ	Max	Unit
LOGIC INPUTS (SDIO, SCLK, CSB, PDWN/STBY)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage	Full	0.8 × SPIVDD			V
Logic 0 Voltage	Full	0		0.5	V
Input Resistance	Full		30		kΩ
LOGIC OUTPUT (SDIO)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage (I_{OH} = 800 µA)	Full	0.8 × SPIVDD			V
Logic 0 Voltage (I_{OL} = 50 µA)	Full	0		0.5	V
SYNC INPUTS (SYNCINB+, SYNCINB−)					
Logic Compliance	Full		LVDS/LVPECL/CMOS		
Differential Input Voltage	Full	400	1200	1800	mV p-p
Input Common-Mode Voltage	Full	0.6	0.85	2.0	V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance	Full			2.5	pF
LOGIC OUTPUTS (FD_A, FD_B)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage	Full	0.8 × SPIVDD			V
Logic 0 Voltage	Full	0		0.5	V
Input Resistance	Full		30		kΩ
DIGITAL OUTPUTS (SERDOUTx±, x = 0 TO 7)					
Logic Compliance	Full		CML		
Differential Output Voltage	Full	360		770	mV p-p
Output Common-Mode Voltage (V_{CM}), AC-Coupled	25°C	0		1.8	V
Short-Circuit Current (I_{DSHORT})	25°C	−100		+100	mA
Differential Return Loss (RL_{DIFF})[1]	25°C	8			dB
Common-Mode Return Loss (RL_{CM})[1]	25°C	6			dB
Differential Termination Impedance	Full	80	100	120	Ω

[1] Differential and common-mode return loss is measured from 100 MHz to 0.75 MHz × baud rate.

SWITCHING SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.50 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate (1250 MSPS), 1.58 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK					
Clock Rate (at CLK+/CLK− Pins)	Full	0.3		4	GHz
Maximum Sample Rate[1]	Full	1250			MSPS
Minimum Sample Rate[2]	Full	300			MSPS
Clock Pulse Width					
High	Full	400			ps
Low	Full	400			ps
OUTPUT PARAMETERS					
Unit Interval (UI)[3]	Full	320	160		ps
Rise Time (t_R) (20% to 80% into 100 Ω Load)	25°C	24	32		ps
Fall Time (t_F) (20% to 80% into 100 Ω Load)	25°C	24	32		ps
PLL Lock Time	25°C		2		ms
Data Rate per Channel (NRZ)[4]	25°C	3.125	6.25	12.5	Gbps

Parameter	Temperature	Min	Typ	Max	Unit
LATENCY[5]					
Pipeline Latency	Full		55		Clock cycles
Fast Detect Latency	Full			28	Clock cycles
Wake-Up Time[6]					
Standby	25°C		1		ms
Power-Down	25°C			4	ms
APERTURE					
Aperture Delay (t_A)	Full		530		ps
Aperture Uncertainty (Jitter, t_j)	Full		55		fs rms
Out-of-Range Recovery Time	Full		1		Clock cycles

[1] The maximum sample rate is the clock rate after the divider.
[2] The minimum sample rate operates at 300 MSPS with L = 1.
[3] Baud rate = 1/UI. A subset of this range is supported by the AD9691.
[4] Default L = 8. This number can be changed based on the sample rate and decimation ratio.
[5] No DDCs used. L = 8, M = 2, and F = 1.
[6] Wake-up time is the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLK+ to SYSREF+ TIMING REQUIREMENTS	See Figure 2				
t_{SU_SR}	Device clock to SYSREF+ setup time		117		ps
t_{H_SR}	Device clock to SYSREF+ hold time		−96		ps
SPI TIMING REQUIREMENTS	See Figure 3				
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK signal	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK must be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK must be in a logic low state	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 3)	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 3)	10			ns

Timing Diagrams

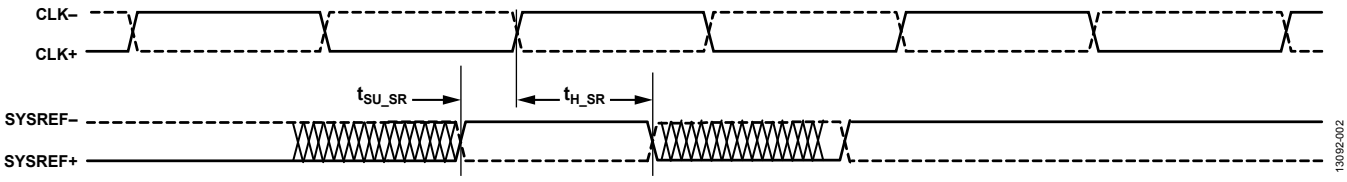


Figure 2. SYSREF+ Setup and Hold Timing Diagram

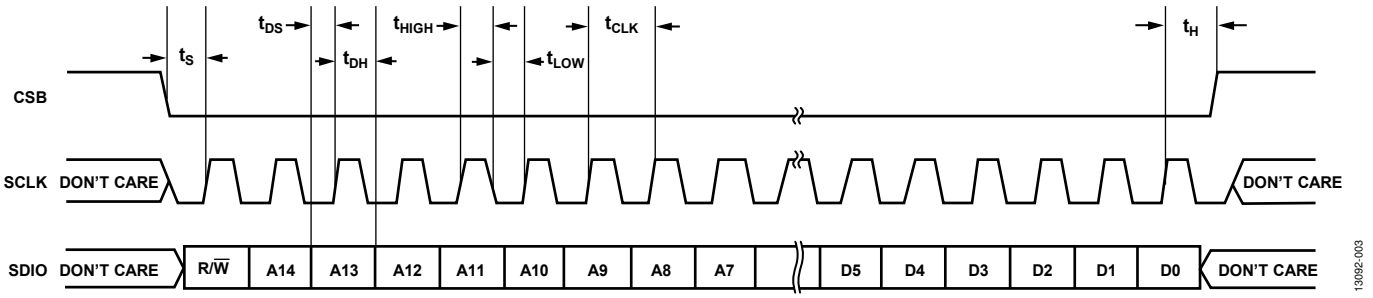


Figure 3. SPI Timing Diagram

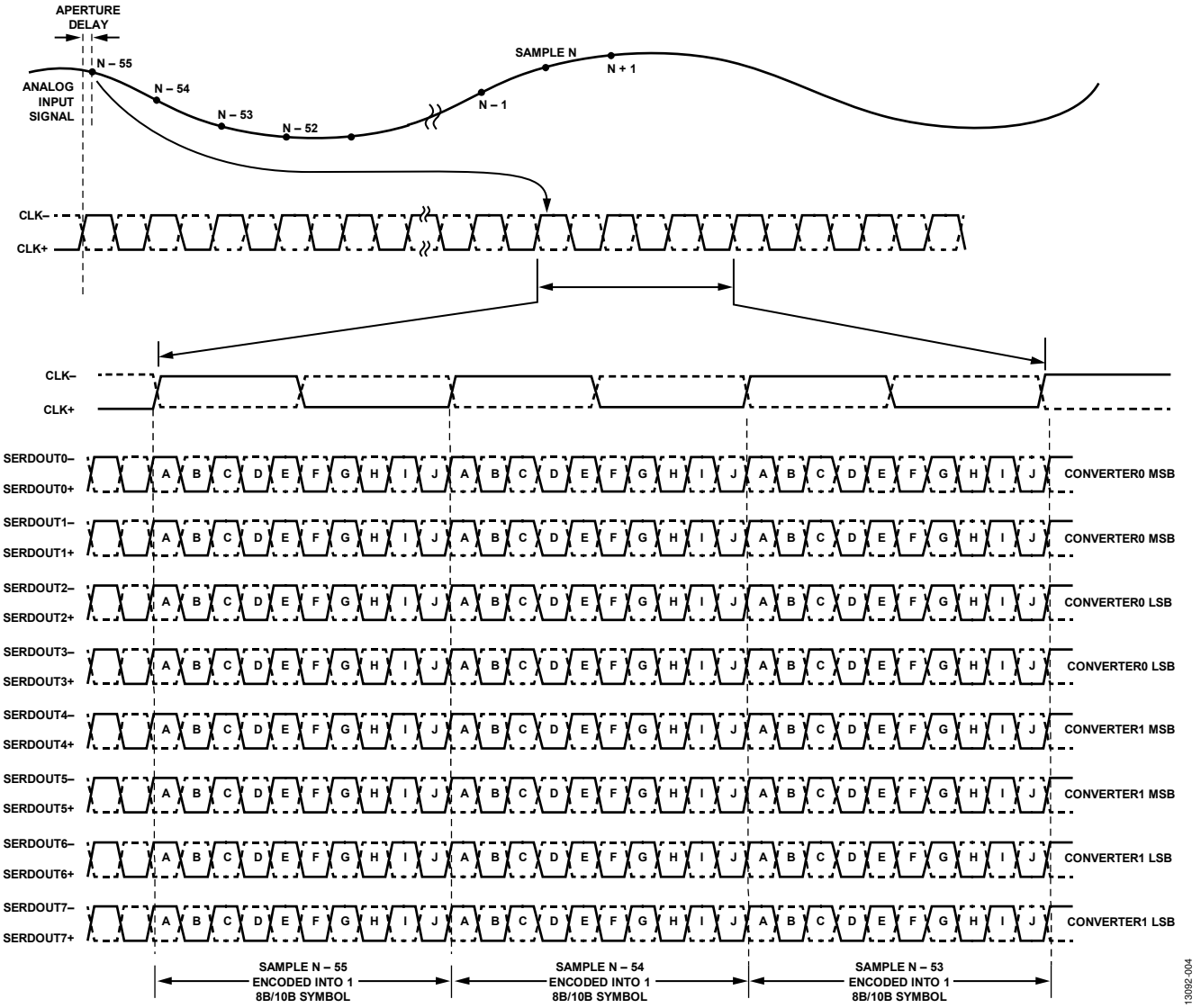


Figure 4. Data Output Timing (Full Bandwidth Mode, L = 8, M = 2, F = 1)

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD1 to AGND	1.32 V
AVDD1_SR to AGND	1.32 V
AVDD2 to AGND	2.75 V
AVDD3 to AGND	3.63 V
DVDD to DGND	1.32 V
DRVDD to DRGND	1.32 V
SPIVDD to AGND	3.63 V
AGND to DRGND	−0.3 V to +0.3 V
VIN±x to AGND	3.2 V
SCLK, SDIO, CSB to AGND	−0.3 V to SPIVDD + 0.3 V
PDWN/STBY to AGND	−0.3 V to SPIVDD + 0.3 V
Environmental	
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature	115°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Typical θ_{JA}, Ψ_{JB}, θ_{JC_TOP}, and θ_{JC_BOT} values are specified vs. the number of printed circuit board (PCB) layers in different airflow velocities (in m/sec). Airflow increases heat dissipation effectively reducing θ_{JA} and Ψ_{JB}. The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 7.

Table 7.

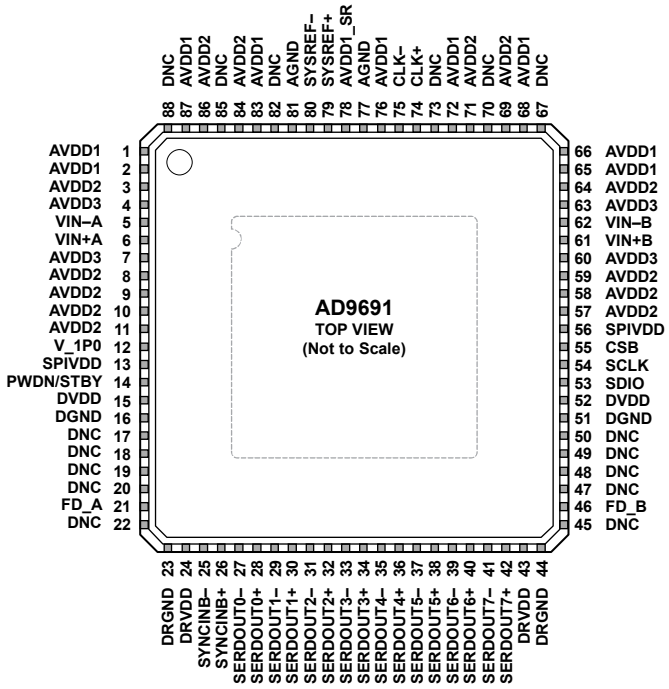
PCB Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	Ψ_{JB}[1, 3]	θ_{JC_TOP}[1, 4]	θ_{JC_BOT}[1, 4]	Unit
JEDEC 2s2p Board	0.0	17.41	4.70	6.01	1.12	°C/W
	1.0	13.83	4.32	N/A[5]	N/A[5]	°C/W
	2.5	12.47	4.21	N/A[5]	N/A[5]	°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2s2p test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per JEDEC JESD51-8 (still air).
[4] Per MIL-STD 883, Method 1012.1.
[5] N/A means not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. DNC = DO NOT CONNECT. THESE PINS MUST BE LEFT UNCONNECTED.
2. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE GROUND REFERENCE FOR AVDDX. THE EXPOSED THERMAL PAD MUST BE CONNECTED TO AGND.

13092-005

Figure 5. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
Power Supplies			
0	EPAD	Ground	Exposed Pad. The exposed thermal pad on the bottom of the package provides the ground reference for AVDDx. The exposed thermal pad must be connected to AGND.
1, 2, 65, 66, 68, 72, 76, 83, 87	AVDD1	Supply	Analog Power Supply (1.25 V Nominal).
3, 8, 9, 10, 11, 57, 58, 59, 64, 69, 71, 84, 86	AVDD2	Supply	Analog Power Supply (2.50 V Nominal).
4, 7, 60, 63	AVDD3	Supply	Analog Power Supply (3.3 V Nominal).
13, 56	SPIVDD	Supply	Digital Power Supply for SPI (1.8 V to 3.3 V).
15, 52	DVDD	Supply	Digital Power Supply (1.25 V Nominal).
16, 51	DGND	Ground	Ground Reference for DVDD.
23, 44	DRGND	Ground	Ground Reference for DRVDD.
24, 43	DRVDD	Supply	Digital Driver Power Supply (1.25 V Nominal).
77, 81	AGND[1]	Ground	Ground Reference for SYSREF±.
78	AVDD1_SR[1]	Supply	Analog Power Supply for SYSREF± (1.25 V Nominal).
Analog			
5, 6	VIN−A, VIN+A	Input	ADC A Analog Input Complement/True.
12	V_1P0	Input/DNC	1.0 V Reference Voltage Input/Do Not Connect. This pin is configurable through the SPI as a no connect or as an input. Do not connect this pin if using the internal reference. This pin requires a 1.0 V reference voltage input if using an external voltage reference source.
61, 62	VIN+B, VIN−B	Input	ADC B Analog Input True/Complement.
74, 75	CLK+, CLK−	Input	Clock Input True/Complement.

Pin No.	Mnemonic	Type	Description
CMOS Outputs			
21, 46	FD_A, FD_B	Output	Fast Detect Outputs for Channel A and Channel B, respectively.
Digital Inputs			
25, 26	SYNCINB−, SYNCINB+	Input	Active Low JESD204B LVDS Sync Input Complement/True.
79, 80	SYSREF+, SYSREF−	Input	Active Low JESD204B LVDS System Reference Input True/Complement.
Data Outputs			
27, 28	SERDOUT0−, SERDOUT0+	Output	Lane 0 Output Data Complement/True.
29, 30	SERDOUT1−, SERDOUT1+	Output	Lane 1 Output Data Complement/True.
31, 32	SERDOUT2−, SERDOUT2+	Output	Lane 2 Output Data Complement/True.
33, 34	SERDOUT3−, SERDOUT3+	Output	Lane 3 Output Data Complement/True.
35, 36	SERDOUT4−, SERDOUT4+	Output	Lane 4 Output Data Complement/True.
37, 38	SERDOUT5−, SERDOUT5+	Output	Lane 5 Output Data Complement/True.
39, 40	SERDOUT6−, SERDOUT6+	Output	Lane 6 Output Data Complement/True.
41, 42	SERDOUT7−, SERDOUT7+	Output	Lane 7 Output Data Complement/True.
Device Under Test (DUT) Controls			
14	PDWN/STBY	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby.
53	SDIO	Input/output	SPI Serial Data Input/Output.
54	SCLK	Input	SPI Serial Clock.
55	CSB	Input	SPI Chip Select (Active Low).
No Connections			
17, 18, 19, 20, 22, 45, 47, 48, 49, 50, 67, 70, 73, 82, 85, 88	DNC		Do No Connect. These pins must be left unconnected.

[1] To ensure proper ADC operation, connect AVDD1_SR and AGND separately from the AVDD1 and EPAD connection. For more information, see the Applications Information section.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 1.25 V, AVDD1_SR = 1.25 V, AVDD2 = 2.50 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate (1250 MSPS), 1.58 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, default SPI settings, clock divider = 2, T_A = 25°C, 128k FFT sample, unless otherwise noted.

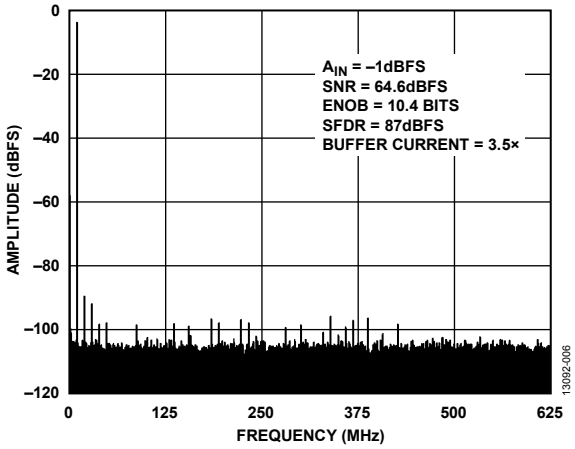


Figure 6. Single-Tone FFT with f_{IN} = 10.3 MHz

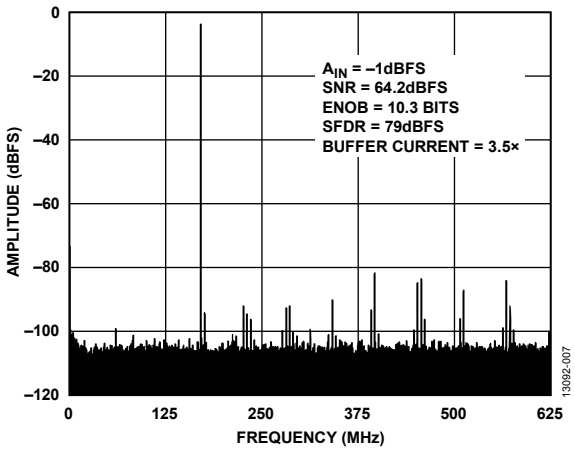


Figure 7. Single-Tone FFT with f_{IN} = 170.3 MHz

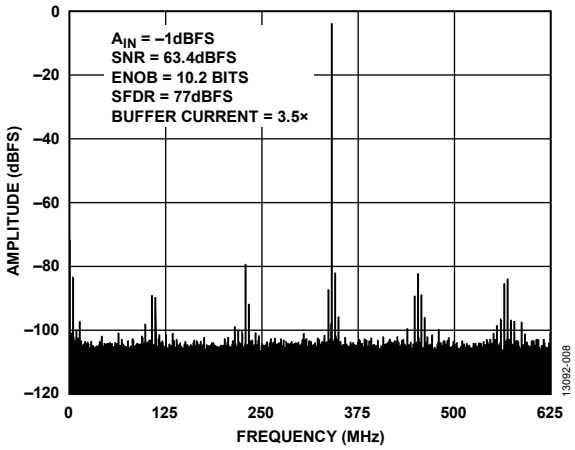


Figure 8. Single-Tone FFT with f_{IN} = 340.3 MHz

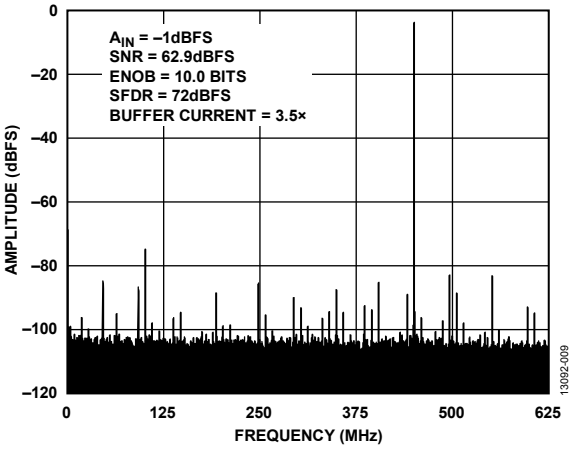


Figure 9. Single-Tone FFT with f_{IN} = 450.3 MHz

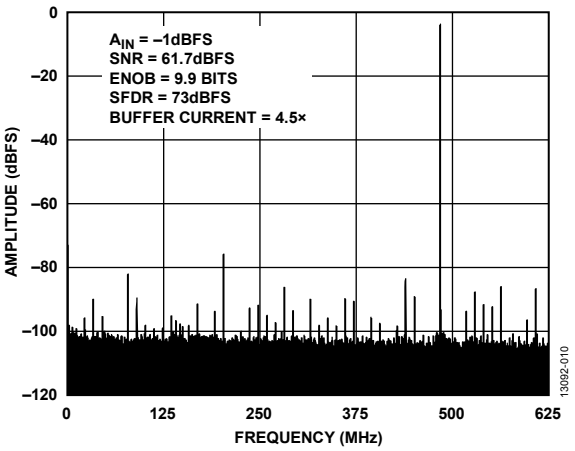


Figure 10. Single-Tone FFT with f_{IN} = 752.3 MHz

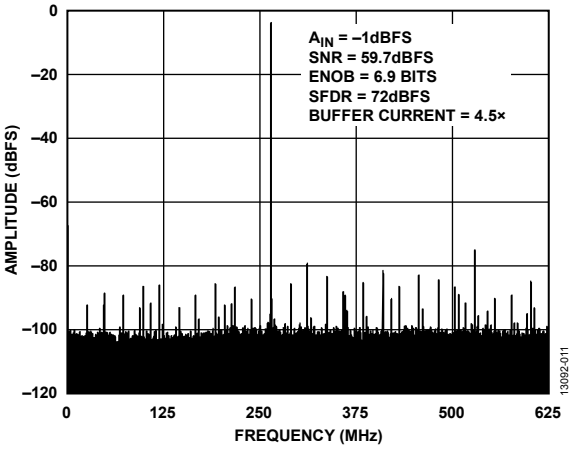


Figure 11. Single-Tone FFT with f_{IN} = 985.3 MHz

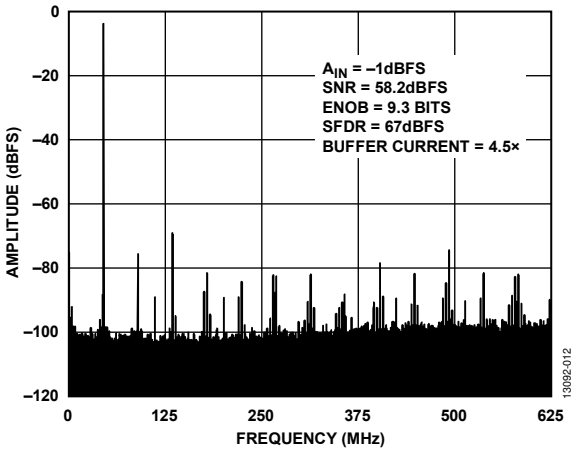


Figure 12. Single-Tone FFT with f_{IN} = 1205.3 MHz

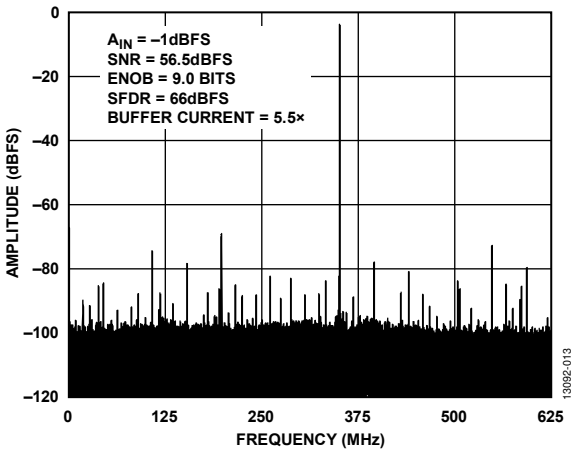


Figure 13. Single-Tone FFT with f_{IN} = 1600.3 MHz

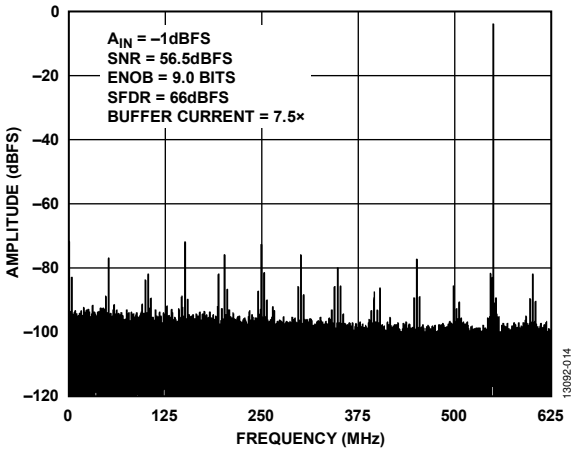


Figure 14. Single-Tone FFT with f_{IN} = 1950.3 MHz

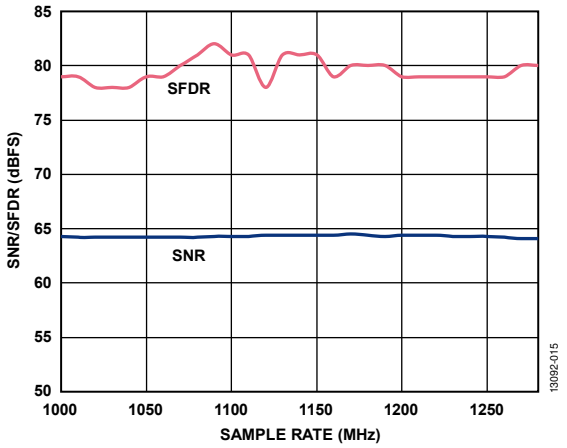


Figure 15. SNR/SFDR vs. Sample Rate (f_S), f_{IN} = 170.3 MHz, Buffer Current = 3.0×

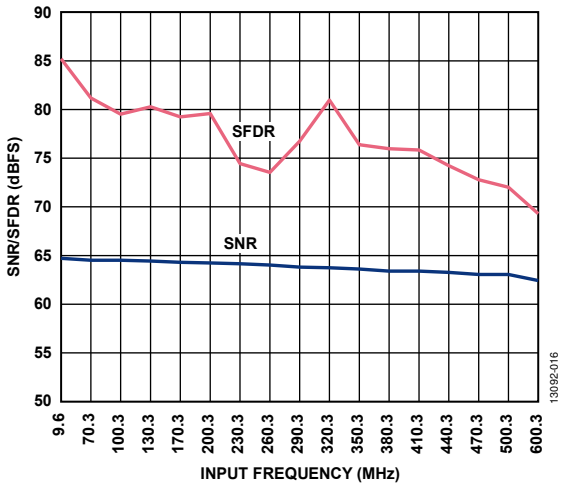


Figure 16. SNR/SFDR vs. Input Frequency (f_{IN}), f_{IN} < 600 MHz, Buffer Current = 3.5× (See Figure 41 and Table 9)

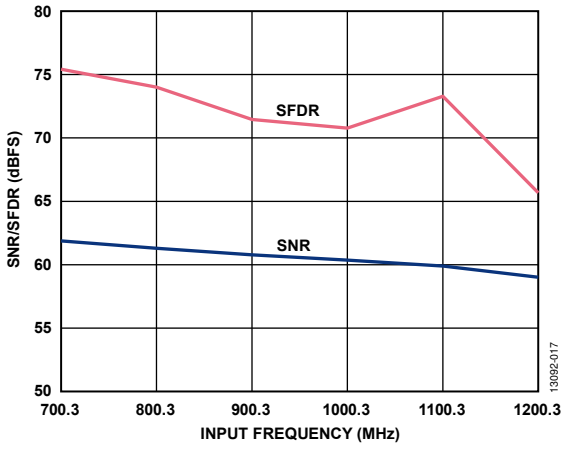


Figure 17. SNR/SFDR vs. Input Frequency (f_{IN}), 700 MHz < f_{IN} < 1200 MHz, Buffer Current = 4.5× (See Figure 41 and Table 9)

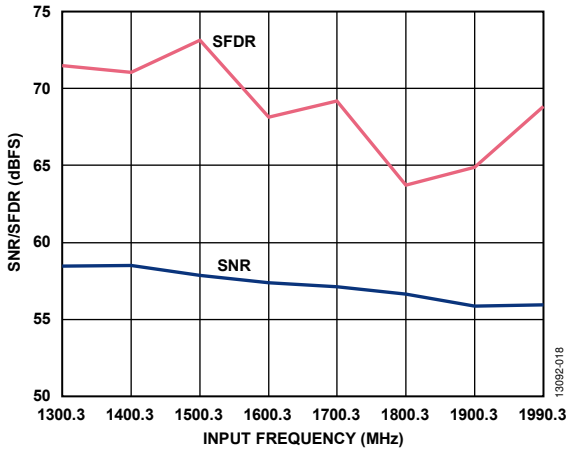


Figure 18. SNR/SFDR vs. Input Frequency (f_{IN}), 1300 MHz < f_{IN} < 2000 MHz, Buffer Current = 7.5× (See Figure 41 and Table 9)

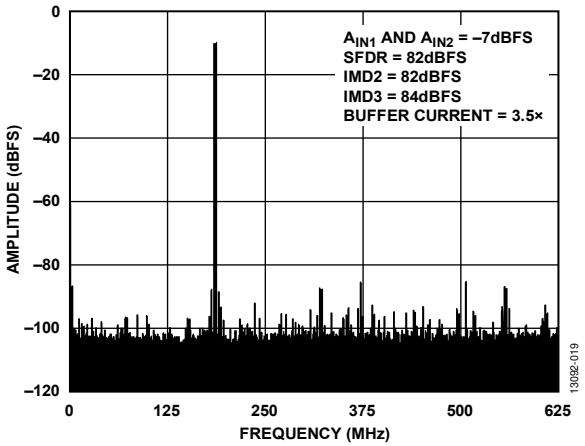


Figure 19. Two-Tone FFT, f_{IN1} = 184 MHz, f_{IN2} = 187 MHz

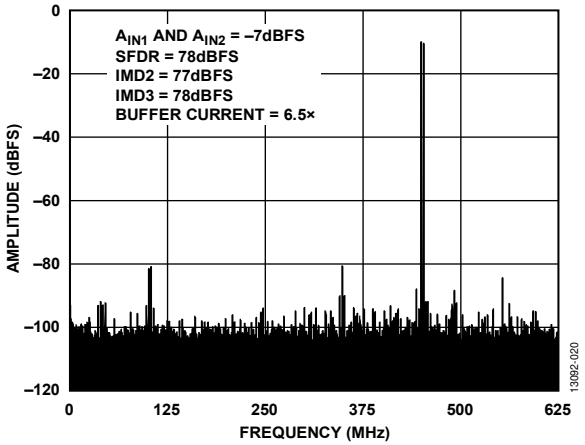


Figure 20. Two-Tone FFT, f_{IN1} = 449 MHz, f_{IN2} = 452 MHz

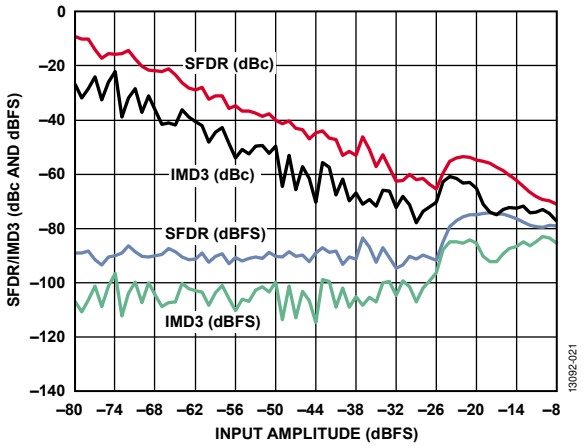


Figure 21. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184 MHz and f_{IN2} = 187 MHz

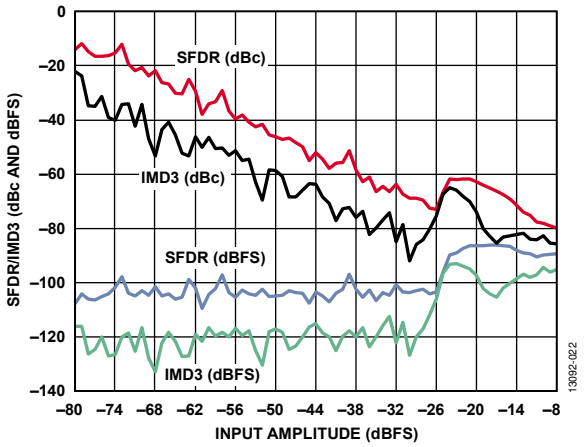


Figure 22. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 449 MHz and f_{IN2} = 452 MHz

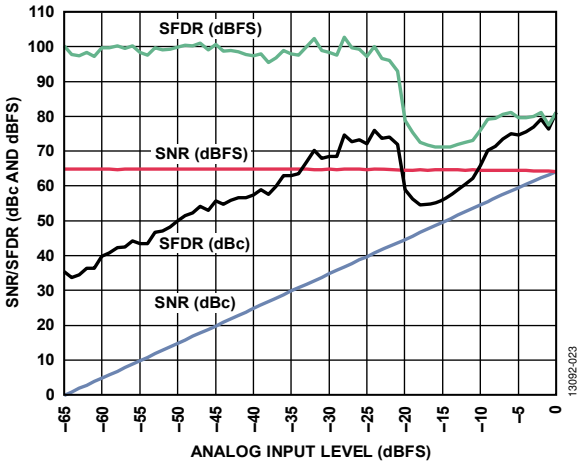


Figure 23. SNR/SFDR vs. Analog Input Level, f_{IN} = 170.3 MHz, Buffer Current = 3.5×

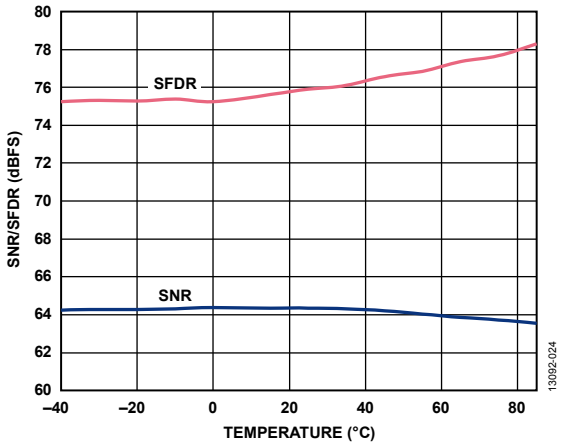


Figure 24. SNR/SFDR vs. Temperature, f_{IN} = 170.3 MHz

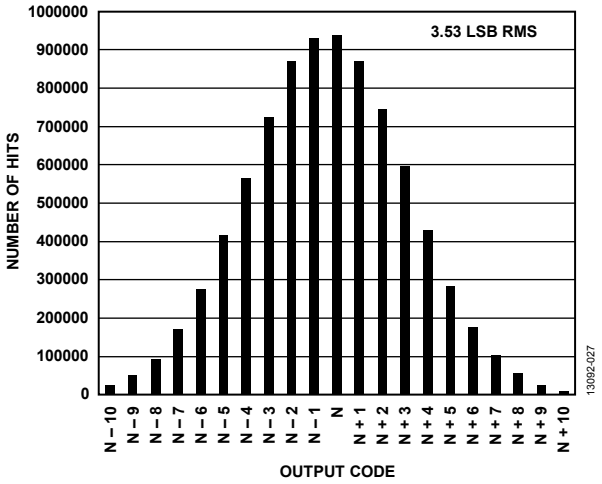


Figure 27. Input Referred Noise Histogram

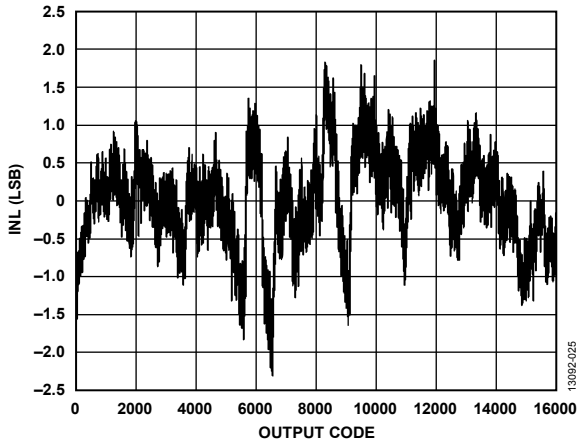


Figure 25. INL, f_{IN} = 10.3 MHz

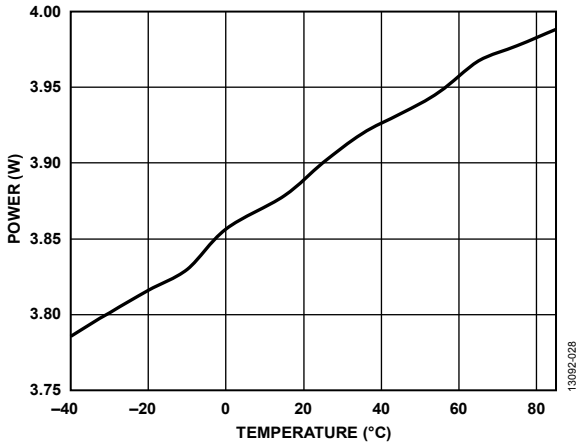


Figure 28. Power vs. Temperature

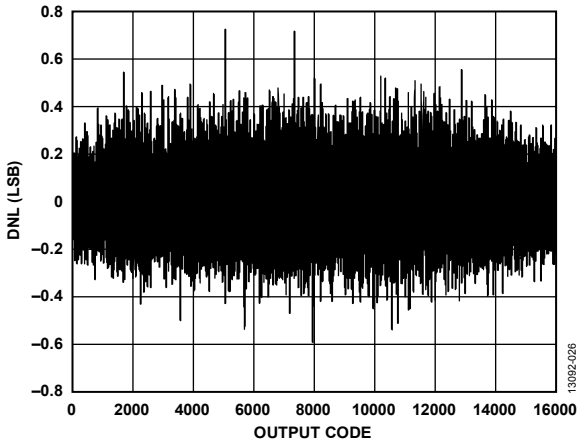


Figure 26. DNL, f_{IN} = 10 MHz

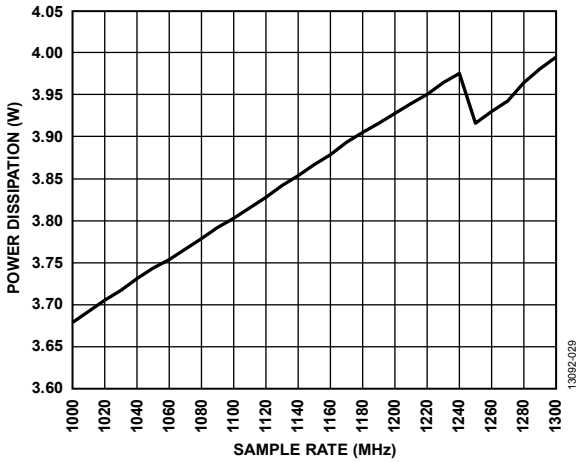


Figure 29. Power Dissipation vs. Sample Rate (f_S)

EQUIVALENT CIRCUITS

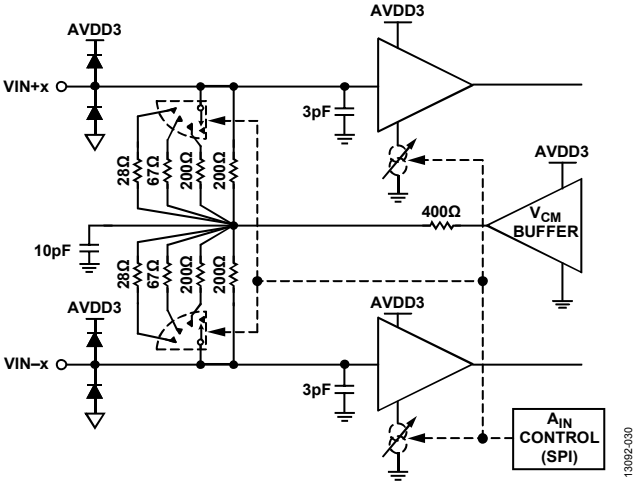


Figure 30. Analog Inputs

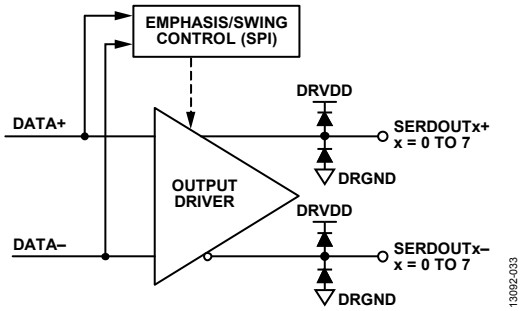


Figure 33. Digital Outputs

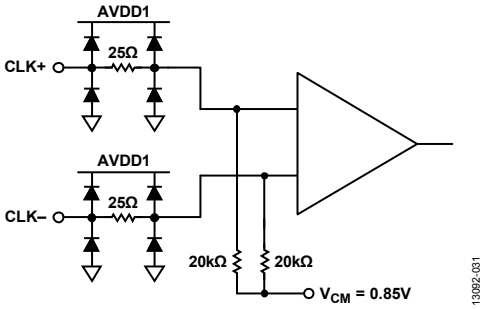


Figure 31. Clock Inputs

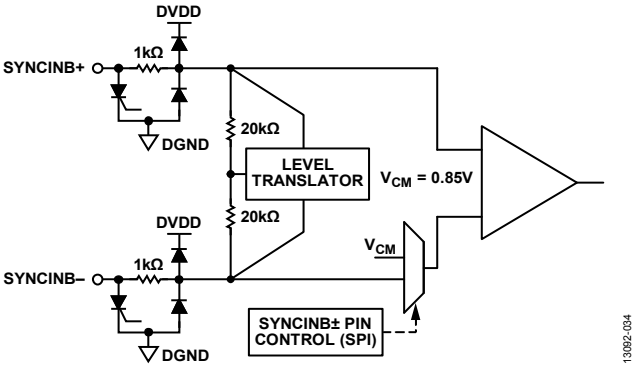


Figure 34. SYNCINB± Inputs

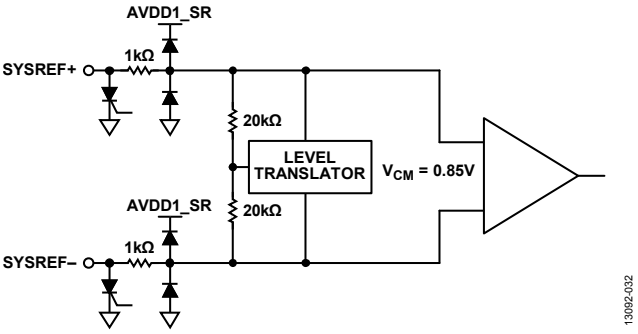


Figure 32. SYSREF± Inputs

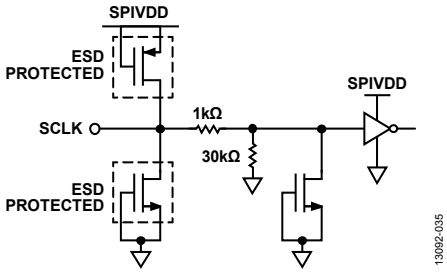


Figure 35. SCLK Input

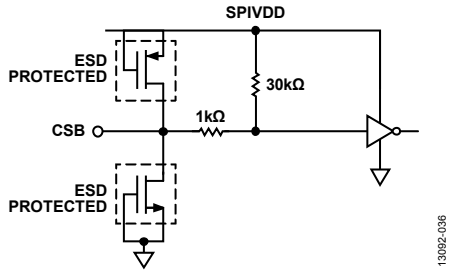


Figure 36. CSB Input

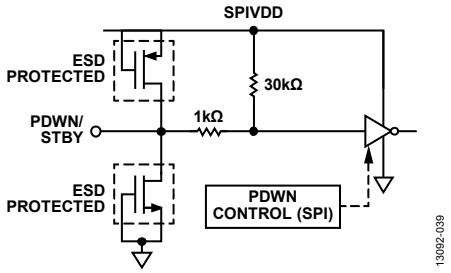


Figure 39. PDWN/STBY Input

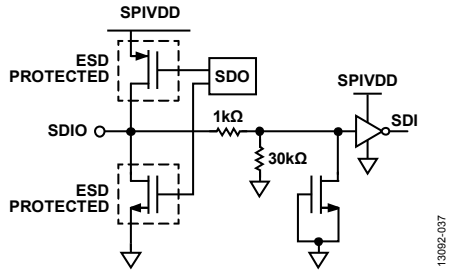


Figure 37. SDIO Input

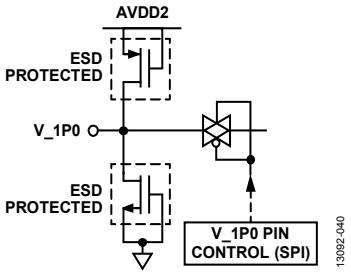


Figure 40. V_1P0 Input

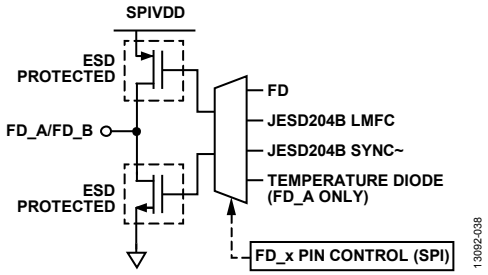


Figure 38. FD_A/FD_B Outputs

THEORY OF OPERATION

The AD9691 has two analog input channels and four JESD204B output lane pairs. The ADC is designed to sample wide bandwidth analog signals of up to 1.5 GHz. The AD9691 is optimized for wide input bandwidth, a high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

The AD9691 has several functions that simplify the AGC function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

The Subclass 1 JESD204B-based, high speed serialized output data rate can be configured in one-lane (L = 1), two-lane (L = 2), four-lane (L = 4), and eight-lane (L = 8) configurations, depending on the sample rate and the decimation ratio (DCM). Multiple device synchronization is supported through the SYSREF± and SYNCINB± input pins.

ADC ARCHITECTURE

The architecture of the AD9691 consists of an input buffered pipelined ADC. The input buffer provides a termination impedance to the analog input signal. This termination impedance can be changed using the SPI to meet the termination needs of the driver or amplifier. The default termination value is set to 400 Ω. The equivalent circuit diagram of the analog input termination is shown in Figure 30. The input buffer is optimized for high linearity, low noise, and low power.

The input buffer provides a linear high input impedance (for ease of drive) and reduces the kickback from the ADC. The buffer is optimized for high linearity, low noise, and low power. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample; at the same time, the remaining stages operate with the preceding samples. Sampling occurs on the rising edge of the clock.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9691 is a differential buffer. The internal common-mode voltage of the buffer is 2.05 V. The clock signal alternately switches the input circuit between sample mode and hold mode. When the input circuit is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor, in series with each input, helps reduce the peak transient current injected from the output stage of the driving source. In addition, place low Q inductors or ferrite beads on each section of the input to reduce high differential capacitance at the analog inputs and, thus, achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Place either a differential capacitor or two single-ended capacitors on the inputs to provide a matching passive network. This configuration ultimately creates a low-pass filter at the input, which limits unwanted broadband noise. For more information, see the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005). In general, the precise values depend on the application.

For best dynamic performance, the source impedances driving VIN+x and VIN−x must be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates a differential reference that defines the span of the ADC core.

The maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9691, the available span is 1.58 V p-p differential.

Differential Input Configurations

There are several ways to drive the AD9691, either actively or passively. However, optimum performance is achieved by driving the analog input differentially.

For applications where SNR and SFDR are key parameters, differential transformer coupling is the recommended input configuration (see Figure 41 and Table 9) because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9691.

For low to midrange frequencies, a double balun or double transformer network (see Figure 41) is recommended for optimum performance of the AD9691. For higher frequencies in the second and third Nyquist zones, it is better to remove some of the front-end passive components to ensure wideband operation (see Table 9).

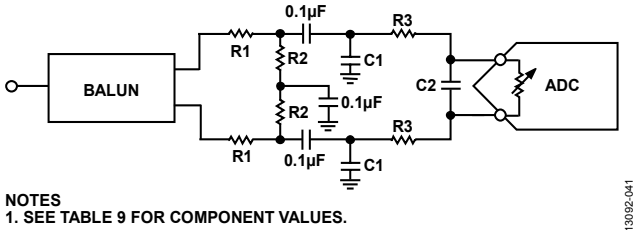


Figure 41. Differential Transformer-Coupled Configuration

Table 9. Differential Transformer-Coupled Input Configuration Component Values

Frequency Range	Transformer/Balun	R1 (Ω)	R2 (Ω)	R3 (Ω)	C1 (pF)	C2 (pF)
<625 MHz	BAL-0006/BAL-0006SMG/ETC1-1-13	10	50	15	Open	3
>625 MHz	BAL-0006/BAL-0006SMG	10	50	0	Open	Open

Input Common Mode

The analog inputs of the AD9691 are internally biased to the common mode as shown in Figure 42. The common-mode buffer has a limited range in that the performance suffers greatly if the common-mode voltage drops by more than 100 mV. Therefore, in dc-coupled applications, set the common-mode voltage to 2.05 V ± 100 mV to ensure proper ADC operation.

Analog Input Controls and SFDR Optimization

The AD9691 offers flexible controls for the analog inputs, such as input termination and buffer current. All of the available controls are shown in Figure 42.

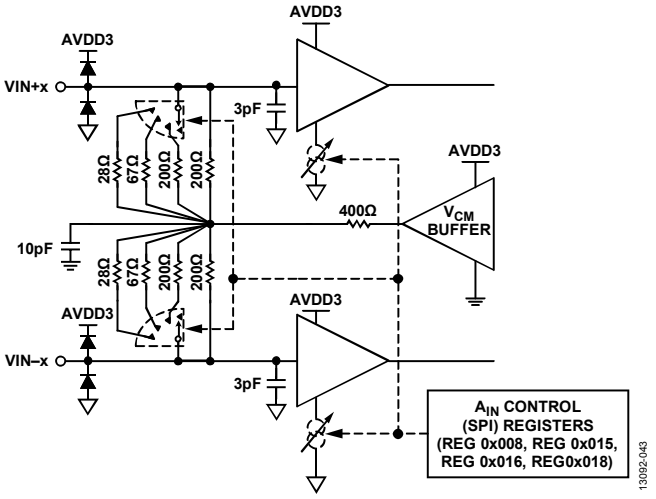


Figure 42. Analog Input Controls

Using Register 0x018, the buffer currents on each channel can be scaled to optimize the SFDR over various input frequencies and bandwidths of interest. As the input buffer currents are set, the amount of current required by the AVDD3 supply changes. This relationship is shown in Figure 43. For a complete list of buffer current settings, see Table 35.

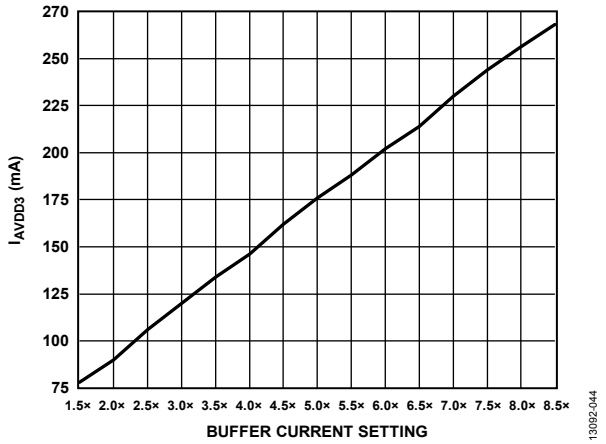


Figure 43. AVDD3 Power (I_{AVDD3}) vs. Buffer Current Setting

Figure 44, Figure 45, and Figure 46 show how the SFDR can be optimized using the buffer current setting in Register 0x018 for different Nyquist zones. At frequencies greater than 1 GHz, it is better to run the ADC at input amplitudes less than −1 dBFS (−3 dBFS, for example). This greatly improves the linearity of the converted signal without sacrificing SNR performance.

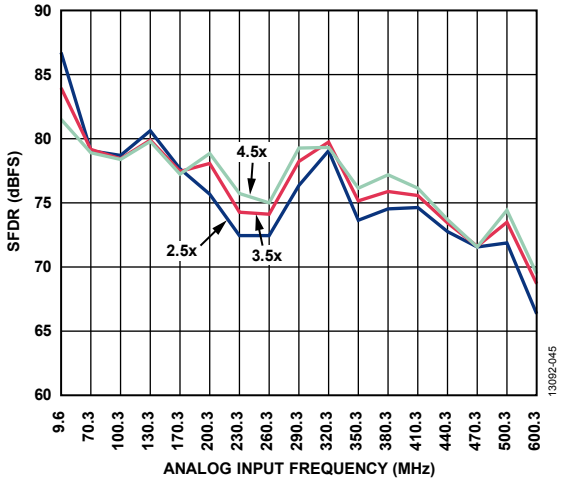


Figure 44. Buffer Current Sweeps, SFDR vs. Analog Input Frequency vs. I_{BUFF}; f_{IN} < 600 MHz

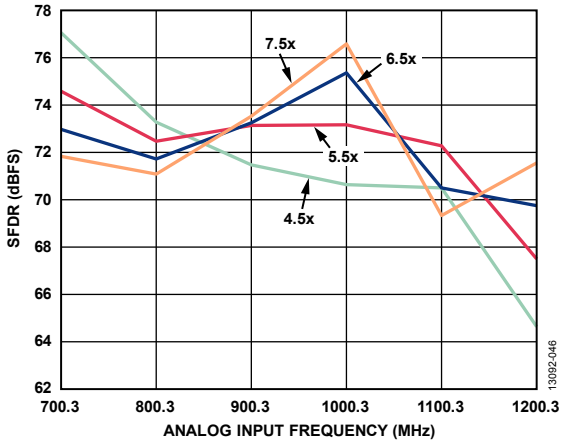


Figure 45. Buffer Current Sweeps, SFDR vs. Analog Input Frequency vs. I_{BUFF}; 700 MHz < f_{IN} < 1200 MHz

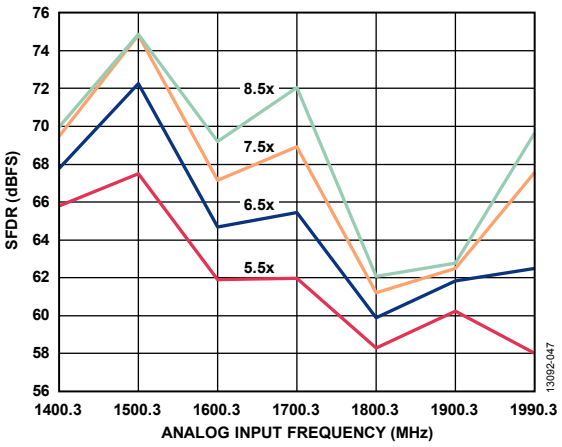


Figure 46. Buffer Current Sweeps, SFDR vs. Analog Input Frequency vs. I_{BUFF}; 1300 MHz < f_{IN} < 2000 MHz

Table 10 shows the recommended buffer current and full-scale voltage settings for the different analog input frequency ranges.

Table 10. SFDR Optimization for Input Frequencies

Input Frequency	Input Buffer Current Control Setting (Register 0x018)	Buffer Control 2 Register (Register 0x935)
<500 MHz	3.5×	0x04
500 MHz to 1 GHz	5.5× or 6.5×	0x00
>1 GHz	6.5× or higher	0x00

Absolute Maximum Input Swing

The absolute maximum input swing allowed at the inputs of the AD9691 is 4.3 V p-p differential. Signals operating near or at this level can cause permanent damage to the ADC.

VOLTAGE REFERENCE

A stable and accurate 1.0 V voltage reference is built into the AD9691. This internal 1.0 V reference sets the full-scale input range of the ADC. For more information on adjusting the input swing, see Table 35. Figure 47 shows the block diagram of the internal 1.0 V reference controls.

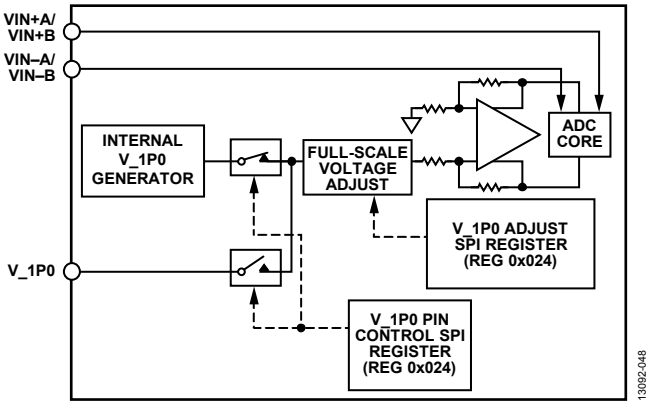


Figure 47. Internal Reference Configuration and Controls

Register 0x024 enables the user to either use this internal 1.0 V reference, or to provide an external 1.0 V reference. When using an external voltage reference, provide a 1.0 V reference. The full-scale adjustment is made using the SPI, irrespective of the reference voltage. For more information on adjusting the full-scale level of the AD9691, see the Memory Map Register Table section.

The use of an external reference may be necessary, in some applications, to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 48 shows the typical drift characteristics of the internal 1.0 V reference.

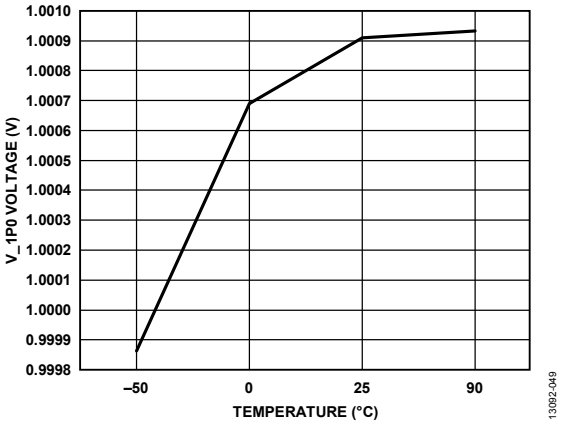


Figure 48. Typical V_1P0 Drift

The external reference must be a stable 1.0 V reference. The ADR130 is a good option for providing the 1.0 V reference. Figure 49 shows how the ADR130 can be used to provide the external 1.0 V reference to the AD9691. The grayed out areas show unused blocks within the AD9691 when using the ADR130 to provide the external reference.

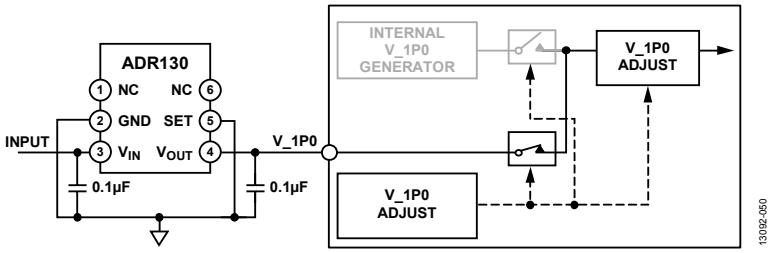


Figure 49. External Reference Using the ADR130

CLOCK INPUT CONSIDERATIONS

For optimum performance, drive the AD9691 sample clock inputs (CLK+ and CLK−) with a differential signal. This signal is typically ac-coupled to the CLK+ and CLK− pins via a transformer or clock drivers. These pins are biased internally and require no additional biasing.

Figure 50 shows a preferred method for clocking the AD9691. The low jitter clock source is converted from a single-ended signal to a differential signal using an RF transformer.

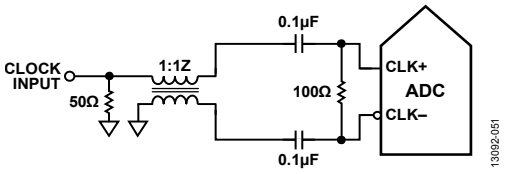


Figure 50. Transformer-Coupled Differential Clock

Another option is to ac couple a differential CML or LVDS signal to the sample clock input pins, as shown in Figure 51 and Figure 52.

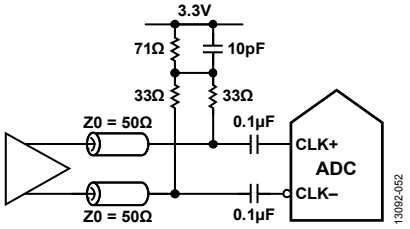


Figure 51. Differential CML Sample Clock

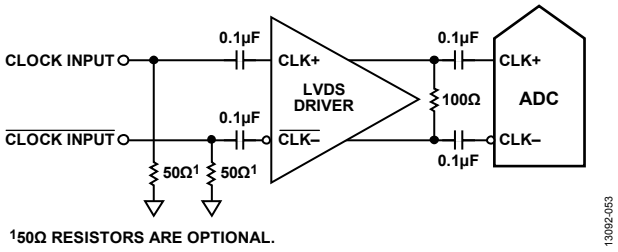


Figure 52. Differential LVDS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to the clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. In applications where the clock duty cycle cannot be guaranteed to be 50%, a higher multiple frequency clock can be supplied to the device. The AD9691 can be clocked at 1.5 GHz with the internal clock divider set to 2. The output of the divider offers a 50% duty cycle, high slew rate (fast edge) clock signal to the internal ADC. See the Memory Map section for more details on using this feature.

Input Clock Divider ½ Period Delay Adjust

The input clock divider inside the AD9691 provides phase delay in increments of ½ the input clock cycle. Register 0x10C can be programmed to enable this delay independently for each channel. Changing this register does not affect the stability of the JESD204B link.

Input Clock Divider

The AD9691 contains an input clock divider with the ability to divide the Nyquist input clock by 1, 2, 4, or 8. The divider ratios can be selected using Register 0x10B. This is shown in Figure 53.

The maximum frequency at the CLK± inputs is 4 GHz. This is the limit of the divider. In applications where the clock input is a multiple of the sample clock, the appropriate divider ratio must be programmed into the clock divider before applying the clock signal. This ensures that the current transients during device startup are controlled.

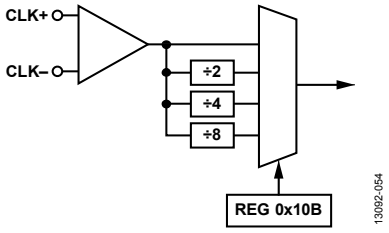


Figure 53. Clock Divider Circuit

The AD9691 clock divider can be synchronized using the external SYSREF± input. A valid SYSREF± signal causes the clock divider to reset to a programmable state. Enable this feature by setting Bit 7 of Register 0x10D. This synchronization feature allows multiple devices to have their clock dividers aligned to guarantee simultaneous input sampling. See the Multichip Synchronization section for more information.

Clock Fine Delay Adjust

The AD9691 sampling edge instant can be adjusted by writing to Register 0x117 and Register 0x118. Setting Bit 0 of Register 0x117 enables the feature, and Register 0x118, Bits[7:0] set the value of the delay. This value can be programmed individually for each channel. The clock delay can be adjusted from −151.7 ps to +150 ps in 1.7 ps increments. The clock delay adjust takes effect immediately when it is enabled via SPI writes. Enabling the clock fine delay adjust in Register 0x117 causes a datapath reset. However, the contents of Register 0x118 can be changed without affecting the stability of the JESD204B link.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated by

$$SNR = 20\log_{10}(2 \times \pi \times f_A \times t_J)$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 54).

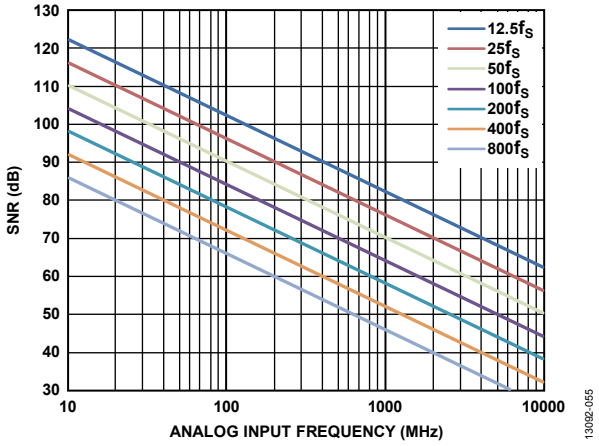


Figure 54. Ideal SNR vs. Analog Input Frequency and Jitter

Treat the clock input as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9691. Separate power supplies for clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. If the clock is generated from another type of source (by gating, dividing, or other methods), retime the clock by the original clock at the last step. For more in-depth information about jitter performance as it relates to ADCs, see the AN-501 Application Note and the AN-756 Application Note.

POWER-DOWN/STANDBY MODE

The AD9691 has a PDWN/STBY pin that configures the device in power-down or standby mode. The default operation is the power-down function. The PDWN/STBY pin is a logic high pin. When in power-down mode, the JESD204B link is disrupted. The power-down option can also be set via Register 0x03F and Register 0x040.

In standby mode, the JESD204B link is not disrupted and transmits zeros for all converter samples. This can be changed using Register 0x571, Bit 7 to select /K/ characters.

TEMPERATURE DIODE

The AD9691 contains a diode-based temperature sensor for measuring the temperature of the die. This diode can output a voltage and serve as a coarse temperature sensor to monitor the internal die temperature.

The temperature diode voltage can be output to the FD_A pin using the SPI. Use Register 0x028, Bit 0 to enable or disable the diode. Register 0x028 is a local register; therefore, Channel A must be selected in the device index register (Register 0x008) to enable the temperature diode readout. Configure the FD_A pin to output the diode voltage by programming Register 0x040, Bits[2:0]. See Table 35 for more information.

The voltage response of the temperature diode (SPIVDD = 1.8 V) is shown in Figure 55.

Figure 55. Diode Voltage vs. Temperature

ADC OVERRANGE AND FAST DETECT

In receiver applications, it is desirable to have a mechanism to reliably determine when the converter is about to clip. The standard overrange bit in the JESD204B outputs provides information on the state of the analog input that is of limited usefulness. Therefore, it is helpful to have a programmable threshold below full scale that allows time to reduce the gain before the clip actually occurs. In addition, because input signals can have significant slew rates, the latency of this function is of major concern. Highly pipelined converters can have significant latency. The AD9691 contains fast detect circuitry for individual channels to monitor the threshold and assert the FD_A and FD_B pins.

ADC OVERRANGE

The ADC overrange indicator is asserted when an overrange is detected on the input of the ADC. The overrange indicator can be embedded within the JESD204B link as a control bit (when CSB > 0). The latency of this overrange indicator matches the sample latency.

The AD9691 also records any overrange condition in any of the four virtual converters. For more information on the virtual converters, see Figure 61. The overrange status of each virtual converter is registered as a sticky bit in Register 0x563. The contents of Register 0x563 can be cleared using Register 0x562, by toggling the bits corresponding to the virtual converter to the set and reset positions.

FAST THRESHOLD DETECTION (FD_A AND FD_B)

The fast detect (FD) bit (enabled via the control bits in Register 0x559 and Register 0x55A) is immediately set whenever the absolute value of the input signal exceeds the programmable upper threshold level. The FD bit is cleared only when the absolute value of the input signal drops below the lower threshold level for greater than the programmable dwell time. This feature provides hysteresis and prevents the FD bit from excessively toggling.

The operation of the upper threshold and lower threshold registers, along with the dwell time registers, is shown in Figure 56.

The FD indicator is asserted if the input magnitude exceeds the value programmed in the fast detect upper threshold registers, located at Register 0x247 and Register 0x248. The selected threshold register is compared with the signal magnitude at the output of the ADC. The fast upper threshold detection has a latency of 28 clock cycles (maximum). The approximate upper threshold magnitude is defined by

$$\textit{Upper Threshold Magnitude}\ (\text{dBFS}) = 20\log(\textit{Threshold Magnitude}/2^{13})$$

The FD indicators are not cleared until the signal drops below the lower threshold for the programmed dwell time. The lower threshold is programmed in the fast detect lower threshold registers, located at Register 0x249 and Register 0x24A. The fast detect lower threshold register is a 13-bit register that is compared with the signal magnitude at the output of the ADC. This comparison is subject to the ADC pipeline latency, but is accurate in terms of converter resolution. The lower threshold magnitude is defined by

$$\textit{Lower Threshold Magnitude}\ (\text{dBFS}) = 20\log(\textit{Threshold Magnitude}/2^{13})$$

For example, to set an upper threshold of −6 dBFS, write 0xFFF to Register 0x247 and Register 0x248. To set a lower threshold of −10 dBFS, write 0xA1D to Register 0x249 and Register 0x24A.

To program the dwell time from 1 to 65,535 sample clock cycles, place the desired value in the fast detect dwell time registers, located at Register 0x24B and Register 0x24C. See the Memory Map section (Register 0x040, and Register 0x245 to Register 0x24C in Table 35) for more details.

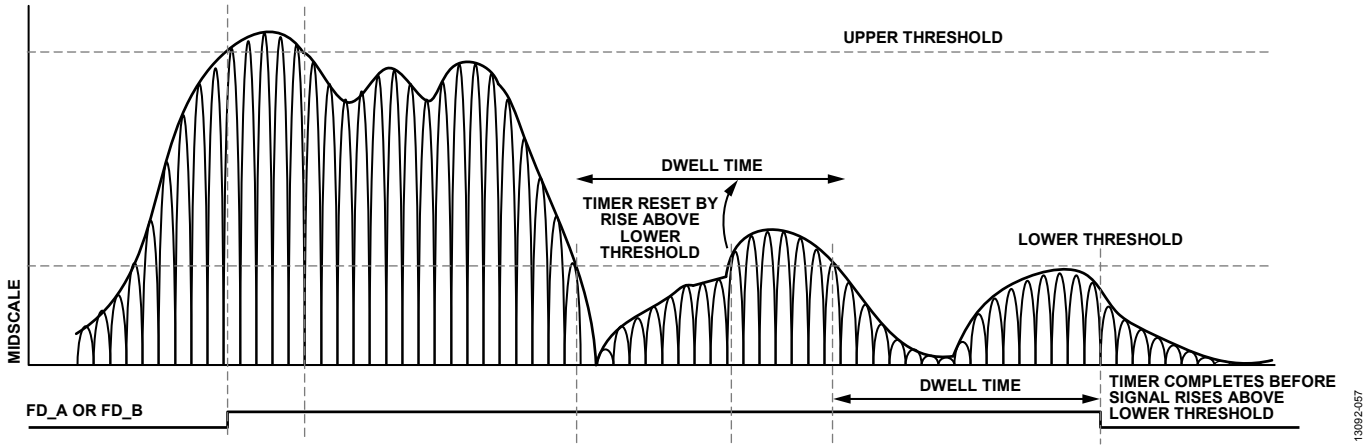


Figure 56. Threshold Settings for FD_A and FD_B Signals

SIGNAL MONITOR

The signal monitor block provides additional information about the signal being digitized by the ADC. The signal monitor computes the peak magnitude of the digitized signal. This information can be used to drive an AGC loop to optimize the range of the ADC in the presence of real-world signals.

The results of the signal monitor block can be obtained either by reading back the internal values from the SPI port or by embedding the signal monitoring information into the JESD204B interface as special control bits. A global, 24-bit programmable period controls the duration of the measurement. Figure 57 shows the simplified block diagram of the signal monitor block.

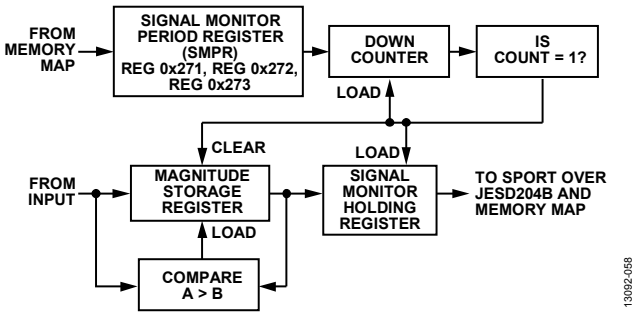


Figure 57. Signal Monitor Block

The peak detector captures the largest signal within the observation period. The detector only observes the magnitude of the signal. The resolution of the peak detector is a 13-bit value, and the observation period is 24 bits and represents converter output samples. The peak magnitude can be derived by using the following equation:

$$Peak\ Magnitude\ (\text{dBFS}) = 20\log(Peak\ Detector\ Value/2^{13})$$

The magnitude of the input port signal is monitored over a programmable time period, which is determined by the signal monitor period register (SMPR). The peak detector function is enabled by setting Bit 1 of Register 0x270 in the signal monitor control register. The 24-bit SMPR must be programmed before activating this mode.

After enabling this mode, the value in the SMPR is loaded into a monitor period timer, which decrements at the decimated clock rate. The magnitude of the input signal is compared to the value in the internal magnitude storage register (not accessible to the user), and the greater of the two is updated as the current peak level. The initial value of the magnitude storage register is set to the current ADC input signal magnitude. This comparison continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the 13-bit peak level value is transferred to the signal monitor holding register, which can be read through the memory map or output through the SPORT over the JESD204B interface. The monitor period timer is reloaded with the value in the SMPR, and the countdown is restarted. In addition, the magnitude of the first input sample is updated in the magnitude storage register, and the comparison and update procedure continues.

SPORT Over JESD204B

The signal monitor data can also be serialized and sent over the JESD204B interface as control bits. These control bits must be deserialized from the samples to reconstruct the statistical data. This function is enabled by setting Bits[1:0] of Register 0x279 and Bit 1 of Register 0x27A. Figure 58 shows two different example configurations for the signal monitor control bit locations inside the JESD204B samples. A maximum of three control bits can be inserted into the JESD204B samples; however, only one control bit is required for the signal monitor. Control bits are inserted from MSB to LSB. If only one control bit is to be inserted (CS = 1), only the most significant control bit is used (see Example Configuration 1 and Example Configuration 2 in Figure 58). To select the SPORT over JESD204B option, program Register 0x559, Register 0x55A, and Register 0x58F. See Table 35 for more information on setting these bits.

Figure 59 shows the 25-bit frame data that encapsulates the peak detector value. The frame data is transmitted MSB first with five 5-bit subframes. Each subframe contains a start bit that can be used by a receiver to validate the deserialized data. Figure 60 shows the SPORT over JESD204B signal monitor data with a monitor period timer set to 80 samples.