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14-Bit, 1300 MSPS/625 MSPS, JESD204B, Dual Analog-to-Digital Converter

Data Sheet **AD9695**

FEATURES

- JESD204B (Subclass 1) coded serial digital outputs
  - Lane rates up to 16 Gbps
- 1.6 W total power at 1300 MSPS
  - 800 mW per ADC channel
- SNR = 65.6 dBFS at 172 MHz (1.59 V p-p input range)
- SFDR = 78 dBFS at 172.3 MHz (1.59 V p-p input range)
- Noise density
  - −153.9 dBFS/Hz (1.59 V p-p input range)
  - −155.6 dBFS/Hz (2.04 V p-p input range)
- 0.95 V, 1.8 V, and 2.5 V supply operation
- No missing codes
- Internal ADC voltage reference
- Flexible input range
  - 1.36 V p-p to 2.04 V p-p (1.59 V p-p typical)
- 2 GHz usable analog input full power bandwidth
- >95 dB channel isolation/crosstalk
- Amplitude detect bits for efficient AGC implementation
- 2 integrated digital downconverters per ADC channel
  - 48-bit NCO
  - Programmable decimation rates
- Differential clock input
- SPI control
  - Integer clock divide by 2 and divide by 4
  - Flexible JESD204B lane configurations
- On-chip dithering to improve small signal linearity

APPLICATIONS

- Communications
- Diversity multiband, multimode digital receivers
  - 3G/4G, TD-SCDMA, WCDMA, GSM, LTE
- General-purpose software radios
- Ultrawideband satellite receiver
- Instrumentation
  - Oscilloscopes
  - Spectrum analyzers
  - Network analyzers
  - Integrated RF test solutions
- Radars
- Electronic support measures, electronic counter measures, and electronic counter-counter measures
- High speed data acquisition systems
- DOCSIS 3.0 CMTS upstream receive paths
- Hybrid fiber coaxial digital reverse path receivers
- Wideband digital predistortion

FUNCTIONAL BLOCK DIAGRAM

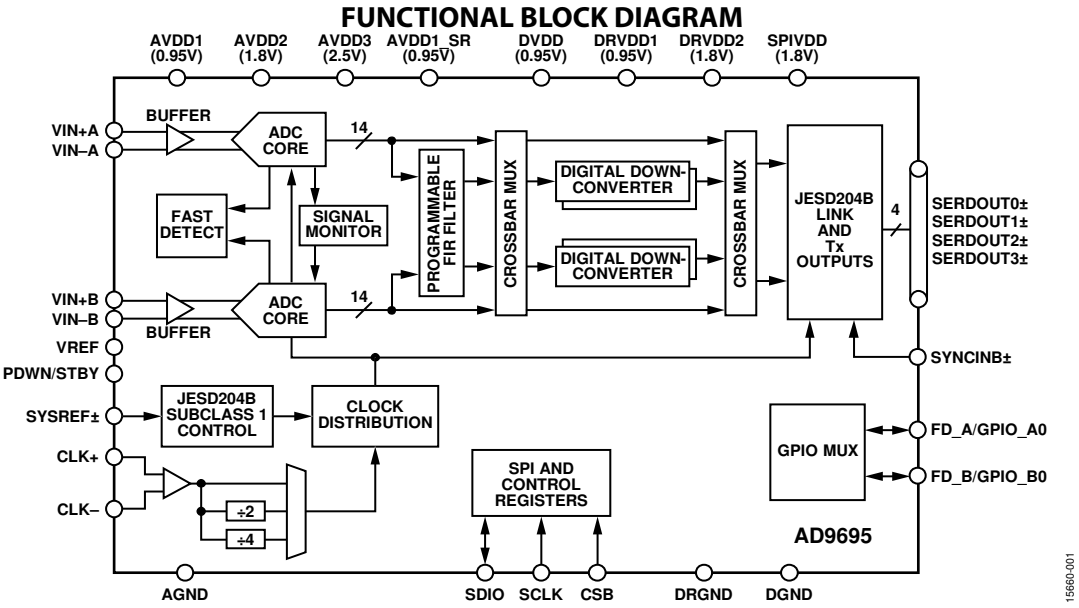

Figure 1.

Rev. A Document Feedback

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9/2017—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9695 is a dual, 14-bit, 1300 MSPS/625 MSPS analog-to-digital converter (ADC). The device has an on-chip buffer and a sample-and-hold circuit designed for low power, small size, and ease of use. This product is designed to support communications applications capable of direct sampling wide bandwidth analog signals of up to 2 GHz. The −3 dB bandwidth of the ADC input is 2 GHz. The AD9695 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. The analog input and clock signals are differential inputs. The ADC data outputs are internally connected to four digital downconverters (DDCs) through a crossbar mux. Each DDC consists of multiple signal processing stages: a 48-bit frequency translator (numerically controlled oscillator (NCO)), and decimation filters. The NCO has the option to select up to 16 preset bands over the general-purpose input/output (GPIO) pins, or use a coherent fast frequency hopping mechanism for band selection. Operation of the AD9695 between the DDC modes is selectable via SPI-programmable profiles.

In addition to the DDC blocks, the AD9695 has several functions that simplify the automatic gain control (AGC) function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect control bits in Register 0x0245 of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input. In addition to the fast detect outputs, the AD9695 also offers signal monitoring capability. The signal monitoring block provides additional information about the signal being digitized by the ADC.

The user can configure the Subclasss 1 JESD204B-based high speed serialized output using either one lane, two lanes, or four lanes, depending on the DDC configuration and the acceptable lane rate of the receiving logic device. Multidevice synchronization is supported through the SYSREF± and SYNCINB± input pins.

The AD9695 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using a 3-wire serial port interface (SPI) and or PDWN/STBY pin.

The AD9695 is available in a Pb-free, 64-lead LFCSP and is specified over the −40°C to +105°C junction temperature range. This product may be protected by one or more U.S. or international patents.

Note that, throughout this data sheet, multifunction pins, such as FD_A/GPIO_A0, are referred to either by the entire pin name or by a single function of the pin, for example, FD_A, when only that function is relevant.

PRODUCT HIGHLIGHTS

1. Low power consumption per channel.
2. JESD204B lane rate support up to 16 Gbps.
3. Wide, full power bandwidth supports intermediate frequency (IF) sampling of signals up to 2 GHz.
4. Buffered inputs ease filter design and implementation.
5. Four integrated wideband decimation filters and NCO blocks supporting multiband receivers.
6. Programmable fast overrange detection.
7. On-chip temperature diode for system thermal management.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 0.95 V, AVDD1_SR = 0.95 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.95 V, DRVDD1 = 0.95 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, clock divider = 2, default input full scale, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, and sample rate = 625 MSPS (AD9695-625 speed grade), sample rate = 1300 MSPS (AD9695-1300 speed grade), DCS on (AD9695-1300 speedgrade), DCS off (AD9695-625 speed grade), unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of −40°C to +105°C. Typical specifications represent performance at T_J = 35°C (T_A = 25°C for the AD9695-625 speed grade) and T_J = 40°C (T_A = 25°C for the AD9695-1300 speed grade).

Table 1.

	1300 MSPS			625 MSPS			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	14			14			Bits
ACCURACY							
No Missing Codes		Guaranteed			Guaranteed		
Offset Error[1]		5			5		Codes
Offset Matching	−0.48	0	+0.48	−0.25	0	+0.25	% FSR
Gain Error	−2.9	±1	+2.9	−2.6	±2.22	+2.6	% FSR
Gain Matching	−2.64	±0.18	+2.64	−2.5	±0.18	+2.5	% FSR
Differential Nonlinearity (DNL)	−0.7		0.8	−0.8		+0.8	LSB
Integral Nonlinearity (INL)	−7	±1	5	−5	±2	+5	LSB
TEMPERATURE DRIFT							
Offset Error		±9			±6		ppm/°C
Gain Error		69			123		ppm/°C
INTERNAL VOLTAGE REFERENCE							
Voltage		0.5			0.5		V
INPUT-REFERRED NOISE		3.8			2.7		LSB rms
ANALOG INPUTS							
Differential Input Voltage Range	1.36	1.59	2.04	1.36	1.7	2.04	V p-p
Common-Mode Voltage (V_{CM})		1.41			1.41		V
Differential Input Resistance		200			200		Ω
Differential Input Capacitance		1.75			1.75		pF
Analog Full-Power Bandwidth		2			2		GHz
POWER SUPPLY							
AVDD1	0.93	0.95	0.98	0.93	0.95	0.98	V
AVDD2	1.71	1.8	1.89	1.71	1.8	1.89	V
AVDD3	2.44	2.5	2.56	2.44	2.5	2.56	V
AVDD1_SR	0.93	0.95	0.98	0.93	0.95	0.98	V
DVDD	0.93	0.95	0.98	0.93	0.95	0.98	V
DRVDD1	0.93	0.95	0.98	0.93	0.95	0.98	V
DRVDD2	1.71	1.8	1.89	1.71	1.8	1.89	V
SPIVDD[2]	1.71	1.8	1.89	1.71	1.8	1.89	V
I_{AVDD1}		304	383		182	257	mA
I_{AVDD2}		450	500		267	292	mA
I_{AVDD3}		55	61		29	35	mA
I_{AVDD1_SR}		15	27		9	15	mA
I_{DVDD}		218	400		103	293	mA
I_{DRVDD1}[3]		146	229		103	176	mA
I_{DRVDD2}		25	29		28	35	mA
I_{SPIVDD}		2	5		2	5	mA
POWER CONSUMPTION							
Total Power Dissipation (Including Output Drivers)[4]	1.39	1.6	2	0.86	0.98	1.35	W
Power-Down Dissipation		215			200		mW
Standby[5]		890			740		mW

[1] DC offset calibration on (Register 0x0701, Bit 7 = 1 and Register 0x073B, Bit 7 = 0).
[2] The voltage level on the SPIVDD rail and on the DRVDD2 rail must be the same.
[3] All lanes running. Power dissipation on DRVDD changes with lane rate and number of lanes used.
[4] Default mode. No DDCs used.
[5] Can be controlled by SPI.

AC SPECIFICATIONS—1300 MSPS

AVDD1 = 0.95 V, AVDD1_SR = 0.95 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.95 V, DRVDD1 = 0.95 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, clock divider = 2, default input full scale, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, and sample rate = 1300 MSPS, DCS on, buffer current settings specified in Table 11, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of −40°C to +105°C. Typical specifications represent performance at T_J = 40°C (T_A = 25°C for the AD9695-1300 speed grade).

Table 2.

	Analog Input Full Scale = 1.36 V p-p			Analog Input Full Scale = 1.59 V p-p			Analog Input Full Scale = 2.04 V p-p			
Parameter[1]	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
ANALOG INPUT FULL SCALE		1.36			1.59			2.04		V p-p
NOISE DENSITY[2]		−152.6			−153.9			−155.6		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)										
f_{IN} = 10.3 MHz		64.4			65.7			67.5		dBFS
f_{IN} = 172.3 MHz		64.4		64.5	65.6			67.5		dBFS
f_{IN} = 340 MHz		64.3			65.6			67.3		dBFS
f_{IN} = 750 MHz		64.0			65.2			66.6		dBFS
f_{IN} = 1000 MHz		63.8			64.9			66.1		dBFS
f_{IN} = 1400 MHz		63.2			64.2			65.2		dBFS
f_{IN} = 1700 MHz		62.7			63.6			64.5		dBFS
f_{IN} = 1980 MHz		62.3			63.0			63.9		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)										
f_{IN} = 10.3 MHz		64.3			65.4			66.1		dBFS
f_{IN} = 172.3 MHz		64.3		64.3	65.4			66.2		dBFS
f_{IN} = 340 MHz		64.2			65.3			65.7		dBFS
f_{IN} = 750 MHz		63.9			65.0			65.5		dBFS
f_{IN} = 1000 MHz		63.6			64.7			65.7		dBFS
f_{IN} = 1400 MHz		63.1			63.8			62.9		dBFS
f_{IN} = 1700 MHz		62.6			63.4			64.2		dBFS
f_{IN} = 1980 MHz		62.1			62.8			61.8		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)										
f_{IN} = 10.3 MHz		10.3			10.5			10.6		Bits
f_{IN} = 172.3 MHz		10.3		10.3	10.5			10.7		Bits
f_{IN} = 340 MHz		10.3			10.5			10.6		Bits
f_{IN} = 750 MHz		10.3			10.5			10.5		Bits
f_{IN} = 1000 MHz		10.2			10.4			10.6		dBFS
f_{IN} = 1400 MHz		10.1			10.3			10.1		dBFS
f_{IN} = 1700 MHz		10.1			10.2			10.3		dBFS
f_{IN} = 1980 MHz		10.0			10.1			9.9		dBFS
SPURIOUS FREE DYNAMIC RANGE (SFDR)										
f_{IN} = 10.3 MHz		81			79			73		dBFS
f_{IN} = 172.3MHz		81		74	78			72		dBFS
f_{IN} = 340 MHz		80			77			71		dBFS
f_{IN} = 750 MHz		83			80			72		dBFS
f_{IN} = 1000 MHz		82			81			79		dBFS
f_{IN} = 1400 MHz		80			76			67		dBFS
f_{IN} = 1700 MHz		80			80			78		dBFS
f_{IN} = 1980 MHz		81			79			68		dBFS

Parameter[1]	Analog Input Full Scale = 1.36 V p-p			Analog Input Full Scale = 1.59 V p-p			Analog Input Full Scale = 2.04 V p-p			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
WORST OTHER, EXCLUDING 2ND OR 3RD HARMONIC										
f_{IN} = 10.3 MHz		−96			−94			−101		dBFS
f_{IN} = 172.3 MHz		−95			−96	−85		−95		dBFS
f_{IN} = 340 MHz		−98			−99			−98		dBFS
f_{IN} = 750 MHz		−95			−95			−92		dBFS
f_{IN} = 1000 MHz		−96			−93			−91		dBFS
f_{IN} = 1400 MHz		−90			−89			−86		dBFS
f_{IN} = 1700 MHz		−91			−90			−84		dBFS
f_{IN} = 1980 MHz		−90			−90			−77		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD), AIN1 AND AIN2 = −7.0 dBFS										
f_{IN1} = 170.8 MHz, f_{IN2} = 173.8 MHz		−84			−84			−83		dBFS
f_{IN1} = 343.5 MHz, f_{IN2} = 346.5 MHz		−83			−82			−81		dBFS
CROSSTALK[3]		>95			>95			>95		dB
Overrange Condition[4]		>95			>95			>95		dB
ANALOG INPUT BANDWIDTH, FULL POWER[5]		2			2			2		GHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Noise density is measured at a low analog input frequency (10 MHz).
[3] Crosstalk is measured at 10 MHz with a −1.0 dBFS analog input on one channel, and no input on the adjacent channel.
[4] The overrange condition is specified with 3 dB of the full-scale input range.
[5] Full power bandwidth is the bandwidth of operation to achieve proper ADC performance.

AC SPECIFICATIONS—625 MSPS

AVDD1 = 0.95 V, AVDD1_SR = 0.95 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.95 V, DRVDD1 = 0.95 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, clock divider = 2, default input full scale, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, and sample rate = 625 MSPS, DCS off, buffer current setting specified in Table 11, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of −40°C to +105°C. Typical specifications represent performance at T_J = 35°C (T_A = 25°C for the AD9695-625 speed grade).

Table 3.

	Analog Input Full Scale = 1.36 V p-p			Analog Input Full Scale = 1.7 V p-p			Analog Input Full Scale = 2.04 V p-p			
Parameter[1]	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
ANALOG INPUT FULL SCALE		1.36			1.7			2.04		V p-p
NOISE DENSITY[2]		−150.5			−152.3			−153.5		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)										
f_{IN} = 10.3 MHz		65.5			67.3			68.6		dBFS
f_{IN} = 172.3 MHz		65.4		65.5	67.2			68.5		dBFS
f_{IN} = 340 MHz		65.4			67.1			68.3		dBFS
f_{IN} = 750 MHz		65.0			66.6			67.7		dBFS
f_{IN} = 1000 MHz		64.8			66.3			67.3		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)										
f_{IN} = 10.3 MHz		65.5			66.9			67.2		dBFS
f_{IN} = 172.3 MHz		65.4		66.3	67.0			68.0		dBFS
f_{IN} = 340 MHz		65.2			67.0			67.9		dBFS
f_{IN} = 750 MHz		64.9			65.4			67.0		dBFS
f_{IN} = 1000 MHz		64.6			65.0			67.0		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)										
f_{IN} = 10.3 MHz		10.6			10.8			10.9		Bits
f_{IN} = 172.3 MHz		10.6		10.6	10.8			11.0		Bits
f_{IN} = 340 MHz		10.5			10.8			11.0		Bits
f_{IN} = 750 MHz		10.5			10.6			10.8		Bits
f_{IN} = 1000 MHz		10.4			10.5			10.8		Bits
SPURIOUS FREE DYNAMIC RANGE (SFDR)										
f_{IN} = 10.3 MHz		88			79			74		dBFS
f_{IN} = 172.3MHz		88		75	89			78		dBFS
f_{IN} = 340 MHz		79			80			77		dBFS
f_{IN} = 750 MHz		83			84			77		dBFS
f_{IN} = 1000 MHz		85			83			82		dBFS
WORST OTHER, EXCLUDING 2ND OR 3RD HARMONIC										
f_{IN} = 10.3 MHz		−100			−101			−99		dBFS
f_{IN} = 172.3 MHz		−101			−97	−90		−99		dBFS
f_{IN} = 340 MHz		−100			−102			−98		dBFS
f_{IN} = 750 MHz		−98			−98			−100		dBFS
f_{IN} = 1000 MHz		−100			−98			−100		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD), AIN1 AND AIN2 = −7.0 dBFS										
f_{IN1} = 170.8 MHz, f_{IN2} = 173.8 MHz		−88			−88			−83		dBFS
f_{IN1} = 343.5 MHz, f_{IN2} = 346.5 MHz		−89			−89			−84		dBFS
CROSSTALK[3]		>95			>95			>95		dB
Overrange Condition[4]		>95			>95			>95		dB

Parameter[1]	Analog Input Full Scale = 1.36 V p-p			Analog Input Full Scale = 1.7 V p-p			Analog Input Full Scale = 2.04 V p-p			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ANALOG INPUT BANDWIDTH, FULL POWER[5]		2			2			2		GHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Noise density is measured at a low analog input frequency (10 MHz).
[3] Crosstalk is measured at 10 MHz with a −1.0 dBFS analog input on one channel, and no input on the adjacent channel.
[4] The overrange condition is specified with 3 dB of the full-scale input range.
[5] Full power bandwidth is the bandwidth of operation to achieve proper ADC performance.

DIGITAL SPECIFICATIONS

AVDD1 = 0.95 V, AVDD1_SR = 0.95 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.95 V, DRVDD1 = 0.95 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, clock divider = 2, default input full scale, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, and sample rate = 625 MSPS (AD9695-625 speed grade), sample rate = 1300 MSPS (AD9695-1300 speed grade), DCS on (AD9695-1300 speedgrade), DCS off (AD9695-625 speed grade), unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of −40°C to +105°C. Typical specifications represent performance at T_J = 35°C (T_A = 25°C for the AD9695-625 speed grade) and T_J = 40°C (T_A = 25°C for the AD9695-1300 speed grade).

Table 4.

Parameter	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)				
Logic Compliance		LVDS/LVPECL		
Differential Input Voltage	400	800	1600	mV p-p
Input Common-Mode Voltage		0.65		V
Input Resistance (Differential)		32		kΩ
Input Capacitance (Differential)			0.9	pF
SYSREF INPUTS (SYSREF+, SYSREF−)				
Logic Compliance		LVDS/LVPECL		
Differential Input Voltage	400	800	1800	mV p-p
Input Common-Mode Voltage		0.65	2	V
Input Resistance (Differential)		18		kΩ
Input Capacitance (Differential)		1		pF
LOGIC INPUTS (SDIO, SCLK, CSB, PDWN/STBY, FD_A/GPIO_A0, FD_B/GPIO_B0)				
Logic Compliance		CMOS		
Logic 1 Voltage	0.75 × SPIVDD			V
Logic 0 Voltage	0		0.35 × SPIVDD	V
Input Resistance		30		kΩ
LOGIC OUTPUT (SDIO, FD_A, FD_B)				
Logic Compliance		CMOS		
Logic 1 Voltage (I_{OH} = 4 mA)	SPIVDD − 0.45			V
Logic 0 Voltage (I_{OL} = 4 mA)	0		0.45	V
SYNCIN INPUTS (SYNCINB−, SYNCINB+)				
Logic Compliance		LVDS/LVPECL/CMOS		
Differential Input Voltage	400	800	1800	mV p-p
Input Common-Mode Voltage		0.65	2	V
Input Resistance (Differential)		18		kΩ
Input Capacitance (Single-Ended per Pin)		1		pF
DIGITAL OUTPUTS (SERDOUTx±, x = 0 TO 3)				
Logic Compliance		SST		
Differential Output Voltage	360	520	770	mV p-p
Differential Termination Impedance	80	100	1200	Ω

SWITCHING SPECIFICATIONS

AVDD1 = 0.95 V, AVDD1_SR = 0.95 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.95 V, DRVDD1 = 0.95 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, clock divider = 2, default input full scale, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, and sample rate = 625 MSPS (AD9695-625 speed grade), sample rate = 1300 MSPS (AD9695-1300 speed grade), DCS on (AD9695-1300 speedgrade), DCS off (AD9695-625 speed grade), unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of −40°C to +105°C. Typical specifications represent performance at T_J = 35°C (T_A = 25°C for the AD9695-625 speed grade) and T_J = 40°C (T_A = 25°C for the AD9695-1300 speed grade).

Table 5.

	1300 MSPS			625 MSPS			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK							
Clock Rate (at CLK+/CLK− Pins)	0.24		2.8	0.24		2.8	GHz
Maximum Sample Rate[1]	1400			640			MSPS
Minimum Sample Rate[2]	240			240			MSPS
Clock Pulse Width[3]							
High	156.25			156.25			ps
Low	156.25			156.25			ps
OUTPUT PARAMETERS							
Unit Interval (UI)[4]	62.5	76.9		62.5	160		ps
Rise Time (t_R) (20% to 80% into 100 Ω Load)		28			28		ps
Fall Time (t_F) (20% to 80% into 100 Ω Load)		28			28		ps
Phase-Locked Loop (PLL) Lock Time		5			5		ms
Data Rate per Channel (NRZ)[5]	1.6875	13	16	1.6875	6.25	16	Gbps
LATENCY[6]							
Pipeline Latency		56			56		Clock cycles
Fast Detect Latency		26			26		Clock cycles
Wake-Up Time[7]							
Standby		400			400		us
Power-Down		15			15		ms
APERTURE							
Aperture Delay (t_A)		192			159.5		ps
Aperture Uncertainty (Jitter, t_J)		43			49.2		fs rms
Out of Range Recovery Time		1			1		Clock cycles

[1] The maximum sample rate is the clock rate after the divider.
[2] The minimum sample rate operates at 240 MSPS. See SPI Register 0x011A to reduce the threshold of the clock detect circuit.
[3] Clock duty stabilizer (DCS) on. See SPI Register 0x011C and 0x011E to enable DCS.
[4] Baud rate = 1/UI. A subset of this range can be supported.
[5] Default L = 4. This number can change based on the sample rate and decimation ratio.
[6] No DDCs used. L = 4, M = 2, and F = 1.
[7] Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 6.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLK+ to SYSREF+ TIMING REQUIREMENTS	See Figure 3				
t_{SU_SR}	Device clock to SYSREF+ setup time		−70		ps
t_{H_SR}	Device clock to SYSREF+ hold time		120		ps
SPI TIMING REQUIREMENTS	See Figure 4				
t_{DS}	Setup time between the data and the rising edge of SCLK	4			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK must be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK must be in a logic low state	10			ns
t_{ACCESS}	Maximum time delay between falling edge of SCLK and output data valid for a read operation		6	10	ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the CSB rising edge (not shown in Figure 4)	10			ns

Timing Diagrams

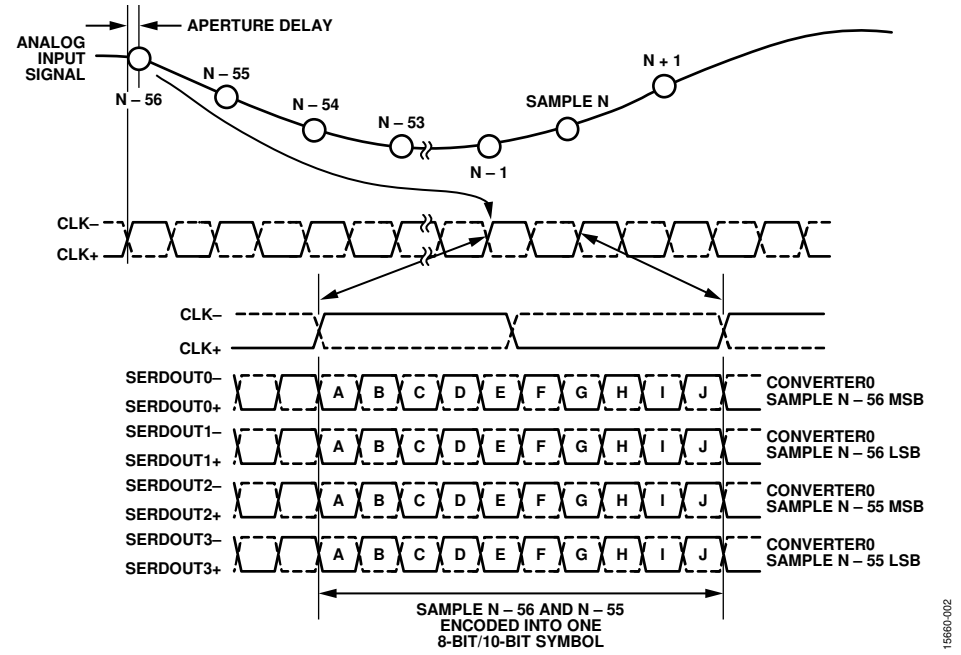

Figure 2. Data Output Timing Diagram

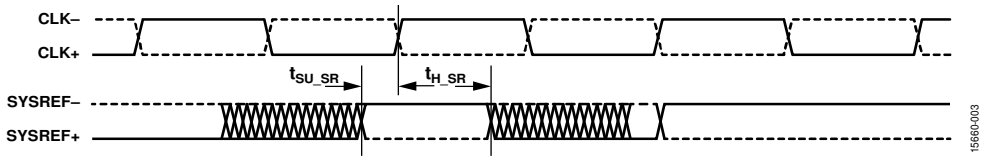

Figure 3. SYSREF± Setup and Hold Timing Diagram

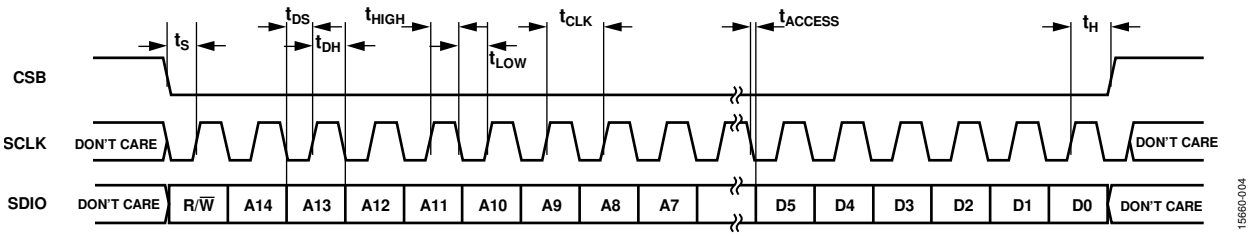

Figure 4. SPI Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Electrical	
AVDD1 to AGND	1.05 V
AVDD1_SR to AGND	1.05 V
AVDD2 to AGND	2.00 V
AVDD3 to AGND	2.70 V
DVDD to DGND	1.05 V
DRVDD1 to DRGND	1.05 V
DRVDD2 to DRGND	2.00 V
SPIVDD to DGND	2.00 V
AGND to DRGND	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
DGND to DRGND	−0.3 V to +0.3 V
VIN±x to AGND	AGND − 0.3 V to AVDD3 + 0.3 V
CLK± to AGND	AGND − 0.3 V to AVDD1 + 0.3 V
SCLK, SDIO, CSB to DGND	DGND − 0.3 V to SPIVDD + 0.3 V
PDWN/STBY to DGND	DGND − 0.3 V to SPIVDD + 0.3 V
SYSREF± to AGND	2.5 V
SYNCINB± to DRGND	2.5 V
Junction Temperature Range (T_J)	−40°C to +125°C
Storage Temperature Range, Ambient (T_A)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Typical θ_{JA}, θ_{JB}, and θ_{JC} are specified vs. the number of printed circuit board (PCB) layers in different airflow velocities (in m/sec). Airflow increases heat dissipation effectively reducing θ_{JA} and θ_{JB}. In addition, metal in direct contact with the package leads and exposed pad from metal traces, through holes, ground, and power planes, reduces θ_{JA}. Thermal performance for actual applications requires careful inspection of the conditions in an application. The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 7.

Table 8. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1,2]	θ_{JC_BOT}[1,3]	θ_{JC_TOP}[1,3]	θ_{JB}[1,4]	θ_{JT}[1,2]	Unit
CP-64-17	0	22.5	1.7	7.6	4.3	0.2	°C/W
	1.0	17.9					°C/W
	2.5	16.8					°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

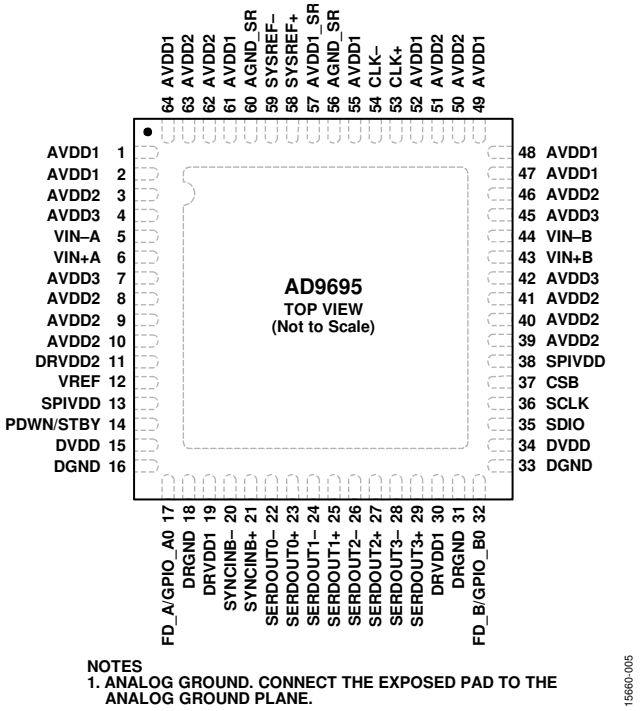

Figure 5. Pin Configuration (Top View)

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1, 2, 47 to 49, 52, 55, 61, 64	AVDD1	Power supply	Analog Power Supply (0.95 V Nominal).
3, 8 to 10, 39 to 41, 46, 50, 51, 62, 63	AVDD2	Power supply	Analog Power Supply (1.8 V Nominal).
4, 7, 42, 45	AVDD3	Power supply	Analog Power Supply (2.5 V Nominal).
5, 6	VIN−A, VIN+A	Analog input	ADC A Analog Input Complement/True.
11	DRVDD2	Power supply	Digital Driver Power Supply (1.8 V Nominal).
12	VREF	Input/output	Reference Voltage Input (0.50 V)/Do Not Connect. This pin is configurable through the SPI as a no connect pin or as an input. Do not connect this pin if using the internal reference. This pin requires a 0.50 V reference voltage input if using an external voltage reference source.
13, 38	SPIVDD	Power supply	Digital Power Supply for SPI (1.8 V Nominal).
14	PDWN/STBY	Digital control input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby.
15, 34	DVDD	Power supply	Digital Power Supply (0.95 V Nominal).
16, 33	DGND	Ground power supply	Digital Control Ground Supply. These pins connect to the digital ground plane.
17	FD_A/GPIO_A0	CMOS output	Fast Detect Output for Channel A (FD_A). General-purpose input/output (GPIO) Pin A0 (GPIO_A0).
32	FD_B/GPIO_B0	CMOS output	Fast Detect Output for Channel B (FD_B). GPIO Pin B0 (GPIO_B0).
18, 31	DRGND	Ground power supply	Digital Driver Ground Supply. This pin connects to the digital driver ground plane.
19, 30	DRVDD1	Power supply	Digital Driver Power Supply (0.95 V Nominal).
20	SYNCINB−	Digital input	Active Low JESD204B LVDS/CMOS Sync Input True.
21	SYNCINB+	Digital input	Active Low JESD204B LVDS Sync Input Complement.
22, 23	SERDOUT0−, SERDOUT0+	Data output	Lane 0 Output Data Complement/True.
24, 25	SERDOUT1−, SERDOUT1+	Data output	Lane 1 Output Data Complement/True.

Pin No.	Mnemonic	Type	Description
26, 27	SERDOUT2− SERDOUT2+	Data output	Lane 2 Output Data Complement/True.
28, 29	SERDOUT3−, SERDOUT3+	Data output	Lane 3 Output Data Complement/True.
35	SDIO	Digital control input/output	SPI Serial Data Input/Output.
36	SCLK	Digital control input	SPI Serial Clock.
37	CSB	Digital control input	SPI Chip Select (Active Low).
43, 44	VIN+B, VIN−B	Analog input	ADC B Analog Input True/Complement.
53, 54	CLK+, CLK−	Analog input	Clock Input True/Complement.
56, 60	AGND_SR	Ground power supply	Ground Reference for SYSREF±.
57	AVDD1_SR	Power supply	Analog Power Supply for SYSREF± (0.95 V Nominal).
58, 59	SYSREF+, SYSREF−	Digital input	Active High JESD204B LVDS System Reference Input Complement/True.
	EPAD	Ground power supply	Analog Ground. Connect the exposed pad to the analog ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

1300 MSPS

AVDD1 = 0.95 V, AVDD1_SR = 0.95 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.95 V, DRVDD1 = 0.95 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, clock divider = 2, default input full scale, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, sample rate = 625 MSPS (AD9695-625 speed grade), sample rate = 1300 MSPS (AD9695-1300 speed grade), DCS on (AD9695-1300 speedgrade), DCS off (AD9695-625 speed grade), buffer current setting specified in Table 11, dc offset calibration enabled, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of −40°C to +105°C. Typical specifications represent performance at T_J = 35°C (T_A = 25°C for the AD9695-625 speed grade) and T_J = 40°C (T_A = 25°C for the AD9695-1300 speed grade).

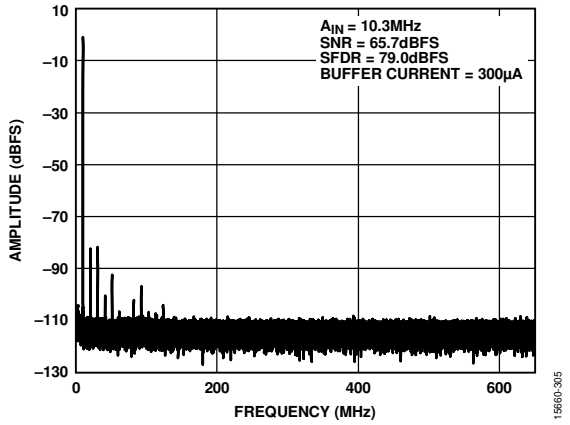

Figure 6. Single-Tone FFT with Analog Input Frequency (f_{IN}) = 10.3 MHz

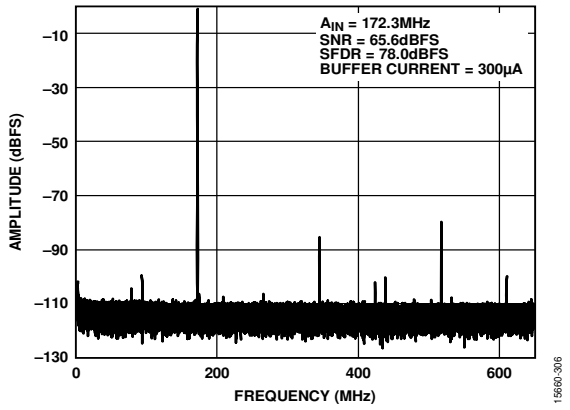

Figure 7. Single-Tone FFT with Analog Input Frequency (f_{IN}) = 172.3 MHz

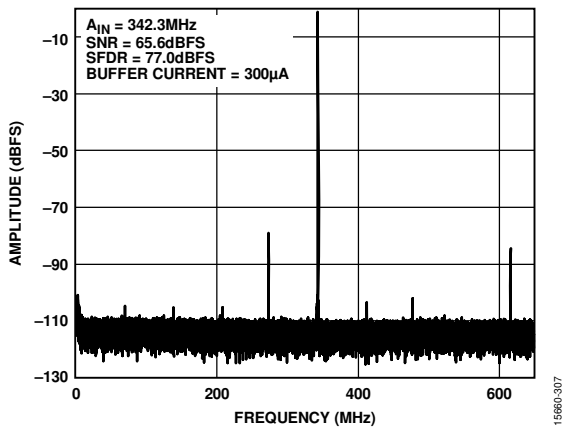

Figure 8. Single-Tone FFT with f_{IN} = 342.3 MHz

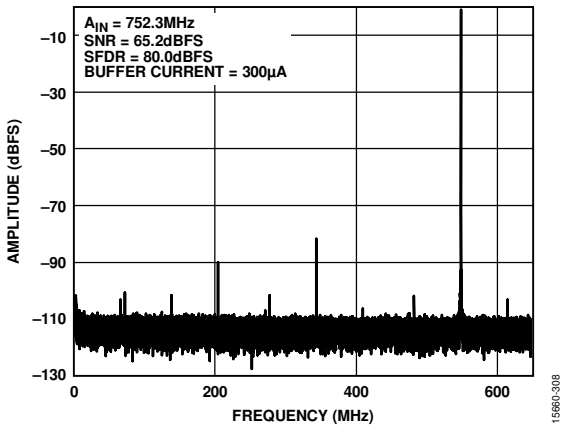

Figure 9. Single-Tone FFT with f_{IN} =752.3 MHz

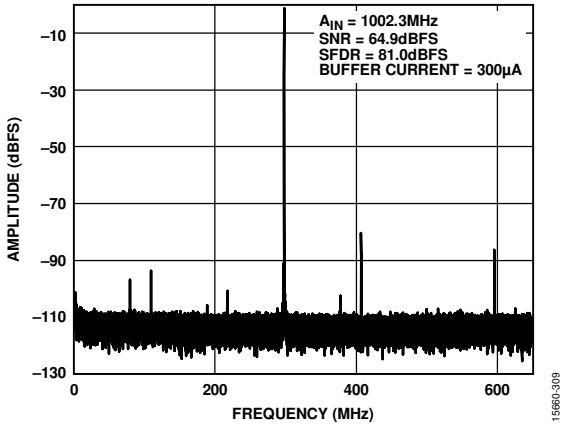

Figure 10. Single-Tone FFT with f_{IN} = 1002.3 MHz

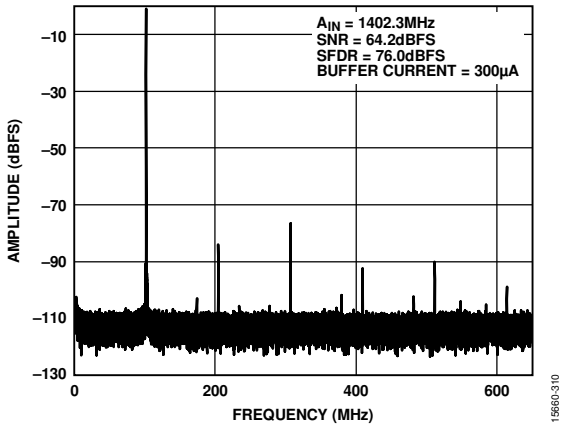

Figure 11. Single-Tone FFT with f_{IN} = 1402.3 MHz

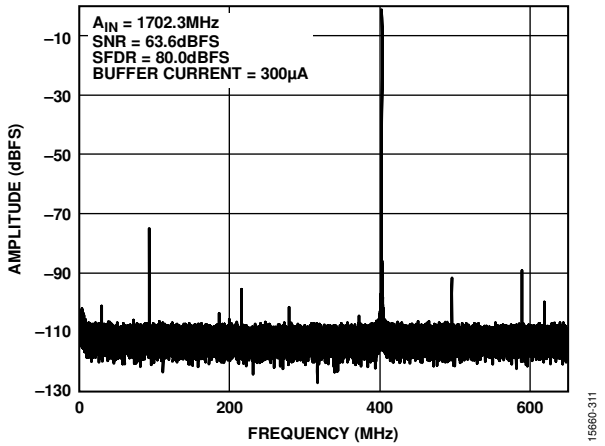

Figure 12. Single-Tone FFT with f_{IN} = 1702.3 MHz

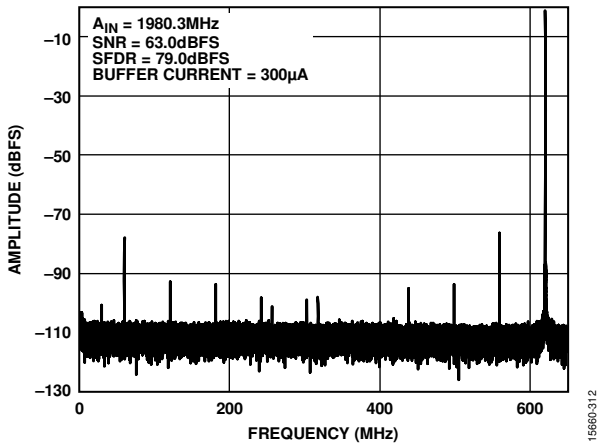

Figure 13. Single-Tone FFT with f_{IN} = 1980.3 MHz

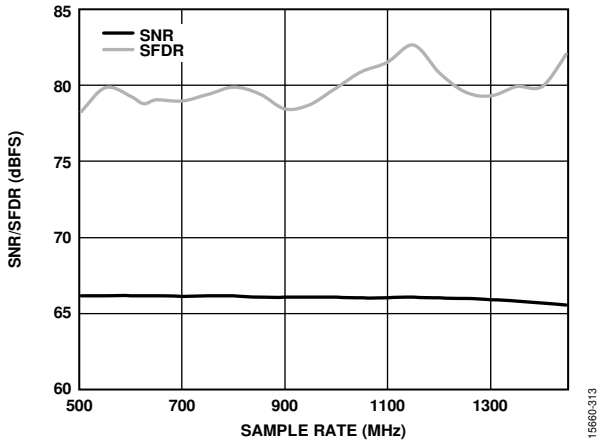

Figure 14. SNR/SFDR vs. Sample Rate, f_{IN} =172.3 MHz

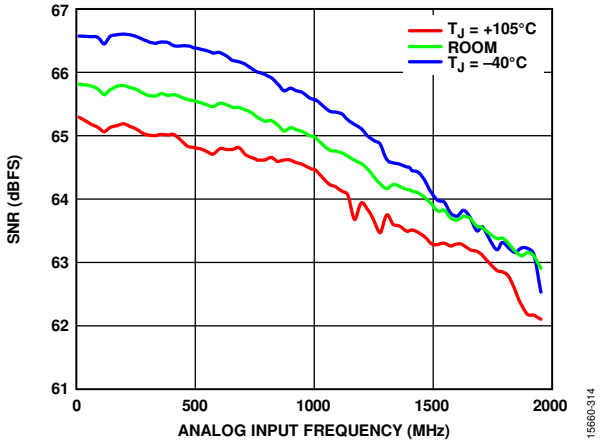

Figure 15. SNR vs. Analog Input Frequency (f_{IN}) at Minimum, Room, and Maximum Temperatures

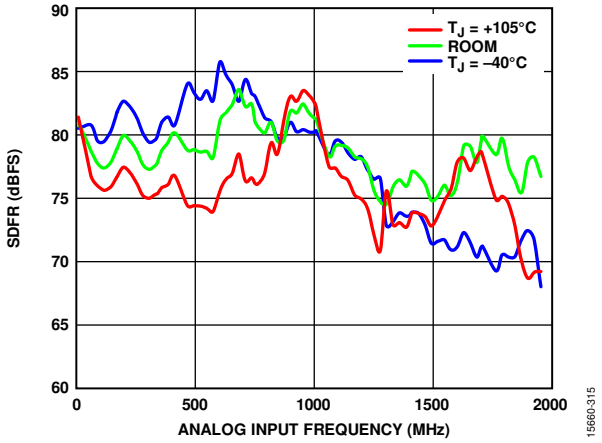

Figure 16. SFDR vs. Analog Input Frequency (f_{IN}) at Minimum, Room, and Maximum Temperatures

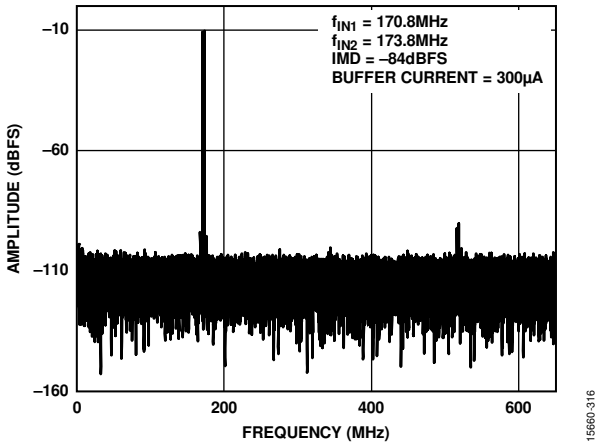

Figure 17. Two-Tone FFT; f_{IN1} = 170.8 MHz, f_{IN2} = 173.8 MHz

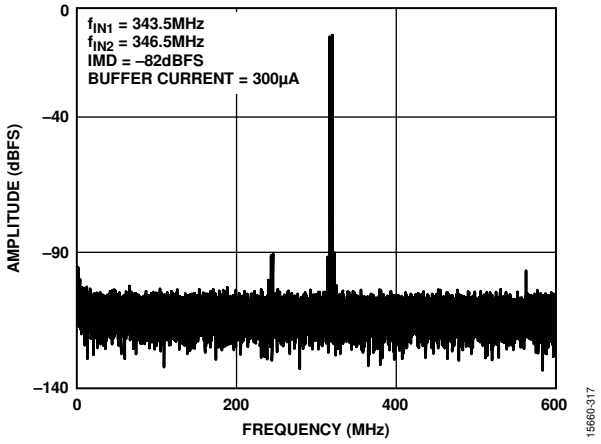

Figure 18. Two-Tone FFT; f_{IN1} = 343.5 MHz, f_{IN2} = 346.5 MHz

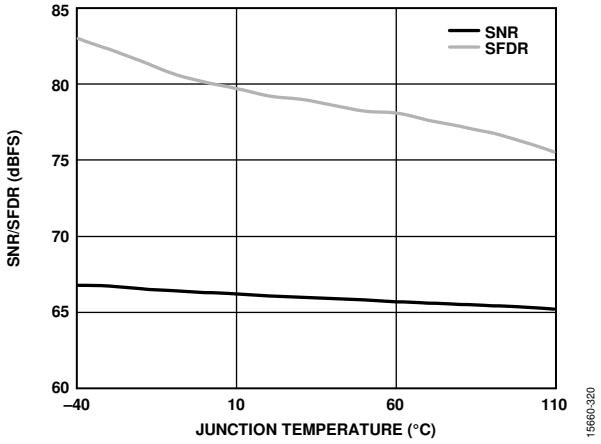

Figure 21. SNR/SFDR vs. Junction Temperature, f_{IN} = 172.3 MHz

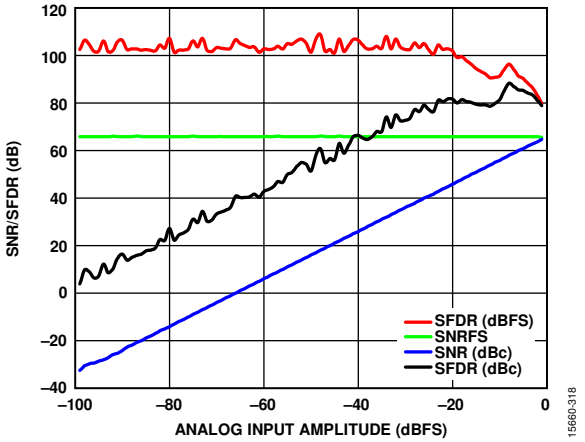

Figure 19. SNR/SFDR vs. Analog Input Amplitude, f_{IN} = 172.3 MHz

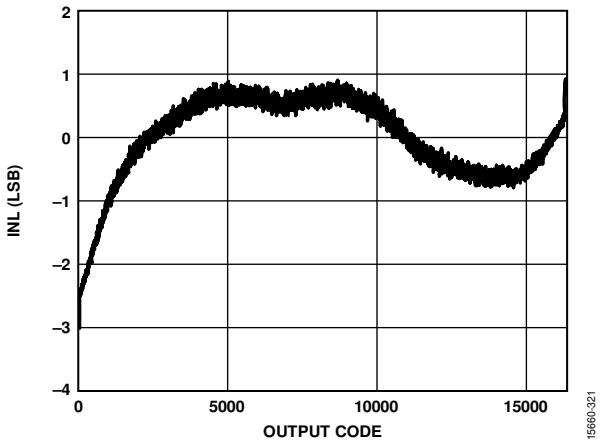

Figure 22. INL, f_{IN} = 10.3 MHz

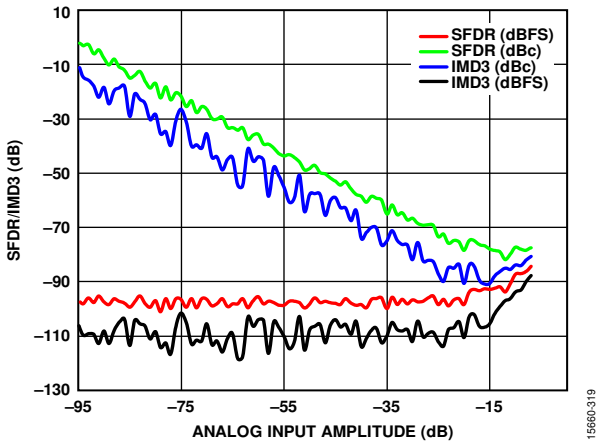

Figure 20. SFDR/IMD3 vs. Analog Input Amplitude, f_{IN} = 172.3 MHz

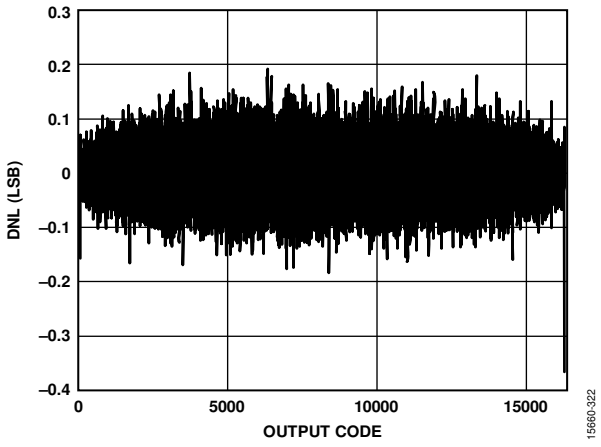

Figure 23. DNL, f_{IN} = 10.3 MHz

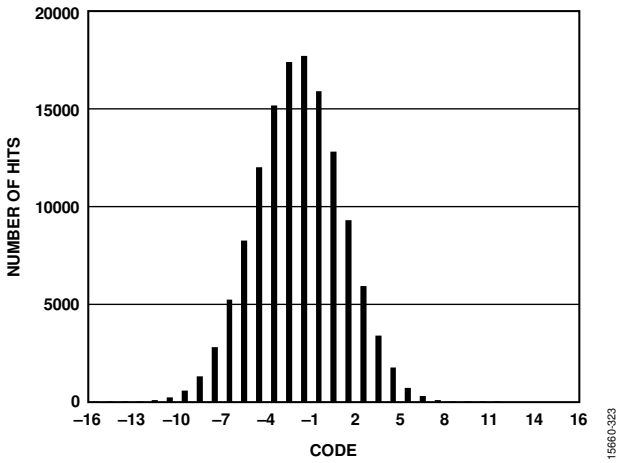

Figure 24. Input Referred Noise Histogram

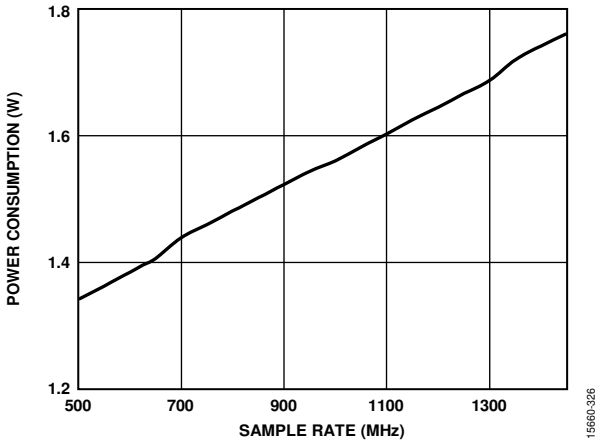

Figure 27. Total Power Dissipation vs. Sample Rate (f_S)

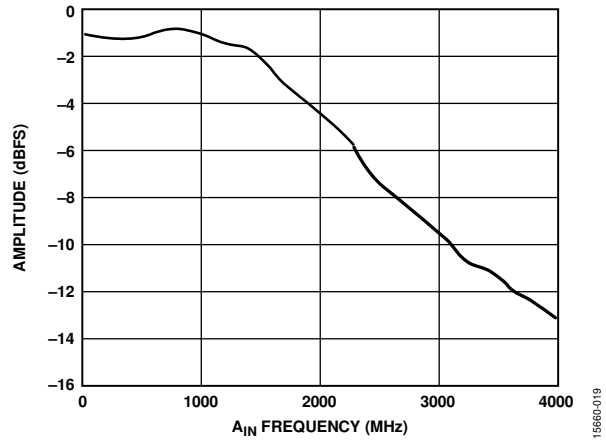

Figure 25. Full Power Bandwidth

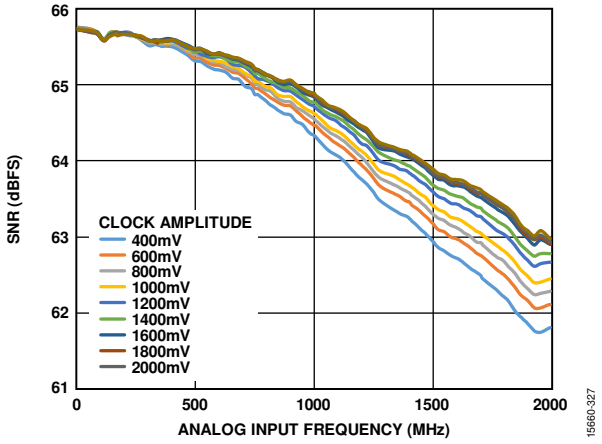

Figure 28. SNR vs. Analog Input Frequency at Different Clock Amplitudes

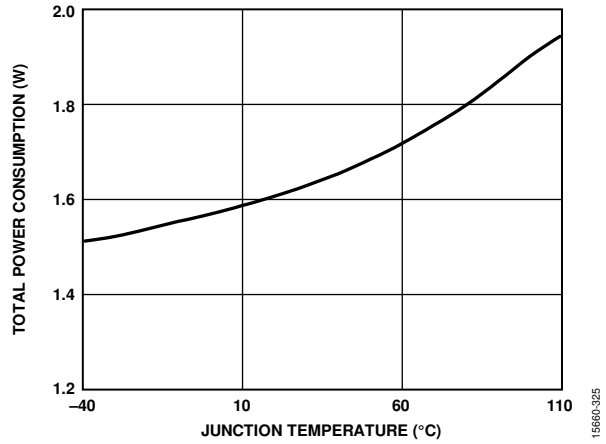

Figure 26. Total Power Dissipation vs. Junction Temperature

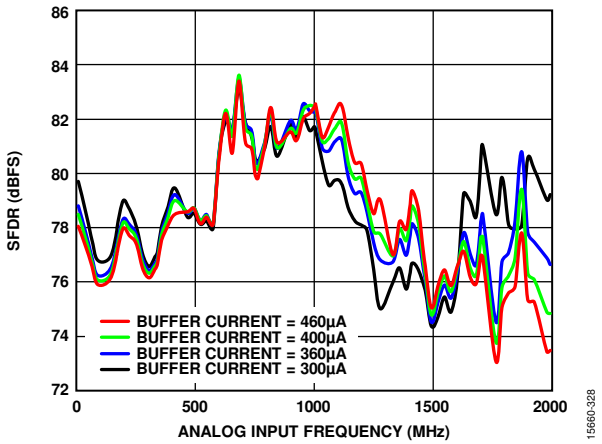

Figure 29. SFDR vs. Analog Input Frequency with Different Buffer Current Settings

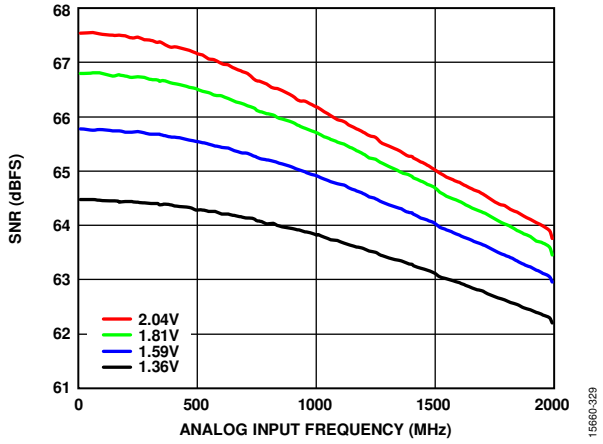

Figure 30. SNR vs. Analog Input Frequency with Different Analog Input Full-Scale Values

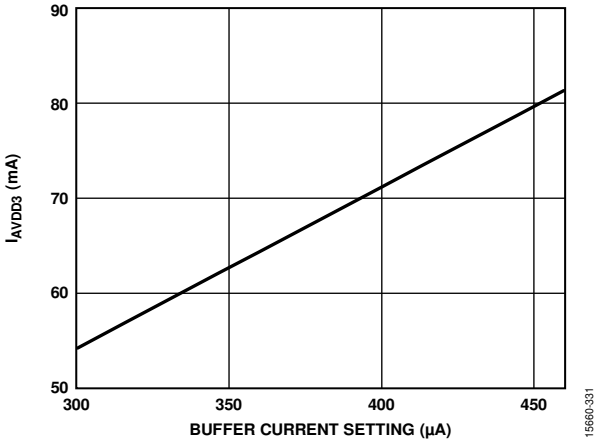

Figure 32. I_{AVDD3} vs. Buffer Control 1 Setting in Register 0x1A4C

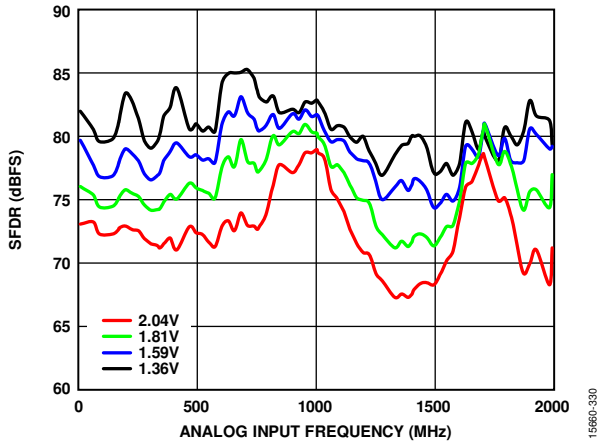

Figure 31. SFDR vs. Analog Input Frequency with Different Analog Input Full-Scale Values

625 MSPS

AVDD1 = 0.95 V, AVDD1_SR = 0.95 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.95 V, DRVDD1 = 0.95 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, clock divider = 2, default input full scale, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, sample rate = 625 MSPS (AD9695-625 speed grade), sample rate = 1300 MSPS (AD9695-1300 speed grade), DCS on (AD9695-1300 speedgrade), DCS off (AD9695-625 speed grade), buffer current setting specified in Table 11, and dc offset calibration enabled, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of −40°C to +105°C. Typical specifications represent performance at T_J = 35°C (T_A = 25°C for the AD9695-625 speed grade) and T_J = 40°C (T_A = 25°C for the AD9695-1300 speed grade).

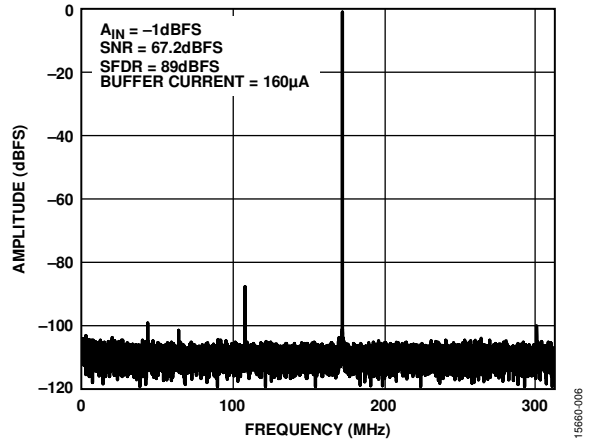

Figure 33. Single-Tone FFT with Analog Input Frequency (f_{IN}) = 172.3 MHz

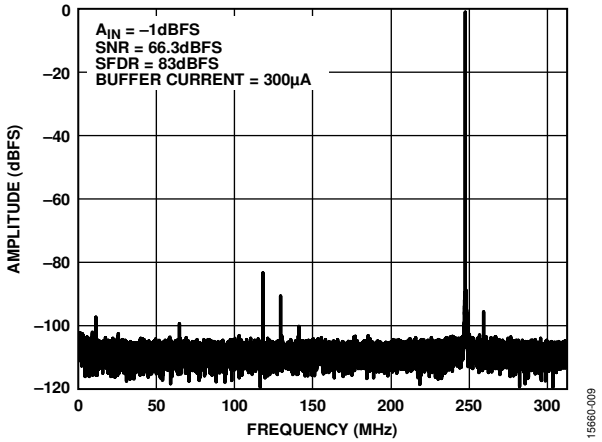

Figure 36. Single-Tone FFT with f_{IN} = 1000 MHz

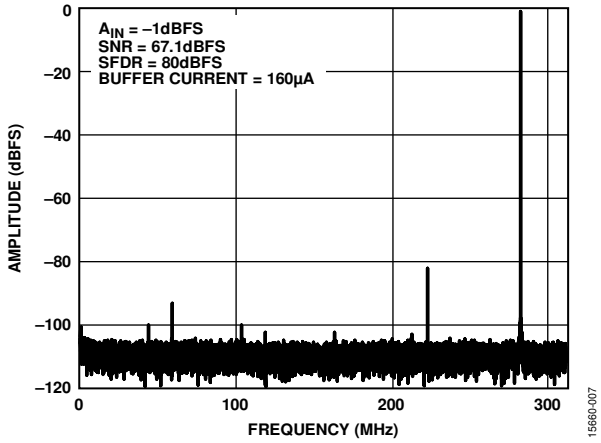

Figure 34. Single-Tone FFT with f_{IN} = 340 MHz

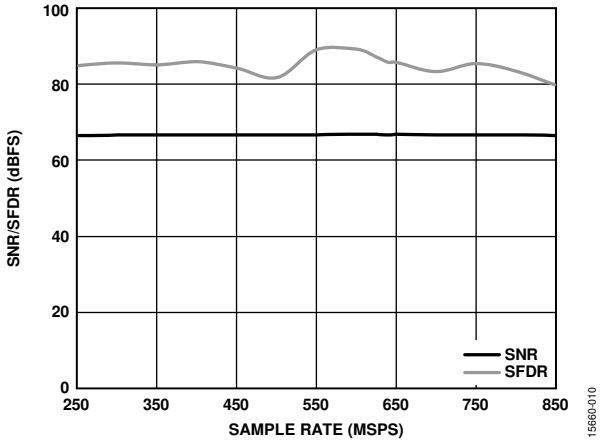

Figure 37. SNR/SFDR vs. Sample Rate, f_{IN} =172.3 MHz

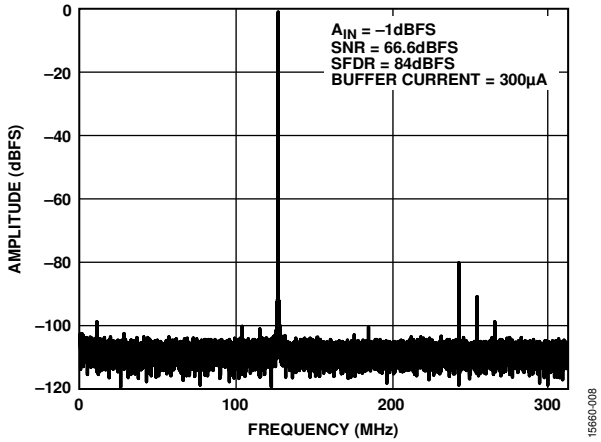

Figure 35. Single-Tone FFT with f_{IN} =750 MHz

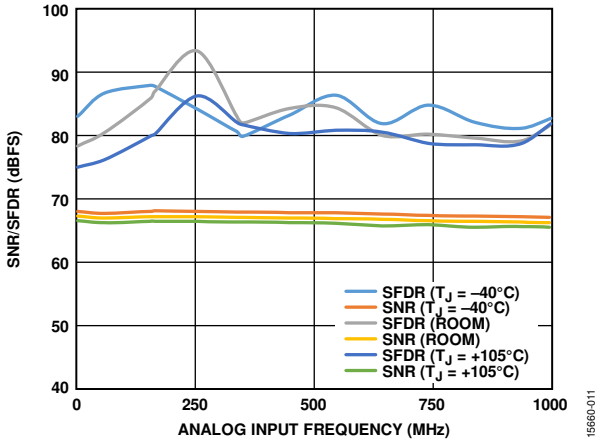

Figure 38. SNR/SFDR vs. Analog Input Frequency (f_{IN}) at Minimum, Room, and Maximum Temperatures

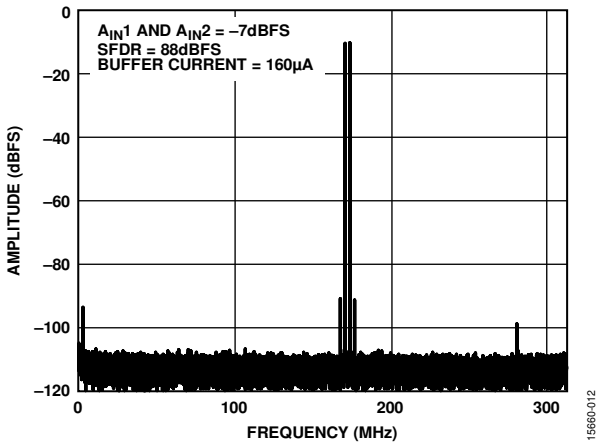

Figure 39. Two-Tone FFT; f_{IN1} = 170.8 MHz, f_{IN2} = 173.8 MHz

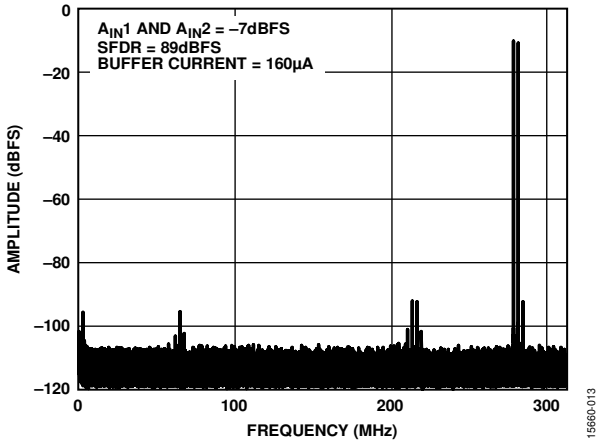

Figure 40. Two-Tone FFT; f_{IN1} = 343.5 MHz, f_{IN2} = 346.5 MHz

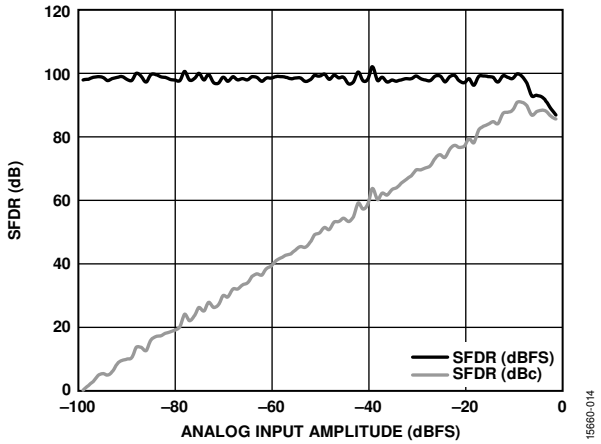

Figure 41. SNR/SFDR vs. Analog Input Amplitude, f_{IN} = 172.3 MHz

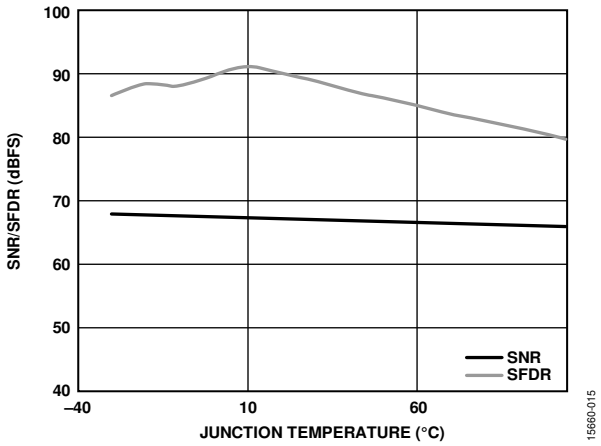

Figure 42. SNR/SFDR vs. Junction Temperature, f_{IN} = 172.3 MHz

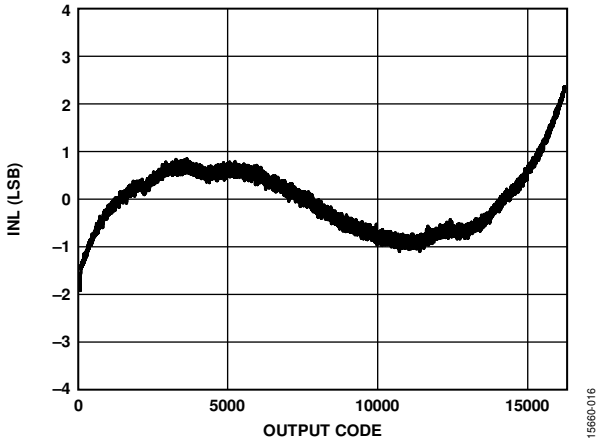

Figure 43. INL, f_{IN} = 10.3 MHz

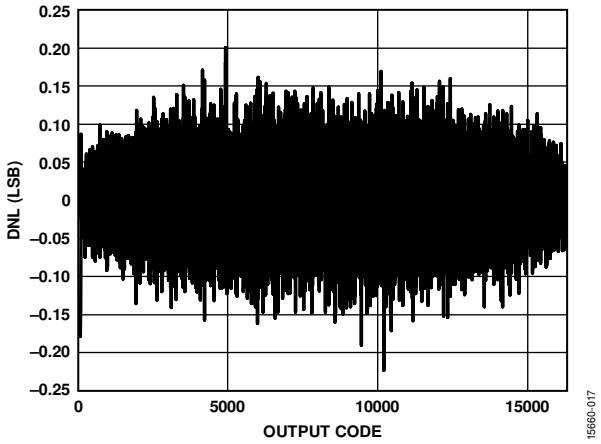

Figure 44. DNL, f_{IN} = 10.3 MHz

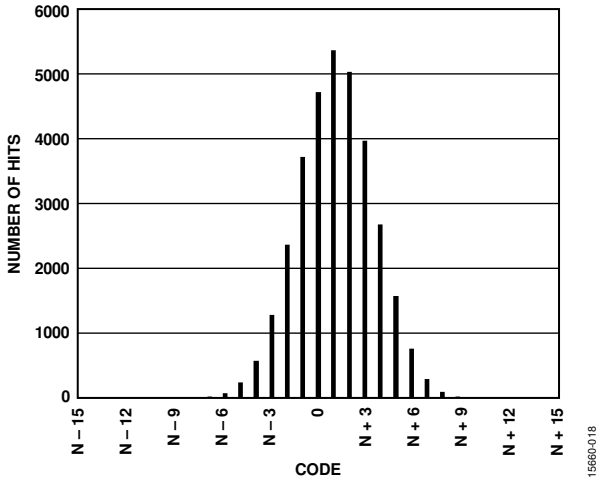

Figure 45. Input Referred Noise Histogram

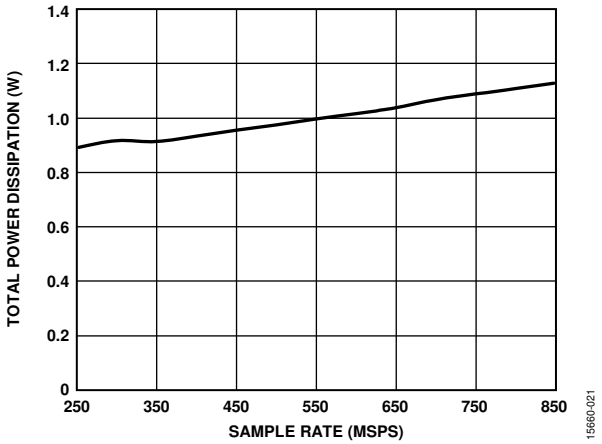

Figure 48. Total Power Dissipation vs. Sample Rate (f_S)

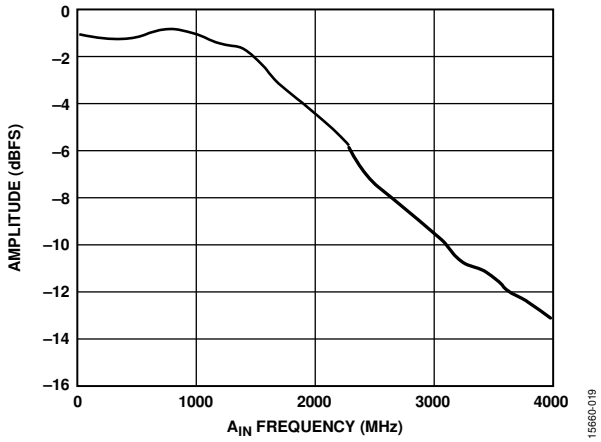

Figure 46. Full Power Bandwidth

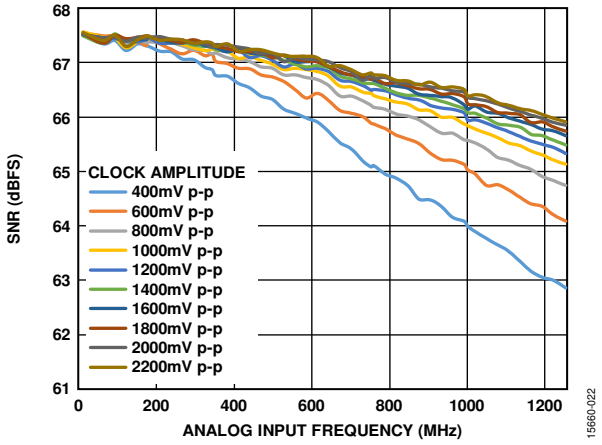

Figure 49. SNR vs. Analog Input Frequency at Different Clock Amplitudes

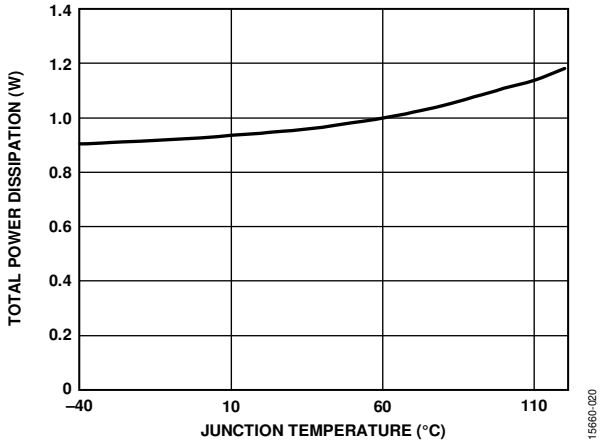

Figure 47. Total Power Dissipation vs. Junction Temperature

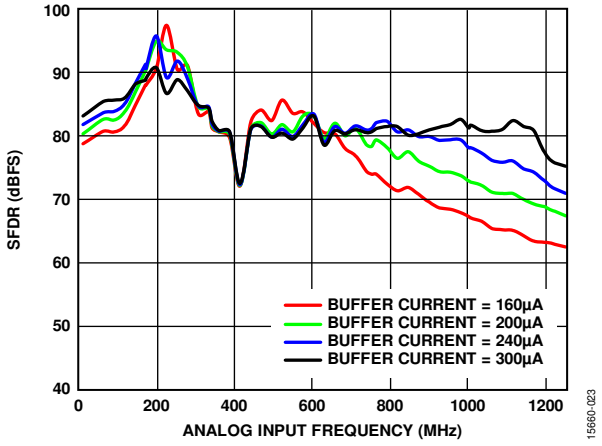

Figure 50. SFDR vs. Analog Input Frequency with Different Buffer Current Settings (A_{IN} < 1250 MHz)

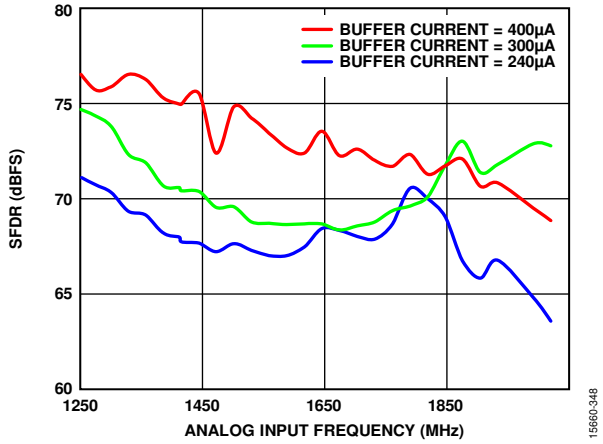

Figure 51. SFDR vs. Analog Input Frequency with Different Buffer Current Settings (A_{IN} > 1250 MHz), Register 0x1B03 = 0x02, Register 0x1B08 = 0xC1, Register 0x1B10 = 0x1C

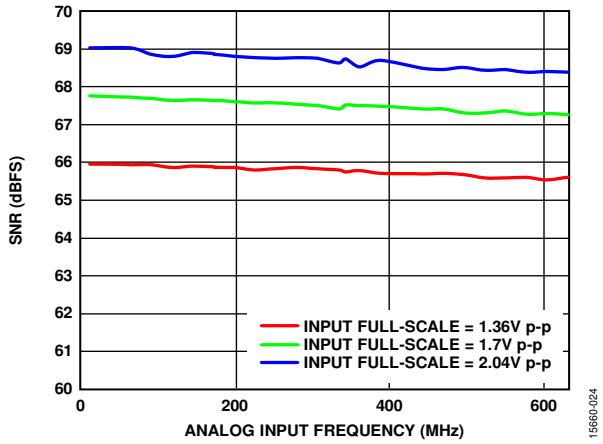

Figure 52. SNR vs. Analog Input Frequency with Different Analog Input Full-Scale Values (A_{IN} < 650 MHz)

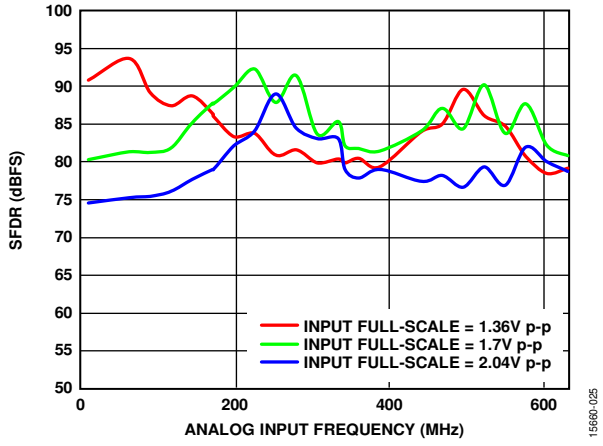

Figure 53. SFDR vs. Analog Input Frequency with Different Analog Input Full-Scale Values (A_{IN} < 650 MHz)

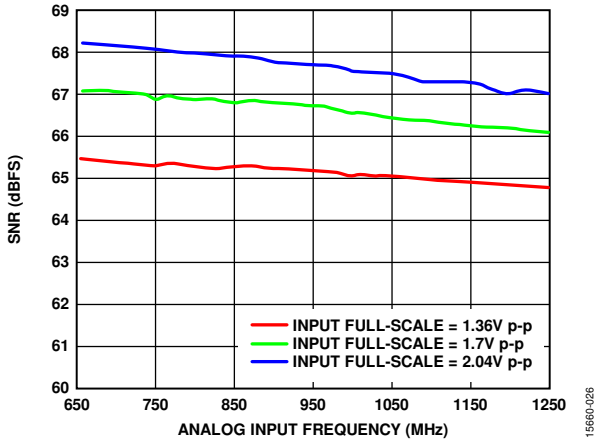

Figure 54. SNR vs. Analog Input Frequency with Different Analog Input Full-Scale Values (A_{IN} > 650 MHz)

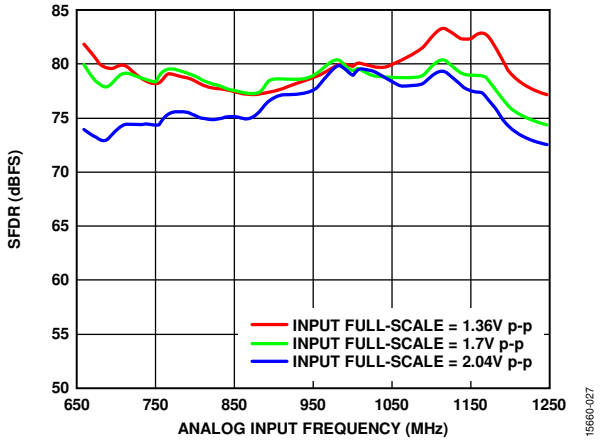

Figure 55. SFDR vs. Analog Input Frequency with Different Analog Input Full-Scale Values (A_{IN} > 650 MHz)

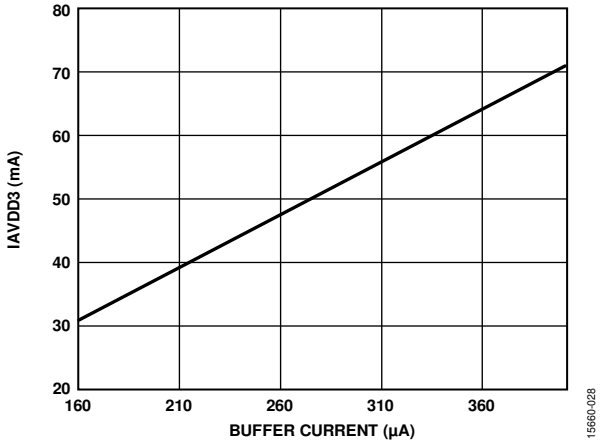

Figure 56. I_{AVDD3} vs. Buffer Control 1 Setting in Register 0x1A4C

EQUIVALENT CIRCUITS

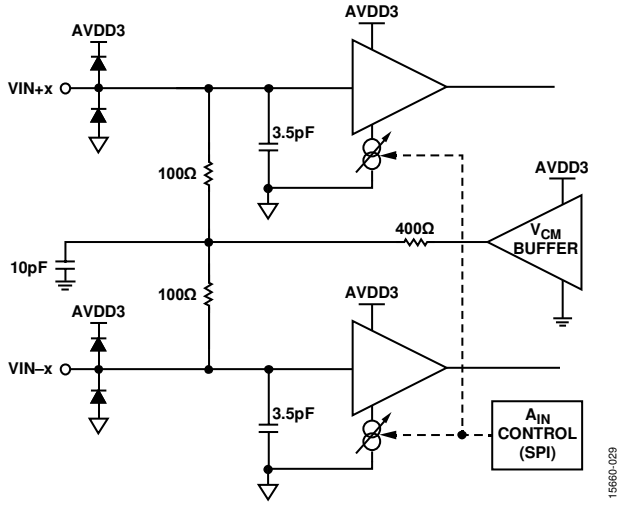

Figure 57. Analog Inputs

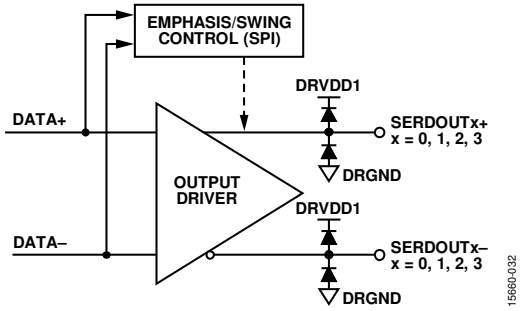

Figure 60. Digital Outputs

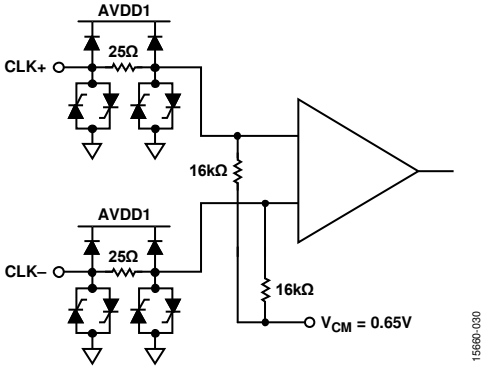

Figure 58. Clock Inputs

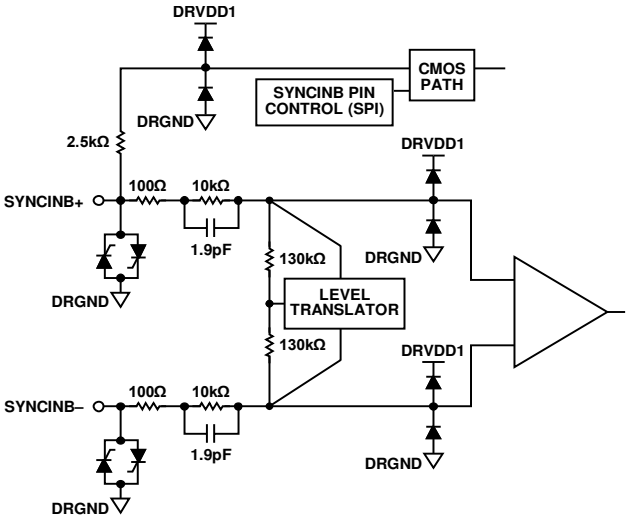

Figure 61. SYNCINB± Inputs

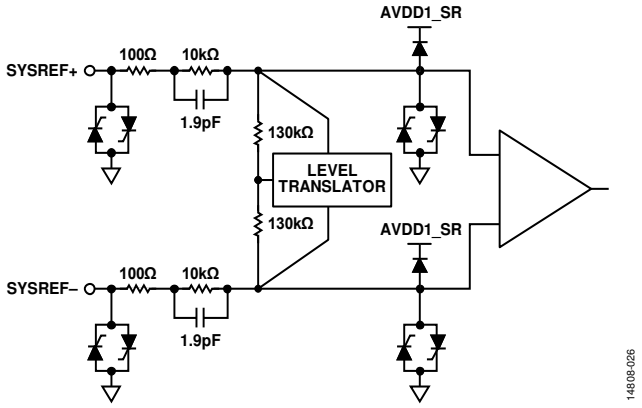

Figure 59. SYSREF± Inputs

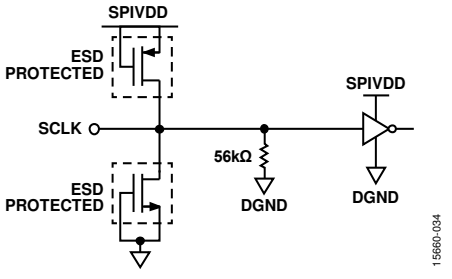

Figure 62. SCLK Input