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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

8-/10-/12-/14-Bit, 175 MSPS TxDAC Digital-to-Analog Converters

Data Sheet

AD9704/AD9705/AD9706/AD9707

FEATURES

175 MSPS update rate
Low power member of pin-compatible TxDAC product family
Low power dissipation
12 mW at 80 MSPS, 1.8 V
50 mW at 175 MSPS, 3.3 V
Wide supply voltage: 1.7 V to 3.6 V
SFDR to Nyquist
AD9707: 84 dBc at 5 MHz output
AD9707: 83 dBc at 10 MHz output
AD9707: 75 dBc at 20 MHz output
Adjustable full-scale current outputs: 1 mA to 5 mA
On-chip 1.0 V reference
CMOS-compatible digital interface
Common-mode output: adjustable 0 V to 1.2 V
Power-down mode <2 mW at 3.3 V (SPI controllable)
Self-calibration
Compact 32-lead LFCSP_VQ, RoHS compliant package

GENERAL DESCRIPTION

The AD9704/AD9705/AD9706/AD9707 are the fourth-generation family in the TxDAC series of high performance, CMOS digital-to-analog converters (DACs). This pin-compatible, 8-/10-/12-/14-bit resolution family is optimized for low power operation, while maintaining excellent dynamic performance. The AD9704/AD9705/AD9706/AD9707 family is pin-compatible with the AD9748/AD9740/AD9742/AD9744 family of TxDAC converters and is specifically optimized for the transmit signal path of communication systems. All of the devices share the same interface, LFCSP_VQ package, and pinout, providing an upward or downward component selection path based on performance, resolution, and cost. The AD9704/AD9705/AD9706/AD9707 offers exceptional ac and dc performance, while supporting update rates up to 175 MSPS.

The flexible power supply operating range of 1.7 V to 3.6 V and low power dissipation of the AD9704/AD9705/AD9706/AD9707 parts make them well-suited for portable and low power applications.

Power dissipation of the AD9704/AD9705/AD9706/AD9707 can be reduced to 15 mW, with a small trade-off in performance, by lowering the full-scale current output. In addition, a power-down mode reduces the standby power dissipation to approximately 2.2 mW.

The AD9704/AD9705/AD9706/AD9707 has an optional serial peripheral interface (SPI®) that provides a higher level of programmability to enhance performance of the DAC. An adjustable output, common-mode feature allows for easy interfacing to other components that require common modes from 0 V to 1.2 V.

Edge-triggered input latches and a 1.0 V temperature-compensated band gap reference have been integrated to provide a complete, monolithic DAC solution. The digital inputs support 1.8 V and 3.3 V CMOS logic families.

PRODUCT HIGHLIGHTS

1. Pin Compatible. The AD9704/AD9705/AD9706/AD9707 line of TxDAC® converters is pin-compatible with the AD9748/AD9740/AD9742/AD9744 TxDAC line (LFCSP_VQ package).
2. Low Power. Complete CMOS DAC operates on a single supply of 3.6 V down to 1.7 V, consuming 50 mW (3.3 V) and 12 mW (1.8 V). The DAC full-scale current can be reduced for lower power operation. Sleep and power-down modes are provided for low power idle periods.
3. Self-Calibration. Self-calibration enables true 14-bit INL and DNL performance in the AD9707.
4. Twos Complement/Binary Data Coding Support. Data input supports twos complement or straight binary data coding.
5. Flexible Clock Input. A selectable high speed, single-ended, and differential CMOS clock input supports 175 MSPS conversion rate.
6. Device Configuration. Device can be configured through pin strapping, and SPI control offers a higher level of programmability.
7. Easy Interfacing to Other Components. Adjustable common-mode output allows for easy interfacing to other signal chain components that accept common-mode levels from 0 V to 1.2 V.
8. On-Chip Voltage Reference. The AD9704/AD9705/AD9706/AD9707 include a 1.0 V temperature-compensated band gap voltage reference.
9. Industry-Standard 32-Lead LFCSP_VQ Package.

Rev. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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FUNCTIONAL BLOCK DIAGRAM

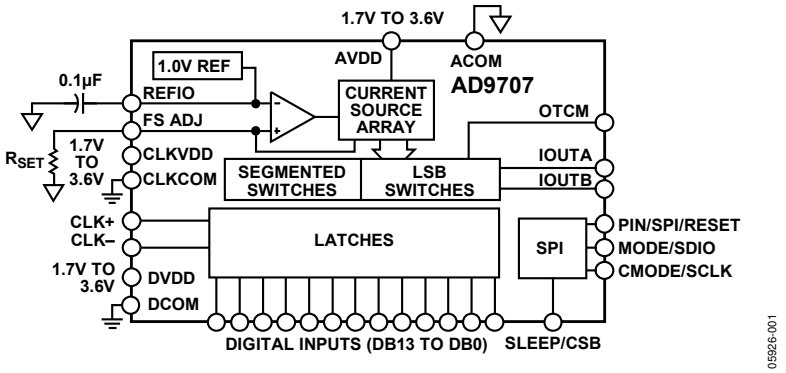

Figure 1.

SPECIFICATIONS

DC SPECIFICATIONS (3.3 V)

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V, I_{OUTFS} = 2 mA, unless otherwise noted.

Table 1.

	AD9707			AD9706			AD9705			AD9704			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	14			12			10			8			Bits
DC ACCURACY[1]													
Integral Nonlinearity (INL) Precalibration		±1.4	±6.0		±0.41	±1.48		±0.10	±0.36		±0.03	±0.09	LSB
Integral Nonlinearity (INL) Postcalibration		±0.9			±0.30			±0.10					LSB
Differential Nonlinearity (DNL) Precalibration		±1.2	±4.4		±0.35	±1.17		±0.09	±0.31		±0.02	±0.08	LSB
Differential Nonlinearity (DNL) Postcalibration		±0.4			±0.13			±0.03					LSB
ANALOG OUTPUT													
Offset Error	−0.03	0	+0.03	−0.03	0	+0.03	−0.03	0	+0.03	−0.03	0	+0.03	% of FSR
Gain Error (With External Reference)	−2.7	−0.1	+2.7	−2.7	−0.1	+2.7	−2.7	−0.1	+2.7	−2.7	−0.1	+2.7	% of FSR
Gain Error (With Internal Reference)	−2.7	−0.1	+2.7	−2.7	−0.1	+2.7	−2.7	−0.1	+2.7	−2.7	−0.1	+2.7	% of FSR
Full-Scale Output Current[2]	1	2	5	1	2	5	1	2	5	1	2	5	mA
Output Compliance Range (From OTCM to IOUTA/IOUTB)	−0.8		+0.8	−0.8		+0.8	−0.8		+0.8	−0.8		+0.8	V
Output Resistance		200			200			200			200		MΩ
Output Capacitance		5			5			5			5		pF
REFERENCE OUTPUT													
Reference Voltage	0.98	1.025	1.08	0.98	1.025	1.08	0.98	1.025	1.08	0.98	1.025	1.08	V
Reference Output Current[3]		100			100			100			100		nA
REFERENCE INPUT													
Input Compliance Range	0.1		1.25	0.1		1.25	0.1		1.25	0.1		1.25	V
Reference Input Resistance (Reference Powered Up)		10			10			10			10		kΩ
Reference Input Resistance (Reference Powered Down)		1			1			1			1		MΩ
TEMPERATURE COEFFICIENTS													
Offset Drift		0			0			0			0		ppm of FSR/°C
Gain Drift (Without Internal Reference)		±29			±29			±29			±29		ppm of FSR/°C
Gain Drift (With Internal Reference)		±40			±40			±40			±40		ppm of FSR/°C
Reference Voltage Drift		±25			±25			±25			±25		ppm/°C
POWER SUPPLY													
Supply Voltage													
AVDD		3.3	3.6		3.3	3.6		3.3	3.6		3.3	3.6	V
DVDD		3.3	3.6		3.3	3.6		3.3	3.6		3.3	3.6	V
CLKVDD		3.3	3.6		3.3	3.6		3.3	3.6		3.3	3.6	V
Analog Supply Current (I_{AVDD})		5.2	6.7		5.2	6.7		5.1	6.7		5.1	6.7	mA
Digital Supply Current (I_{DVDD})[4]		5.9	6.6		5.4	6.6		5.0	6.6		4.6	6.6	mA
Clock Supply Current (I_{CLKVDD})[4]		4.1	4.7		4.1	4.7		4.1	4.7		4.1	4.7	mA
Power Dissipation[4]		50.2	57		48.5	57		46.9	57		45.5	57	mW
Supply Current Sleep Mode (I_{AVDD})		0.37	0.4		0.37	0.4		0.37	0.4		0.37	0.4	mA

Parameter	AD9707 Min	AD9707 Typ	AD9707 Max	AD9706 Min	AD9706 Typ	AD9706 Max	AD9705 Min	AD9705 Typ	AD9705 Max	AD9704 Min	AD9704 Typ	AD9704 Max	Unit
Supply Current Power-Down Mode (I_{AVDD})		0.7	7.5		0.7	7.5		0.7	7.5		0.7	7.5	µA
Supply Current Clock Power-Down Mode (I_{DVDD})[5]		0.6	1		0.6	1		0.6	1		0.6	1	mA
Supply Current Clock Power-Down Mode (I_{CLKVDD})[5]		42.5	64		42.5	64		42.5	64		42.5	64	µA
Power Supply Rejection Ratio (AVDD)[6]	−0.2	+0.03	+0.2	−0.2	+0.03	+0.2	−0.2	+0.03	+0.2	−0.2	+0.03	+0.2	% of FSR/V
OPERATING RANGE	−40		+85	−40		+85	−40		+85	−40		+85	°C

[1] Measured at IOUTA, driving a virtual ground.
[2] Normal full scale current, I_{OUTFS} is 32 × the I_{REF} current.
[3] Use an external buffer amplifier with an input bias current <100 nA to drive any external load.
[4] Measured at f_{CLOCK} = 175 MSPS and f_{OUT} = 1.0 MHz, using a differential clock.
[5] Measured at f_{CLOCK} = 100 MSPS and f_{OUT} = 1.0 MHz, using a differential clock.
[6] ± 5% power supply variation.

DYNAMIC SPECIFICATIONS (3.3 V)

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V, I_{OUTFS} = 2 mA, differential transformer coupled output, 453 Ω differentially terminated unless otherwise noted.

Table 2.

Parameter	AD9707 Min	AD9707 Typ	AD9707 Max	AD9706 Min	AD9706 Typ	AD9706 Max	AD9705 Min	AD9705 Typ	AD9705 Max	AD9704 Min	AD9704 Typ	AD9704 Max	Unit
DYNAMIC PERFORMANCE													
Maximum Output Update Rate, f_{CLOCK}	175			175			175			175			MSPS
Output Settling Time, t_{ST} (to 0.1%)[1]		11			11			11			11		ns
Output Propagation Delay, t_{PD}		4			4			4			4		ns
Glitch Impulse		5			5			5			5		pV-s
Output Rise Time (10% to 90%)[1]		2.5			2.5			2.5			2.5		ns
Output Fall Time (10% to 90%)[1]		2.5			2.5			2.5			2.5		ns
AC LINEARITY													
Spurious-Free Dynamic Range to Nyquist													
f_{CLOCK} = 10 MSPS, f_{OUT} = 2.1 MHz		84			84			84			70		dBc
f_{CLOCK} = 25 MSPS, f_{OUT} = 2.1 MHz		84			83			84			68		dBc
f_{CLOCK} = 65 MSPS, f_{OUT} = 5.1 MHz		84			84			84			70		dBc
f_{CLOCK} = 65 MSPS, f_{OUT} = 10.1 MHz		83			83			83			71		dBc
f_{CLOCK} = 80 MSPS, f_{OUT} = 1.0 MHz	74	83		72	82		72	82		66	70		dBc
f_{CLOCK} = 125 MSPS, f_{OUT} = 15.1 MHz		78			78			78			68		dBc
f_{CLOCK} = 125 MSPS, f_{OUT} = 25.1 MHz		77			77			76			69		dBc
f_{CLOCK} = 175 MSPS, f_{OUT} = 20.1 MHz		75			75			75			69		dBc
f_{CLOCK} = 175 MSPS, f_{OUT} = 40.1 MHz		72			71			71			67		dBc
Noise Spectral Density													
f_{CLOCK} = 175 MSPS, f_{OUT} = 6.0 MHz, I_{OUTFS} = 2 mA		−152			−152			−144			−136		dBc/Hz
f_{CLOCK} = 175 MSPS, f_{OUT} = 6.0 MHz, I_{OUTFS} = 5 mA		−161											dBc/Hz
f_{CLOCK} = 175 MSPS, f_{OUT} = 6.0 MHz, I_{OUTFS} = 1 mA		−146											dBc/Hz

[1] Measured single-ended into 500 Ω load.

DIGITAL SPECIFICATIONS (3.3 V)

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V, I_{OUTFS} = 2 mA, unless otherwise noted.

Table 3.

	AD9707			AD9706			AD9705			AD9704			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DIGITAL INPUTS[1]													
Logic 1 Voltage	2.1	3		2.1	3		2.1	3		2.1	3		V
Logic 0 Voltage		0	0.9		0	0.9		0	0.9		0	0.9	V
Logic 1 Current	−10		+10	−10		+10	−10		+10	−10		+10	µA
Logic 0 Current			10			10			10			10	µA
Input Capacitance		5			5			5			5		pF
Input Setup Time, t_S, +25°C	1.4			1.4			1.4			1.4			ns
Input Hold Time, t_H, +25°C	0.3			0.3			0.3			0.3			ns
Input Setup Time, t_S, −40°C to +85°C	1.6			1.6			1.6			1.6			ns
Input Hold Time, t_H, −40°C to +85°C	0.6			0.6			0.6			0.6			ns
Latch Pulse Width, t_{LPW}	2.8			2.8			2.8			2.8			ns
CLK INPUTS[2]													
Input Voltage Range	0		3	0		3	0		3	0		3	V
Common-Mode Voltage	0.75	1.5	2.25	0.75	1.5	2.25	0.75	1.5	2.25	0.75	1.5	2.25	V
Differential Voltage	0.5	1.5		0.5	1.5		0.5	1.5		0.5	1.5		V

[1] Includes CLK+ pin in single-ended clock input mode.
[2] Applicable to CLK+ input and CLK– input when configured for differential clock input mode.

DC SPECIFICATIONS (1.8 V)

T_{MIN} to T_{MAX}, AVDD = 1.8 V, DVDD = 1.8 V, CLKVDD = 1.8 V, I_{OUTFS} = 2 mA, unless otherwise noted.

Table 4.

	AD9707			AD9706			AD9705			AD9704			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	14			12			10			8			Bits
DC ACCURACY[1]													
Integral Nonlinearity (INL) Precalibration		±1.4	±6.03		±0.42	±1.50		±0.10	±0.36		±0.03	±0.09	LSB
Differential Nonlinearity (DNL) Precalibration		±1.2	±4.34		±0.36	±1.17		±0.09	±0.30		±0.02	±0.07	LSB
ANALOG OUTPUT													
Offset Error	−0.03	0	+0.03	−0.03	0	+0.03	−0.03	0	+0.03	−0.03	0	+0.03	% of FSR
Gain Error (With Internal Reference)	−2.7	−0.2	+2.7	−2.7	−0.2	+2.7	−2.7	−0.2	+2.7	−2.7	−0.2	+2.7	% of FSR
Full-Scale Output Current[2]	1	2	2.5	1	2	2.5	1	2	2.5	1	2	2.5	mA
Output Compliance Range (With OTCM = AGND)	−0.8		+0.8	−0.8		+0.8	−0.8		+0.8	−0.8		+0.8	V
Output Resistance		200			200			200			200		MΩ
Output Capacitance		5			5			5			5		pF
REFERENCE OUTPUT													
Reference Voltage	0.98	1.025	1.08	0.98	1.025	1.08	0.98	1.025	1.08	0.98	1.025	1.08	V
Reference Output Current[3]		100			100			100			100		nA
REFERENCE INPUT													
Input Compliance Range	0.1		1.25	0.1		1.25	0.1		1.25	0.1		1.25	V
Reference Input Resistance (Reference Powered Up)		10			10			10			10		kΩ
Reference Input Resistance (External Reference)		1			1			1			1		MΩ
TEMPERATURE COEFFICIENTS													
Offset Drift		0			0			0			0		ppm of FSR/°C
Gain Drift (Without Internal Reference)		±30			±30			±30			±30		ppm of FSR/°C
Gain Drift (With Internal Reference)		±60			±60			±60			±60		ppm of FSR/°C
Reference Voltage Drift		±25			±25			±25			±25		ppm/°C
POWER SUPPLY													
Supply Voltage													
AVDD	1.7	1.8		1.7	1.8		1.7	1.8		1.7	1.8		V
DVDD	1.7	1.8		1.7	1.8		1.7	1.8		1.7	1.8		V
CLKVDD	1.7	1.8		1.7	1.8		1.7	1.8		1.7	1.8		V
Analog Supply Current (I_{AVDD})[4]		3.8	4.8		3.8	4.8		3.8	4.8		3.8	4.8	mA
Digital Supply Current (I_{DVDD})[4, 5]		1.3	1.5		1.2	1.5		1.1	1.5		1.0	1.5	mA
Clock Supply Current (I_{CLKVDD})[4, 5]		1.3	1.5		1.3	1.5		1.3	1.5		1.3	1.5	mA
Power Dissipation[4, 5]		11.5	13.2		11.3	13.2		11.1	13.2		11.0	13.2	mW
Supply Current Sleep Mode (I_{AVDD})		0.3	0.4		0.3	0.4		0.3	0.4		0.3	0.4	mA
Supply Current Power-Down Mode (I_{AVDD})		5	6		5	6		5	6		5	6	µA
Supply Current Clock Power-Down Mode (I_{DVDD})[5]		0.22	0.28		0.22	0.28		0.22	0.28		0.22	0.28	mA
Supply Current Clock Power-Down Mode (I_{CLKVDD})[5]		9.5	16		9.5	16		9.5	16		9.5	16	µA

Parameter	AD9707 Min	AD9707 Typ	AD9707 Max	AD9706 Min	AD9706 Typ	AD9706 Max	AD9705 Min	AD9705 Typ	AD9705 Max	AD9704 Min	AD9704 Typ	AD9704 Max	Unit
Power Supply Rejection Ratio (AVDD)[6]	−2	−0.1	+2	−2	−0.1	+2	−2	−0.1	+2	−2	−0.1	+2	% of FSR/V
OPERATING RANGE	−40		+85	−40		+85	−40		+85	−40		+85	°C

[1] Measured at IOUTA, driving a virtual ground.
[2] Nominal full-scale current, I_{OUTFS}, is 32 × the I_{REF} current.
[3] Use an external buffer amplifier with an input bias current <100 nA to drive any external load.
[4] Measured at I_{OUTFS} = 1 mA.
[5] Measured at f_{CLOCK} = 80 MSPS and f_{OUT} = 1 MHz, using a differential clock.
[6] ±5% power supply variation.

DYNAMIC SPECIFICATIONS (1.8 V)

T_{MIN} to T_{MAX}, AVDD = 1.8 V, DVDD = 1.8 V, CLKVDD = 1.8 V, I_{OUTFS} = 1 mA, differential transformer coupled output, 453 Ω differentially terminated unless otherwise noted.

Table 5.

Parameter	AD9707 Min	AD9707 Typ	AD9707 Max	AD9706 Min	AD9706 Typ	AD9706 Max	AD9705 Min	AD9705 Typ	AD9705 Max	AD9704 Min	AD9704 Typ	AD9704 Max	Unit
DYNAMIC PERFORMANCE													
Maximum Output Update Rate, f_{CLOCK}	125			125			125			125			MSPS
Output Settling Time, t_{ST}, (to 0.1%)[1]		11			11			11			11		ns
Output Propagation Delay (t_{PD})		5.6			5.6			5.6			5.6		ns
Glitch Impulse		5			5			5			5		pV-s
Output Rise Time (10% to 90%)[1]		2.5			2.5			2.5			2.5		ns
Output Fall Time (10% to 90%)[1]		2.5			2.5			2.5			2.5		ns
AC LINEARITY													
Spurious-Free Dynamic Range to Nyquist													
f_{CLOCK} = 10 MSPS; f_{OUT} = 2.1 MHz		86			86			85			70		dBc
f_{CLOCK} = 25 MSPS; f_{OUT} = 2.1 MHz		87			86			84			68		dBc
f_{CLOCK} = 25 MSPS; f_{OUT} = 5.1 MHz		82			82			82			68		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 10.1 MHz		82			79			78			70		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 15.1 MHz		77			76			74			69		dBc
f_{CLOCK} = 80 MSPS; f_{OUT} = 1.0 MHz	74	82		72	82		72	82		66	70		dBc
f_{CLOCK} = 80 MSPS; f_{OUT} = 15.1 MHz		77			77			77			68		dBc
f_{CLOCK} = 80 MSPS; f_{OUT} = 30.1 MHz		60			59			59			60		dBc
Noise Spectral Density													
f_{CLOCK} = 80 MSPS; f_{OUT} = 10 MHz; I_{OUTFS} = 1 mA		−145			−144			−140			−128		dBc/Hz
f_{CLOCK} = 80 MSPS; f_{OUT} = 10 MHz; I_{OUTFS} = 2 mA		−151											dBc/Hz

[1] Measured single-ended into 500 Ω load.

DIGITAL SPECIFICATIONS (1.8 V)

T_{MIN} to T_{MAX}, AVDD = 1.8 V, DVDD = 1.8 V, CLKVDD = 1.8 V, I_{OUTFS} = 1 mA, unless otherwise noted.

Table 6.

	AD9707			AD9706			AD9705			AD9704			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DIGITAL INPUTS[1]													
Logic 1 Voltage	1.2	1.8		1.2	1.8		1.2	1.8		1.2	1.8		V
Logic 0 Voltage		0	0.5		0	0.5		0	0.5		0	0.5	V
Logic 1 Current	−10		+10	−10		+10	−10		+10	−10		+10	µA
Logic 0 Current			+10			+10			+10			+10	µA
Input Capacitance		5			5			5			5		pF
Input Setup Time, t_S, 25°C	2.3			2.3			2.3			2.3			ns
Input Hold Time, t_H, 25°C	0			0			0			0			ns
Input Setup Time, t_S, −40°C to +85°C	2.4			2.4			2.4			2.4			ns
Input Hold Time, t_H, −40°C to +85°C	0.1			0.1			0.1			0.1			ns
Latch Pulse Width, t_{LPW}	6.2			6.2			6.2			6.2			ns
CLK INPUTS[2]													
Input Voltage Range	0		1.8	0		1.8	0		1.8	0		1.8	V
Common-Mode Voltage	0.4	0.9	1.3	0.4	0.9	1.3	0.4	0.9	1.3	0.4	0.9	1.3	V
Differential Voltage	0.5	1.5		0.5	1.5		0.5	1.5		0.5	1.5		V

[1] Includes CLK+ pin in single-ended clock input mode.
[2] Applicable to CLK+ input and CLK– input when configured for differential clock input mode.

TIMING DIAGRAM

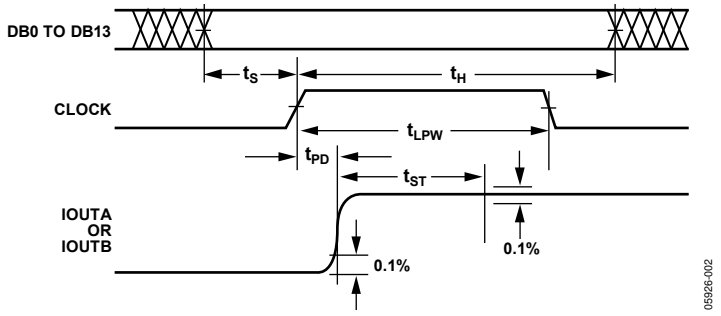

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
AVDD to ACOM	−0.3 V to +3.9 V
DVDD to DCOM	−0.3 V to +3.9 V
CLKVDD to CLKCOM	−0.3 V to +3.9 V
ACOM to DCOM	−0.3 V to +0.3 V
ACOM to CLKCOM	−0.3 V to +0.3 V
DCOM to CLKCOM	−0.3 V to +0.3 V
AVDD to DVDD	−3.9 V to +3.9 V
AVDD to CLKVDD	−3.9 V to +3.9 V
DVDD to CLKVDD	−3.9 V to +3.9 V
SLEEP to DCOM	−0.3 V to DVDD + 0.3 V
Digital Inputs, MODE to DCOM	−0.3 V to DVDD + 0.3 V
IOUTA, IOUTB to ACOM	−1.0 V to AVDD + 0.3 V
REFIO, FS ADJ, OTCM to ACOM	−0.3 V to AVDD + 0.3 V
CLK+, CLK–, CMODE to CLKCOM	−0.3 V to CLKVDD + 0.3 V
Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Thermal impedance measurements were taken on a 4-layer board in still air, in accordance with EIA/JESD51-7.

Table 8. Thermal Resistance

Package Type	θ_{JA}	Unit
32-Lead LFCSP_VQ	32.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

AD9707

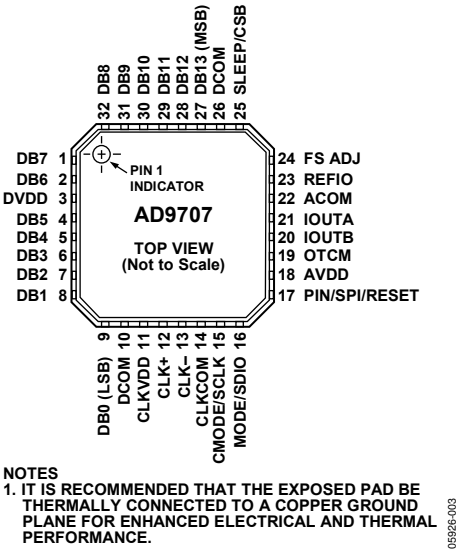

Figure 3. AD9707 Pin Configuration

Table 9. AD9707 Pin Function Descriptions

Pin No.	Mnemonic	Description
28 to 32, 1, 2, 4 to 8	DB12 to DB1	Data Bit 12 to Data Bit 1.
3	DVDD	Digital Supply Voltage (1.7 V to 3.6 V).
9	DB0 (LSB)	Least Significant Data Bit (LSB).
10, 26	DCOM	Digital Common.
11	CLKVDD	Clock Supply Voltage (1.7 V to 3.6 V).
12	CLK+	Positive Differential Clock Input.
13	CLK–	Negative Differential Clock Input.
14	CLKCOM	Clock Common.
15	CMODE/SCLK	In pin mode, this pin selects the clock input type. Connect to CLKCOM for single-ended clock receiver (drive CLK+ and float CLK–). Connect to CLKVDD for differential receiver. In SPI mode, this pin is the serial data clock input.
16	MODE/SDIO	In pin mode, this pin selects the input data format. Connect to DCOM for straight binary, and DVDD for twos complement. In SPI mode, this pin acts as SPI data input/output.
17	PIN/SPI/RESET	Selects SPI Mode or Pin Mode Operation. Active high for pin mode operation and active low for SPI mode operation. Pulse high to reset SPI registers to default values.
18	AVDD	Analog Supply Voltage (1.7 V to 3.6 V).
19	OTCM	Adjustable Output Common Mode. Refer to the Theory of Operation section for details.
20	IOUTB	Complementary DAC Current Output. Full-scale current is sourced when all data bits are 0s.
21	IOUTA	DAC Current Output. Full-scale current is sourced when all data bits are 1s.
22	ACOM	Analog Common.
23	REFIO	Reference Input/Output. Serves as reference input when internal reference disabled. Serves as 1.0 V reference output when internal reference is activated. Requires a 0.1 µF capacitor to ACOM when internal reference is activated.
24	FS ADJ	Full-Scale Current Output Adjust.
25	SLEEP/CSB	In pin mode, active high powers down chip. In SPI mode, this pin is the serial port chip select (active low).
27	DB13 (MSB)	Most Significant Data Bit (MSB).
	EPAD	It is recommended that the exposed pad be thermally connected to a copper ground plane for enhanced electrical and thermal performance.

AD9706

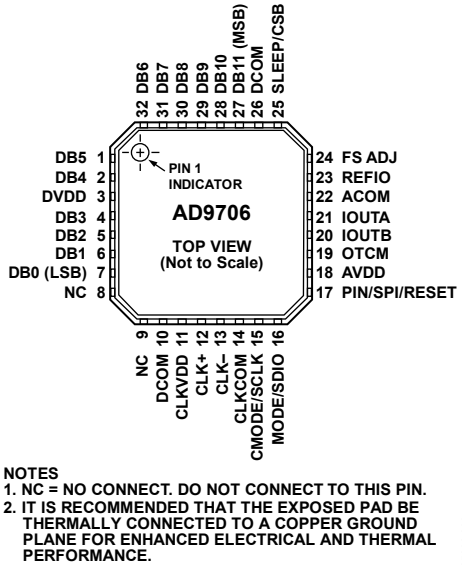

Figure 4. AD9706 Pin Configuration

Table 10. AD9706 Pin Function Descriptions

Pin No.	Mnemonic	Description
28 to 32, 1, 2, 4 to 6	DB10 to DB1	Data Bit 10 to Data Bit 1.
3	DVDD	Digital Supply Voltage (1.7 V to 3.6 V).
7	DB0 (LSB)	Least Significant Data Bit (LSB).
8, 9	NC	No Connect.
10, 26	DCOM	Digital Common.
11	CLKVDD	Clock Supply Voltage (1.7 V to 3.6 V).
12	CLK+	Positive Differential Clock Input.
13	CLK–	Negative Differential Clock Input.
14	CLKCOM	Clock Common.
15	CMODE/SCLK	In pin mode, this pin selects the clock input type. Connect to CLKCOM for single-ended clock receiver (drive CLK+ and float CLK–). Connect to CLKVDD for differential receiver. In SPI mode, this pin is the serial data clock input.
16	MODE/SDIO	In pin mode, this pin selects the input data format. Connect to DCOM for straight binary, and DVDD for twos complement. In SPI mode, this pin acts as SPI data input/output.
17	PIN/SPI/RESET	Selects SPI Mode or Pin Mode Operation. Active high for pin mode operation, and active low for SPI mode operation. Pulse high to reset SPI registers to default values.
18	AVDD	Analog Supply Voltage (1.7 V to 3.6 V).
19	OTCM	Adjustable Output Common Mode. Refer to the Theory of Operation section for details.
20	IOUTB	Complementary DAC Current Output. Full-scale current is sourced when all data bits are 0s.
21	IOUTA	DAC Current Output. Full-scale current is sourced when all data bits are 1s.
22	ACOM	Analog Common.
23	REFIO	Reference Input/Output. Serves as reference input when internal reference disabled. Serves as 1.0 V reference output when internal reference is activated. Requires a 0.1 µF capacitor to ACOM when internal reference is activated.
24	FS ADJ	Full-Scale Current Output Adjust.
25	SLEEP/CSB	In pin mode, active high powers down chip. In SPI mode, this pin is the serial port chip select (active low).
27	DB11 (MSB)	Most Significant Data Bit (MSB).
	EPAD	It is recommended that the exposed pad be thermally connected to a copper ground plane for enhanced electrical and thermal performance.

AD9705

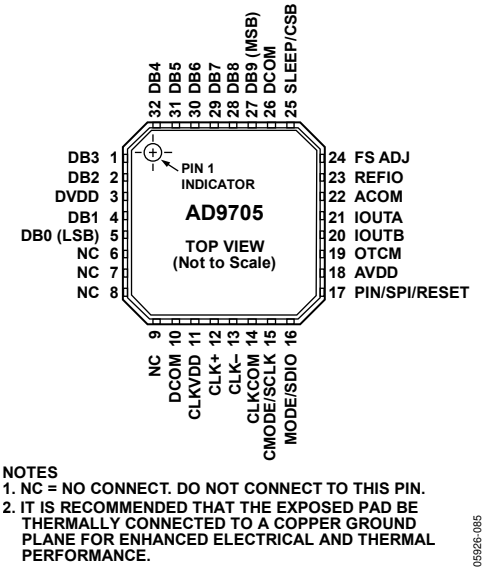

Figure 5. AD9705 Pin Configuration

Table 11. AD9705 Pin Function Descriptions

Pin No.	Mnemonic	Description
28 to 32, 1, 2, 4	DB8 to DB1	Data Bit 8 to Data Bit 1.
3	DVDD	Digital Supply Voltage (1.7 V to 3.6 V).
5	DB0 (LSB)	Least Significant Data Bit (LSB).
6 to 9	NC	No Connect.
10, 26	DCOM	Digital Common.
11	CLKVDD	Clock Supply Voltage (1.7 V to 3.6 V).
12	CLK+	Positive Differential Clock Input.
13	CLK–	Negative Differential Clock Input.
14	CLKCOM	Clock Common.
15	CMODE/SCLK	In pin mode, this pin selects the clock input type. Connect to CLKCOM for single-ended clock receiver (drive CLK+ and float CLK–). Connect to CLKVDD for differential receiver. In SPI mode, this pin is the serial data clock input.
16	MODE/SDIO	In pin mode, this pin selects the input data format. Connect to DCOM for straight binary, and DVDD for twos complement. In SPI mode, this pin acts as SPI data input/output.
17	PIN/SPI/RESET	Selects SPI Mode or Pin Mode Operation. Active high for pin mode operation and active low for SPI mode operation. Pulse high to reset SPI registers to default values.
18	AVDD	Analog Supply Voltage (1.7 V to 3.6 V).
19	OTCM	Adjustable Output Common Mode. Refer to the Theory of Operation section for details.
20	IOUTB	Complementary DAC Current Output. Full-scale current is sourced when all data bits are 0s.
21	IOUTA	DAC Current Output. Full-scale current is sourced when all data bits are 1s.
22	ACOM	Analog Common.
23	REFIO	Reference Input/Output. Serves as reference input when internal reference disabled. Serves as 1.0 V reference output when internal reference is activated. Requires a 0.1 µF capacitor to ACOM when internal reference is activated.
24	FS ADJ	Full-Scale Current Output Adjust.
25	SLEEP/CSB	In pin mode, active high powers down chip. In SPI mode, this pin is the serial port chip select (active low).
27	DB9 (MSB)	Most Significant Data Bit (MSB).
	EPAD	It is recommended that the exposed pad be thermally connected to a copper ground plane for enhanced electrical and thermal performance.

AD9704

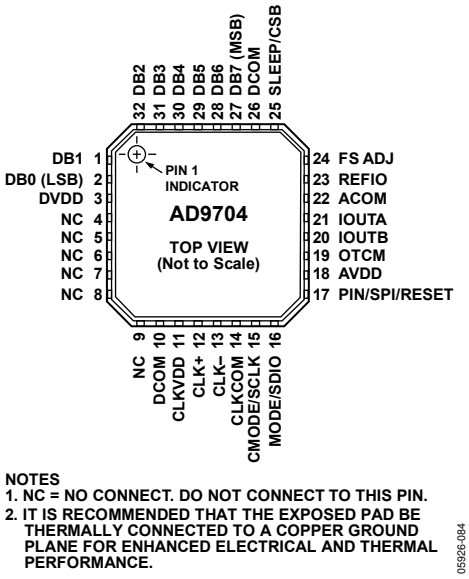

Figure 6. AD9704 Pin Configuration

Table 12. AD9704 Pin Function Descriptions

Pin No.	Mnemonic	Description
28 to 32, 1	DB6 to DB1	Data Bit 6 to Data Bit 1.
2	DB0 (LSB)	Least Significant Data Bit (LSB).
3	DVDD	Digital Supply Voltage (1.7 V to 3.6 V).
4 to 9	NC	No Connect.
10, 26	DCOM	Digital Common.
11	CLKVDD	Clock Supply Voltage (1.7 V to 3.6 V).
12	CLK+	Positive Differential Clock Input.
13	CLK–	Negative Differential Clock Input.
14	CLKCOM	Clock Common.
15	CMODE/SCLK	In pin mode, this pin selects the clock input type. Connect to CLKCOM for single-ended clock receiver (drive CLK+ and float CLK–). Connect to CLKVDD for differential receiver. In SPI mode, this pin is the serial data clock input.
16	MODE/SDIO	In pin mode, this pin selects the input data format. Connect to DCOM for straight binary, and DVDD for twos complement. In SPI mode, this pin acts as SPI data input/output.
17	PIN/SPI/RESET	Selects SPI Mode or Pin Mode Operation. Active high for pin mode operation and active low for SPI mode operation. Pulse high to reset SPI registers to default values.
18	AVDD	Analog Supply Voltage (1.7 V to 3.6 V).
19	OTCM	Adjustable Output Common Mode. Refer to the Theory of Operation section for details.
20	IOUTB	Complementary DAC Current Output. Full-scale current is sourced when all data bits are 0s.
21	IOUTA	DAC Current Output. Full-scale current is sourced when all data bits are 1s.
22	ACOM	Analog Common.
23	REFIO	Reference Input/Output. Serves as reference input when internal reference disabled. Serves as 1.0 V reference output when internal reference is activated. Requires a 0.1 µF capacitor to ACOM when internal reference is activated.
24	FS ADJ	Full-Scale Current Output Adjust.
25	SLEEP/CSB	In pin mode, active high powers down chip. In SPI mode, this pin is the serial port chip select (active low).
27	DB7 (MSB)	Most Significant Data Bit (MSB).
	EPAD	It is recommended that the exposed pad be thermally connected to a copper ground plane for enhanced electrical and thermal performance.

TYPICAL PERFORMANCE CHARACTERISTICS

AD9707

VDD = 3.3 V, I_{OUTFS} = 2 mA, unless otherwise noted.

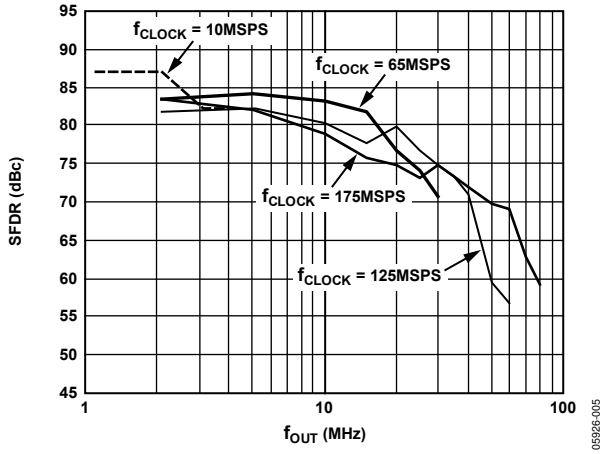

Figure 7. SFDR vs. f_{OUT}

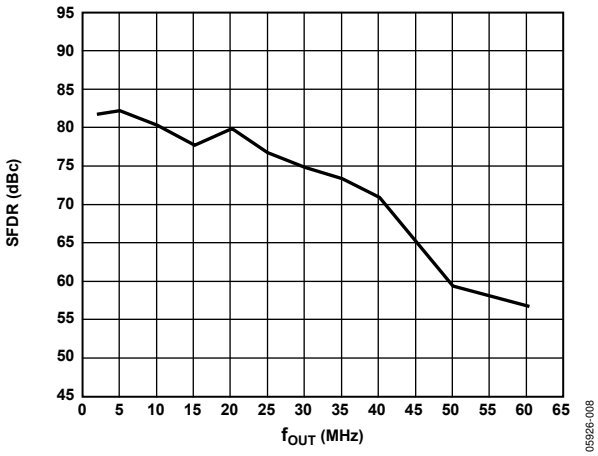

Figure 10. SFDR vs. f_{OUT} @ 125 MSPS

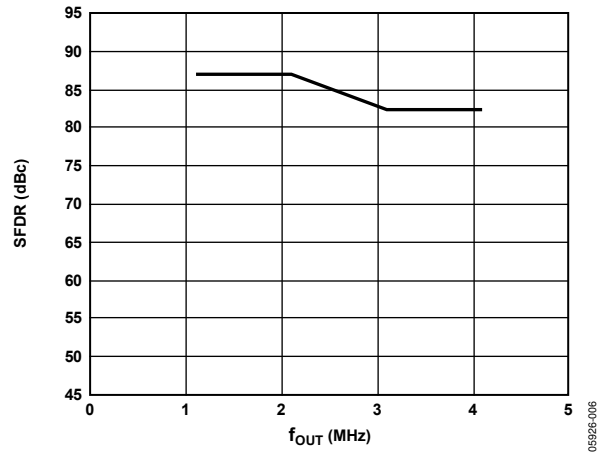

Figure 8. SFDR vs. f_{OUT} @ 10 MSPS

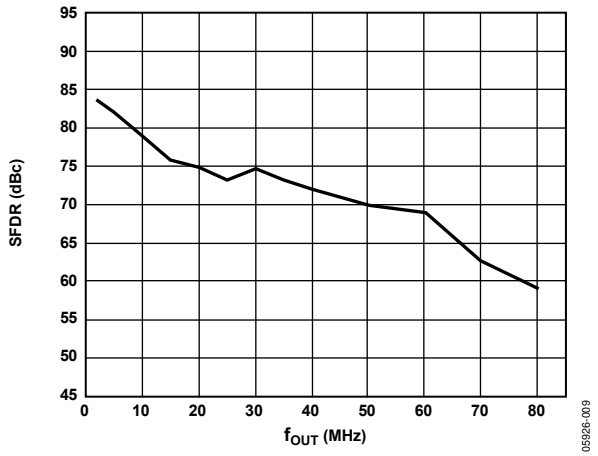

Figure 11. SFDR vs. f_{OUT} @ 175 MSPS

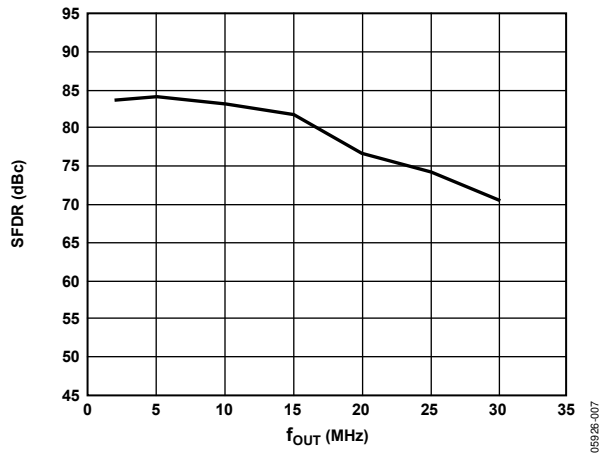

Figure 9. SFDR vs. f_{OUT} @ 65 MSPS

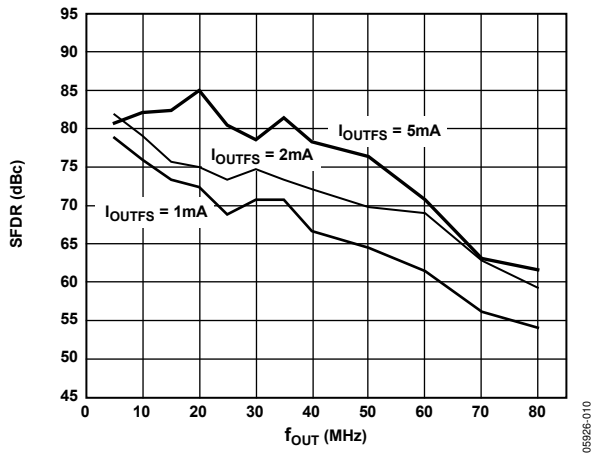

Figure 12. SFDR vs. f_{OUT} and I_{OUTFS} @ 175 MSPS

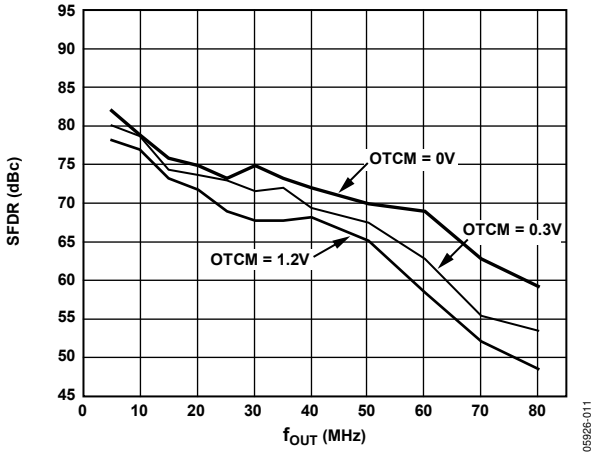

Figure 13. SFDR vs. f_{OUT} and OTCM @ 175 MSPS

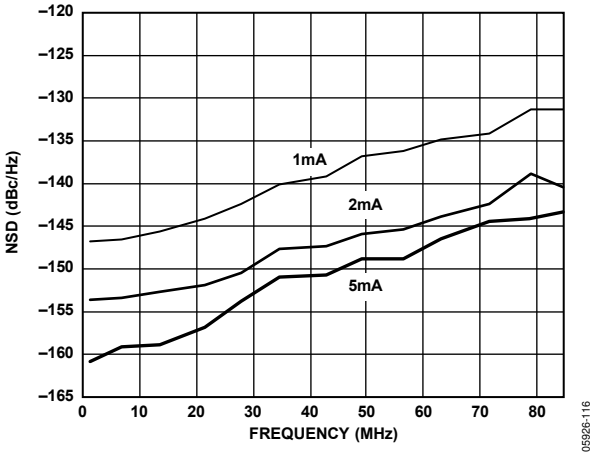

Figure 16. NSD vs. f_{OUT} and I_{OUTFS} @ 175 MSPS

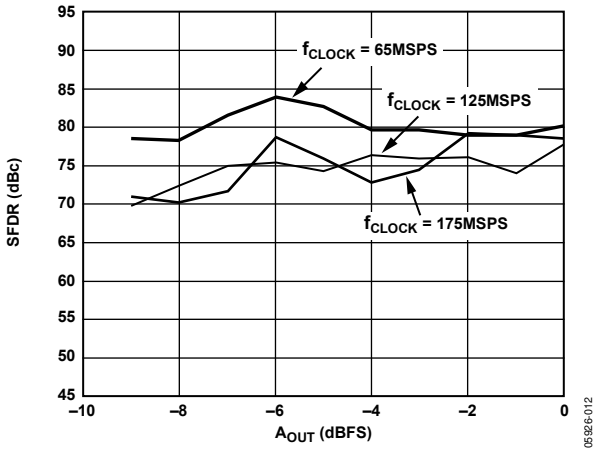

Figure 14. SFDR vs. A_{OUT} and f_{CLOCK} at $f_{OUT} = f_{CLOCK}/5$

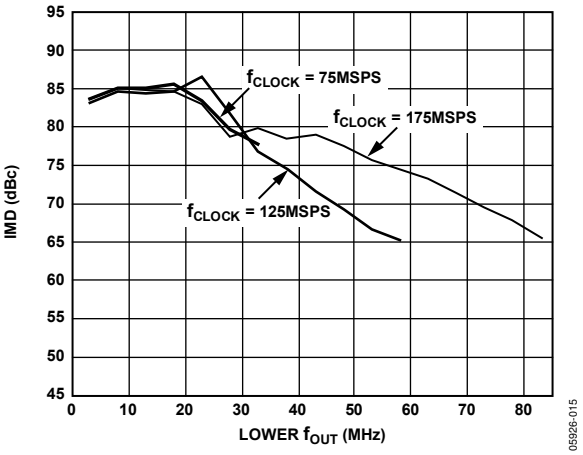

Figure 17. Dual-Tone IMD vs. Lower f_{OUT} and f_{CLOCK} @ 0 dBFS

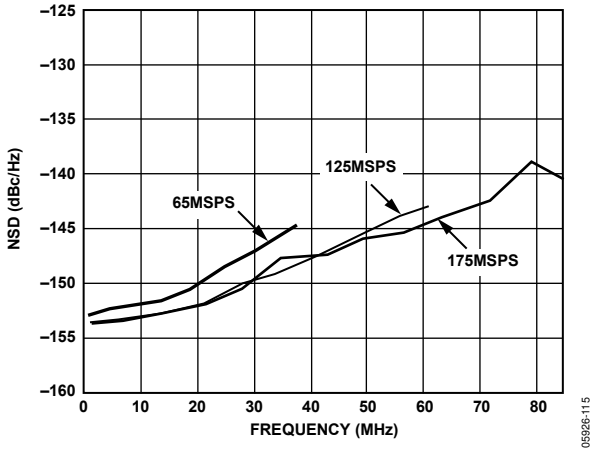

Figure 15. NSD vs. f_{OUT} and f_{CLOCK} @ 0 dBFS

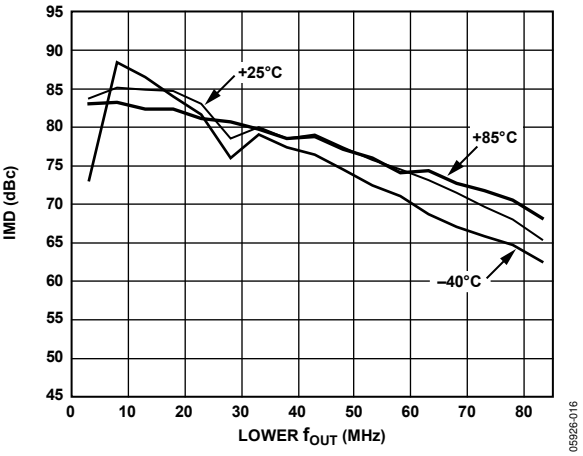

Figure 18. Dual-Tone IMD vs. Lower f_{OUT} and Temperature at 0 dBFS, 175 MSPS

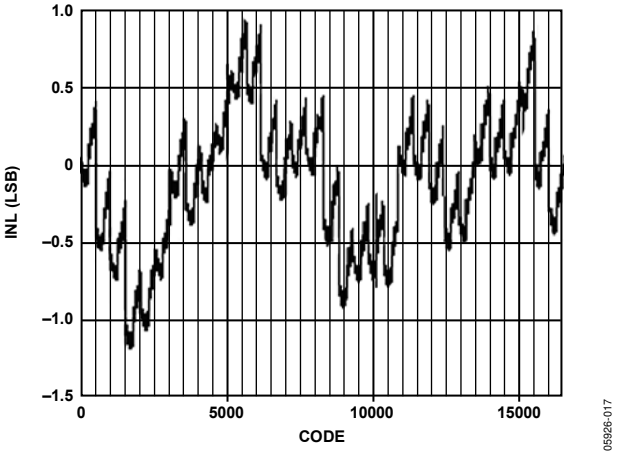

Figure 19. Typical Uncalibrated INL

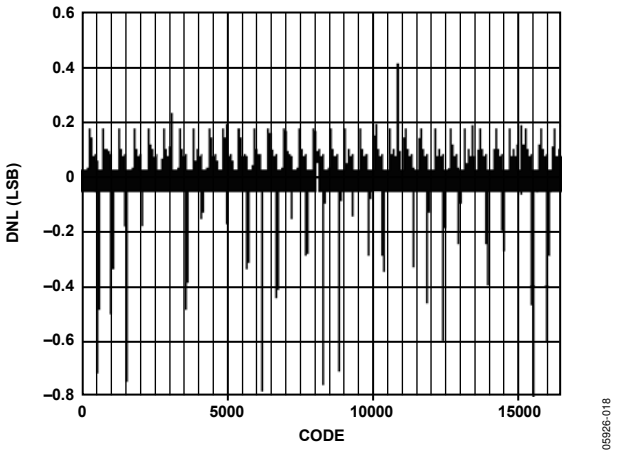

Figure 20. Typical Uncalibrated DNL

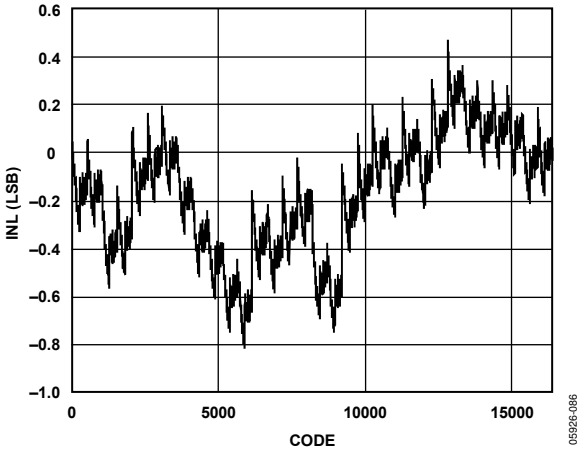

Figure 21. Typical Calibrated INL

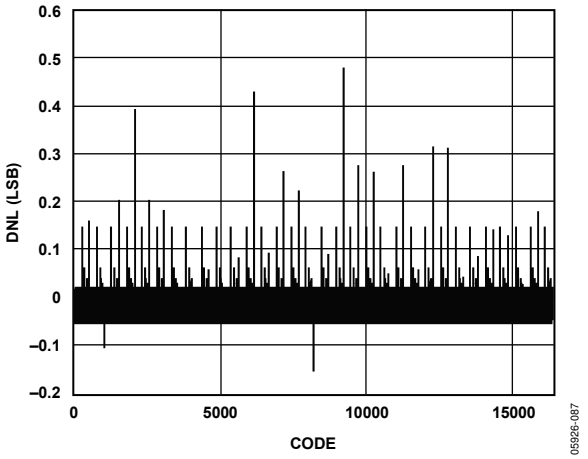

Figure 22. Typical Calibrated DNL

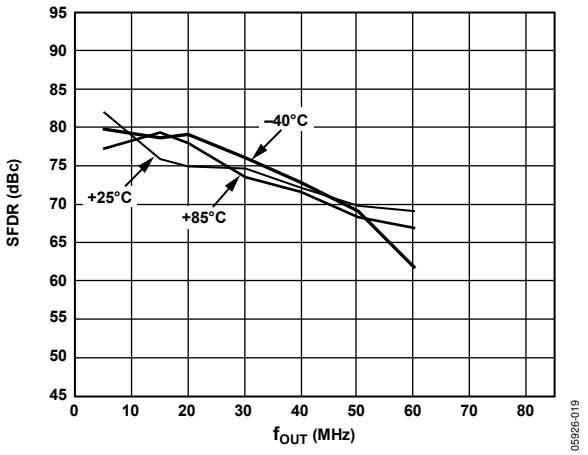

Figure 23. SFDR vs. f_{OUT} and Temperature @ 175 MSPS

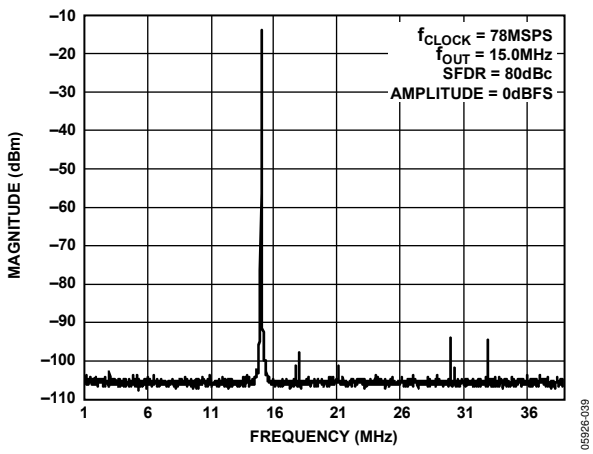

Figure 24. Single-Tone SFDR

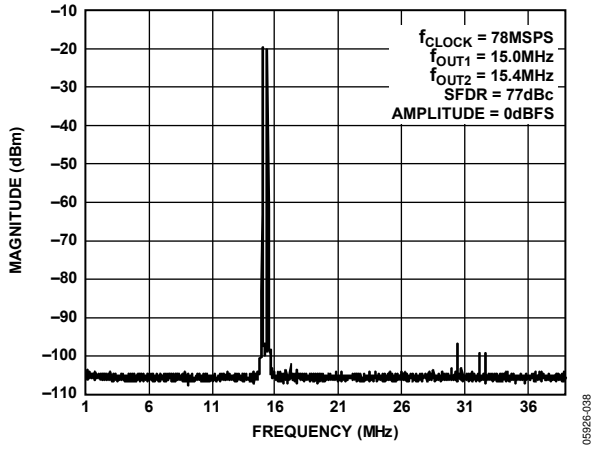

Figure 25. Dual-Tone SFDR

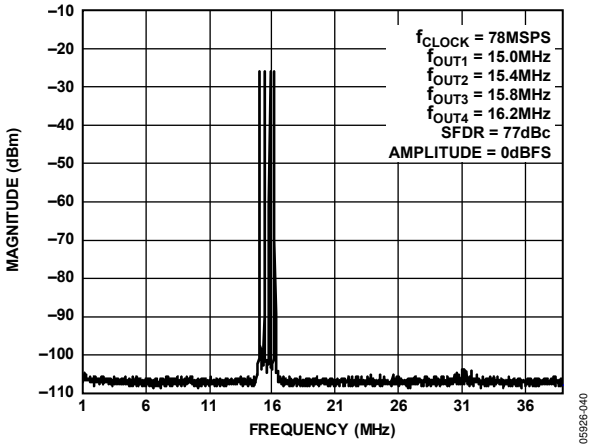

Figure 26. Four-Tone SFDR

VDD = 1.8 V, I_{OUTFS} = 1 mA, unless otherwise noted.

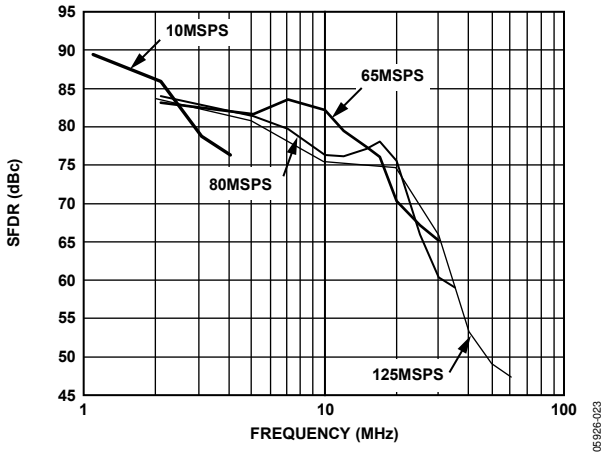

Figure 27. SFDR vs. f_{OUT}

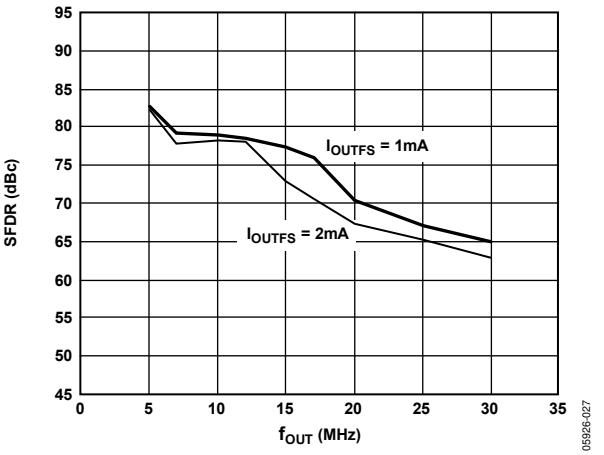

Figure 30. SFDR vs. f_{OUT} and I_{OUTFS} at 65 MSPS

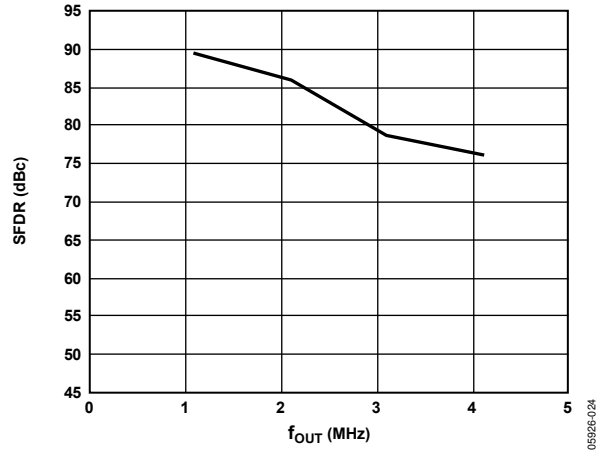

Figure 28. SFDR vs. f_{OUT} at 10 MSPS

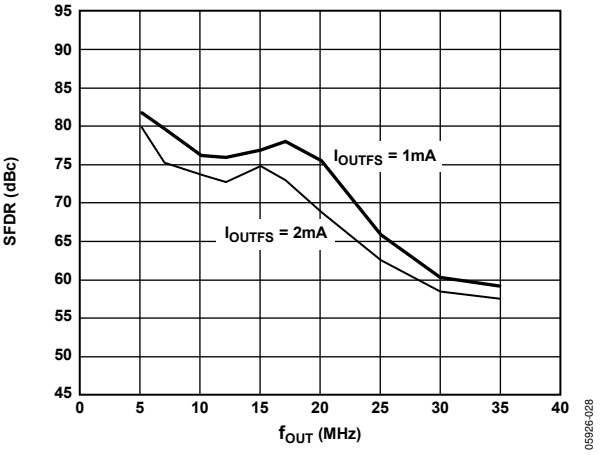

Figure 31. SFDR vs. f_{OUT} and I_{OUTFS} at 80 MSPS

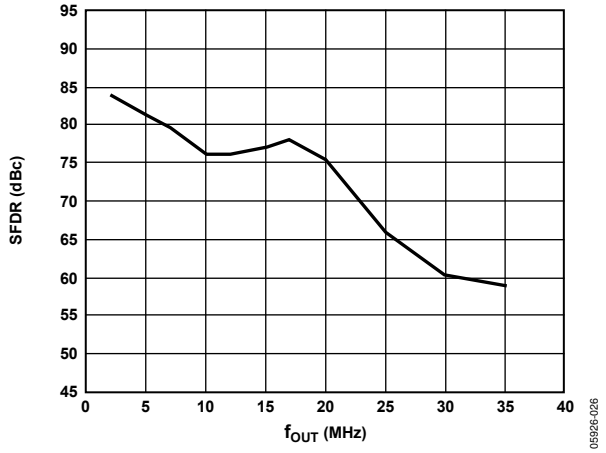

Figure 29. SFDR vs. f_{OUT} at 80 MSPS

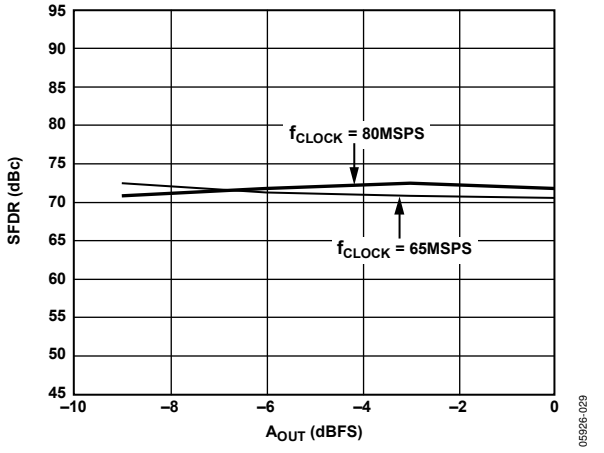

Figure 32. SFDR vs. A_{OUT} at $f_{OUT} = f_{CLOCK}/5$

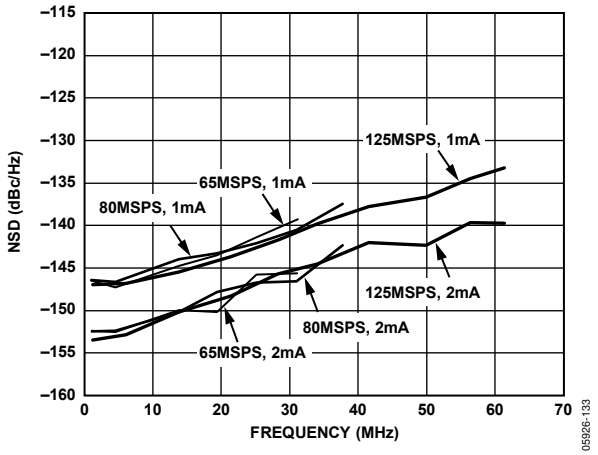

Figure 33. NSD vs. f_{OUT}, f_{CLOCK}, and I_{OUTFS} at 0 dBFS

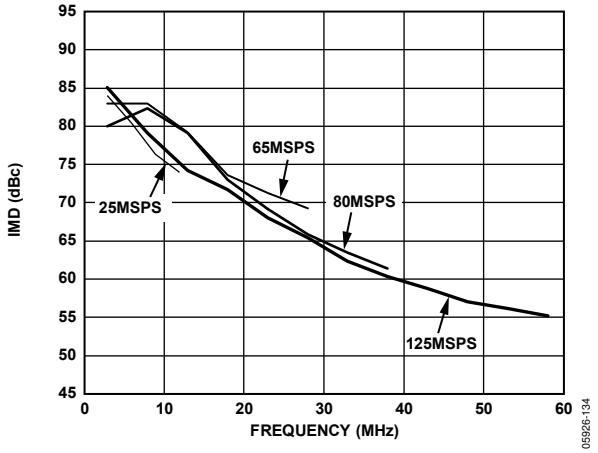

Figure 34. Dual-Tone IMD vs. Lower f_{OUT} at I_{OUTFS} = 1 mA and 0 dBFS

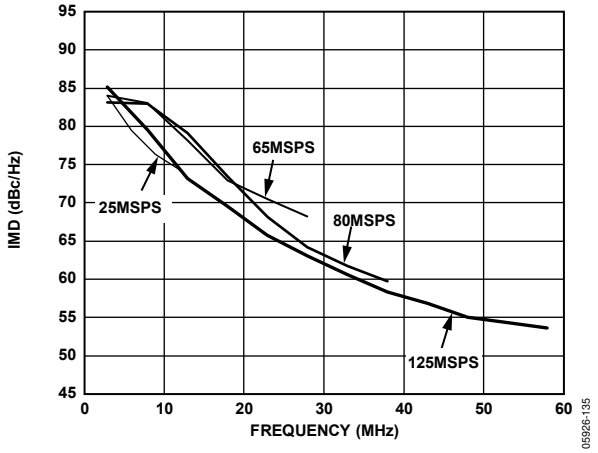

Figure 35. Dual-Tone IMD vs. Lower f_{OUT} at I_{OUTFS} = 2 mA and 0 dBFS

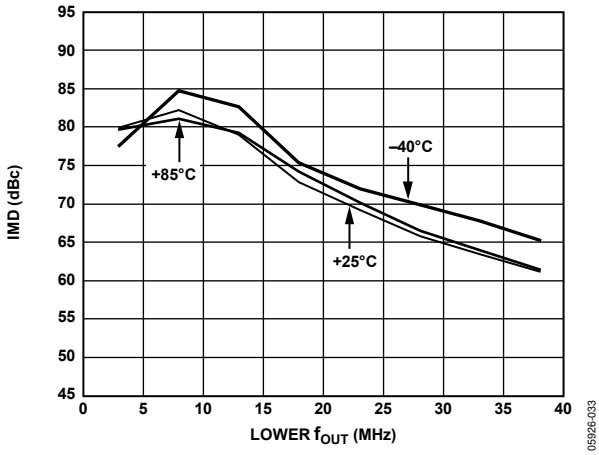

Figure 36. Dual-Tone IMD vs. Lower f_{OUT} and Temperature at 80 MSPS, I_{OUTFS} = 1 mA and 0 dBFS

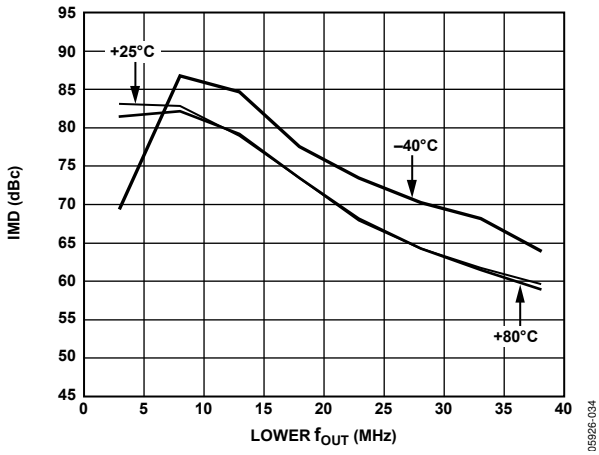

Figure 37. Dual-Tone IMD vs. Lower f_{OUT} and Temperature at 80 MSPS, I_{OUTFS} = 2 mA and 0 dBFS

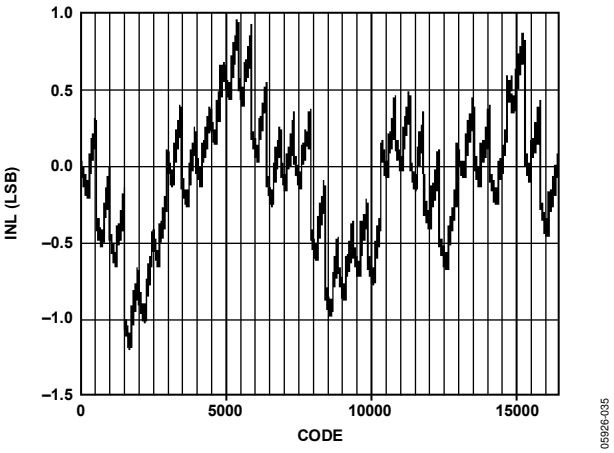

Figure 38. Typical Uncalibrated INL

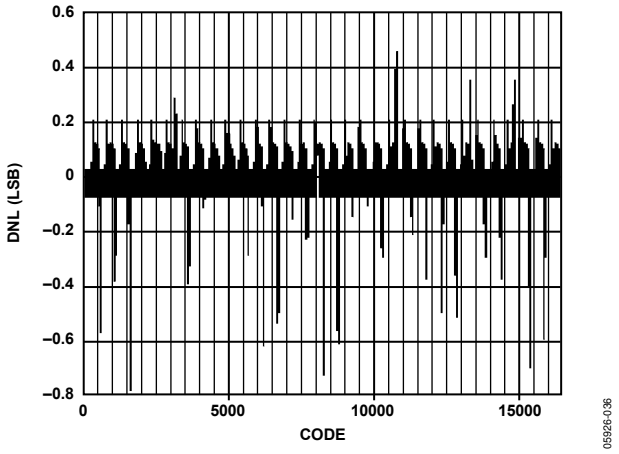

Figure 39. Typical Uncalibrated DNL

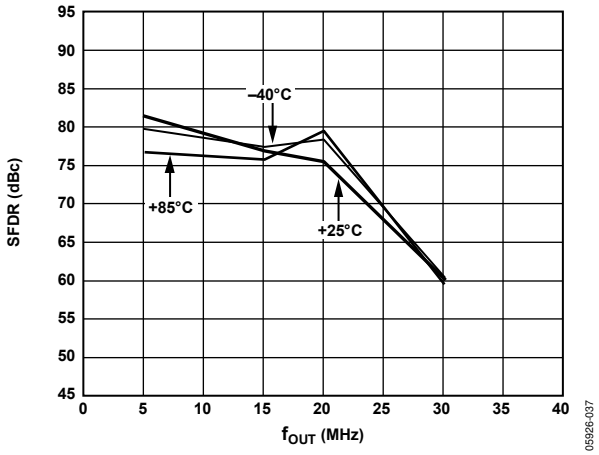

Figure 40. SFDR vs. Temperature at 80 MSPS

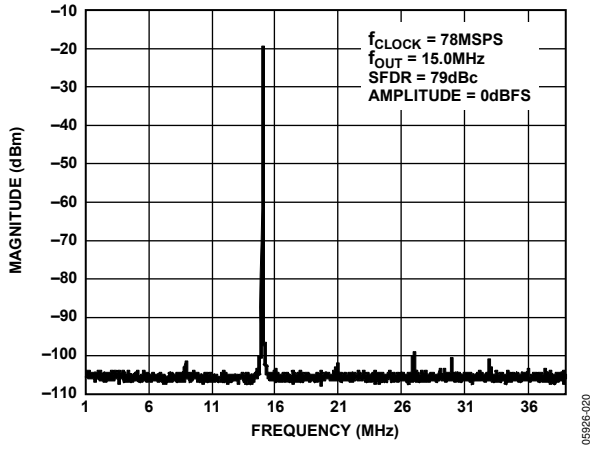

Figure 41. Single-Tone SFDR

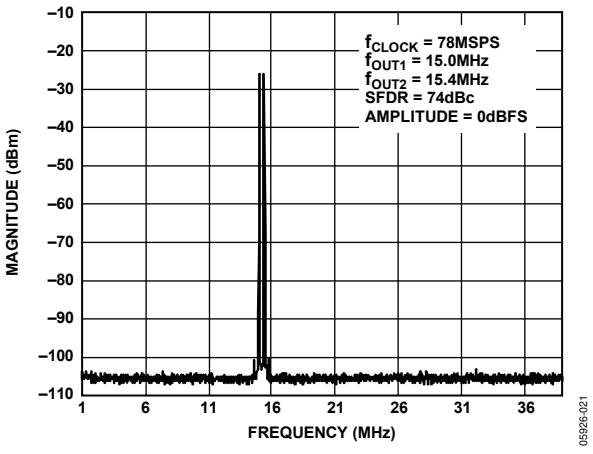

Figure 42. Dual-Tone SFDR

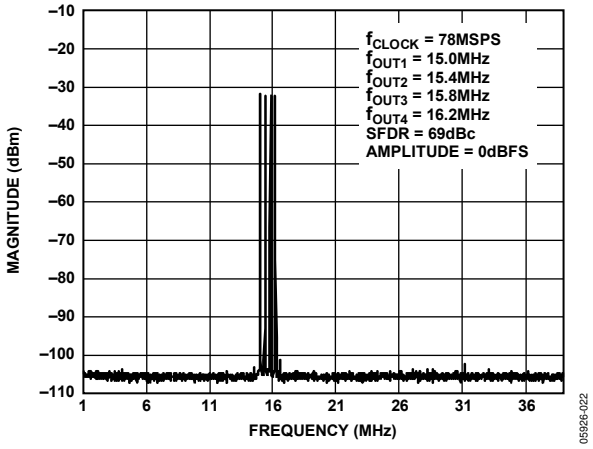

Figure 43. Four-Tone SFDR

AD9704, AD9705, AND AD9706

VDD = 3.3 V, I_{OUTFS} = 2 mA, unless otherwise noted.

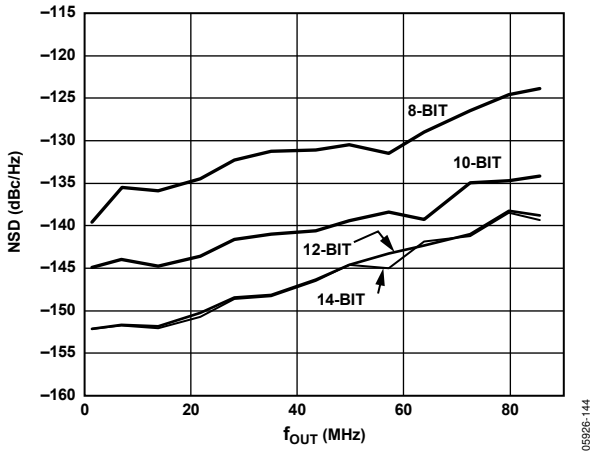

Figure 44. AD9704, AD9705, AD9706, AD9707 NSD vs. f_{OUT} at 0 dBFS, 175 MSPS

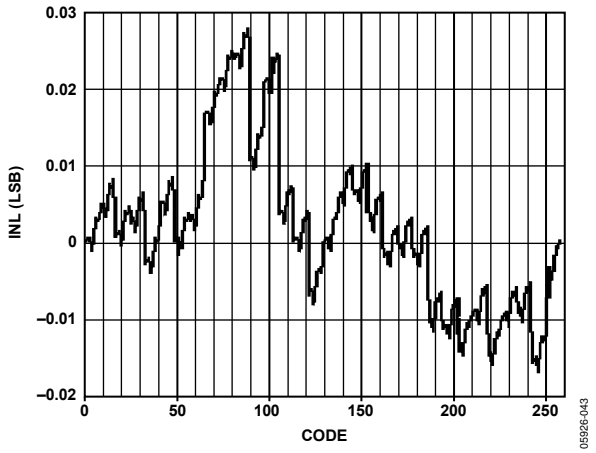

Figure 45. AD9704 Typical Uncalibrated INL

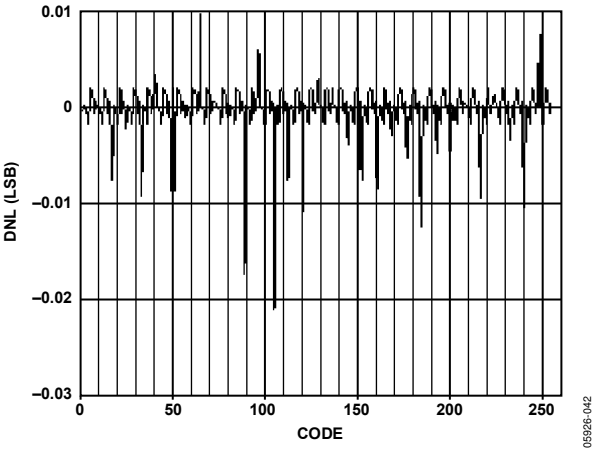

Figure 46. AD9704 Typical Uncalibrated DNL

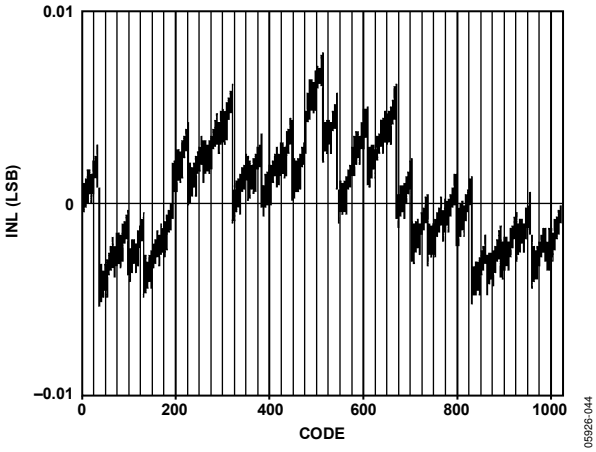

Figure 47. AD9705 Typical Uncalibrated INL

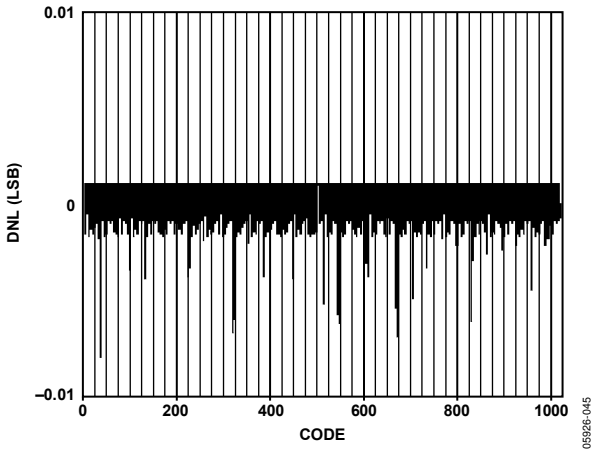

Figure 48. AD9705 Typical Uncalibrated DNL

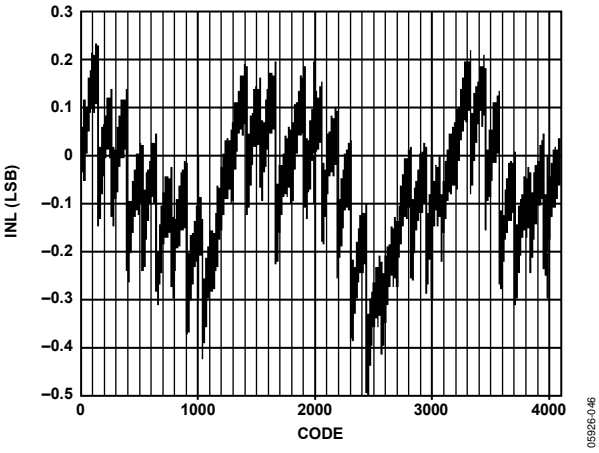

Figure 49. AD9706 Typical Uncalibrated INL

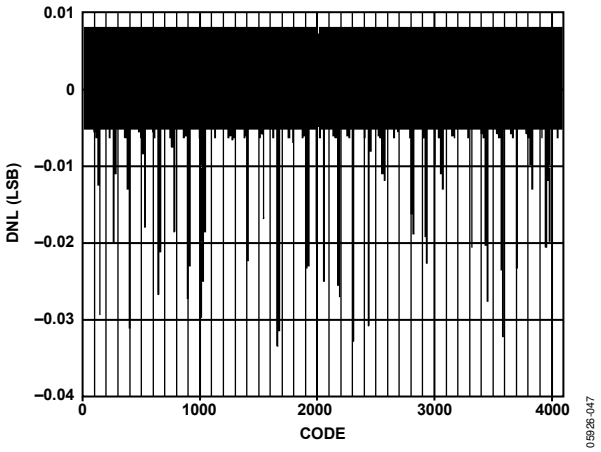

Figure 50. AD9706 Typical Uncalibrated DNL

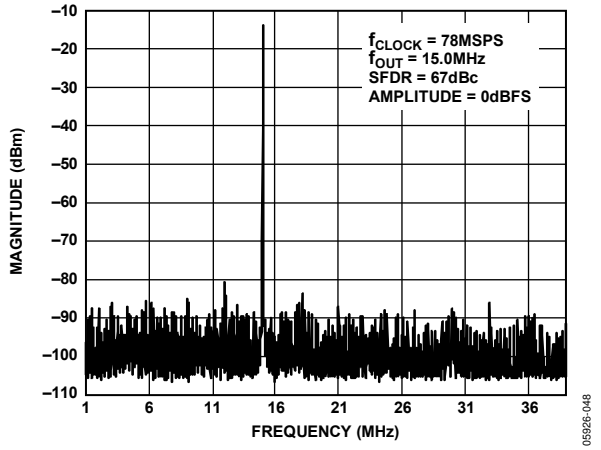

Figure 51. AD9704 Single-Tone SFDR

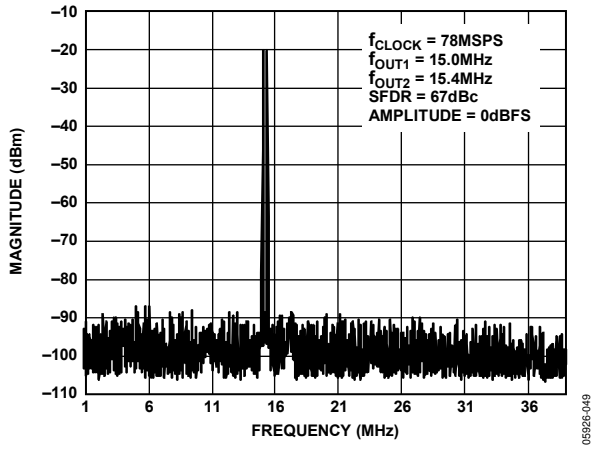

Figure 52. AD9704 Dual-Tone SFDR

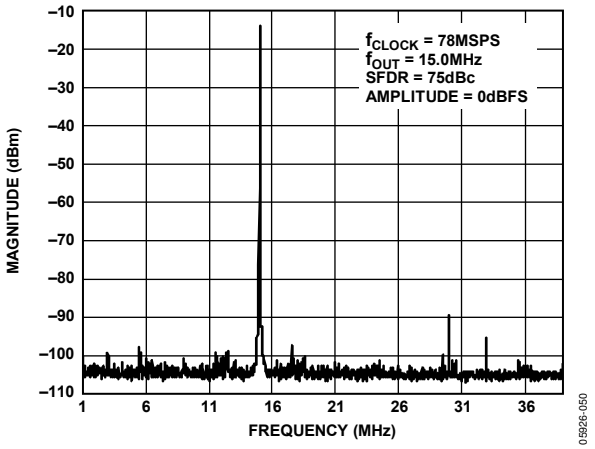

Figure 53. AD9705 Single-Tone SFDR

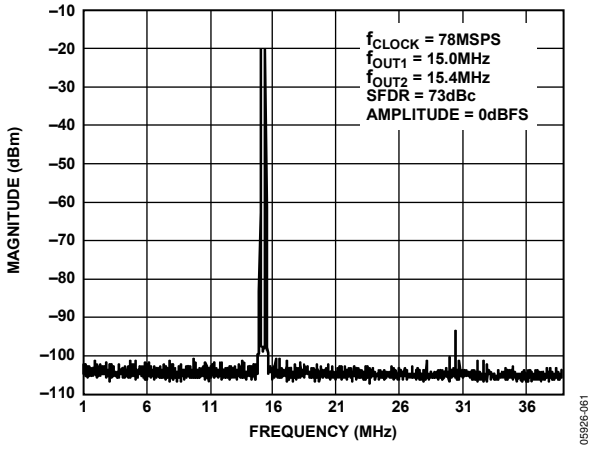

Figure 54. AD9705 Dual-Tone SFDR

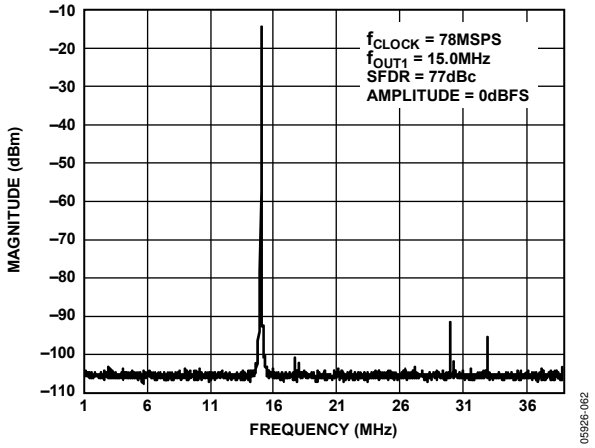

Figure 55. AD9706 Single-Tone SFDR

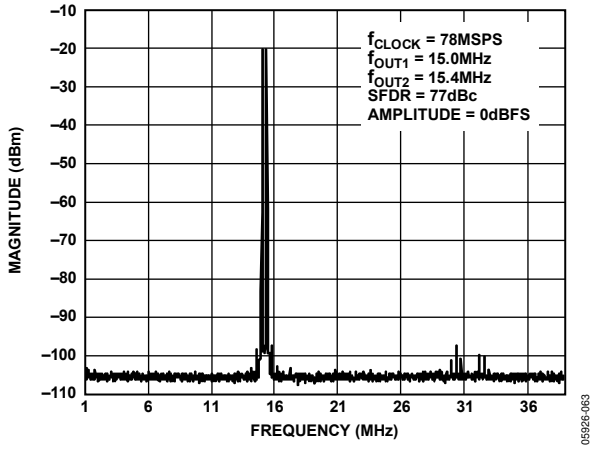

Figure 56. AD9706 Dual-Tone SFDR