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Dual, Low Power, 8-/10-/12-/14-Bit TxDAC Digital-to-Analog Converters

AD9714/AD9715/AD9716/AD9717

FEATURES

Power dissipation @ 3.3 V, 2 mA output
- **37 mW @ 10 MSPS**
- **86 mW @ 125 MSPS**

Sleep mode: <3 mW @ 3.3 V
Supply voltage: 1.8 V to 3.3 V
SFDR to Nyquist
- **84 dBc @ 1 MHz output**
- **75 dBc @ 10 MHz output**

AD9717 NSD @ 1 MHz output, 125 MSPS, 2 mA: –151 dBc/Hz
Differential current outputs: 1 mA to 4 mA
2 on-chip auxiliary DACs
CMOS inputs with single-port operation
Output common mode: adjustable 0 V to 1.2 V
Small footprint 40-lead LFCSP RoHS-compliant package

APPLICATIONS

Wireless infrastructures
- **Picocell, femtocell base stations**

Medical instrumentation
- **Ultrasound transducer excitation**

Portable instrumentation
- **Signal generators, arbitrary waveform generators**

GENERAL DESCRIPTION

The AD9714/AD9715/AD9716/AD9717 are pin-compatible, dual, 8-/10-/12-/14-bit, low power digital-to-analog converters (DACs) that provide a sample rate of 125 MSPS. These TxDAC® converters are optimized for the transmit signal path of communication systems. All the devices share the same interface, package, and pinout, providing an upward or downward component selection path based on performance, resolution, and cost.

The AD9714/AD9715/AD9716/AD9717 offer exceptional ac and dc performance and support update rates up to 125 MSPS.

The flexible power supply operating range of 1.8 V to 3.3 V and low power dissipation of the AD9714/AD9715/AD9716/AD9717 make them well-suited for portable and low power applications.

PRODUCT HIGHLIGHTS

1. Low Power.
   DACs operate on a single 1.8 V to 3.3 V supply; total power consumption reduces to 35 mW at 125 MSPS with a 1.8 V supply. Sleep and power-down modes are provided for low power idle periods.
2. CMOS Clock Input.
   High speed, single-ended CMOS clock input supports a 125 MSPS conversion rate.
3. Easy Interfacing to Other Components.
   Adjustable output common mode from 0 V to 1.2 V allows easy interfacing to other components that accept common-mode levels greater than 0 V.

Rev. A

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REVISION HISTORY

3/09—Rev. 0 to Rev. A

8/08—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

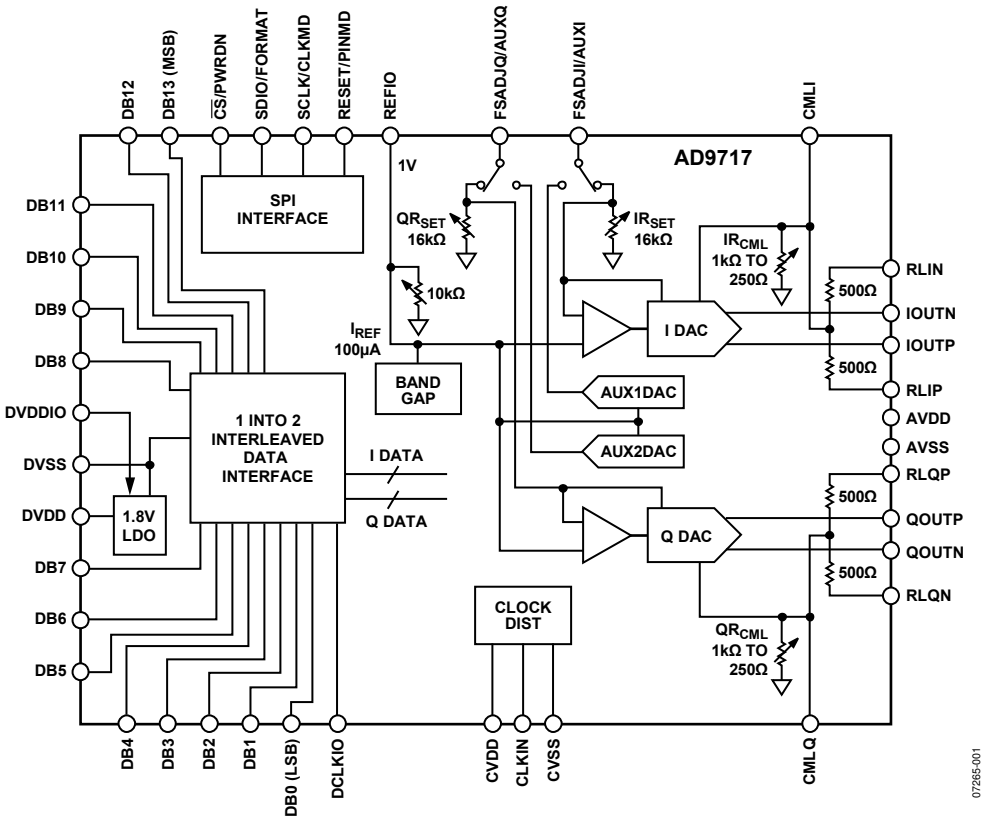

Figure 1.

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 1.8 V, DVDDIO = 3.3 V, CVDD = 3.3 V, I_{xOUTFS} = 2 mA, maximum sample rate, unless otherwise noted.

Table 1.

	AD9714			AD9715			AD9716			AD9717			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		8			10			12			14		Bits
ACCURACY, AVDD = DVDDIO = CVDD = 3.3 V													
Differential Nonlinearity (DNL)													
Precalibration		±0.02			±0.08			±0.4			±1.7		LSB
Postcalibration		±0.003			±0.01			±0.2			±1.0		LSB
Integral Nonlinearity (INL)													
Precalibration		±0.025			±0.13			±0.4			±1.8		LSB
Postcalibration		±0.01			±0.05			±0.3			±1.3		LSB
ACCURACY, AVDD = DVDDIO = CVDD = 1.8 V													
Differential Nonlinearity (DNL)													
Precalibration		±0.02			±0.08			±0.4			±1.2		LSB
Postcalibration		±0.005			±0.01			±0.2			±1.0		LSB
Integral Nonlinearity (INL)													
Precalibration		±0.025			±0.12			±0.4			±1.5		LSB
Postcalibration		±0.02			±0.05			±0.25			±1.1		LSB
MAIN DAC OUTPUTS													
Offset Error	−1	0	+1	−1	0	+1	−1	0	+1	−1	0	+1	mV
Gain Error													
Internal Reference	−2		+2	−2		+2	−2		+2	−2		+2	% of FSR
Full-Scale Output Current[1]													
AVDD = 3.3 V	1	2	4	1	2	4	1	2	4	1	2	4	mA
AVDD = 1.8 V	1	2	2.5	1	2	2.5	1	2	2.5	1	2	2.5	mA
Output Compliance Range	−0.5	0	+1.2	−0.5	0	+1.2	−0.5	0	+1.2	−0.5	0	+1.2	V
Output Resistance		200			200			200			200		MΩ
Crosstalk, Q DAC to I DAC													
f_{OUT} = 30 MHz		97			97			97			97		dB
f_{OUT} = 60 MHz		78			78			78			78		dB
MAIN DAC TEMPERATURE DRIFT													
Offset		0			0			0			0		ppm/°C
Gain		±40			±40			±40			±40		ppm/°C
Reference Voltage		±25			±25			±25			±25		ppm/°C
AUXDAC OUTPUTS													
Resolution		10			10			10			10		Bits
Full-Scale Output Current (Current Sourcing Mode)		125			125			125			125		µA
Voltage Output Mode	V_{SS}		V_{DD}	V_{SS}		V_{DD}	V_{SS}		V_{DD}	V_{SS}		V_{DD}	V
Output Compliance Range (Sourcing 1 mA)	V_{SS}		V_{DD} − 0.25	V_{SS}		V_{DD} − 0.25	V_{SS}		V_{DD} − 0.25	V_{SS}		V_{DD} − 0.25	V
Output Compliance Range (Sinking 1 mA)	V_{SS} + 0.25		V_{DD}	V_{SS} + 0.25		V_{DD}	V_{SS} + 0.25		V_{DD}	V_{SS} + 0.25		V_{DD}	V
Output Resistance in Current Output Mode, AV_{SS} to 1 V		1			1			1			1		MΩ
AUX DAC Monotonicity Guaranteed		10			10			10			10		Bits
REFERENCE OUTPUT													
Internal Reference Voltage	0.98	1.025	1.08	0.98	1.025	1.08	0.98	1.025	1.08	0.98	1.025	1.08	V
Output Resistance		10			10			10			10		kΩ

Parameter	AD9714 Min	AD9714 Typ	AD9714 Max	AD9715 Min	AD9715 Typ	AD9715 Max	AD9716 Min	AD9716 Typ	AD9716 Max	AD9717 Min	AD9717 Typ	AD9717 Max	Unit
REFERENCE INPUT													
Voltage Compliance													
AVDD = 3.3 V	0.1		1.25	0.1		1.25	0.1		1.25	0.1		1.25	V
AVDD = 1.8 V	0.1		1.0	0.1		1.0	0.1		1.0	0.1		1.0	V
Input Resistance External Reference Mode		1			1			1			1		MΩ
DAC MATCHING													
Gain Matching	−1		+1	−1		+1	−1		+1	−1		+1	% FSR
ANALOG SUPPLY VOLTAGES													
AVDD	1.7		3.5	1.7		3.5	1.7		3.5	1.7		3.5	V
CVDD	1.7		3.5	1.7		3.5	1.7		3.5	1.7		3.5	V
DIGITAL SUPPLY VOLTAGES													
DVDD	1.7		1.9	1.7		1.9	1.7		1.9	1.7		1.9	V
DVDDIO	1.7		3.5	1.7		3.5	1.7		3.5	1.7		3.5	V
POWER CONSUMPTION, AVDD = DVDDIO = CVDD = 3.3 V													
f_{DAC} = 125 MSPS, IF = 12.5 MHz		86			86			86			86		mW
I_{AVDD}		10			10			10			10		mA
$I_{DVDD} + I_{DVDDIO}$		11			11			11			11		mA
I_{CVDD}		3			3			3			3		mA
Power-Down Mode with Clock		50			50			50			50		mW
Power-Down Mode, No Clock		1.5			1.5			1.5			1.5		mW
Power Supply Rejection Ratio		−0.04			−0.04			−0.04			−0.04		% FSR/V
POWER CONSUMPTION, AVDD = DVDDIO = CVDD = 1.8 V.													
f_{DAC} = 125 MSPS, IF = 12.5 MHz		35			35			35			35		mW
I_{AVDD}		10			10			10			10		mA
$I_{DVDD} + I_{DVDDIO}$		8			8			8			8		mA
I_{CVDD}		1.5			1.5			1.5			1.5		mA
Power-Down Mode with Clock		12			12			12			12		mW
Power-Down Mode, No Clock		850			850			850			850		µW
Power Supply Rejection Ratio		−0.001			−0.001			−0.001			−0.001		% FSR/V
OPERATING RANGE	−40	+25	+85	−40	+25	+85	−40	+25	+85	−40	+25	+85	°C

[1] Based on a 10 kΩ external resistor.

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 1.8 V, DVDDIO = 3.3 V, CVDD = 3.3 V, I_{xOUTFS} = 2 mA, maximum sample rate, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
DAC CLOCK INPUT (CLKIN)				
V_{IH}	2.1	3		V
V_{IL}		0	0.9	V
Maximum Clock Rate			125	MSPS
SERIAL PERIPHERAL INTERFACE				
Maximum Clock Rate (SCLK)		25		MHz
Minimum Pulse Width High		20		ns
Minimum Pulse Width Low		20		ns
INPUT DATA				
1.8 V Q Channel or DCLKIO Falling Edge				
Setup		0.25		ns
Hold		1.2		ns
1.8 V I Channel or DCLKIO Rising Edge				
Setup		0.13		ns
Hold		1.1		ns
3.3 V Q Channel or DCLKIO Falling Edge				
Setup		−0.2		ns
Hold		1.5		ns
3.3 V I Channel or DCLKIO Rising Edge				
Setup		−0.2		ns
Hold		1.6		ns
V_{IH}	2.1	3		V
V_{IL}		0	0.9	V

AC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 1.8 V, DVDDIO = 3.3 V, CVDD = 3.3 V, I_{xOUTFS} = 2 mA, maximum sample rate, unless otherwise noted.

Table 3.

	AD9714			AD9715			AD9716			AD9717			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SPURIOUS-FREE DYNAMIC RANGE (SFDR)													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		75			82			83			84		dBc
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		60			61			62			63		dBc
TWO TONE INTERMODULATION DISTORTION (IMD)													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		86			87			88			89		dBc
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		71			71			71			71		dBc
NOISE SPECTRAL DENSITY (NSD) EIGHT-TONE, 500 kHz TONE SPACING													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		−129			−141			−149			−152		dBc/Hz
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		−123			−135			−137			−141		dBc/Hz
W-CDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER													
f_{DAC} = 61.44 MSPS, f_{OUT} = 20 MHz		−71			−71			−71			−71		dBc
f_{DAC} = 122.88 MSPS, f_{OUT} = 30 MHz		−72			−72			−72			−72		dBc

T_{MIN} to T_{MAX}, AVDD = 1.8 V, DVDD = 1.8 V, DVDDIO = 1.8 V, CVDD = 1.8 V, I_{xOUTFS} = 2 mA, maximum sample rate, unless otherwise noted.

Table 4.

	AD9714			AD9715			AD9716			AD9717			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SPURIOUS-FREE DYNAMIC RANGE (SFDR)													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		75			78			79			80		dBc
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		55			56			57			58		dBc
TWO TONE INTERMODULATION DISTORTION (IMD)													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		79			80			84			85		dBc
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		53			53			53			53		dBc
NOISE SPECTRAL DENSITY (NSD) EIGHT-TONE, 500 kHz TONE SPACING													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		−132			−141			−146			−148		dBc/Hz
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		−126			−131			−131			−132		dBc/Hz
W-CDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER													
f_{DAC} = 61.44 MSPS, f_{OUT} = 20 MHz		−68			−68			−68			−68		dBc
f_{DAC} = 122.88 MSPS, f_{OUT} = 30 MHz		−68			−68			−68			−68		dBc

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
AVDD, DVDDIO, CVDD to AVSS, DVSS, CVSS	−0.3 V to +3.9 V
DVDD to DVSS	−0.3 V to +2.1 V
AVSS to DVSS, CVSS	−0.3 V to +0.3 V
DVSS to AVSS, CVSS	−0.3 V to +0.3 V
CVSS to AVSS, DVSS	−0.3 V to +0.3 V
REFIO, FSADJQ, FSADJI, CMLQ, CMLI to AVSS	−0.3 V to AVDD + 0.3 V
QOUTP, QOUTN, IOUTP, IOUTN, RLQP, RLQN, RLIP, RLIN to AVSS	−1.0 V to AVDD + 0.3 V
DBn[1] (MSB) to DB0 (LSB), $\overline{CS}$, SCLK, SDIO, RESET to DVSS	−0.3 V to DVDDIO + 0.3 V
CLKIN to CVSS	−0.3 V to CVDD + 0.3 V
Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

[1] n stands for 7 for the AD9714, 9 for the AD9715, 11 for the AD9716, and 13 for the AD9717.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 6.

Package Type	θ_{JA}	θ_{JB}[1]	θ_{JC}[1]	Unit
40-Lead LFCSP (with No Airflow Movement)	29.8	19.0	3.4	°C/W

[1] These calculations are intended to represent the thermal performance of the indicated packages using a JEDEC multilayer test board. Do not assume the same level of thermal performance in actual applications without a careful inspection of the conditions in the application to determine that they are similar to those assumed in these calculations.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

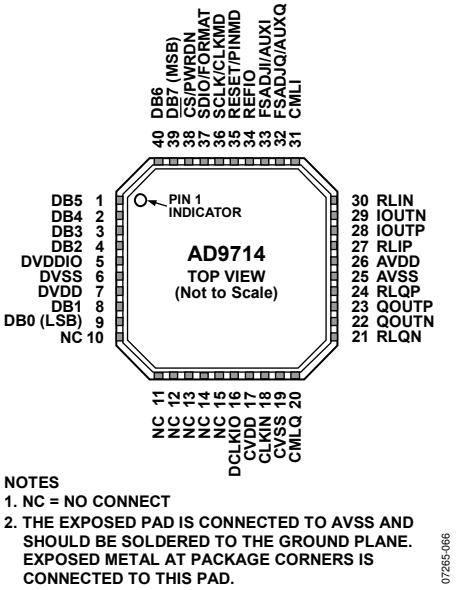

Figure 2. AD9714 Pin Configuration

Table 7. AD9714 Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4	DB[5:2]	Digital Inputs.
5	DVDDIO	Digital I/O Supply Voltage (1.8 V to 3.3 V Nominal).
6	DVSS	Digital Common.
7	DVDD	Digital Core Supply Voltage (1.8 V). Strap DVDD to DVDDIO at 1.8 V. If DVDDIO > 1.8 V, bypass DVDD with a 1.0 µF capacitor; however, do not otherwise connect it. The LDO should not drive external loads.
8	DB1	Digital Inputs.
9	DB0 (LSB)	Digital Input (LSB).
10 to 15	NC	No Connect. These pins are not connected to the chip.
16	DCLKIO	Data Input/Output Clock. Clock used to qualify input data.
17	CVDD	Sampling Clock Supply Voltage (1.8 V to 3.3 V). CVDD must be ≥ DVDD.
18	CLKIN	LVCMOS Sampling Clock Input.
19	CVSS	Sampling Clock Supply Voltage Common.
20	CMLQ	Q DAC Output Common-Mode Level. When the internal on chip (QR_{CML}) is enabled, this pin is connected to the on-chip QR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (QR_{CML}) is disabled, this pin is the common-mode load for Q DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
21	RLQN	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTN externally.
22	QOUTN	Complementary Q DAC Current Output. Full-scale current is sourced when all data bits are 0s.
23	QOUTP	Q DAC Current Output. Full-scale current is sourced when all data bits are 1s.
24	RLQP	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTP externally.
25	AVSS	Analog Common.
26	AVDD	Analog Supply Voltage (1.8 V to 3.3 V).
27	RLIP	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTP externally.
28	IOUTP	I DAC Current Output. Full-scale current is sourced when all data bits are 1s.
29	IOUTN	Complementary I DAC Current Output. Full-scale current is sourced when all data bits are 0s.
30	RLIN	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTN externally.

Pin No.	Mnemonic	Description
31	CMLI	I DAC Output Common-Mode Level. When the internal on chip (IR_{CML}) is enabled, this pin is connected to the on-chip IR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (IR_{CML}) is disabled, this pin is the common-mode load for I DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
32	FSADJQ/AUXQ	Full-Scale Current Output Adjust (FSADJQ). When the internal on chip (QR_{SET}) is disabled, this pin is the full-scale current output adjust for Q DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current. Auxiliary Q DAC Output (AUXQ). When the internal on chip (QR_{SET}) is enabled, this pin is the auxiliary Q DAC output.
33	FSADJI/AUXI	Full-Scale Current Output Adjust (FSADJI). When the internal on chip (IR_{SET}) is disabled, this pin is full-scale current output adjust for I DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current. Auxiliary I DAC Output (AUXI). When the internal on chip (IR_{SET}) is enabled, this pin is the auxiliary I DAC output.
34	REFIO	Reference Input/Output. Serves as a reference input when the internal reference is disabled. Provides a 1.0 V reference output when in internal reference mode (a 0.1 µF capacitor to AVSS is required).
35	RESET/PINMD	This pin defines the operation mode of the part. A logic low (pull-down to DVSS) sets the part in SPI mode. Pulse RESET high to reset the SPI registers to their default values. A logic high (pull-up to DVDDIO) puts the device into pin mode (PINMD).
36	SCLK/CLKMD	Clock Input for Serial Port (SCLK). In SPI mode, this pin is the clock input for the serial port. Clock Mode (CLKMD). In pin mode, CLKMD determines the phase of the internal retiming clock. When DCLKIO = CLKIN, tie it to 0. When DCLKIO ≠ CLKIN, pulse 0 to 1 to edge trigger the internal retimer (see the Retimer section).
37	SDIO/FORMAT	Serial Port Input/Output (SDIO). In SPI mode, this pin is the bidirectional data line for serial port. Format Pin (FORMAT). In pin mode, FORMAT determines the data format of digital data. A logic low (pull-down to DVSS) selects the binary input data format. A logic high (pull-up to DVDDIO) selects the two complement input data format.
38	$\overline{CS}$/PWRDN	Active Low Chip Select ($\overline{CS}$). In SPI mode, this pin serves as the active low chip select. In pin mode, a logic high (pull-up to DVDDIO) powers down the device, except for the SPI port. Power-Down (PWRDN). In pin mode, PWRDN powers down the device except for the SPI port.
39	DB7 (MSB)	Digital Input (MSB).
40	DB6	Digital Input.
41 (EPAD)	Exposed Pad (EPAD)	The exposed pad is connected to AVSS and should be soldered to the ground plane. Exposed metal at the package corners is connected to this pad.

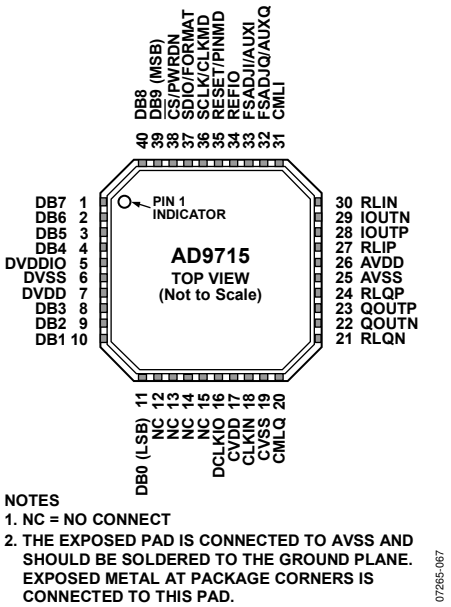

Figure 3. AD9715 Pin Configuration

Table 8. AD9715 Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4	DB[7:4]	Digital Inputs.
5	DVDDIO	Digital I/O Supply Voltage (1.8 V to 3.3 V Nominal).
6	DVSS	Digital Common.
7	DVDD	Digital Core Supply Voltage (1.8 V). Strap DVDD to DVDDIO at 1.8 V. If DVDDIO > 1.8 V, bypass DVDD with a 1.0 µF capacitor; however, do not otherwise connect it. The LDO should not drive external loads.
8 to 10	DB[3:1]	Digital Inputs.
11	DB0 (LSB)	Digital Input (LSB).
12 to 15	NC	No Connect. These pins are not connected to the chip.
16	DCLKIO	Data Input/Output Clock. Clock used to qualify input data.
17	CVDD	Sampling Clock Supply Voltage (1.8 V to 3.3 V). CVDD must be ≥ DVDD.
18	CLKIN	LVCMOS Sampling Clock Input.
19	CVSS	Sampling Clock Supply Voltage Common.
20	CMLQ	Q DAC Output Common-Mode Level. When the internal on chip (QR_{CML}) is enabled, this pin is connected to the on-chip QR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (QR_{CML}) is disabled, this pin is the common-mode load for Q DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
21	RLQN	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTN externally.
22	QOUTN	Complementary Q DAC Current Output. Full-scale current is sourced when all data bits are 0s.
23	QOUTP	Q DAC Current Output. Full-scale current is sourced when all data bits are 1s.
24	RLQP	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTP externally.
25	AVSS	Analog Common.
26	AVDD	Analog Supply Voltage (1.8 V to 3.3 V).
27	RLIP	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTP externally.
28	IOUTP	I DAC Current Output. Full-scale current is sourced when all data bits are 1s.
29	IOUTN	Complementary I DAC Current Output. Full-scale current is sourced when all data bits are 0s.
30	RLIN	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTN externally.

Pin No.	Mnemonic	Description
31	CMLI	I DAC Output Common-Mode Level. When the internal on chip (IR_{CML}) is enabled, this pin is connected to the on-chip IR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (IR_{CML}) is disabled, this pin is the common-mode load for I DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
32	FSADJQ/AUXQ	Full-Scale Current Output Adjust (FSADJQ). When the internal on chip (QR_{SET}) is disabled, this pin is the full-scale current output adjust for Q DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current. Auxiliary Q DAC Output (AUXQ). When the internal on chip (QR_{SET}) is enabled, this pin is the auxiliary Q DAC output.
33	FSADJI/AUXI	Full-Scale Current Output Adjust (FSADJI). When the internal on chip (IR_{SET}) is disabled, this pin is the full-scale current output adjust for I DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current. Auxiliary I DAC Output (AUXI). When the internal on chip (IR_{SET}) is enabled, this pin is the auxiliary I DAC output.
34	REFIO	Reference Input/Output. Serves as a reference input when the internal reference is disabled. Provides a 1.0 V reference output when in internal reference mode (a 0.1 µF capacitor to AVSS is required).
35	RESET/PINMD	This pin defines the operation mode of the part. A logic low (pull-down to DVSS) sets the part in SPI mode. Pulse RESET high to reset the SPI registers to their default values. A logic high (pull-up to DVDDIO) puts the device into pin mode (PINMD).
36	SCLK/CLKMD	Clock Input for Serial Port (SCLK). In SPI mode, this pin is the clock input for the serial port. Clock Mode (CLKMD). In pin mode, CLKMD determines the phase of the internal retiming clock. When DCLKIO = CLKIN, tie it to 0. When DCLKIO ≠ CLKIN, pulse 0 to 1 to edge trigger the internal retimer (see the Retimer section).
37	SDIO/FORMAT	Serial Port Input/Output (SDIO). In SPI mode, this pin is the bidirectional data line for the serial port. Format Pin (FORMAT). In pin mode, FORMAT determines the data format of digital data. A logic low (pull-down to DVSS) selects the binary input data format. A logic high (pull-up to DVDDIO) selects the twos complement input data format.
38	$\overline{CS}$/PWRDN	Active Low Chip Select ($\overline{CS}$). In SPI mode, this pin serves as the active low chip select. Power-Down (PWRDN). In pin mode, a logic high (pull-up to DVDDIO) powers down the device, except for the SPI port.
39	DB9 (MSB)	Digital Input (MSB).
40	DB8	Digital Input.
41 (EPAD)	Exposed Pad (EPAD)	The exposed pad is connected to AVSS and should be soldered to the ground plane. Exposed metal at the package corners is connected to this pad.

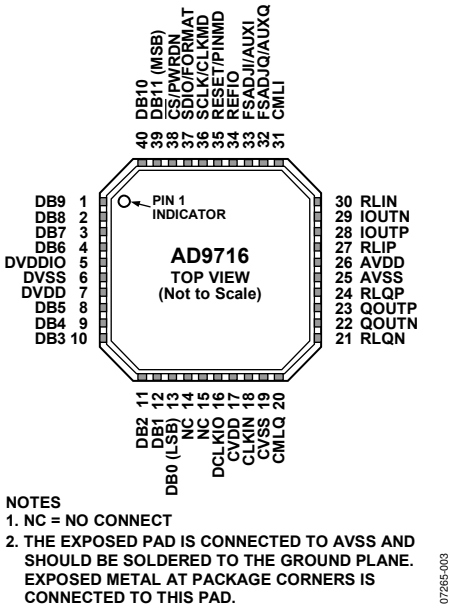

Figure 4. AD9716 Pin Configuration

Table 9. AD9716 Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4	DB[9:6]	Digital Inputs.
5	DVDDIO	Digital I/O Supply Voltage (1.8 V to 3.3 V Nominal).
6	DVSS	Digital Common.
7	DVDD	Digital Core Supply Voltage (1.8 V). Strap DVDD to DVDDIO at 1.8 V. If DVDDIO > 1.8 V, bypass DVDD with a 1.0 µF capacitor; however, do not otherwise connect it. The LDO should not drive external loads.
8 to 12	DB[5:1]	Digital Inputs.
13	DB0 (LSB)	Digital Input (LSB).
14, 15	NC	No Connect. These pins are not connected to the chip.
16	DCLKIO	Data Input/Output Clock. Clock used to qualify input data.
17	CVDD	Sampling Clock Supply Voltage (1.8 V to 3.3 V). CVDD must be ≥ DVDD.
18	CLKIN	LVCMOS Sampling Clock Input.
19	CVSS	Sampling Clock Supply Voltage Common.
20	CMLQ	Q DAC Output Common-Mode Level. When the internal on chip (QR_{CML}) is enabled, this pin is connected to the on-chip QR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (QR_{CML}) is disabled, this pin is the common-mode load for Q DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
21	RLQN	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTN externally.
22	QOUTN	Complementary Q DAC Current Output. Full-scale current is sourced when all data bits are 0s.
23	QOUTP	Q DAC Current Output. Full-scale current is sourced when all data bits are 1s.
24	RLQP	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTP externally.
25	AVSS	Analog Common.
26	AVDD	Analog Supply Voltage (1.8 V to 3.3 V).
27	RLIP	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTP externally.
28	IOUTP	I DAC Current Output. Full-scale current is sourced when all data bits are 1s.
29	IOUTN	Complementary I DAC Current Output. Full-scale current is sourced when all data bits are 0s.
30	RLIN	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTN externally.

Pin No.	Mnemonic	Description
31	CMLI	I DAC Output Common-Mode Level. When the internal on chip (IR_{CML}) is enabled, this pin is connected to the on-chip IR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (IR_{CML}) is disabled, this pin is the common-mode load for I DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
32	FSADJQ/AUXQ	Full-Scale Current Output Adjust (FSADJQ). When the internal on chip (QR_{SET}) is disabled, this pin is the full-scale current output adjust for Q DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current. Auxiliary Q DAC Output (AUXQ). When the internal on chip (QR_{SET}) is enabled, this pin is the auxiliary Q DAC output.
33	FSADJI/AUXI	Full-Scale Current Output Adjust (FSADJI). When the internal on chip (IR_{SET}) is disabled, this pin is the full-scale current output adjust for I DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current. Auxiliary I DAC Output (AUXI). When the internal on chip (IR_{SET}) is enabled, this pin is the auxiliary I DAC output.
34	REFIO	Reference Input/Output. Serves as a reference input when the internal reference is disabled. Provides a 1.0 V reference output when in internal reference mode (a 0.1 µF capacitor to AVSS is required).
35	RESET/PINMD	This pin defines the operation mode of the part. A logic low (pull-down to DVSS) sets the part in SPI mode. Pulse RESET high to reset the SPI registers to their default values. A logic high (pull-up to DVDDIO) puts the device into pin mode (PINMD).
36	SCLK/CLKMD	Clock Input for Serial Port (SCLK). In SPI mode, this pin is the clock input for the serial port. Clock Mode (CLKMD). In pin mode, CLKMD determines the phase of the internal retiming clock. When DCLKIO = CLKIN, tie it to 0. When DCLKIO ≠ CLKIN, pulse 0 to 1 to edge trigger the internal retimer (see the Retimer section).
37	SDIO/FORMAT	Serial Port Input/Output (SDIO). In SPI mode, this pin is the bidirectional data line for the serial port. Format Pin (FORMAT). In pin mode, FORMAT determines the data format of digital data. A logic low (pull-down to DVSS) selects the binary input data format. A logic high (pull-up to DVDDIO) selects the twos complement input data format.
38	$\overline{CS}$/PWRDN	Active Low Chip Select ($\overline{CS}$). In SPI mode, this pin serves as the active low chip select. Power-Down (PWRDN). In pin mode, a logic high (pull-up to DVDDIO) powers down the device, except for the SPI port.
39	DB11 (MSB)	Digital Input (MSB).
40	DB10	Digital Input.
41 (EPAD)	Exposed Pad (EPAD)	The exposed pad is connected to AVSS and should be soldered to the ground plane. Exposed metal at the package corners is connected to this pad.

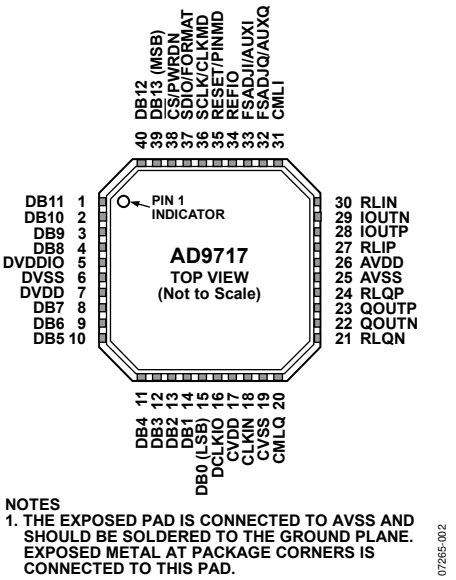

Figure 5. AD9717 Pin Configuration

Table 10. AD9717 Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4	DB[11:8]	Digital Inputs.
5	DVDDIO	Digital I/O Supply Voltage (1.8 V to 3.3 V Nominal).
6	DVSS	Digital Common.
7	DVDD	Digital Core Supply Voltage (1.8 V). Strap DVDD to DVDDIO at 1.8 V. If DVDDIO > 1.8 V, bypass DVDD with a 1.0 µF capacitor; however, do not otherwise connect it. The LDO should not drive external loads.
8 to 14	DB[7:1]	Digital Inputs.
15	DB0 (LSB)	Digital Input (LSB).
16	DCLKIO	Data Input/Output Clock. Clock used to qualify input data.
17	CVDD	Sampling Clock Supply Voltage (1.8 V to 3.3 V). CVDD must be ≥ DVDD.
18	CLKIN	LVCMOS Sampling Clock Input.
19	CVSS	Sampling Clock Supply Voltage Common.
20	CMLQ	Q DAC Output Common-Mode Level. When the internal on chip (QR_{CML}) is enabled, this pin is connected to the on-chip QR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (QR_{CML}) is disabled, this pin is the common-mode load for Q DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
21	RLQN	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTN externally.
22	QOUTN	Complementary Q DAC Current Output. Full-scale current is sourced when all data bits are 0s.
23	QOUTP	Q DAC Current Output. Full-scale current is sourced when all data bits are 1s.
24	RLQP	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTP externally.
25	AVSS	Analog Common.
26	AVDD	Analog Supply Voltage (1.8 V to 3.3 V).
27	RLIP	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTP externally.
28	IOUTP	I DAC Current Output. Full-scale current is sourced when all data bits are 1s.
29	IOUTN	Complementary I DAC Current Output. Full-scale current is sourced when all data bits are 0s.
30	RLIN	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTN externally.

Pin No.	Mnemonic	Description
31	CMLI	I DAC Output Common-Mode Level. When the internal on chip (IR_{CML}) is enabled, this pin is connected to the on-chip IR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (IR_{CML}) is disabled, this pin is the common-mode load for I DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
32	FSADJQ/AUXQ	Full-Scale Current Output Adjust (FSADJQ). When the internal on chip (QR_{SET}) is disabled, this pin is the full-scale current output adjust for Q DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current. Auxiliary Q DAC Output (AUXQ). When the internal on chip (QR_{SET}) is enabled, this pin is the auxiliary Q DAC output.
33	FSADJI/AUXI	Full-Scale Current Output Adjust (FSADJI). When the internal on chip (IR_{SET}) is disabled, this pin is the full-scale current output adjust for I DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current. Auxiliary I DAC Output (AUXI). When the internal on chip (IR_{SET}) is enabled, this pin is the auxiliary I DAC output.
34	REFIO	Reference Input/Output. Serves as a reference input when the internal reference is disabled. Provides a 1.0 V reference output when in internal reference mode (a 0.1 µF capacitor to AVSS is required).
35	RESET/PINMD	This pin defines the operation mode of the part. A logic low (pull-down to DVSS) sets the part in SPI mode. Pulse RESET high to reset the SPI registers to their default values. A logic high (pull-up to DVDDIO) puts the device into pin mode (PINMD).
36	SCLK/CLKMD	Clock Input for Serial Port (SCLK). In SPI mode, this pin is the clock input for the serial port. Clock Mode (CLKMD). In pin mode, CLKMD determines the phase of the internal retiming clock. When DCLKIO = CLKIN, tie it to 0. When DCLKIO ≠ CLKIN, pulse 0 to 1 to edge trigger the internal retimer (see the Retimer section).
37	SDIO/FORMAT	Serial Port Input/Output (SDIO). In SPI mode, this pin is the bidirectional data line for the serial port. Format Pin (FORMAT). In pin mode, FORMAT determines the data format of digital data. A logic low (pull-down to DVSS) selects the binary input data format. A logic high (pull-up to DVDDIO) selects the twos complement input data format.
38	$\overline{CS}$/PWRDN	Active Low Chip Select ($\overline{CS}$). In SPI mode, this pin serves as the active low chip select. Power-Down (PWRDN). In pin mode, a logic high (pull-up to DVDDIO) powers down the device, except for the SPI port.
39	DB13 (MSB)	Digital Input (MSB).
40	DB12	Digital Input.
41 (EPAD)	Exposed Pad (EPAD)	The exposed pad is connected to AVSS and should be soldered to the ground plane. Exposed metal at the package corners is connected to this pad.

TYPICAL PERFORMANCE CHARACTERISTICS

I_{xOUTFS} = 2 mA, maximum sample rate, unless otherwise noted. DVDD is always at 1.8 V.

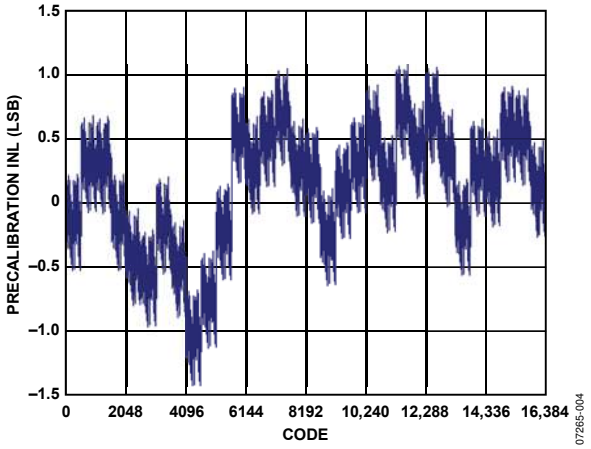

Figure 6. AD9717 Precalibration INL at 1.8 V (DVDD = 1.8 V)

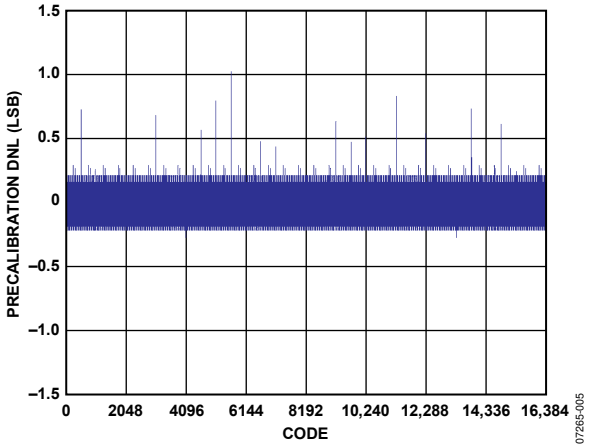

Figure 7. AD9717 Precalibration DNL at 1.8 V (DVDD = 1.8 V)

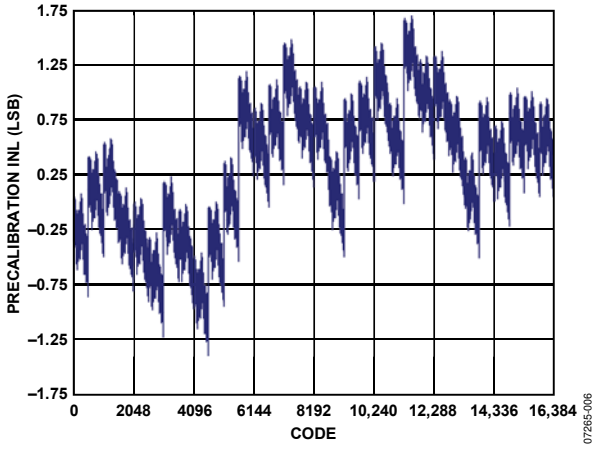

Figure 8. AD9717 Precalibration INL at 3.3 V (DVDD = 1.8 V)

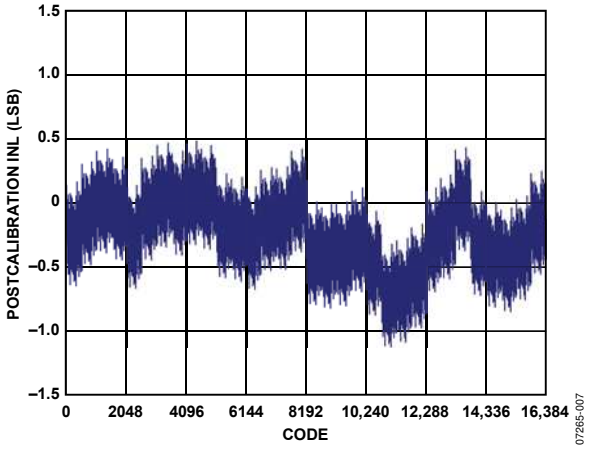

Figure 9. AD9717 Postcalibration INL at 1.8 V (DVDD = 1.8 V)

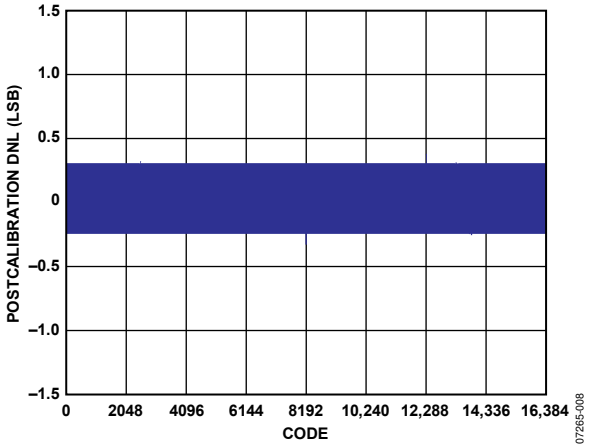

Figure 10. AD9717 Postcalibration DNL at 1.8 V (DVDD = 1.8 V)

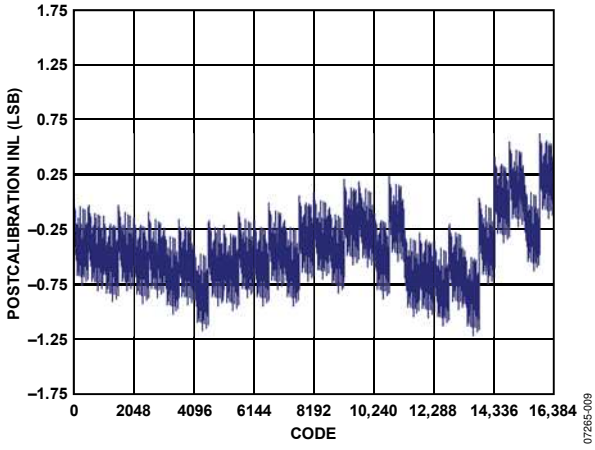

Figure 11. AD9717 Postcalibration INL at 3.3 V (DVDD = 1.8 V)

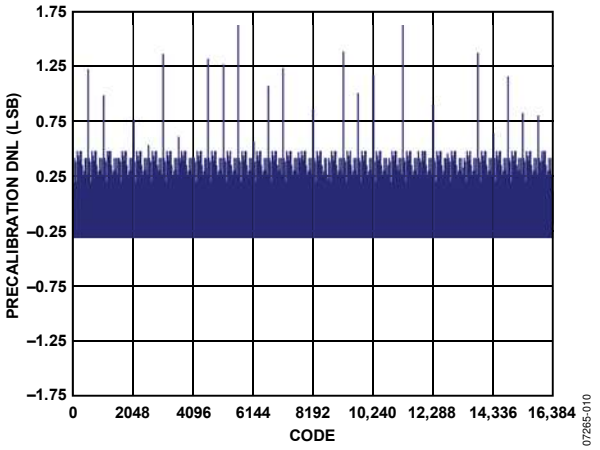

Figure 12. AD9717 Precalibration DNL at 3.3 V

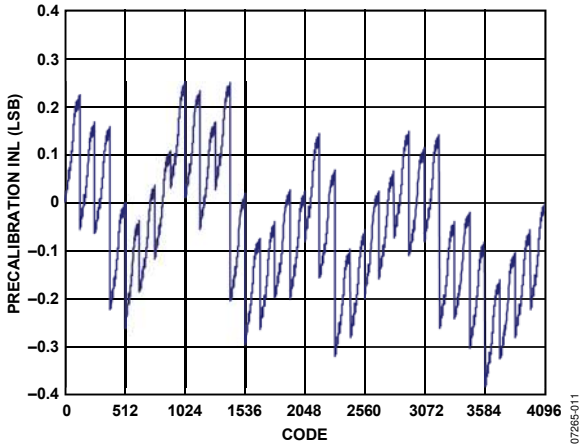

Figure 13. AD9716 Precalibration INL at 1.8 V

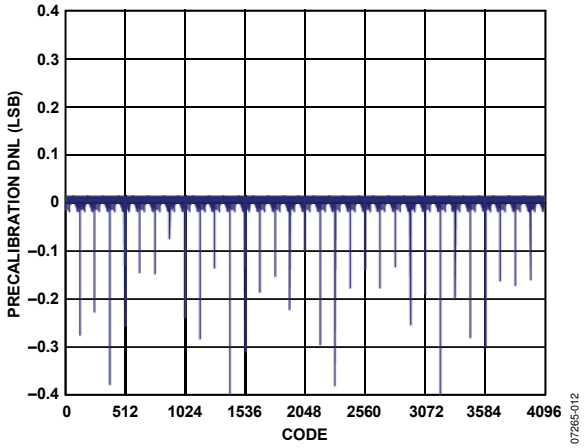

Figure 14. AD9716 Precalibration DNL at 1.8 V

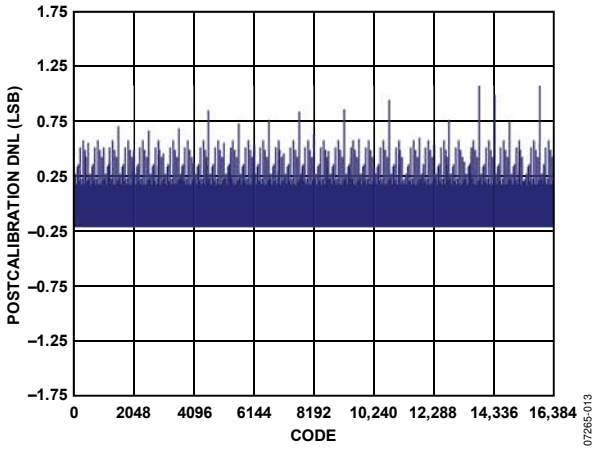

Figure 15. AD9717 Postcalibration DNL at 3.3 V

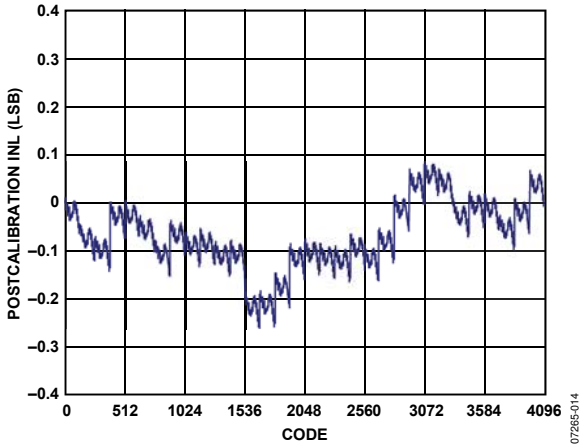

Figure 16. AD9716 Postcalibration INL at 1.8 V

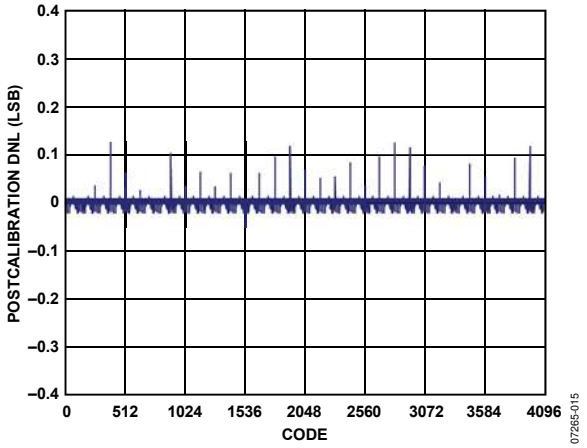

Figure 17. AD9716 Postcalibration DNL at 1.8 V

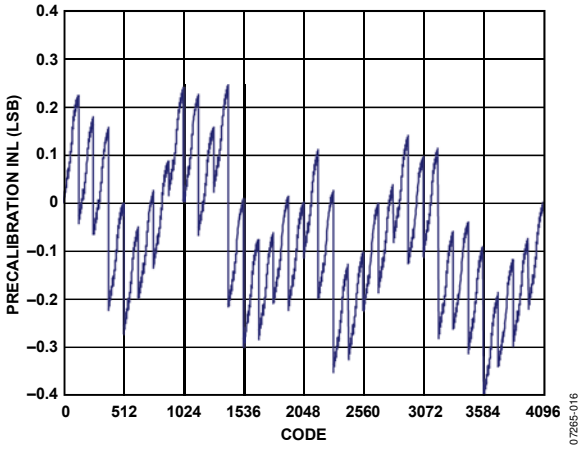

Figure 18. AD9716 Precalibration INL at 3.3 V

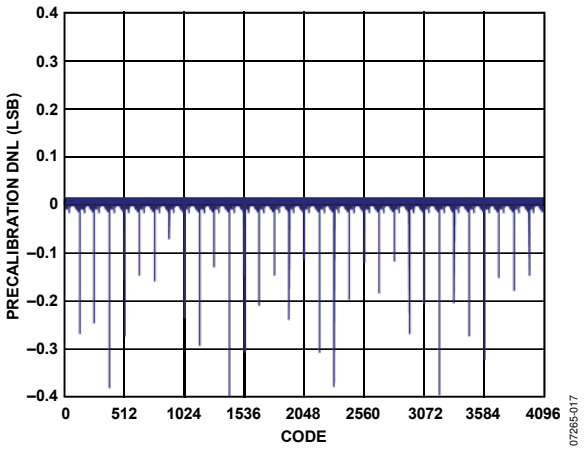

Figure 19. AD9716 Precalibration DNL at 3.3 V

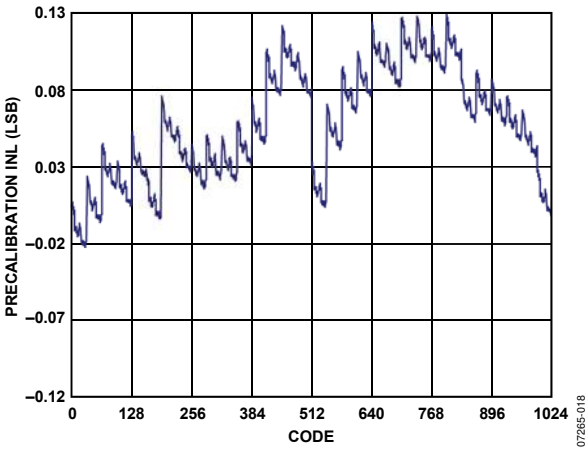

Figure 20. AD9715 Precalibration INL at 1.8 V

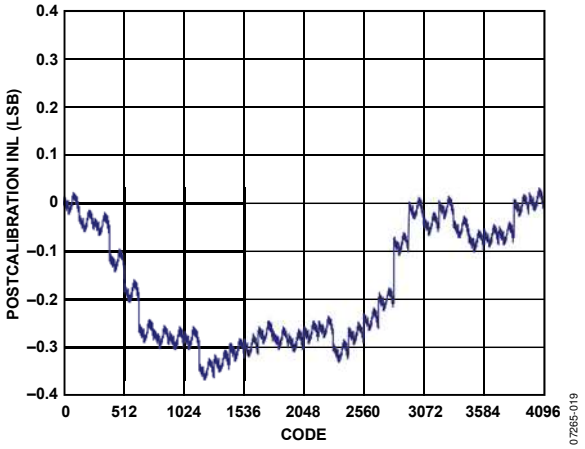

Figure 21. AD9716 Postcalibration INL at 3.3 V

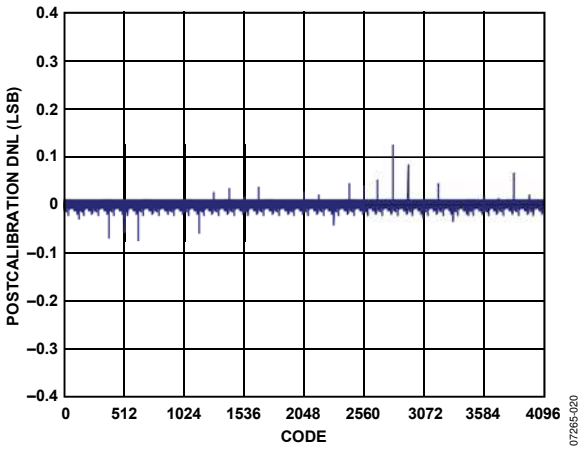

Figure 22. AD9716 Postcalibration DNL at 3.3 V

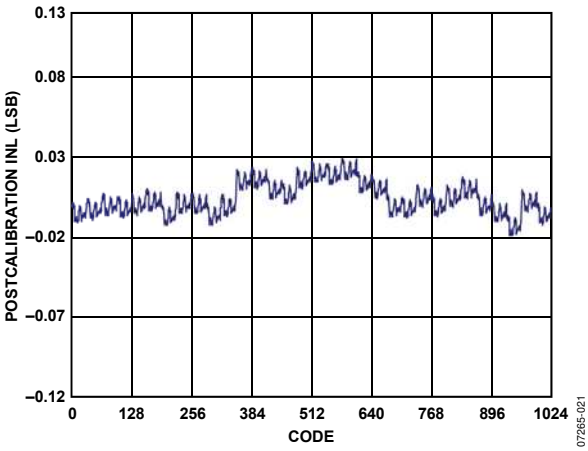

Figure 23. AD9715 Postcalibration INL at 1.8 V

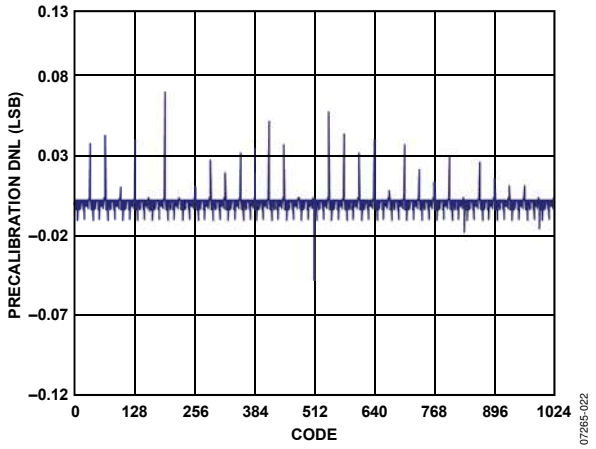

Figure 24. AD9715 Precalibration DNL at 1.8 V

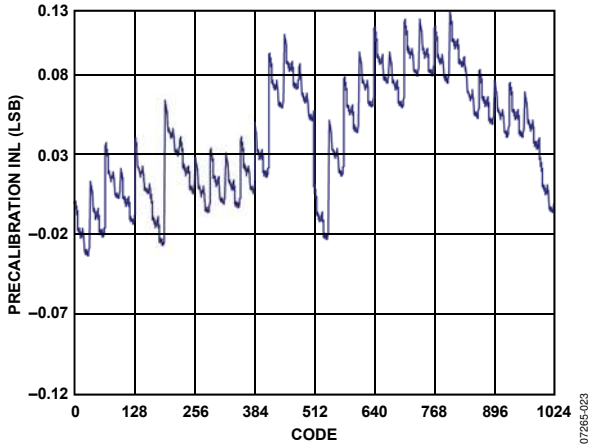

Figure 25. AD9715 Precalibration INL at 3.3 V

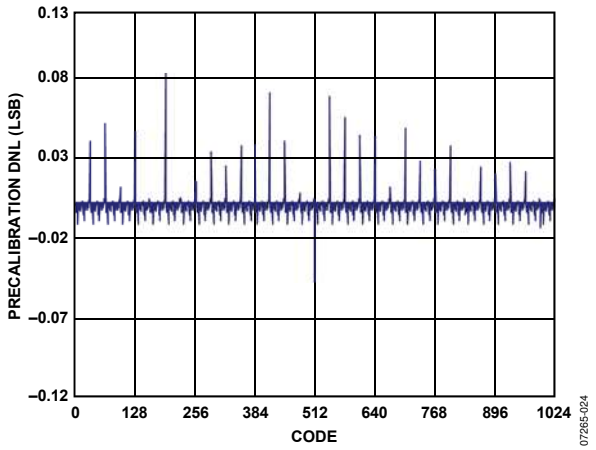

Figure 26. AD9715 Precalibration DNL at 3.3 V

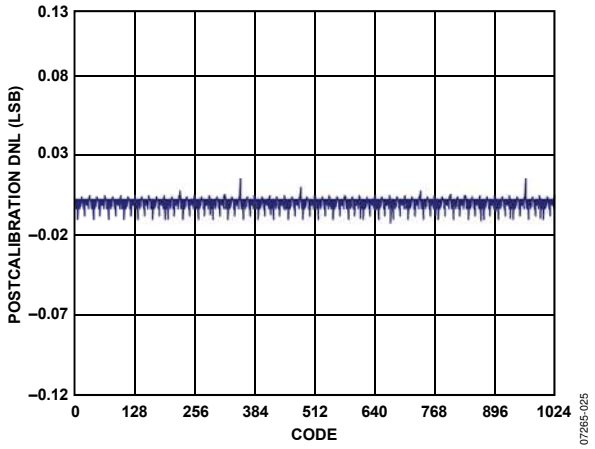

Figure 27. AD9715 Postcalibration DNL at 1.8 V

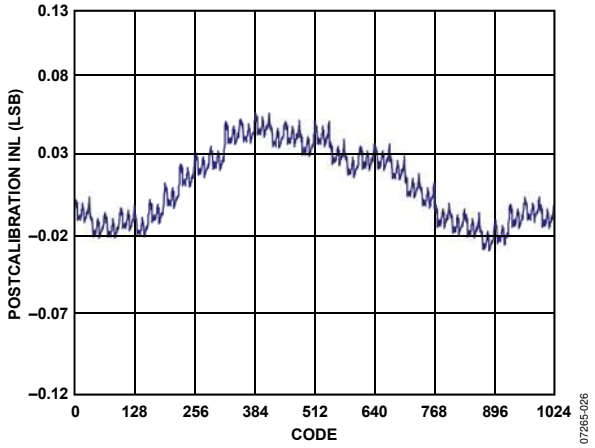

Figure 28. AD9715 Postcalibration INL at 3.3 V

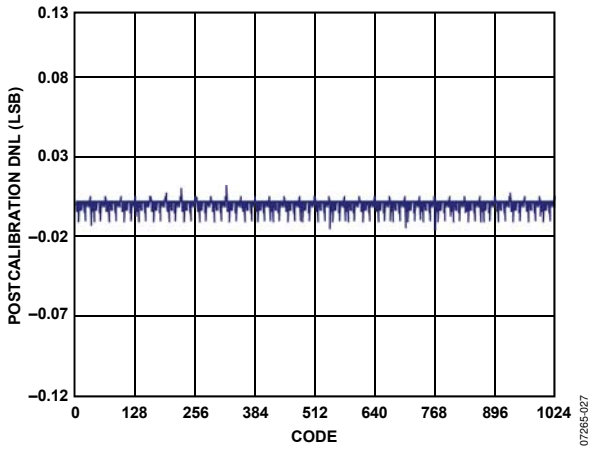

Figure 29. AD9715 Postcalibration DNL at 3.3 V

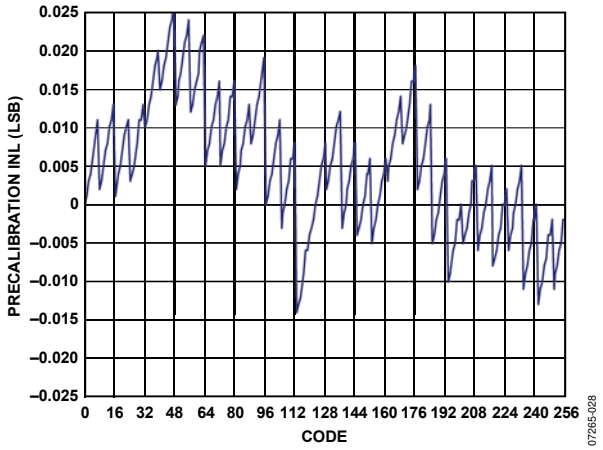

Figure 30. AD9714 Precalibration INL at 1.8 V

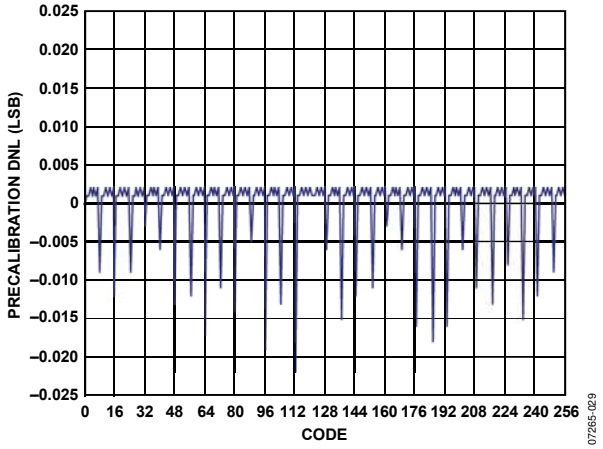

Figure 31. AD9714 Precalibration DNL at 1.8 V

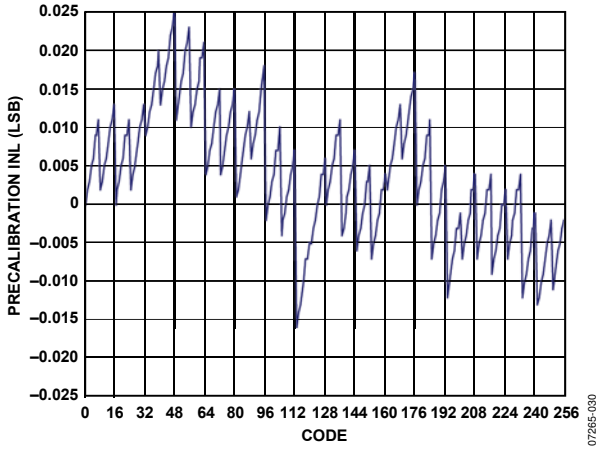

Figure 32. AD9714 Precalibration INL at 3.3 V

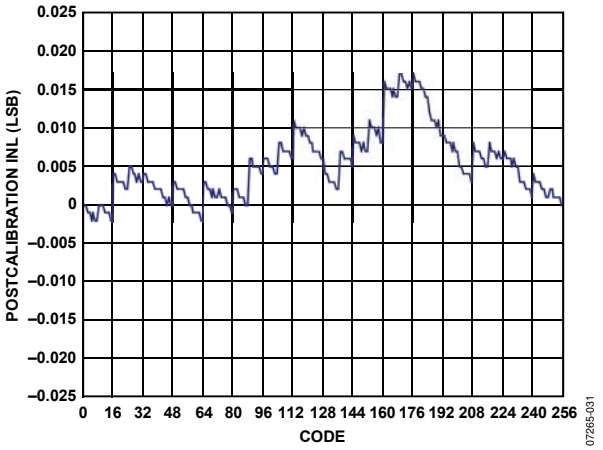

Figure 33. AD9714 Postcalibration INL at 1.8 V

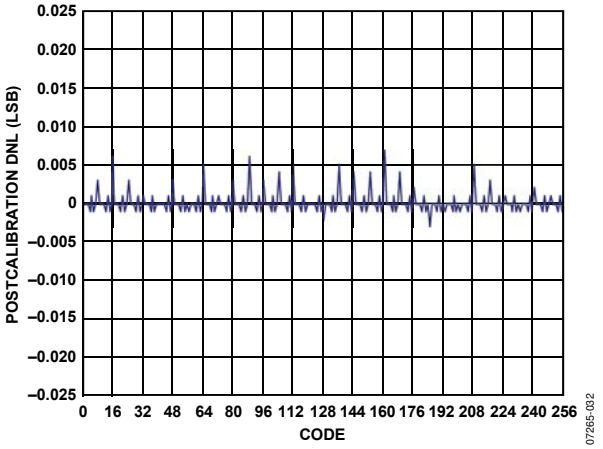

Figure 34. AD9714 Postcalibration DNL at 1.8 V

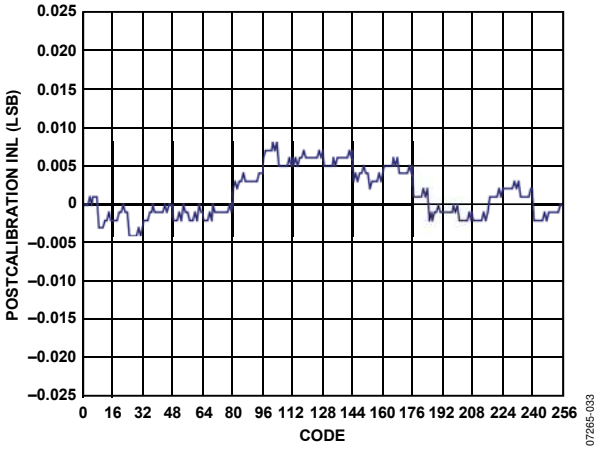

Figure 35. AD9714 Postcalibration INL at 3.3 V

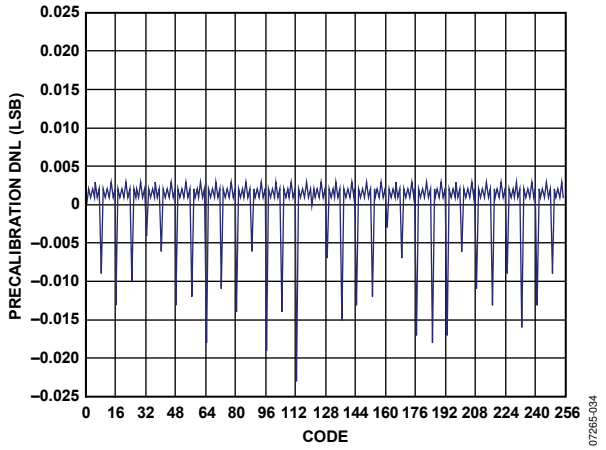

Figure 36. AD9714 Precalibration DNL at 3.3 V

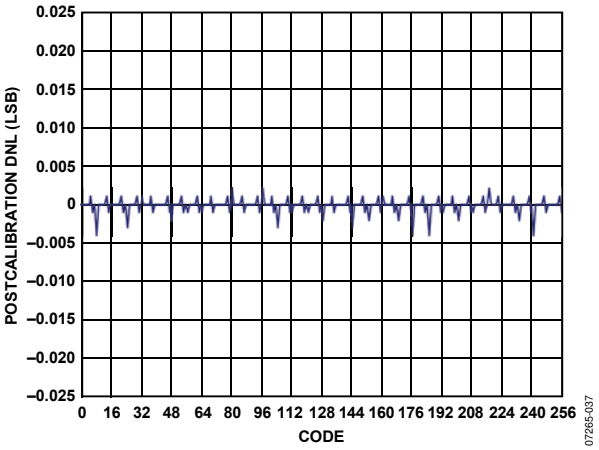

Figure 39. AD9714 Postcalibration DNL at 3.3 V

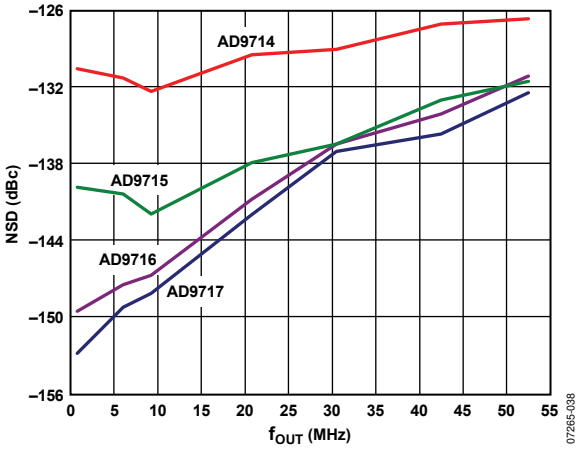

Figure 37. AD9714/AD9715/AD9716/AD9717 Noise Spectral Density at 1.8 V

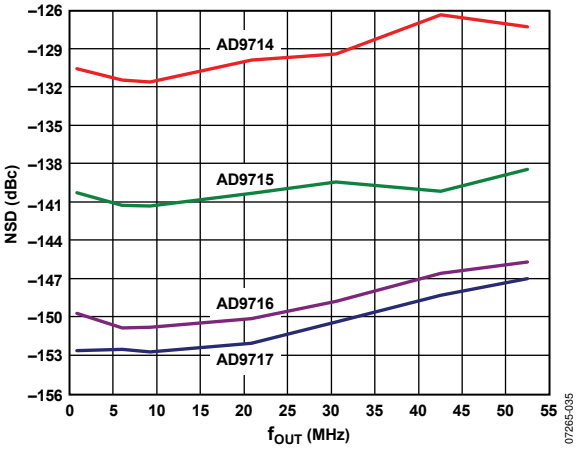

Figure 40. AD9714/AD9715/AD9716/AD9717 Noise Spectral Density at 3.3 V

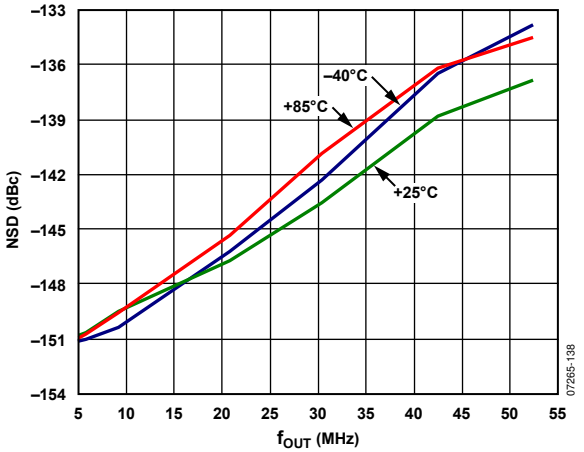

Figure 38. AD9717 Noise Spectral Density at Three Temperatures, 1.8 V

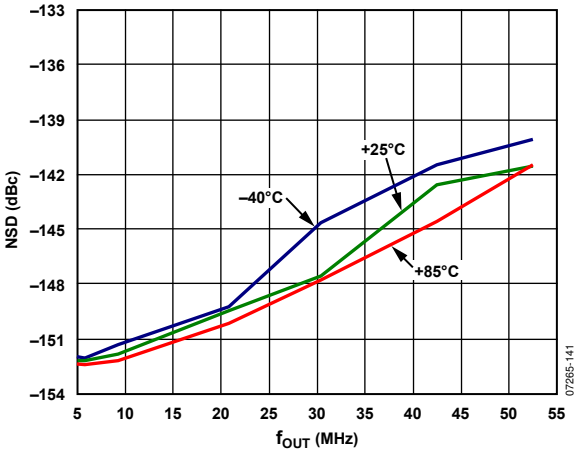

Figure 41. AD9717 Noise Spectral Density at Three Temperatures, 3.3 V

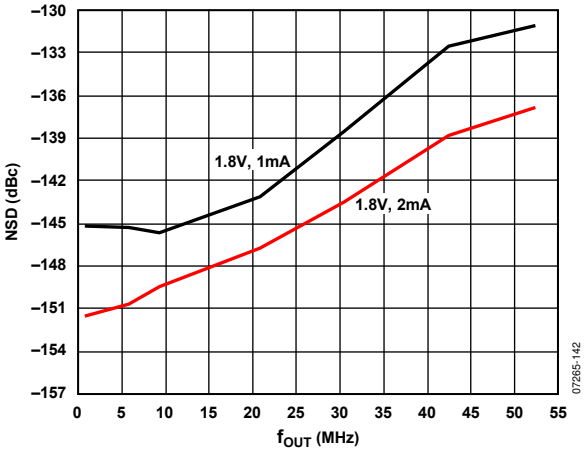

Figure 42. AD9717 Noise Spectral Density at Two Output Currents, 1.8 V

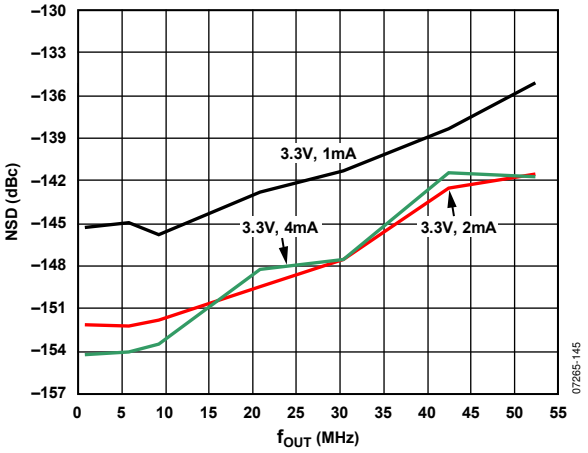

Figure 45. AD9717 Noise Spectral Density at Three Output Currents, 3.3 V

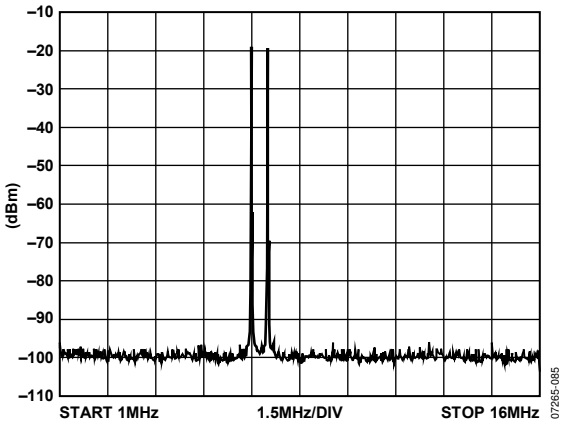

Figure 43. AD9717 Two Tone Spectrum, 1.8 V

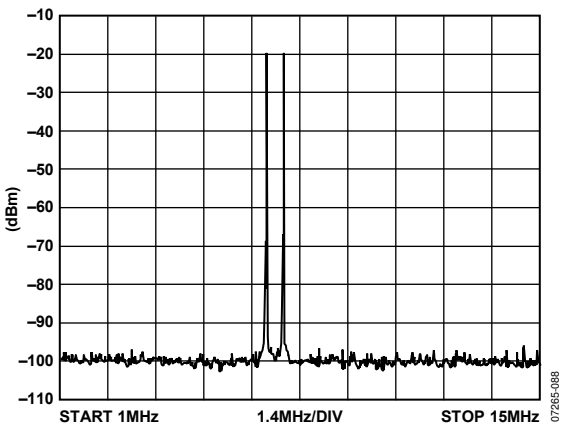

Figure 46. AD9717 Two Tone Spectrum, 3.3 V

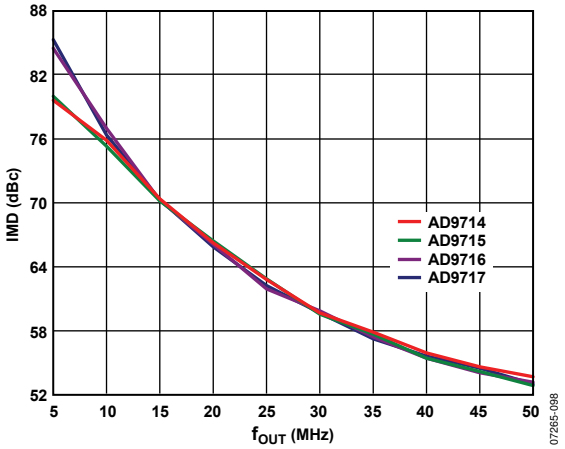

Figure 44. AD9714/AD9715/AD9716/AD9717 IMD at 1.8 V

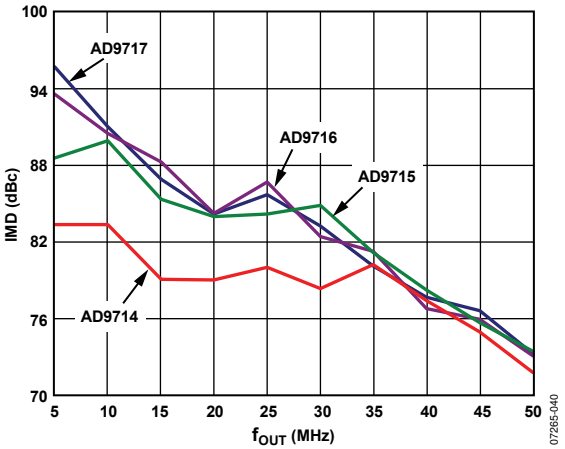

Figure 47. AD9714/AD9715/AD9716/AD9717 IMD at 3.3 V

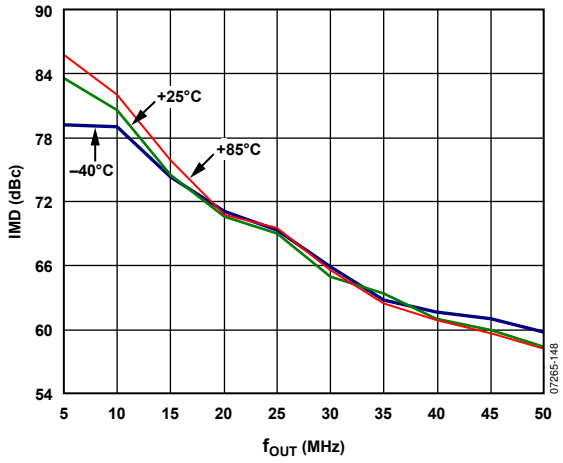

Figure 48. AD9717 IMD at Three Temperatures, 1.8 V

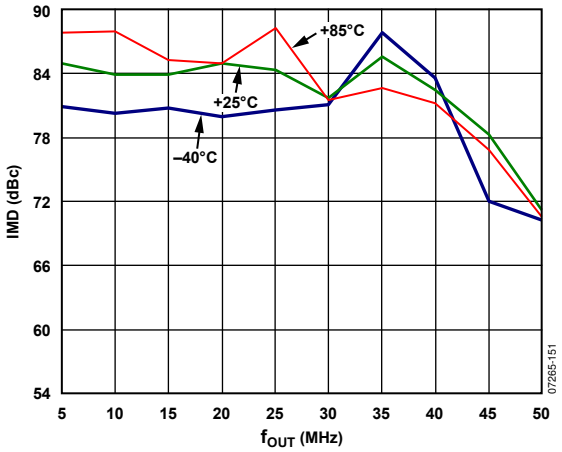

Figure 51. AD9717 IMD at Three Temperatures, 3.3 V

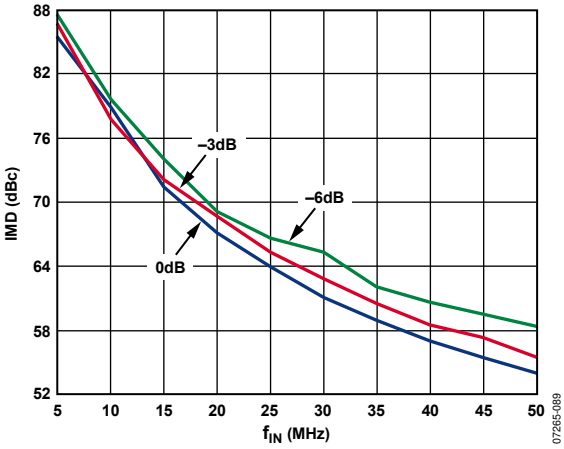

Figure 49. AD9717 IMD at Three Digital Input Levels, 1.8 V

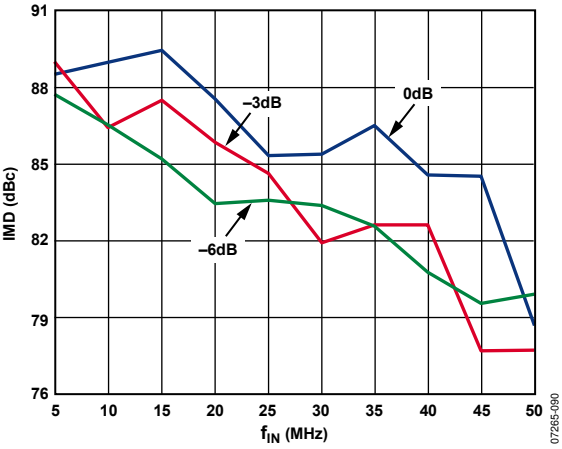

Figure 52. AD9717 IMD at Three Digital Input Levels, 3.3 V

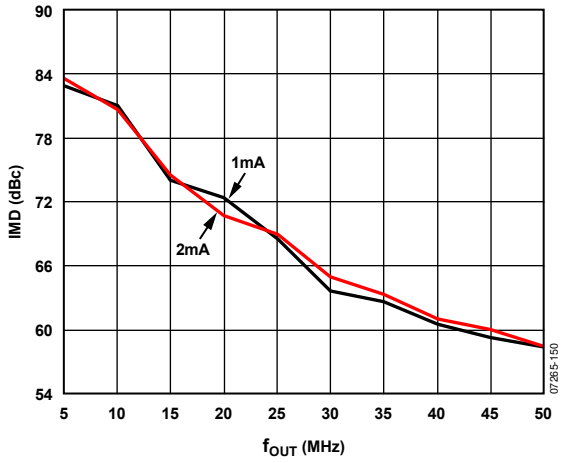

Figure 50. AD9717 IMD at Two Output Currents, 1.8 V

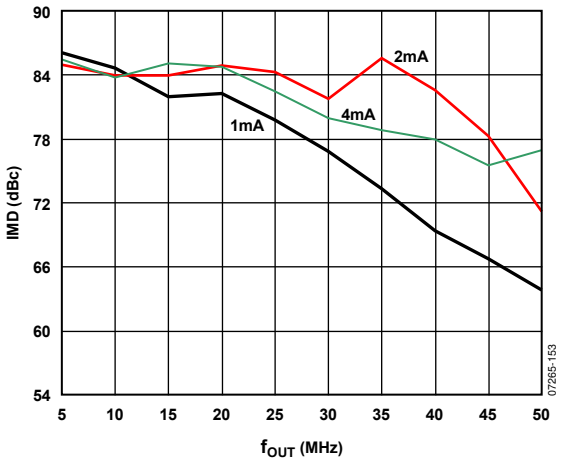

Figure 53. AD9717 IMD at Three Output Currents, 3.3 V