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# 10-/12-/14-Bit, 1200 MSPS DACs

# AD9734/AD9735/AD9736

## FEATURES

- **Pin-compatible family**
- **Excellent dynamic performance**
  - **AD9736: SFDR = 82 dBc at $f_{OUT}$ = 30 MHz**
  - **AD9736: SFDR = 69 dBc at $f_{OUT}$ = 130 MHz**
  - **AD9736: IMD = 87 dBc at $f_{OUT}$ = 30 MHz**
  - **AD9736: IMD = 82 dBc at $f_{OUT}$ = 130 MHz**
- **LVDS data interface with on-chip 100 Ω terminations**
- **Built-in self test**
  - **LVDS sampling integrity**
  - **LVDS-to-DAC data transfer integrity**
- **Low power: 380 mW ($I_{FS}$ = 20 mA; $f_{OUT}$ = 330 MHz)**
- **1.8/3.3 V dual-supply operation**
- **Adjustable analog output**
  - **8.66 mA to 31.66 mA ($R_L$ = 25 Ω to 50 Ω)**
- **On-chip 1.2 V reference**
- **160-lead chip scale ball grid array (CSP_BGA) package**

## APPLICATIONS

- **Broadband communications systems**
  - **Cellular infrastructure (digital predistortion)**
  - **Point-to-point wireless**
  - **CMTS/VOD**
- **Instrumentation, automatic test equipment**
- **Radar, avionics**

## GENERAL DESCRIPTION

The AD9736, AD9735, and AD9734 are high performance, high frequency DACs that provide sample rates of up to 1200 MSPS, permitting multicarrier generation up to their Nyquist frequency. The AD9736 is the 14-bit member of the family, while the AD9735 and the AD9734 are the 12-bit and 10-bit members, respectively. They include a serial peripheral interface (SPI) port that provides for programming of many internal parameters and enables readback of status registers.

A reduced-specification LVDS interface is utilized to achieve the high sample rate. The output current can be programmed over a range of 8.66 mA to 31.66 mA. The AD973x family is manufactured on a 0.18 µm CMOS process and operates from 1.8 V and 3.3 V supplies for a total power consumption of 380 mW in bypass mode. It is supplied in a 160-lead chip scale ball grid array for reduced package parasitics.

## FUNCTIONAL BLOCK DIAGRAM

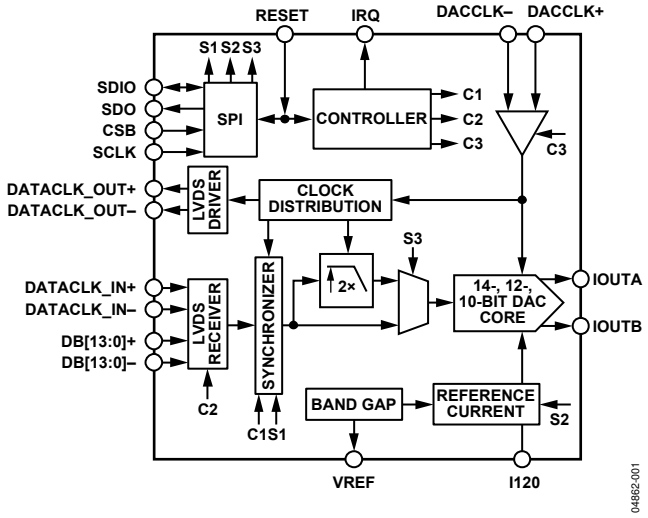


*Figure 1.*

## PRODUCT HIGHLIGHTS

1. Low noise and intermodulation distortion (IMD) features enable high quality synthesis of wideband signals at intermediate frequencies up to 600 MHz.
2. Double data rate (DDR) LVDS data receivers support the maximum conversion rate of 1200 MSPS.
3. Direct pin programmability of basic functions or SPI port access offers complete control of all AD973x family functions.
4. Manufactured on a CMOS process, the AD973x family uses a proprietary switching technique that enhances dynamic performance.
5. The current output(s) of the AD9736 family are easily configured for single-ended or differential circuit topologies.

**Rev. A**


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# TABLE OF CONTENTS

## REVISION HISTORY

**9/06—Rev. 0 to Rev. A**

Updated Format ....Universal
Changes to Table 1 ....5
Changes to Table 2 ....6
Changes to Table 3 ....8
Inserted Table 5 ....9
Replaced Pin Configuration and Function Descriptions Section ....10
Changes to Figure 27 to Figure 38 ....21
Changes to Figure 40 ....23
Changes to Table 9 ....29
Changes to Figure 103 ....56
Changes to Figure 105 ....58
Changes to Figure 107 ....60
Changes to Figure 108 ....61
Changes to Figure 115 ....68
Updated Outline Dimensions ....69
Changes to Ordering Guide ....69

**4/05—Revision 0: Initial Version**

# SPECIFICATIONS

## DC SPECIFICATIONS

AVDD33 = DVDD33 = 3.3 V, CVDD18 = DVDD18 = 1.8 V, maximum sample rate, $I_{FS}$ = 20 mA, 1× mode, 25 Ω, 1% balanced load, unless otherwise noted.

**Table 1.**

| | AD9736 | | | AD9735 | | | AD9734 | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| RESOLUTION | | 14 | | | 12 | | | 10 | | Bits |
| ACCURACY | | | | | | | | | | |
| Integral Nonlinearity (INL) | −5.6 | ±1.0 | +5.6 | −1.5 | ±0.50 | +1.5 | −0.5 | ±0.12 | +0.5 | LSB |
| Differential Nonlinearity (DNL) | −2.1 | ±0.6 | +2.1 | −0.5 | ±0.25 | +0.5 | −0.1 | ±0.06 | +0.1 | LSB |
| ANALOG OUTPUTS | | | | | | | | | | |
| Offset Error | −0.01 | ±0.005 | +0.01 | −0.01 | ±0.005 | +0.01 | −0.01 | ±0.005 | +0.01 | % FSR |
| Gain Error (With Internal Reference) | | ±1.0 | | | ±1.0 | | | ±1.0 | | % FSR |
| Gain Error (Without Internal Reference) | | ±1.0 | | | ±1.0 | | | ±1.0 | | % FSR |
| Full-Scale Output Current | 8.66 | 20.2 | 31.66 | 8.66 | 20.2 | 31.66 | 8.66 | 20.2 | 31.66 | mA |
| Output Compliance Range | −1.0 | | +1.0 | −1.0 | | 1.0 | −1.0 | | +1.0 | V |
| Output Resistance | | 10 | | | 10 | | | 10 | | MΩ |
| Output Capacitance | | 1 | | | 1 | | | 1 | | pF |
| TEMPERATURE DRIFT | | | | | | | | | | |
| Offset | | 0 | | | 0 | | | 0 | | ppm/°C |
| Gain | | 80 | | | 80 | | | 80 | | ppm/°C |
| Reference Voltage[1] | | 40 | | | 40 | | | 40 | | ppm/°C |
| REFERENCE | | | | | | | | | | |
| Internal Reference Voltage[1] | 1.14 | 1.2 | 1.26 | 1.14 | 1.2 | 1.26 | 1.14 | 1.2 | 1.26 | V |
| Output Resistance[2] | | 5 | | | 5 | | | 5 | | kΩ |
| ANALOG SUPPLY VOLTAGES | | | | | | | | | | |
| AVDD33 | 3.13 | 3.3 | 3.47 | 3.13 | 3.3 | 3.47 | 3.13 | 3.3 | 3.47 | V |
| CVDD18 | 1.70 | 1.8 | 1.90 | 1.70 | 1.8 | 1.90 | 1.70 | 1.8 | 1.90 | V |
| DIGITAL SUPPLY VOLTAGES | | | | | | | | | | |
| DVDD33 | 3.13 | 3.3 | 3.47 | 3.13 | 3.3 | 3.47 | 3.13 | 3.3 | 3.47 | V |
| DVDD18 | 1.70 | 1.8 | 1.90 | 1.70 | 1.8 | 1.90 | 1.70 | 1.8 | 1.90 | V |
| SUPPLY CURRENTS | | | | | | | | | | |
| 1× Mode, 1.2 GSPS | | | | | | | | | | |
| $I_{AVDD33}$ | | 25 | | | 25 | | | 25 | | mA |
| $I_{CVDD18}$ | | 47 | | | 47 | | | 47 | | mA |
| $I_{DVDD33}$ | | 10 | | | 10 | | | 10 | | mA |
| $I_{DVDD18}$ | | 122 | | | 122 | | | 122 | | mA |
| FIR Bypass (1×) Mode | | 380 | | | 380 | | | 380 | | mW |
| 2× Mode, 1.2 GSPS | | | | | | | | | | |
| $I_{AVDD33}$ | | 25 | | | 25 | | | 25 | | mA |
| $I_{CVDD18}$ | | 47 | | | 47 | | | 47 | | mA |
| $I_{DVDD33}$ | | 10 | | | 10 | | | 10 | | mA |
| $I_{DVDD18}$ | | 234 | | | 234 | | | 234 | | mA |
| FIR 2× Interpolation Filter Enabled | | 550 | | | 550 | | | 550 | | mW |

| Parameter | AD9736 Min | AD9736 Typ | AD9736 Max | AD9735 Min | AD9735 Typ | AD9735 Max | AD9734 Min | AD9734 Typ | AD9734 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Static, No Clock | | | | | | | | | | |
| $I_{AVDD33}$ | | 25 | | | 25 | | | 25 | | mA |
| $I_{CVDD18}$ | | 8 | | | 8 | | | 8 | | mA |
| $I_{DVDD33}$ | | 10 | | | 10 | | | 10 | | mA |
| $I_{DVDD18}$ | | 2 | | | 2 | | | 2 | | mA |
| FIR Bypass (1×) Mode | | 133 | | | 133 | | | 133 | | mW |
| Sleep Mode, No Clock | | | | | | | | | | |
| $I_{AVDD33}$ | | 2.5 | 3.15 | | 2.5 | 3.15 | | 2.5 | 3.15 | mA |
| FIR Bypass (1×) Mode | | 59 | 65 | | 59 | 65 | | 59 | 65 | mW |
| Power-Down Mode[3] | | | | | | | | | | |
| $I_{AVDD33}$ | | 0.01 | 0.13 | | 0.01 | 0.13 | | 0.01 | 0.13 | mA |
| $I_{CVDD18}$ | | 0.02 | 0.12 | | 0.02 | 0.12 | | 0.02 | 0.12 | mA |
| $I_{DVDD33}$ | | 0.01 | 0.12 | | 0.01 | 0.12 | | 0.01 | 0.12 | mA |
| $I_{DVDD18}$ | | 0.01 | 0.11 | | 0.01 | 0.11 | | 0.01 | 0.11 | mA |
| FIR Bypass (1×) Mode | | 0.12 | 1.24 | | 0.12 | 1.24 | | 0.12 | 1.24 | mW |

[1] Default band gap adjustment (Reg. 0x0E <2:0> = 0x0).
[2] Use an external amplifier to drive any external load.
[3] Typical wake-up time is 8 µs with recommended 1 nF capacitor on VREF pin.

## DIGITAL SPECIFICATIONS

AVDD33 = DVDD33 = 3.3 V, CVDD18 = DVDD18 = 1.8 V, maximum sample rate, $I_{FS}$ = 20 mA, 1× mode, 25 Ω, 1% balanced load, unless otherwise noted. LVDS drivers and receivers are compliant to the IEEE-1596 reduced range link, unless otherwise noted.

**Table 2.**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| LVDS DATA INPUT (DB[13:0]+, DB[13:0]–) DB+ = $V_{IA}$, DB– = $V_{IB}$ | | | | |
| Input Voltage Range, $V_{IA}$ or $V_{IB}$ | 825 | | 1575 | mV |
| Input Differential Threshold, $V_{IDTH}$ | −100 | | +100 | mV |
| Input Differential Hysteresis, $V_{IDTHH} - V_{IDTHL}$ | | 20 | | mV |
| Receiver Differential Input Impedance, $R_{IN}$ | 80 | | 120 | Ω |
| LVDS Input Rate | 1200 | | | MSPS |
| LVDS Minimum Data Valid Period ($t_{MDE}$) | | | 344 | ps |
| LVDS CLOCK INPUT (DATACLK_IN+, DATACLK_IN–) DATACLK_IN+ = $V_{IA}$, DATACLK_IN– = $V_{IB}$ | | | | |
| Input Voltage Range, $V_{IA}$ or $V_{IB}$ | 825 | | 1575 | mV |
| Input Differential Threshold,[1] $V_{IDTH}$ | −100 | | +100 | mV |
| Input Differential Hysteresis, $V_{IDTHH} - V_{IDTHL}$ | | 20 | | mV |
| Receiver Differential Input Impedance, $R_{IN}$ | 80 | | 120 | Ω |
| Maximum Clock Rate | 600 | | | MHz |
| LVDS CLOCK OUTPUT (DATACLK_OUT+, DATACLK_ OUT–) DATACLK_OUT+ = $V_{oa}$, DATACLK_OUT– = $V_{ob}$ 100 Ω Termination | | | | |
| Output Voltage High, $V_{OA}$ or $V_{OB}$ | | | 1375 | mV |
| Output Voltage Low, $V_{OA}$ or $V_{OB}$ | 1025 | | | mV |
| Output Differential Voltage, $\|V_{OD}\|$ | 150 | 200 | 250 | mV |
| Output Offset Voltage, $V_{OS}$ | 1150 | | 1250 | mV |
| Output Impedance, Single-Ended, $R_O$ | 80 | 100 | 120 | Ω |
| $R_O$ Mismatch Between A and B, $\Delta R_O$ | | | 10 | % |
| Change in $\|V_{OD}\|$ Between 0 and 1, $\|\Delta V_{OD}\|$ | | | 25 | mV |
| Change in $V_{OS}$ Between 0 and 1, $\Delta V_{OS}$ | | | 25 | mV |
| Output Current—Driver Shorted to Ground, $I_{SA}$, $I_{SB}$ | | | 20 | mA |
| Output Current—Drivers Shorted Together, $I_{SAB}$ | | | 4 | mA |
| Power-Off Output Leakage, $\|I_{XA}\|$, $\|I_{XB}\|$ | | | 10 | mA |
| Maximum Clock Rate | 600 | | | MHz |
| DAC CLOCK INPUT (CLK+, CLK–) | | | | |
| Input Voltage Range, CLK– or CLK+ | 0 | | 800 | |
| Differential Peak-to-Peak Voltage | 400 | 800 | 1600 | mV |
| Common-Mode Voltage | 300 | 400 | 500 | mV |
| Maximum Clock Rate | 1200 | | | MHz |
| SERIAL PERIPHERAL INTERFACE | | | | |
| Maximum Clock Rate ($f_{SCLK}$, $1/t_{SCLK}$) | | | 20 | MHz |
| Minimum Pulse Width High, $t_{PWH}$ | 20 | | | ns |
| Minimum Pulse Width Low, $t_{PWL}$ | 20 | | | ns |
| Minimum SDIO and CSB to SCLK Setup, $t_{DS}$ | | 10 | | ns |
| Minimum SCLK to SDIO Hold, $t_{DH}$ | | 5 | | ns |
| Maximum SCLK to Valid SDIO and SDO, $t_{DV}$ | | 20 | | ns |
| Minimum SCLK to Invalid SDIO and SDO, $t_{DNV}$ | | 5 | | ns |

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| INPUT (SDI, SDIO, SCLK, CSB) | | | | |
| Voltage in High, $V_{IH}$ | 2.0 | 3.3 | | V |
| Voltage in Low, $V_{IL}$ | | 0 | 0.8 | V |
| Current in High, $I_{IH}$ | −10 | | +10 | µA |
| Current in Low, $I_{IL}$ | −10 | | +10 | µA |
| SDIO OUTPUT | | | | |
| Voltage out High, $V_{OH}$ | 2.4 | | 3.6 | V |
| Voltage out Low, $V_{OL}$ | 0 | | 0.4 | V |
| Current out High, $I_{OH}$ | | 4 | | mA |
| Current out Low, $I_{OL}$ | | 4 | | mA |

[1]Refer to the Input Data Timing section for recommended LVDS differential drive levels.

## AC SPECIFICATIONS

AVDD33 = DVDD33 = 3.3 V, CVDD18 = DVDD18 = 1.8 V, maximum sample rate, $I_{FS}$ = 20 mA, 1× mode, 25 Ω, 1% balanced load, unless otherwise noted.

**Table 3.**

| | AD9736 | | | AD9735 | | | AD9734 | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| DYNAMIC PERFORMANCE | | | | | | | | | | |
| Maximum Update Rate | 1200 | | | 1200 | | | 1200 | | | MSPS |
| SPURIOUS-FREE DYNAMIC RANGE (SFDR) | | | | | | | | | | |
| $f_{DAC}$ = 800 MSPS | | | | | | | | | | |
| $f_{OUT}$ = 20 MHz | | 75 | | | 75 | | | 75 | | dBc |
| $f_{DAC}$ = 1200 MSPS | | | | | | | | | | |
| $f_{OUT}$ = 50 MHz | | 80 | | | 76 | | | 76 | | dBc |
| $f_{OUT}$ = 100 MHz | | 77 | | | 74 | | | 71 | | dBc |
| $f_{OUT}$ = 316 MHz | | 63 | | | 63 | | | 60 | | dBc |
| $f_{OUT}$ = 550 MHz | | 55 | | | 54 | | | 53 | | dBc |
| TWO-TONE INTERMODULATION DISTORTION (IMD) | | | | | | | | | | |
| $f_{DAC}$ = 1200 MSPS | | | | | | | | | | |
| $f_{OUT2} = f_{OUT} + 1.25$ MHz | | | | | | | | | | |
| $f_{OUT}$ = 40 MHz | | 88 | | | 84 | | | 83 | | dBc |
| $f_{OUT}$ = 50 MHz | | 85 | | | 84 | | | 83 | | dBc |
| $f_{OUT}$ = 100 MHz | | 84 | | | 81 | | | 79 | | dBc |
| $f_{OUT}$ = 316 MHz | | 70.5 | | | 67 | | | 66 | | dBc |
| $f_{OUT}$ = 550 MHz | | 65 | | | 60 | | | 60 | | dBc |
| NOISE SPECTRAL DENSITY (NSD) | | | | | | | | | | |
| Single Tone | | | | | | | | | | |
| $f_{DAC}$ = 1200 MSPS | | | | | | | | | | |
| $f_{OUT}$ = 50 MHz | | −165 | | | −162 | | | −154 | | dBm/Hz |
| $f_{OUT}$ = 100 MHz | | −164 | | | −161 | | | −154 | | dBm/Hz |
| $f_{OUT}$ = 241MHz | −158.5 | −160.5 | | | −159.5 | | | −155 | | dBm/Hz |
| $f_{OUT}$ = 316 MHz | | −158 | | | −157 | | | −152 | | dBm/Hz |
| $f_{OUT}$ = 550 MHz | | −155 | | | −155 | | | −149 | | dBm/Hz |
| Eight-Tone | | | | | | | | | | |
| $f_{DAC}$ = 1200 MSPS, 500 kHz Tone Spacing | | | | | | | | | | |
| $f_{OUT}$ = 50 MHz | | −166.5 | | | −163 | | | −154 | | dBm/Hz |
| $f_{OUT}$ = 100 MHz | | −166 | | | −163 | | | −152 | | dBm/Hz |
| $f_{OUT}$ = 241MHz | −163.3 | −165 | | | −161.5 | | | −150.5 | | dBm/Hz |
| $f_{OUT}$ = 316 MHz | | −164 | | | −162 | | | −151 | | dBm/Hz |
| $f_{OUT}$ = 550 MHz | | −162 | | | −160 | | | −150 | | dBm/Hz |

# ABSOLUTE MAXIMUM RATINGS

**Table 4.**

| Parameter | With Respect to | Min | Max |
|---|---|---|---|
| AVDD33 | AVSS | −0.3 V | +3.6 V |
| DVDD33 | DVSS | −0.3 V | +3.6 V |
| DVDD18 | DVSS | −0.3 V | +1.98 V |
| CVDD18 | CVSS | −0.3 V | +1.98 V |
| AVSS | DVSS | −0.3 V | +0.3 V |
| AVSS | CVSS | −0.3 V | +0.3 V |
| DVSS | CVSS | −0.3 V | +0.3 V |
| CLK+, CLK− | CVSS | −0.3 V | CVDD18 + 0.18 V |
| PIN_MODE | DVSS | −0.3 V | DVDD33 + 0.3 V |
| DATACLK_IN, DATACLK_OUT | DVSS | −0.3 V | DVDD33 + 0.3 V |
| LVDS Data Inputs | DVSS | −0.3 V | DVDD33 + 0.3 V |
| IOUTA, IOUTB | AVSS | −1.0 V | AVDD33 + 0.3 V |
| I120, VREF, IPTAT | AVSS | −0.3 V | AVDD33 + 0.3 V |
| IRQ, CSB, SCLK, SDO, SDIO, RESET | DVSS | −0.3 V | DVDD33 + 0.3 V |
| Junction Temperature | | | 150°C |
| Storage Temperature | | −65°C | +150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 5. Thermal Resistance**

| Package Type | $\theta_{JA}$[1] | Unit |
|---|---|---|
| 160-Lead Ball, CSP_BGA | 31.2 | °C/W |

[1] $\theta_{JA}$ measurement in still air.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.


Note that this device in its current form does not meet Analog Devices' standard requirements for ESD as measured against the charged device model (CDM). As such, special care should be used when handling this product, especially in a manufacturing environment. Analog Devices will provide a more ESD-hardy product in the near future at which time this warning will be removed from this data sheet.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

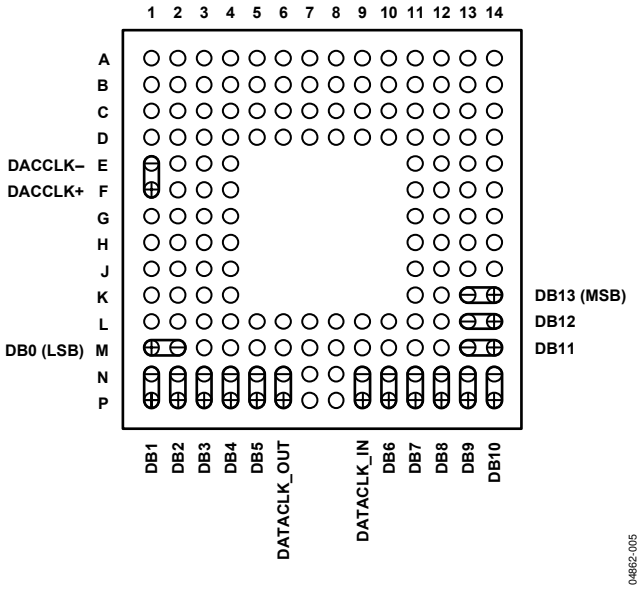


*Figure 2. AD9736 Digital LVDS Input, Clock I/O (Top View)*

**Table 6. AD9736 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| A1, A2, A3, B1, B2, B3, C1, C2, C3, D2, D3 | CVDD18 | 1.8 V Clock Supply. |
| A4, A5, A6, A9, A10, A11, B4, B5, B6, B9, B10, B11, C4, C5, C6, C9, C10, C11, D4, D5, D6, D9, D10, D11 | AVSS | Analog Supply Ground. |
| A7, B7, C7, D7 | IOUTB | DAC Negative Output. 10 mA to 30 mA full-scale output current. |
| A8, B8, C8, D8 | IOUTA | DAC Positive Output. 10 mA to 30 mA full-scale output current. |
| A12, A13, B12, B13, C12, C13, D12, D13 | AVDD33 | 3.3 V Analog Supply. |
| A14 | DNC | Do Not Connect. |
| B14 | I120 | Nominal 1.2 V Reference. Tie to analog ground via 10 kΩ resistor to generate a 120 µA reference current. |
| C14 | VREF | Band Gap Voltage Reference I/O. Tie to analog ground via 1 nF capacitor; output impedance is approximately 5 kΩ. |
| D1, E2, E3, E4, F2, F3, F4, G1, G2, G3, G4 | CVSS | Clock Supply Ground. |
| D14 | IPTAT | Factory Test Pin. Output current, proportional to absolute temperature, is approximately 10 µA at 25°C with a slope of approximately 20 nA/°C. |
| E1, F1 | DACCLK–/DACCLK+ | Negative/Positive DAC Clock Input (DACCLK). |
| E11, E12, F11, F12, G11, G12 | AVSS | Analog Supply Ground Shield. Tie to AVSS at the DAC. |
| E13 | IRQ/UNSIGNED | If PIN_MODE = 0, IRQ: Active low open-drain interrupt request output, pull up to DVDD33 with 10 kΩ resistor.<br>If PIN_MODE = 1, UNSIGNED: Digital input pin where 0 = twos complement input data format, 1 = unsigned. |
| E14 | RESET/PD | If PIN_MODE = 0, RESET: 1 resets the AD9736.<br>If PIN_MODE = 1, PD: 1 puts the AD9736 in the power-down state. |
| F13 | CSB/2× | See the Serial Peripheral Interface section and the Pin Mode Operation section for pin description. |
| F14 | SDIO/FIFO | See the Pin Mode Operation section for pin description. |
| G13 | SCLK/FSC0 | See the Pin Mode Operation section for pin description. |
| G14 | SDO/FSC1 | See the Pin Mode Operation section for pin description. |
| H1, H2, H3, H4, H11, H12, H13, H14, J1, J2, J3, J4, J11, J12, J13, J14 | DVDD18 | 1.8 V Digital Supply. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| K1, K2, K3, K4, K11, K12, L2, L3, L4, L5, L6, L9, L10, L11, L12, M3, M4, M5, M6, M9, M10, M11, M12 | DVSS | Digital Supply Ground. |
| K13, K14 | DB<13>−/DB<13>+ | Negative/Positive Data Input Bit 13 (MSB). Conforms to IEEE-1596 reduced range link. |
| L1 | PIN_MODE | 0 = SPI Mode. SPI is enabled.<br>1 = PIN Mode. SPI is disabled; direct pin control. |
| L7, L8, M7, M8, N7, N8, P7, P8 | DVDD33 | 3.3 V Digital Supply. |
| L13, L14 | DB<12>−/DB<12>+ | Negative/Positive Data Input Bit 12. Conforms to IEEE-1596 reduced range link. |
| M2, M1 | DB<0>−/DB<0>+ | Negative/Positive Data Input Bit 0 (LSB). Conforms to IEEE-1596 reduced range link. |
| M13, M14 | DB<11>−/DB<11>+ | Negative/Positive Data Input Bit 11. Conforms to IEEE-1596 reduced range link. |
| N1, P1 | DB<1>−/DB<1>+ | Negative/Positive Data Input Bit 1. Conforms to IEEE-1596 reduced range link. |
| N2, P2 | DB<2>−/DB<2>+ | Negative/Positive Data Input Bit 2. Conforms to IEEE-1596 reduced range link. |
| N3, P3 | DB<3>−/DB<3>+ | Negative/Positive Data Input Bit 3. Conforms to IEEE-1596 reduced range link. |
| N4, P4 | DB<4>−/DB<4>+ | Negative/Positive Data Input Bit 4. Conforms to IEEE-1596 reduced range link. |
| N5, P5 | DB<5>−/DB<5>+ | Negative/Positive Data Input Bit 5. Conforms to IEEE-1596 reduced range link. |
| N6, P6 | DATACLK_OUT−/ DATACLK_OUT+ | Negative/Positive Data Output Clock. Conforms to IEEE-1596 reduced range link. |
| N9, P9 | DATACLK_IN−/ DATACLK_IN+ | Negative/Positive Data Input Clock. Conforms to IEEE-1596 reduced range link. |
| N10, P10 | DB<6>−/DB<6>+ | Negative/Positive Data Input Bit 6. Conforms to IEEE-1596 reduced range link. |
| N11, P11 | DB<7>−/DB<7>+ | Negative/Positive Data Input Bit 7. Conforms to IEEE-1596 reduced range link. |
| N12, P12 | DB<8>−/DB<8>+ | Negative/Positive Data Input Bit 8. Conforms to IEEE-1596 reduced range link. |
| N13, P13 | DB<9>−/DB<9>+ | Negative/Positive Data Input Bit 9. Conforms to IEEE-1596 reduced range link. |
| N14, P14 | DB<10>−/DB<10>+ | Negative/Positive Data Input Bit 10. Conforms to IEEE-1596 reduced range link. |

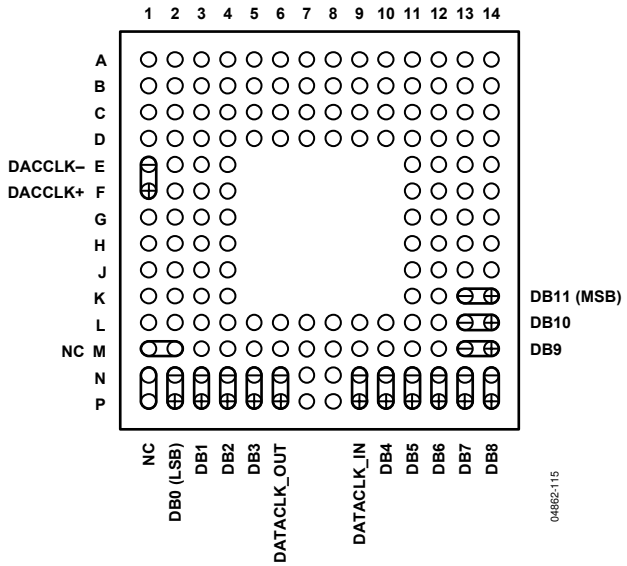


*Figure 3. AD9735 Digital LVDS Input, Clock I/O (Top View)*

**Table 7. AD9735 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| A1, A2, A3, B1, B2, B3, C1, C2, C3, D2, D3 | CVDD18 | 1.8 V Clock Supply. |
| A4, A5, A6, A9, A10, A11, B4, B5, B6, B9, B10, B11, C4, C5, C6, C9, C10, C11, D4, D5, D6, D9, D10, D11 | AVSS | Analog Supply Ground. |
| A7, B7, C7, D7 | IOUTB | DAC Negative Output. 10 mA to 30 mA full-scale output current. |
| A8, B8, C8, D8 | IOUTA | DAC Positive Output. 10 mA to 30 mA full-scale output current. |
| A12, A13, B12, B13, C12, C13, D12, D13 | AVDD33 | 3.3 V Analog Supply. |
| A14 | DNC | Do Not Connect. |
| B14 | I120 | Nominal 1.2 V Reference. Tie to analog ground via 10 kΩ resistor to generate a 120 µA reference current. |
| C14 | VREF | Band Gap Voltage Reference I/O. Tie to analog ground via 1 nF capacitor; output impedance approximately 5 kΩ. |
| D1, E2, E3, E4, F2, F3, F4, G1, G2, G3, G4 | CVSS | Clock Supply Ground. |
| D14 | IPTAT | Factory Test Pin; Output current, proportional to absolute temperature, is approximately 10 µA at 25°C with a slope of approximately 20 nA/°C. |
| E1, F1 | DACCLK–/DACCLK+ | Negative/Positive DAC Clock Input (DACCLK). |
| E11, E12, F11, F12, G11, G12 | AVSS | Analog Supply Ground Shield. Tie to AVSS at the DAC. |
| E13 | IRQ/UNSIGNED | If PIN_MODE = 0, IRQ: Active low open-drain interrupt request output, pull up to DVDD33 with 10 kΩ resistor.<br>If PIN_MODE = 1, UNSIGNED: Digital input pin where 0 = twos complement input data format, 1 = unsigned. |
| E14 | RESET/PD | If PIN_MODE = 0, RESET: 1 resets the AD9735.<br>If PIN_MODE = 1, PD: 1 puts the AD9735 in the power-down state. |
| F13 | CSB/2× | See the Serial Peripheral Interface section and the Pin Mode Operation section for pin description. |
| F14 | SDIO/FIFO | See the Pin Mode Operation section for pin description. |
| G13 | SCLK/FSC0 | See the Pin Mode Operation section for pin description. |
| G14 | SDO/FSC1 | See the Pin Mode Operation section for pin description. |
| H1, H2, H3, H4, H11, H12, H13, H14, J1, J2, J3, J4, J11, J12, J13, J14 | DVDD18 | 1.8 V Digital Supply. |
| K1, K2, K3, K4, K11, K12, L2, L3, L4, L5, L6, L9, L10, L11, L12, M3, M4, M5, M6, M9, M10, M11, M12 | DVSS | Digital Supply Ground. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| K13, K14 | DB<11>−/DB<11>+ | Negative/Positive Data Input Bit 11 (MSB). Conforms to IEEE-1596 reduced range link. |
| L1 | PIN_MODE | 0 = SPI Mode. SPI is enabled.<br>1 = PIN Mode. SPI disabled; direct pin control. |
| L7, L8, M7, M8, N7, N8, P7, P8 | DVDD33 | 3.3 V Digital Supply. |
| L13, L14 | DB<10>−/DB<10>+ | Negative/Positive Data Input Bit 10. Conforms to IEEE-1596 reduced range link. |
| M1, M2 | NC | No Connect. |
| M13, M14 | DB<9>−/DB<9>+ | Negative/Positive Data Input Bit 9. Conforms to IEEE-1596 reduced range link. |
| N1, P1 | NC | No Connect. |
| N2, P2 | DB<0>−/DB<0>+ | Negative/Positive Data Input Bit 0 (LSB). Conforms to IEEE-1596 reduced range link. |
| N3, P3 | DB<1>−/DB<1>+ | Negative/Positive Data Input Bit 1. Conforms to IEEE-1596 reduced range link. |
| N4, P4 | DB<2>−/DB<2>+ | Negative/Positive Data Input Bit 2. Conforms to IEEE-1596 reduced range link. |
| N5, P5 | DB<3>−/DB<3>+ | Negative/Positive Data Input Bit 3. Conforms to IEEE-1596 reduced range link. |
| N6, P6 | DATACLK_OUT−/ DATACLK_OUT+ | Negative/Positive Data Output Clock. Conforms to IEEE-1596 reduced range link. |
| N9, P9 | DATACLK_IN−/ DATACLK_IN+ | Negative/Positive Data Input Clock. Conforms to IEEE-1596 reduced range link. |
| N10, P10 | DB<4>−/DB<4>+ | Negative/Positive Data Input Bit 4. Conforms to IEEE-1596 reduced range link. |
| N11, P11 | DB<5>−/DB<5>+ | Negative/Positive Data Input Bit 5. Conforms to IEEE-1596 reduced range link. |
| N12, P12 | DB<6>−/DB<6>+ | Negative/Positive Data Input Bit 6. Conforms to IEEE-1596 reduced range link. |
| N13, P13 | DB<7>−/DB<7>+ | Negative/Positive Data Input Bit 7. Conforms to IEEE-1596 reduced range link. |
| N14, P14 | DB<8>−/DB<8>+ | Negative/Positive Data Input Bit 8. Conforms to IEEE-1596 reduced range link. |

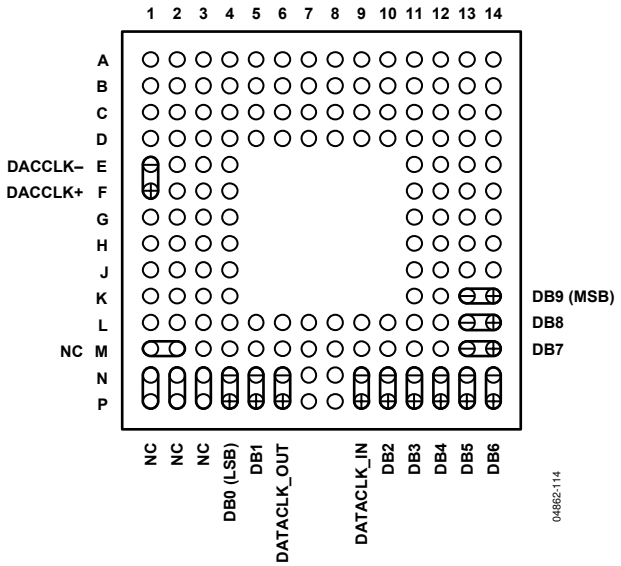


*Figure 4. AD9734 Digital LVDS Input, Clock I/O (Top View)*

**Table 8. AD9734 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| A1, A2, A3, B1, B2, B3, C1, C2, C3, D2, D3 | CVDD18 | 1.8 V Clock Supply. |
| A4, A5, A6, A9, A10, A11, B4, B5, B6, B9, B10, B11, C4, C5, C6, C9, C10, C11, D4, D5, D6, D9, D10, D11 | AVSS | Analog Supply Ground. |
| A7, B7, C7, D7 | IOUTB | DAC Negative Output. 10 mA to 30 mA full-scale output current. |
| A8, B8, C8, D8 | IOUTA | DAC Positive Output. 10 mA to 30 mA full-scale output current. |
| A12, A13, B12, B13, C12, C13, D12, D13 | AVDD33 | 3.3 V Analog Supply. |
| A14 | DNC | Do Not Connect. |
| B14 | I120 | Nominal 1.2 V Reference. Tie to analog ground via 10 kΩ resistor to generate a 120 µA reference current. |
| C14 | VREF | Band Gap Voltage Reference I/O. Tie to analog ground via 1 nF capacitor; output impedance approximately 5 kΩ. |
| D1, E2, E3, E4, F2, F3, F4, G1, G2, G3, G4 | CVSS | Clock Supply Ground. |
| D14 | IPTAT | Factory Test Pin. Output current, proportional to absolute temperature, is approximately 10 µA at 25°C with a slope of approximately 20 nA/°C. |
| E1, F1 | DACCLK–/DACCLK+ | Negative/Positive DAC Clock Input (DACCLK). |
| E11, E12, F11, F12, G11, G12 | AVSS | Analog Supply Ground Shield. Tie to AVSS at the DAC. |
| E13 | IRQ/UNSIGNED | If PIN_MODE = 0, IRQ: Active low open-drain interrupt request output, pull up to DVDD33 with 10 kΩ resistor.<br>If PIN_MODE = 1, UNSIGNED: Digital input pin where 0 = twos complement input data format, 1 = unsigned. |
| E14 | RESET/PD | If PIN_MODE = 0, RESET: 1 resets the AD9734.<br>If PIN_MODE = 1, PD: 1 puts the AD9734 in the power-down state. |
| F13 | CSB/2× | See the Serial Peripheral Interface section and the Pin Mode Operation section for pin description. |
| F14 | SDIO/FIFO | See the Pin Mode Operation section for pin description. |
| G13 | SCLK/FSC0 | See the Pin Mode Operation section for pin description. |
| G14 | SDO/FSC1 | See the Pin Mode Operation section for pin description. |
| H1, H2, H3, H4, H11, H12, H13, H14, J1, J2, J3, J4, J11, J12, J13, J14 | DVDD18 | 1.8 V Digital Supply. |
| K1, K2, K3, K4, K11, K12, L2, L3, L4, L5, L6, L9, L10, L11, L12, M3, M4, M5, M6, M9, M10, M11, M12 | DVSS | Digital Supply Ground. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| K13, K14 | DB<9>−/DB<9>+ | Negative/Positive Data Input Bit 9 (MSB). Conforms to IEEE-1596 reduced range link. |
| L1 | PIN_MODE | 0 = SPI Mode. SPI is enabled.<br>1 = PIN Mode. SPI is disabled; direct pin control. |
| L7, L8, M7, M8, N7, N8, P7, P8 | DVDD33 | 3.3 V Digital Supply. |
| L13, L14 | DB<8>−/DB<8>+ | Negative/Positive Data Input Bit 8. Conforms to IEEE-1596 reduced range link. |
| M1, M2 | NC | No Connect. |
| M13, M14 | DB<7>−/DB<7>+ | Negative/Positive Data Input Bit 7. Conforms to IEEE-1596 reduced range link. |
| N1, P1 | NC | No Connect. |
| N2, P2 | NC | No Connect. |
| N3, P3 | NC | No Connect. |
| N4, P4 | DB<0>−/DB<0>+ | Negative/Positive Data Input Bit 0 (LSB). Conforms to IEEE-1596 reduced range link. |
| N5, P5 | DB<1>−/DB<1>+ | Negative/Positive Data Input Bit 1. Conforms to IEEE-1596 reduced range link. |
| N6, P6 | DATACLK_OUT−/ DATACLK_OUT+ | Negative/Positive Data Output Clock. Conforms to IEEE-1596 reduced range link. |
| N9, P9 | DATACLK_IN−/ DATACLK_IN+ | Negative/Positive Data Input Clock. Conforms to IEEE-1596 reduced range link. |
| N10, P10 | DB<2>−/DB<2>+ | Negative/Positive Data Input Bit 2. Conforms to IEEE-1596 reduced range link. |
| N11, P11 | DB<3>−/DB<3>+ | Negative/Positive Data Input Bit 3. Conforms to IEEE-1596 reduced range link. |
| N12, P12 | DB<4>−/DB<4>+ | Negative/Positive Data Input Bit 4. Conforms to IEEE-1596 reduced range link. |
| N13, P13 | DB<5>−/DB<5>+ | Negative/Positive Data Input Bit 5. Conforms to IEEE-1596 reduced range link. |
| N14, P14 | DB<6>−/DB<6>+ | Negative/Positive Data Input Bit 6. Conforms to IEEE-1596 reduced range link. |

## LOCATION OF SUPPLY AND CONTROL PINS

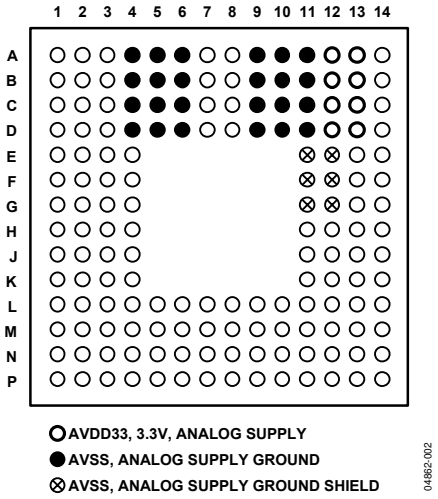


*Figure 5. Analog Supply Pins (Top View)*

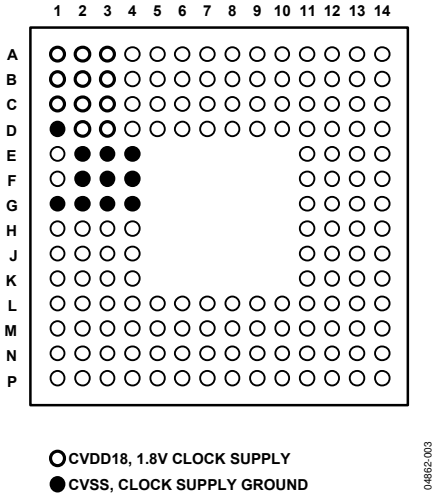


*Figure 6. Clock Supply Pins (Top View)*

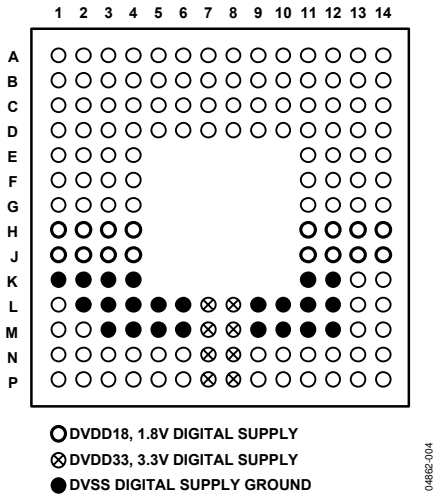


*Figure 7. Digital Supply Pins (Top View)*

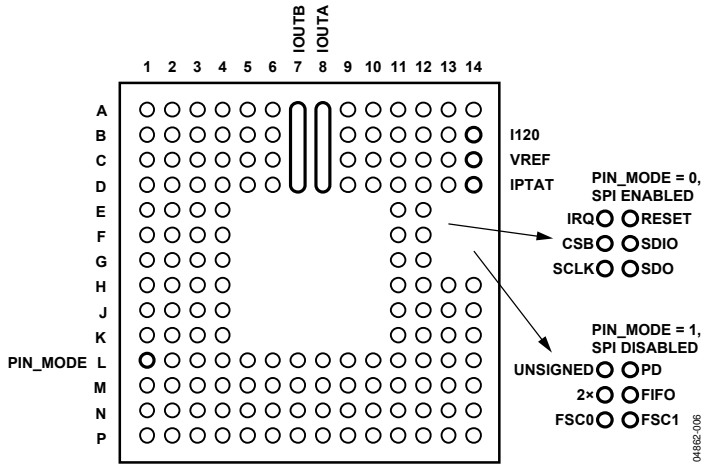


*Figure 8. Analog I/O and SPI Control Pins (Top View)*

# TERMINOLOGY

**Linearity Error (Integral Nonlinearity or INL)**
The maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

**Differential Nonlinearity (DNL)**
The measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

**Monotonicity**
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

**Offset Error**
The deviation of the output current from the ideal of zero. For IOUTA, 0 mA output is expected when the inputs are all 0s. For IOUTB, 0 mA output is expected when all inputs are set to 1s.

**Gain Error**
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

**Output Compliance Range**
The range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

**Temperature Drift**
Specified as the maximum change from the ambient (25°C) value to the value at either $T_{MIN}$ or $T_{MAX}$. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

**Power Supply Rejection**
The maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

**Settling Time**
The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

**Glitch Impulse**
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s.

**Spurious-Free Dynamic Range**
The difference, in dB, between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

**Total Harmonic Distortion (THD)**
The ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal. It is expressed as a percentage or in decibels (dB).

**Multitone Power Ratio**
The spurious-free dynamic range containing multiple carrier tones of equal amplitude. It is measured as the difference between the rms amplitude of a carrier tone to the peak spurious signal in the region of a removed tone.

# TYPICAL PERFORMANCE CHARACTERISTICS

## AD9736 STATIC LINEARITY, 10 mA FULL SCALE

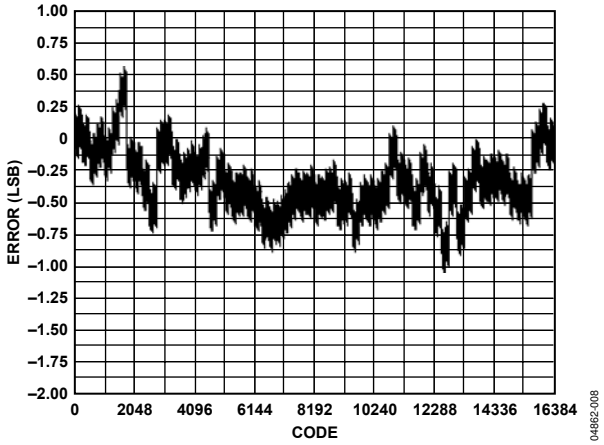


Figure 9. AD9736 INL, –40°C, 10 mA FS

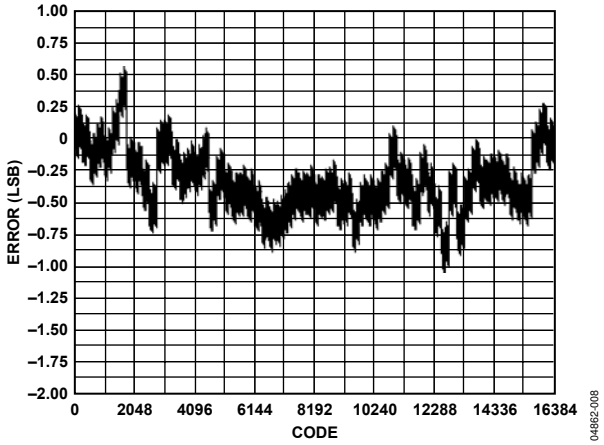


Figure 10. AD9736 INL, 25°C, 10 mA FS

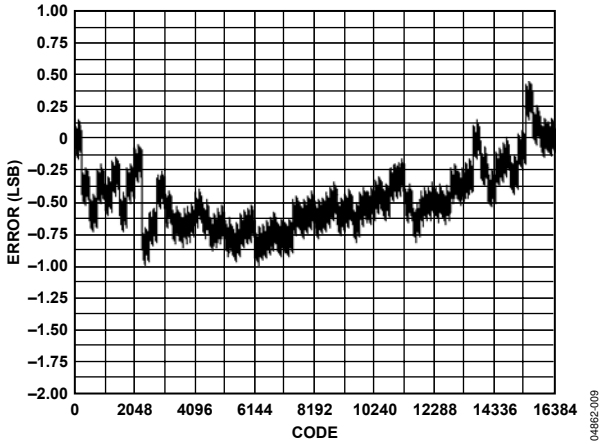


Figure 11. AD9736 INL, 85°C, 10 mA FS

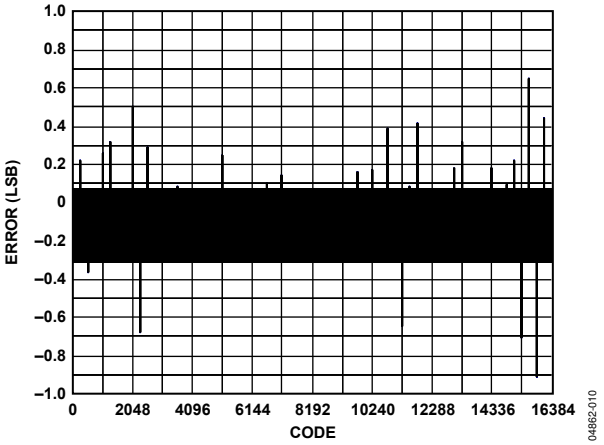


Figure 12. AD9736 DNL, –40°C, 10 mA FS

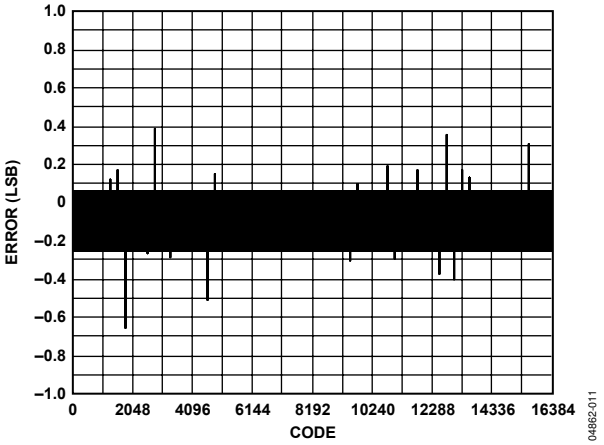


Figure 13. AD9736 DNL, 25°C, 10 mA FS

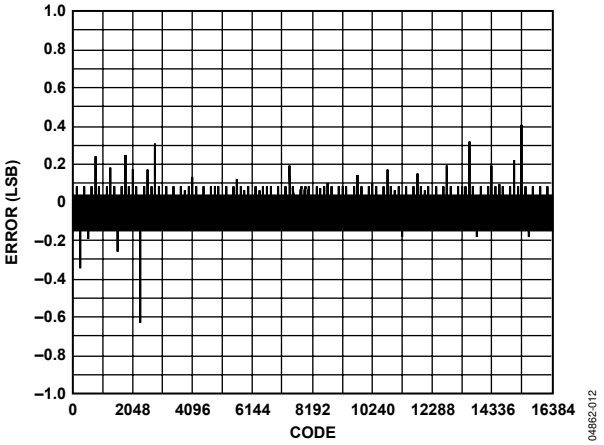


Figure 14. AD9736 DNL, 85°C, 10 mA FS

## AD9736 STATIC LINEARITY, 20 mA FULL SCALE

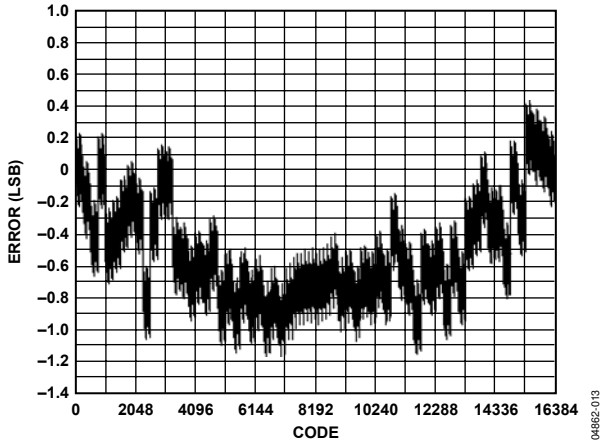


Figure 15. AD9736 INL, −40°C, 20 mA FS

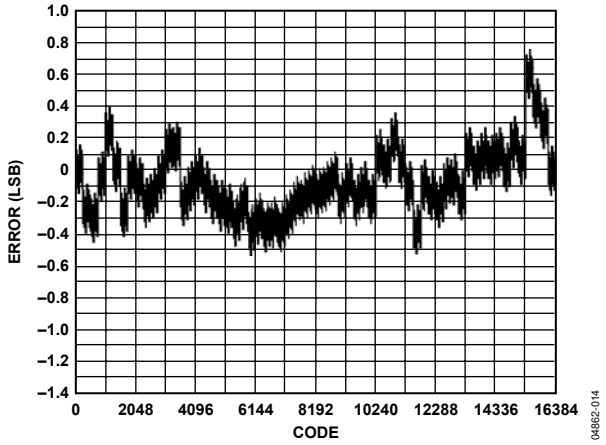


Figure 16. AD9736 INL, 25°C, 20 mA FS

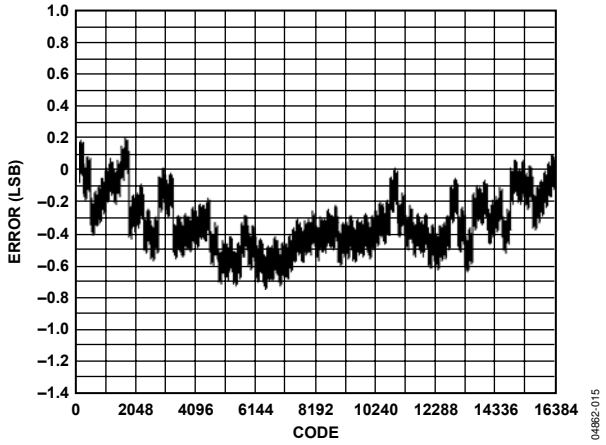


Figure 17. AD9736 INL, 85°C, 20 mA FS

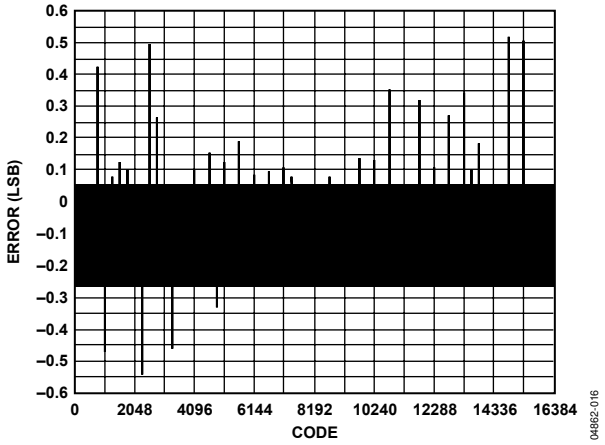


Figure 18. AD9736 DNL, −40°C, 20 mA FS

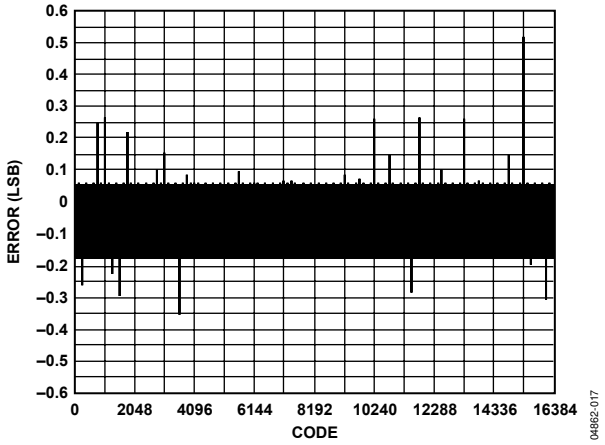


Figure 19. AD9736 DNL, 25°C, 20 mA FS

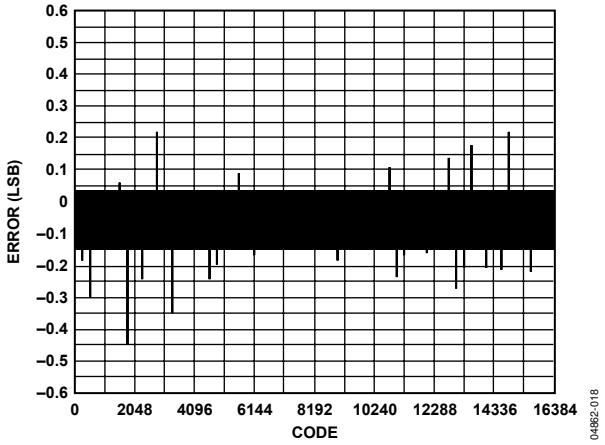


Figure 20. AD9736 DNL, 85°C, 20 mA FS

## AD9736 STATIC LINEARITY, 30 mA FULL SCALE

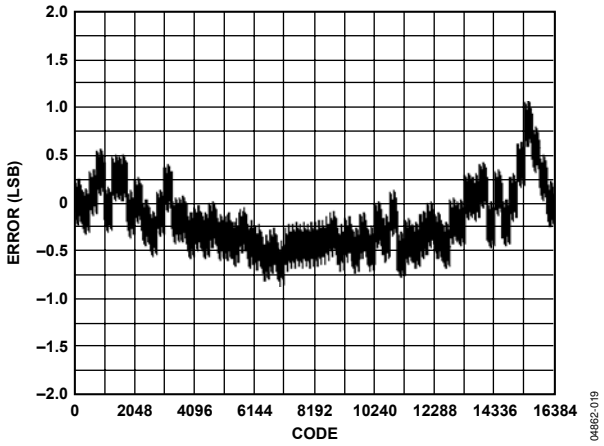


Figure 21. AD9736 INL, −40°C, 30 mA FS

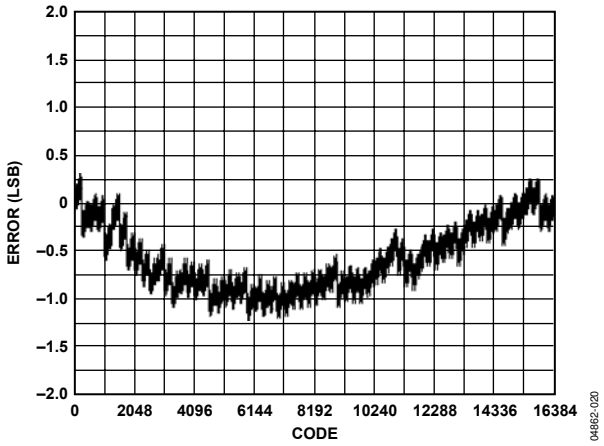


Figure 22. AD9736 INL, 25°C, 30 mA FS

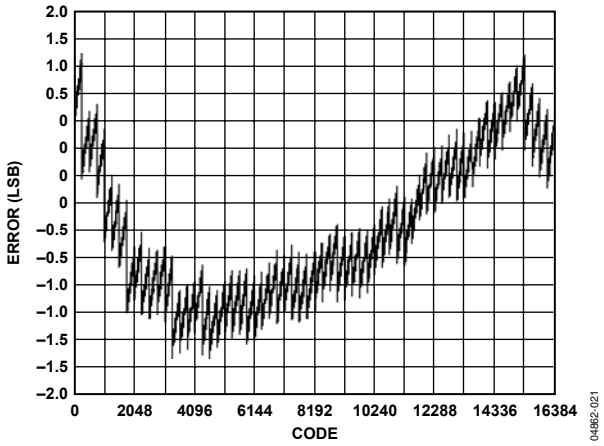


Figure 23. AD9736 INL, 85°C, 30 mA FS

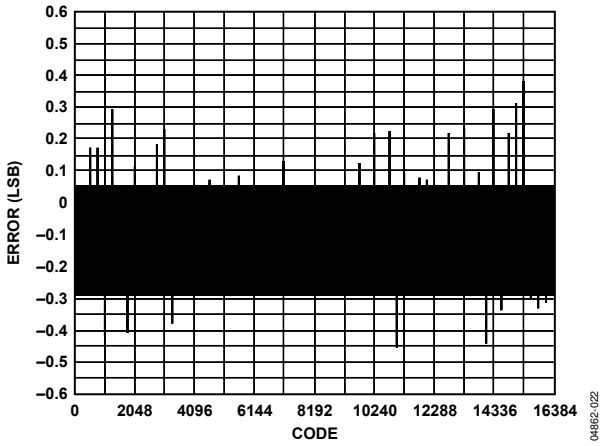


Figure 24. AD9736 DNL, −40°C, 30 mA FS

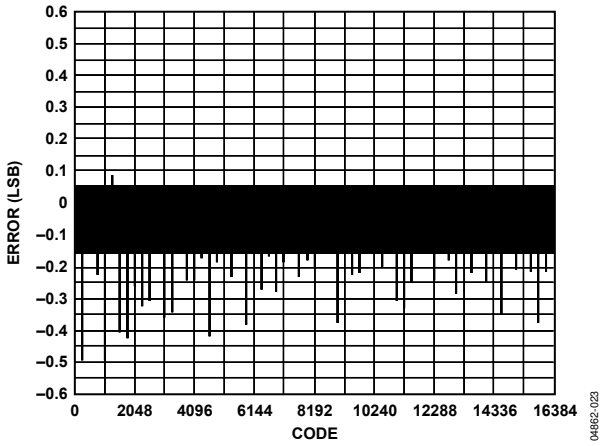


Figure 25. AD9736 DNL, 25°C, 30 mA FS

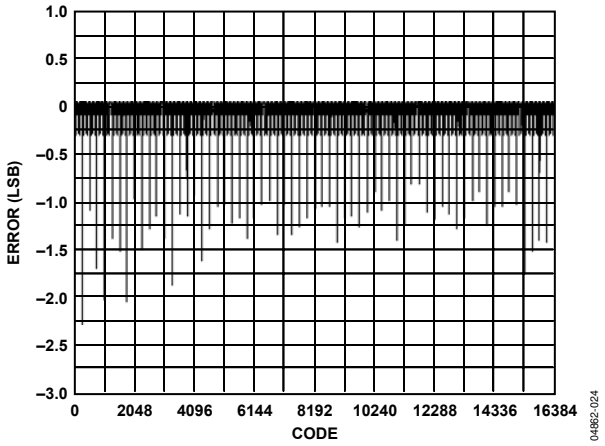


Figure 26. AD9736 DNL, 85°C, 30 mA FS

## AD9735 STATIC LINEARITY, 10 mA, 20 mA, 30 mA FULL SCALE

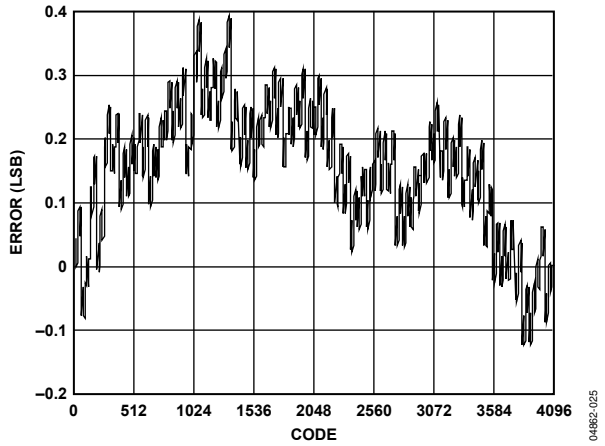


Figure 27. AD9735 INL, 25°C, 10 mA FS

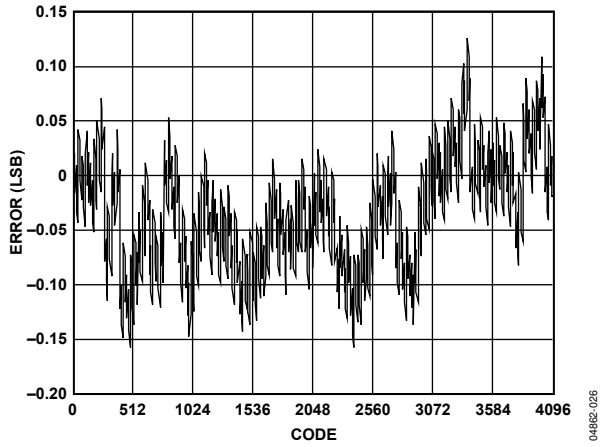


Figure 28. AD9735 INL, 25°C, 20 mA FS

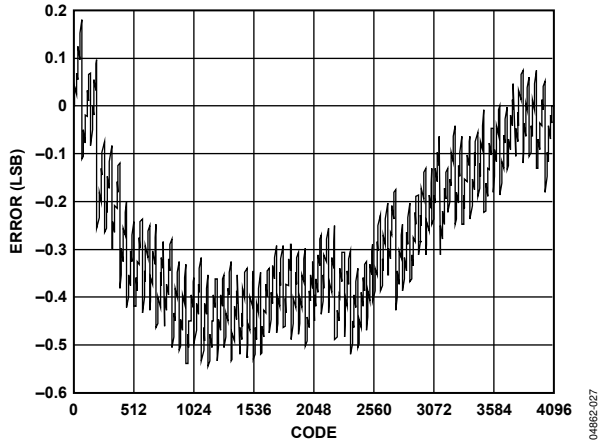


Figure 29. AD9735 INL, 25°C, 30 mA FS

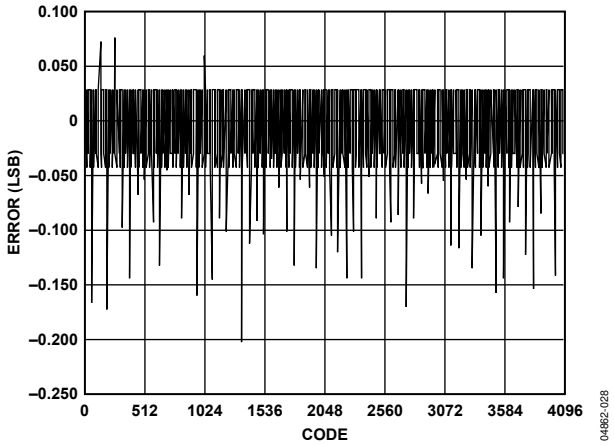


Figure 30. AD9735 DNL, 25°C, 10 mA FS

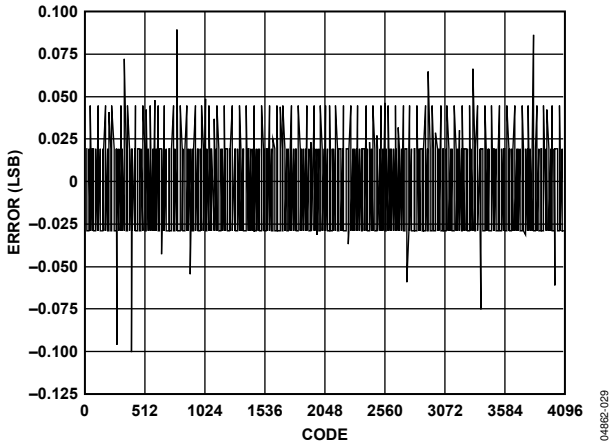


Figure 31. AD9735 DNL, 25°C, 20 mA FS

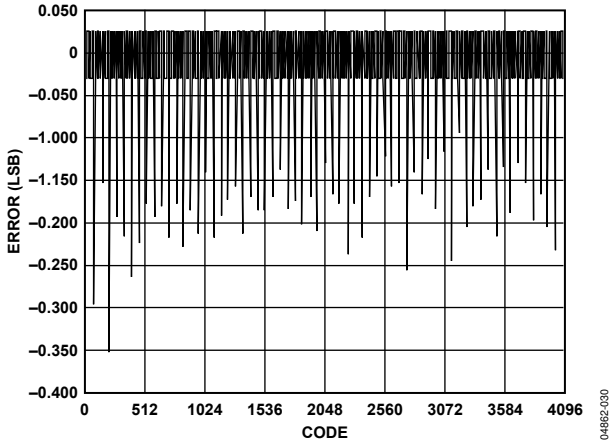


Figure 32. AD9735 DNL, 25°C, 30 mA FS

## AD9734 STATIC LINEARITY, 10 mA, 20 mA, 30 mA FULL SCALE

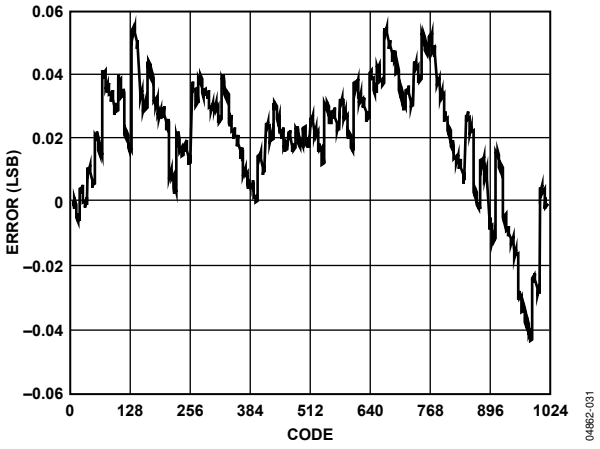


Figure 33. AD9734 INL, 25°C, 10 mA FS

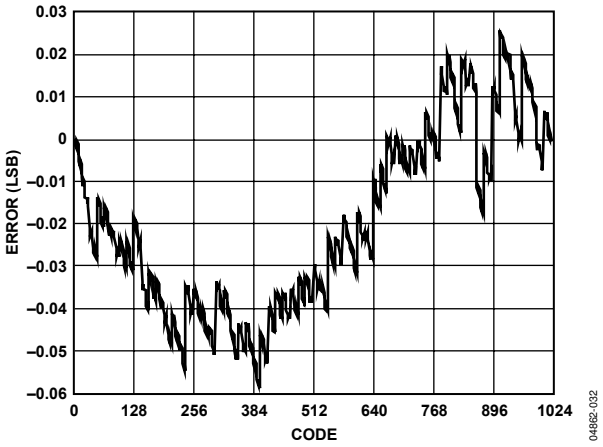


Figure 34. AD9734 INL, 25°C, 20 mA FS

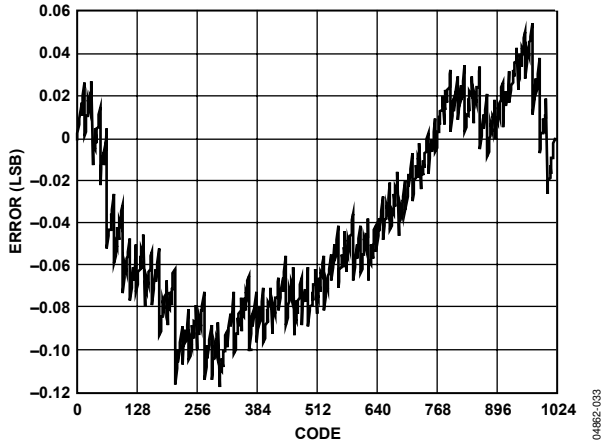


Figure 35. AD9734 INL, 25°C, 30 mA FS

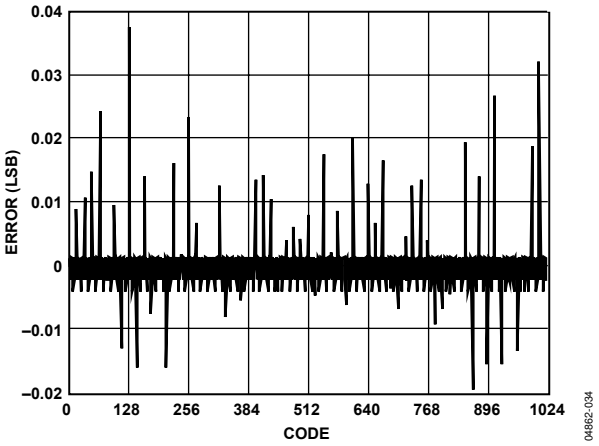


Figure 36. AD9734 DNL, 25°C, 10 mA FS

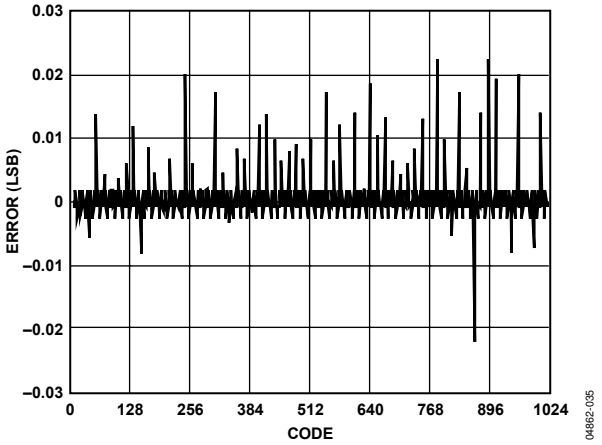


Figure 37. AD9734 DNL, 25°C, 20 mA FS

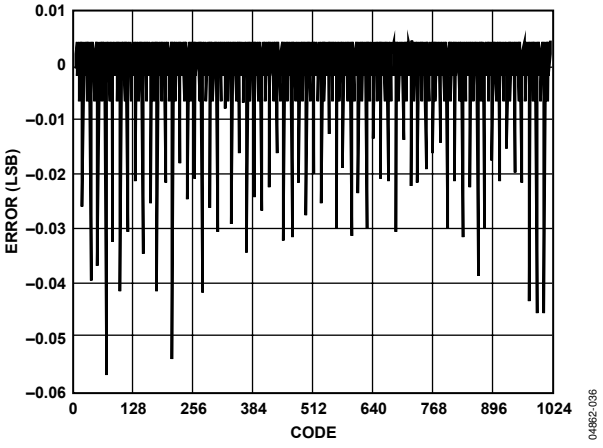


Figure 38. AD9734 DNL, 25°C, 30 mA FS

## AD9736 POWER CONSUMPTION, 20 mA FULL SCALE

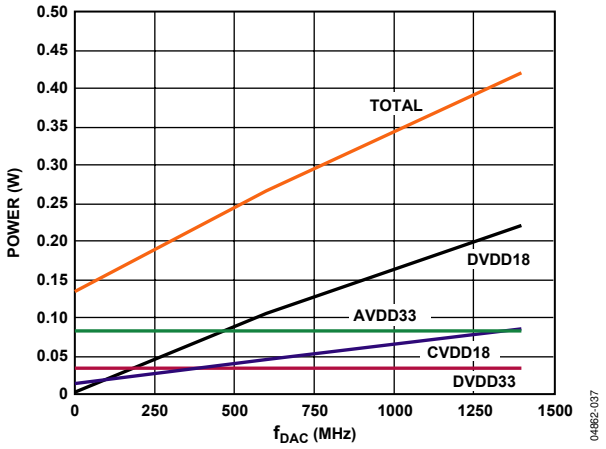


Figure 39. AD9736 1× Mode Power vs. $f_{DAC}$ at 25°C

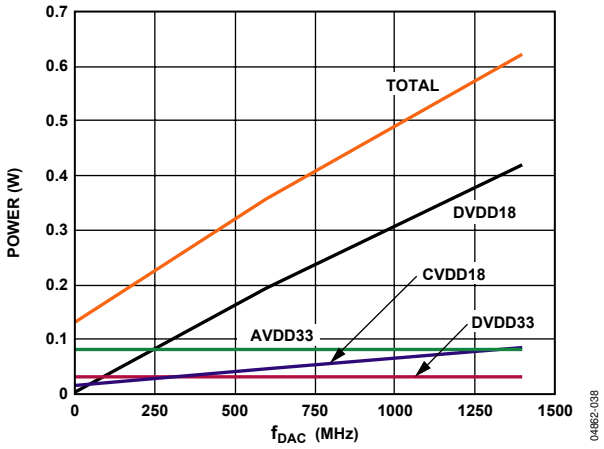


Figure 40. AD9736, 2× Interpolation Mode Power vs. $f_{DAC}$ at 25°C

## AD9736 DYNAMIC PERFORMANCE, 20 mA FULL SCALE

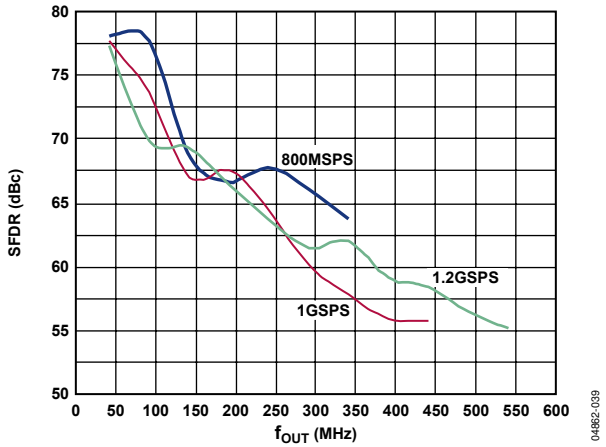


Figure 41. AD9736 SFDR vs. $f_{OUT}$ over $f_{DAC}$ at 25°C

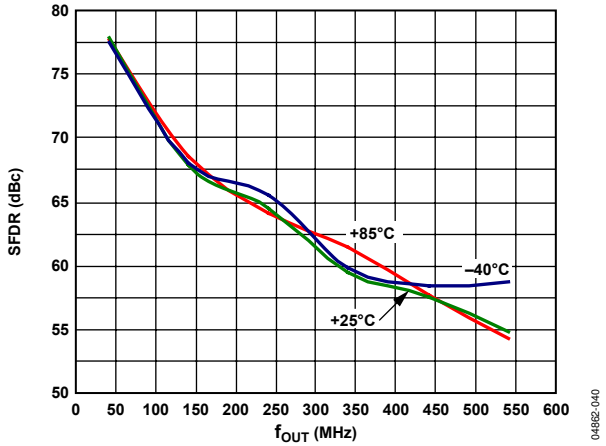


Figure 42. AD9736 SFDR vs. $f_{OUT}$ over Temperature

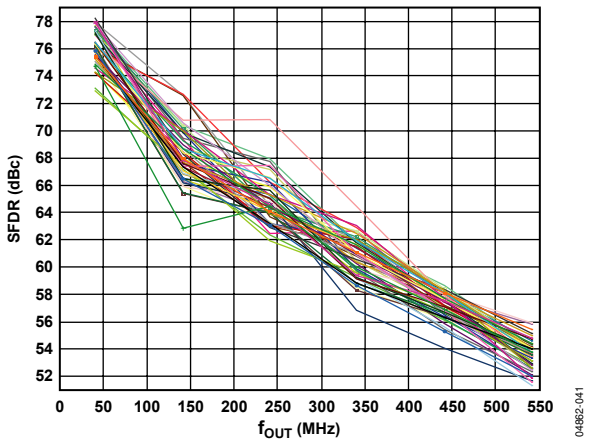


Figure 43. AD9736 SFDR vs. $f_{OUT}$ over 50 Parts, 25°C, 1.2 GSPS

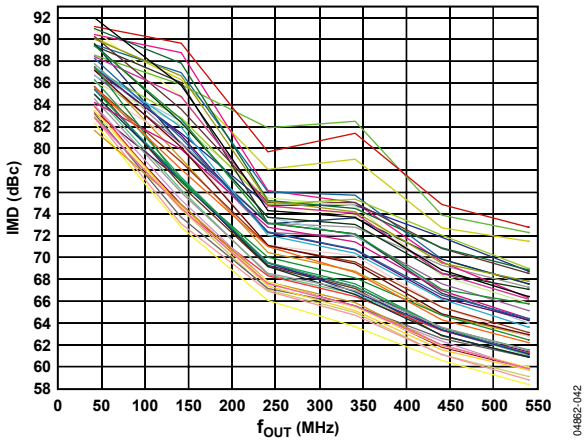


Figure 44. AD9736 IMD vs. $f_{OUT}$ over 50 Parts, 25°C, 1.2 GSPS

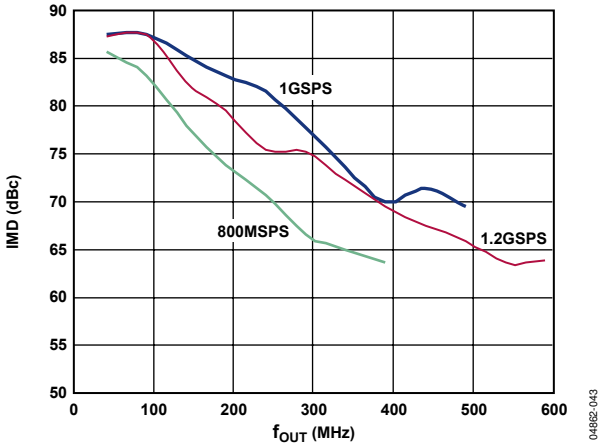


Figure 45. AD9736 IMD vs. $f_{OUT}$ over $f_{DAC}$ at 25°C

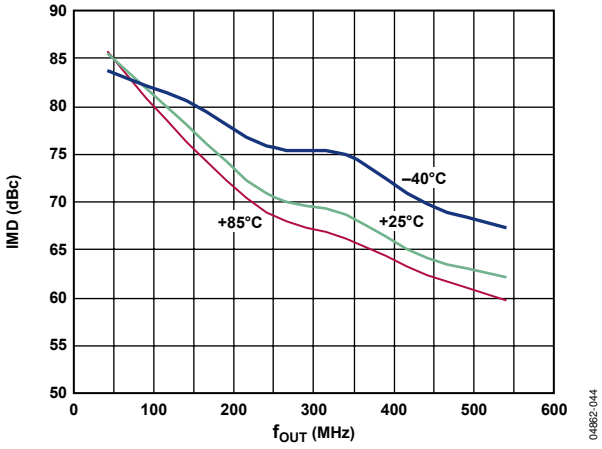


Figure 46. AD9736 IMD vs. $f_{OUT}$ over Temperature, 1.2 GSPS

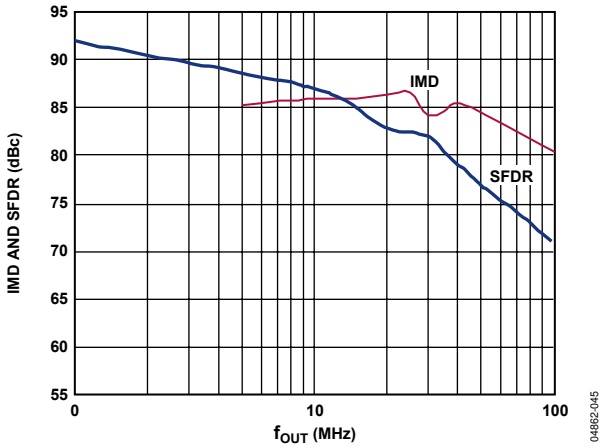


Figure 47. AD9736 Low Frequency IMD and SFDR vs. $f_{OUT}$, 25°C, 1.2 GSPS

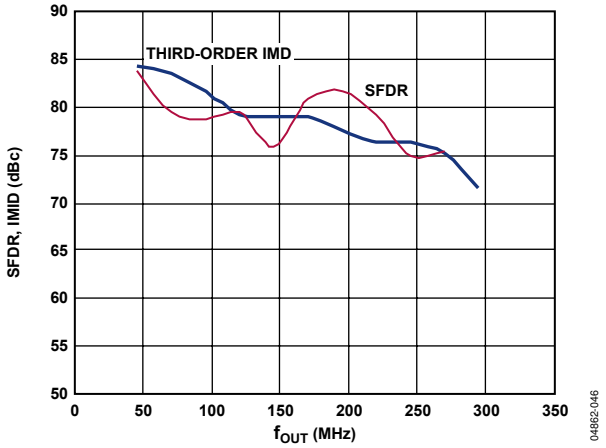


Figure 48. AD9736 IMD and SFDR vs. $f_{OUT}$, 25°C, 1.2 GSPS, 2× Interpolation

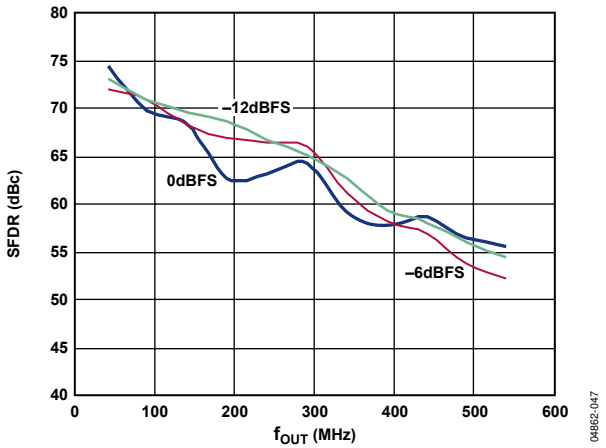


Figure 49. AD9736 SFDR vs. $f_{OUT}$ over $A_{OUT}$, 25°C, 1.2 GSPS

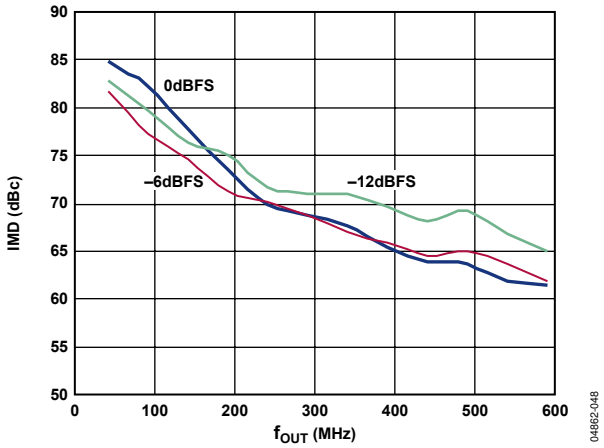


Figure 50. AD9736 IMD vs. $f_{OUT}$ over $A_{OUT}$, 25°C, 1.2 GSPS

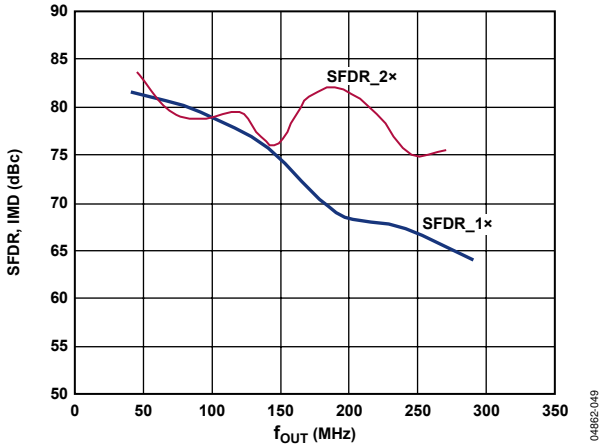


Figure 51. AD9736 SFDR vs. $f_{OUT}$, 25°C, 1.2 GSPS, 1× and 2× Interpolation

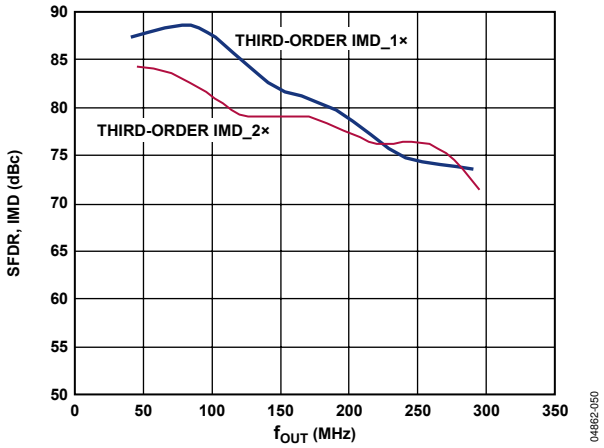


Figure 52. AD9736 IMD vs. $f_{OUT}$, 25°C, 1.2 GSPS, 1× and 2× Interpolation