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11-/14-Bit, 2.5 GSPS, RF Digital-to-Analog Converters

Data Sheet

AD9737A/AD9739A

FEATURES

- Direct RF synthesis at 2.5 GSPS update rate
  - DC to 1.25 GHz in baseband mode
  - 1.25 GHz to 3.0 GHz in mix-mode
- Industry leading single/multicarrier IF or RF synthesis
- Dual-port LVDS data interface
  - Up to 1.25 GSPS operation
  - Source synchronous DDR clocking
- Pin compatible with the AD9739
- Programmable output current: 8.7 mA to 31.7 mA
- Low power: 1.1 W at 2.5 GSPS

APPLICATIONS

- Broadband communications systems
  - DOCSIS CMTS systems
- Military jammers
- Instrumentation, automatic test equipment
- Radar, avionics

FUNCTIONAL BLOCK DIAGRAM

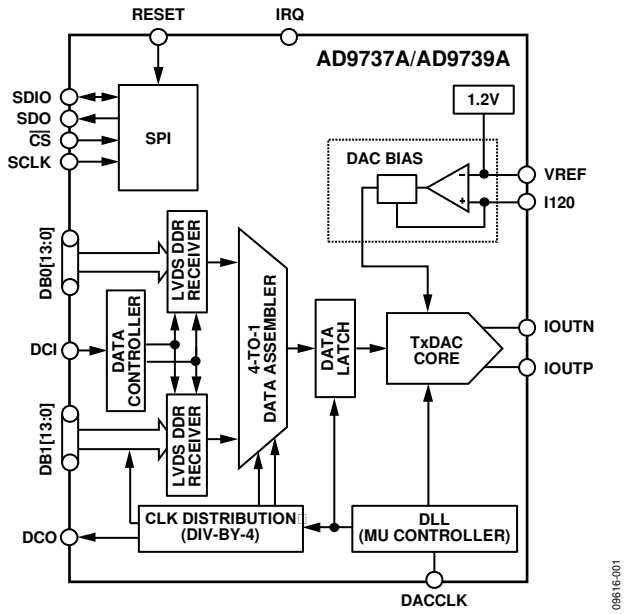

Figure 1.

GENERAL DESCRIPTION

The AD9737A/AD9739A are 11-bit and 14-bit, 2.5 GSPS high performance RF DACs that are capable of synthesizing wideband signals from dc up to 3 GHz. The AD9737A/AD9739A are pin and functionally compatible with the AD9739 with the exception that the AD9737A/AD9739A do not support synchronization or RZ mode, and are specified to operate between 1.6 GSPS and 2.5 GSPS.

By elimination of the synchronization circuitry, some nonideal artifacts such as images and discrete clock spurs remain stationary on the AD9737A/AD9739A between power-up cycles, thus allowing for possible system calibration. AC linearity and noise performance remain the same between the AD9739 and the AD9737A/AD9739A.

The inclusion of on-chip controllers simplifies system integration. A dual-port, source synchronous, LVDS interface simplifies the digital interface with existing FGPA/ASIC technology. On-chip controllers are used to manage external and internal clock domain variations over temperature to ensure reliable data transfer from the host to the DAC core. A serial peripheral interface (SPI) is used for device configuration as well as readback of status registers.

The AD9737A/AD9739A are manufactured on a 0.18 µm CMOS process and operate from 1.8 V and 3.3 V supplies. They are supplied in a 160-ball chip scale ball grid array for reduced package parasitics.

PRODUCT HIGHLIGHTS

1. Ability to synthesize high quality wideband signals with bandwidths of up to 1.25 GHz in the first or second Nyquist zone.
2. A proprietary quad-switch DAC architecture provides exceptional ac linearity performance while enabling mix-mode operation.
3. A dual-port, double data rate, LVDS interface supports the maximum conversion rate of 2500 MSPS.
4. On-chip controllers manage external and internal clock domain skews.
5. Programmable differential current output with an 8.66 mA to 31.66 mA range.

Rev. C

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Reorganized Layout ..... Universal
Moved Revision History Section 3
Deleted ±6% from Table Summary Statement; Changes to Table 1 4
Deleted ±6% from Table Summary Statement, Table 2 5
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Added Figure 7 and Table 7, Renumbered Sequentially 10
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Added Interrupt Request (IRQ) Enable/Status Section, TxDAC Full-Scale Current Setting (I_{OUTFS}) and Sleep Section, TxDAC Quad-Switch Mode of Operation Section, DCI Phase Alignment Status Section, Data Receiver Controller Configuration Section, and Table 14 to Table 18 44
Added Data Receiver Controller_Data Sample Delay Value Section, Data Receiver Controller_DCI Delay Value/Window and Phase Rotation Section, Data Receiver Controller_Delay Line Status Section, Data Receiver Controller Lock/Tracking Status Section, and Table 19 to Table 22 45
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7/11—Rev. 0 to Rev. A

Changed Maximum Update Rate (DACCLK Input) Parameter to DAC Clock Rate Parameter in Table 4 6
Added Adjusted DAC Update Rate Parameter and Endnote 1 in Table 4 6
Updated Outline Dimensions 43

1/11—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

VDDA = VDD33 = 3.3 V, VDDC = VDD = 1.8 V, I_{OUTFS} = 20 mA.

Table 1.

	AD9737A			AD9739A			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		11			14		Bits
ACCURACY							
Integral Nonlinearity (INL)		±0.5			±2.5		LSB
Differential Nonlinearity (DNL)		±0.5			±2.0		LSB
ANALOG OUTPUTS							
Gain Error (with Internal Reference)		5.5			5.5		%
Full-Scale Output Current	8.66	20.2	31.66	8.66	20.2	31.66	mA
Output Compliance Range	−1.0		+1.0	−1.0		+1.0	V
Common-Mode Output Resistance		10			10		MΩ
Differential Output Resistance		70			70		Ω
Output Capacitance		1			1		pF
DAC CLOCK INPUT (DACCLK_P, DACCLK_N)							
Differential Peak-to-Peak Voltage	1.2	1.6	2.0	1.2	1.6	2.0	V
Common-Mode Voltage		900			900		mV
Clock Rate	1.6		2.5	1.6		2.5	GHz
TEMPERATURE DRIFT							
Gain		60			60		ppm/°C
Reference Voltage		20			20		ppm/°C
REFERENCE							
Internal Reference Voltage	1.15	1.2	1.25	1.15	1.2	1.25	V
Output Resistance		5			5		kΩ
ANALOG SUPPLY VOLTAGES							
VDDA	3.1	3.3	3.5	3.1	3.3	3.5	V
VDDC	1.70	1.8	1.90	1.70	1.8	1.90	V
DIGITAL SUPPLY VOLTAGES							
VDD33	3.10	3.3	3.5	3.10	3.3	3.5	V
VDD	1.70	1.8	1.90	1.70	1.8	1.90	V
SUPPLY CURRENTS AND POWER DISSIPATION, 2.0 GSPS							
I_{VDDA}		37	38		37	38	mA
I_{VDDC}		158	167		158	167	mA
I_{VDD33}		14.5	16		14.5	16	mA
I_{VDD}		173	183		173	183	mA
Power Dissipation		0.770			0.770		W
Sleep Mode, I_{VDDA}		2.5	2.75		2.5	2.75	mA
Power-Down Mode (All Power-Down Bits Set in Register 0x01 and Register 0x02)							
I_{VDDA}		0.02			0.02		mA
I_{VDDC}		6			6		mA
I_{VDD33}		0.6			0.6		mA
I_{VDD}		0.1			0.1		mA
SUPPLY CURRENTS AND POWER DISSIPATION, 2.5 GSPS							
I_{VDDC}		223			223		mA
I_{VDD33}		14.5			14.5		mA
I_{VDD}		215			215		mA
Power Dissipation		0.960			0.960		mW

LVDS DIGITAL SPECIFICATIONS

VDDA = VDD33 = 3.3 V, VDDC = VDD = 1.8 V, I_{OUTFS} = 20 mA. LVDS drivers and receivers are compliant to the IEEE Standard 1596.3-1996 reduced range link, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
LVDS DATA INPUTS (DB0[13:0], DB1[13:0])[1]				
Input Common-Mode Voltage Range, V_{COM}	825		1575	mV
Logic High Differential Input Threshold, V_{IH_DTH}	175	400		mV
Logic Low Differential Input Threshold, V_{IL_DTH}	−175	−400		mV
Receiver Differential Input Impedance, R_{IN}	80		120	Ω
Input Capacitance		1.2		pF
LVDS Input Rate	1250			MSPS
LVDS Minimum Data Valid Period (t_{MDE}) (See Figure 159)			344	ps
LVDS CLOCK INPUT (DCI)[2]				
Input Common-Mode Voltage Range, V_{COM}	825		1575	mV
Logic High Differential Input Threshold, V_{IH_DTH}	175	400		mV
Logic Low Differential Input Threshold, V_{IL_DTH}	−175	−400		mV
Receiver Differential Input Impedance, R_{IN}	80		120	Ω
Input Capacitance		1.2		pF
Maximum Clock Rate	625			MHz
LVDS CLOCK OUTPUT (DCO)[3]				
Output Voltage High (DCO_P or DCO_N)			1375	mV
Output Voltage Low (DCO_P or DCO_N)	1025			mV
Output Differential Voltage, $\|V_{OD}\|$	150	200	250	mV
Output Offset Voltage, V_{OS}	1150		1250	mV
Output Impedance, Single-Ended, R_O	80	100	120	Ω
R_O Single-Ended Mismatch			10	%
Maximum Clock Rate	625			MHz

[1] DB0[x]P, DB0[x]N, DB1[x]P, and DB1[x]N pins.
[2] DCI_P and DCI_N pins.
[3] DCO_P and DCO_N pins with 100 Ω differential termination.

SERIAL PORT SPECIFICATIONS

VDDA = VDD33 = 3.3 V, VDDC = VDD = 1.8 V.

Table 3.

Parameter	Min	Typ	Max	Unit
WRITE OPERATION (See Figure 154)				
SCLK Clock Rate, f_{SCLK}, $1/t_{SCLK}$			20	MHz
SCLK Clock High, t_{HIGH}	18			ns
SCLK Clock Low, t_{LOW}	18			ns
SDIO to SCLK Setup Time, t_{DS}	2			ns
SCLK to SDIO Hold Time, t_{DH}	1			ns
$\overline{CS}$ to SCLK Setup Time, t_S	3			ns
SCLK to $\overline{CS}$ Hold Time, t_H	2			ns
READ OPERATION (See Figure 155 and Figure 156)				
SCLK Clock Rate, f_{SCLK}, $1/t_{SCLK}$			20	MHz
SCLK Clock High, t_{HIGH}	18			ns
SCLK Clock Low, t_{LOW}	18			ns
SDIO to SCLK Setup Time, t_{DS}	2			ns
SCLK to SDIO Hold Time, t_{DH}	1			ns
$\overline{CS}$ to SCLK Setup Time, t_S	3			ns
SCLK to SDIO (or SDO) Data Valid Time, t_{DV}			15	ns
$\overline{CS}$ to SDIO (or SDO) Output Valid to High-Z, t_{EZ}		2		ns
INPUTS (SDI, SDIO, SCLK, $\overline{CS}$)				
Voltage in High, V_{IH}	2.0	3.3		V
Voltage in Low, V_{IL}		0	0.8	V
Current in High, I_{IH}	−10		+10	µA
Current in Low, I_{IL}	−10		+10	µA
OUTPUT (SDIO)				
Voltage Out High, V_{OH}	2.4		3.5	V
Voltage Out Low, V_{OL}	0		0.4	V
Current Out High, I_{OH}		4		mA
Current Out Low, I_{OL}		4		mA

AC SPECIFICATIONS

VDDA = VDD33 = 3.3 V, VDDC = VDD = 1.8 V, I_{OUTFS} = 20 mA, f_{DAC} = 2400 MSPS, unless otherwise noted.

Table 4.

	AD9737A			AD9739A			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC PERFORMANCE							
DAC Clock Rate	1600		2500	1600		2500	MSPS
Adjusted DAC Update Rate[1]	1600		2500	1600		2500	MSPS
Output Settling Time to 0.1%		13			13		ns
SPURIOUS-FREE DYNAMIC RANGE (SFDR)							
f_{OUT} = 100 MHz		70			70		dBc
f_{OUT} = 350 MHz		65			65		dBc
f_{OUT} = 550 MHz		58			58		dBc
f_{OUT} = 950 MHz		55			55		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD), $f_{OUT2} = f_{OUT1} + 1.25$ MHz							
f_{OUT} = 100 MHz		94			94		dBc
f_{OUT} = 350 MHz		78			78		dBc
f_{OUT} = 550 MHz		72			72		dBc
f_{OUT} = 950 MHz		68			68		dBc
NOISE SPECTRAL DENSITY (NSD), 0 dBFS SINGLE TONE							
f_{OUT} = 100 MHz		−162			−167		dBm/Hz
f_{OUT} = 350 MHz		−162			−166		dBm/Hz
f_{OUT} = 550 MHz		−161			−164		dBm/Hz
f_{OUT} = 850 MHz		−161			−163		dBm/Hz
WCDMA ACLR (SINGLE CARRIER), ADJACENT/ALTERNATE ADJACENT CHANNEL							
f_{DAC} = 2457.6 MSPS, f_{OUT} = 350 MHz		80/81			80/80		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 950 MHz		75/75			78/79		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 1700 MHz (Mix-Mode)		69/71			74/74		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 2100 MHz (Mix-Mode)		66/67			69/72		dBc

[1] Adjusted DAC updated rate is calculated as f_{DAC} divided by the minimum required interpolation factor. For the AD9737A/AD9739A, the minimum interpolation factor is 1. Thus, with f_{DAC} = 2500 MSPS, f_{DAC}, adjusted, = 2500 MSPS.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
VDDA to VSSA	−0.3 V to +3.6 V
VDD33 to VSS	−0.3 V to +3.6 V
VDD to VSS	−0.3 V to +1.98 V
VDDC to VSSC	−0.3 V to +1.98 V
VSSA to VSS	−0.3 V to +0.3 V
VSSA to VSSC	−0.3 V to +0.3 V
VSS to VSSC	−0.3 V to +0.3 V
DACCLK_P, DACCLK_N to VSSC	−0.3 V to VDDC + 0.18 V
DCI, DCO to VSS	−0.3 V to VDD33 + 0.3 V
LVDS Data Inputs to VSS	−0.3 V to VDD33 + 0.3 V
IOUTP, IOUTN to VSSA	−1.0 V to VDDA + 0.3 V
I120, VREF to VSSA	−0.3 V to VDDA + 0.3 V
IRQ, $\overline{CS}$, SCLK, SDO, SDIO, RESET to VSS	−0.3 V to VDD33 + 0.3 V
Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
160-Ball CSP_BGA	31.2	7.0	°C/W[1]

[1] With no airflow movement.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

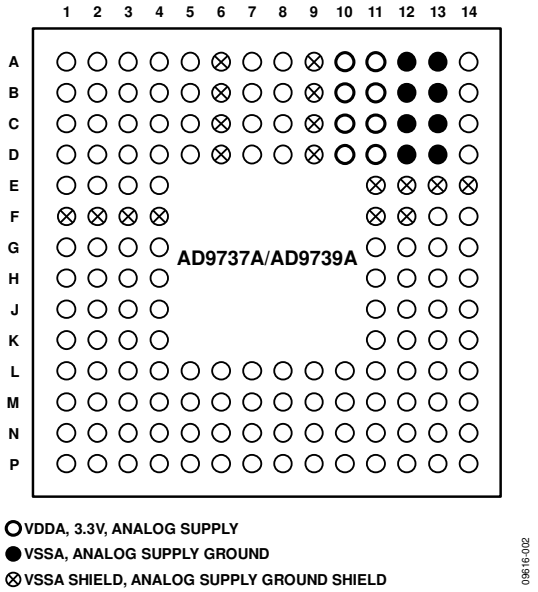

Figure 2. Analog Supply Pins (Top View)

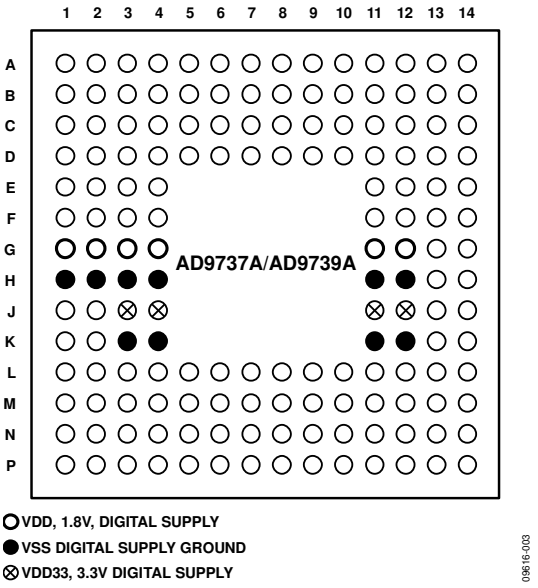

Figure 3. Digital Supply Pins (Top View)

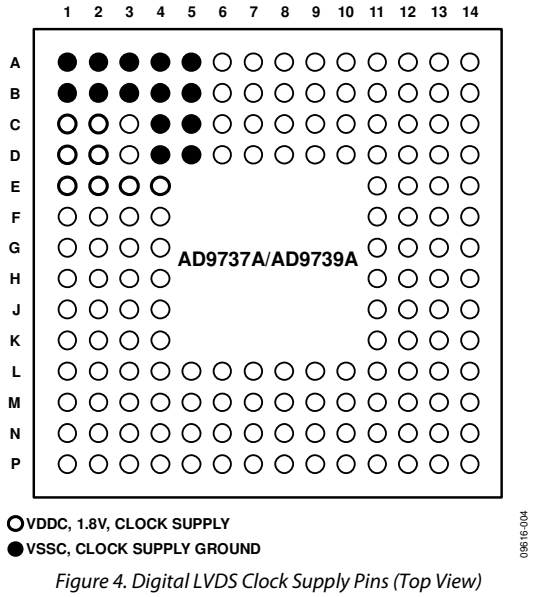

Figure 4. Digital LVDS Clock Supply Pins (Top View)

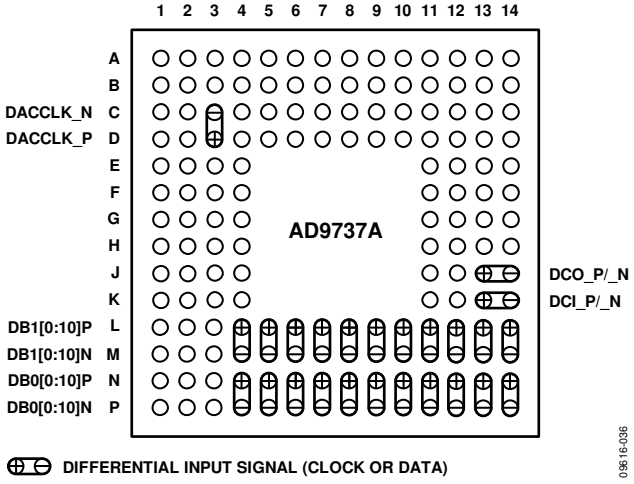

Figure 5. AD9737A Digital LVDS Input, Clock I/O (Top View)

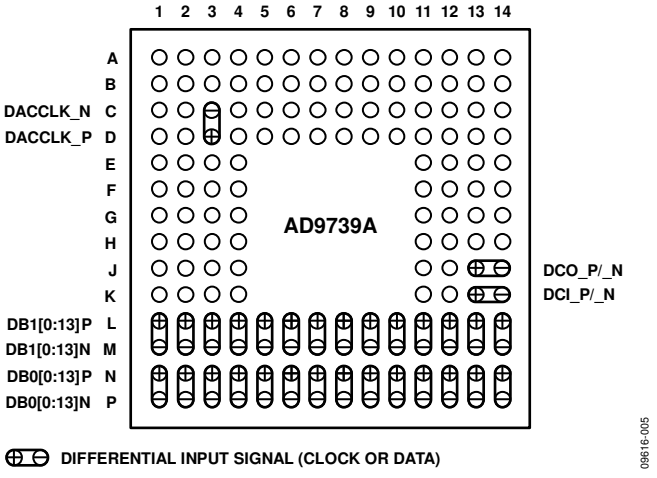

Figure 6. AD9739A Digital LVDS Input, Clock I/O (Top View)

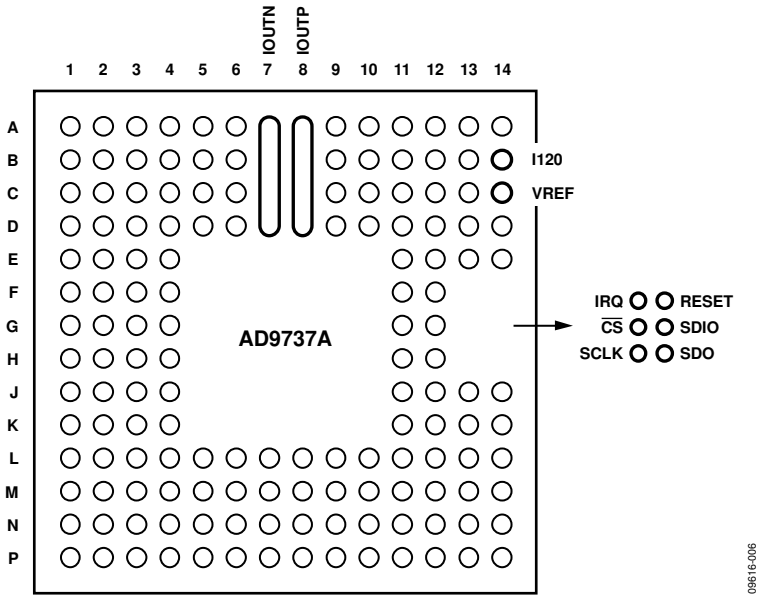

Figure 7. AD9737A Analog I/O and SPI Control Pins (Top View)

Table 7. AD9737A Pin Function Descriptions

Pin No.	Mnemonic	Description
C1, C2, D1, D2, E1, E2, E3, E4	VDDC	1.8 V Clock Supply Input.
A1, A2, A3, A4, A5, B1, B2, B3, B4, B5, C4, C5, D4, D5	VSSC	Clock Supply Ground.
A10, A11, B10, B11, C10, C11, D10, D11	VDDA	3.3 V Analog Supply Input.
A12, A13, B12, B13, C12, C13, D12, D13,	VSSA	Analog Supply Ground.
A6, A9, B6, B9, C6, C9, D6, D9, E11, E12, E13, E14, F1, F2, F3, F4, F11, F12	VSSA Shield	Analog Supply Ground Shield. Tie to VSSA at the DAC.
A14	NC	Do not connect to this pin.
A7, B7, C7, D7	IOUTN	DAC Negative Current Output Source.
A8, B8, C8, D8	IOUTP	DAC Positive Current Output Source.
B14	I120	Nominal 1.2 V Reference. Tie to analog ground via a 10 kΩ resistor to generate a 120 µA reference current.
C14	VREF	Voltage Reference Input/Output. Decouple to VSSA with a 1 nF capacitor.
D14	NC	Factory Test Pin. Do not connect to this pin.
C3, D3	DACCLK_N/DACCLK_P	Negative/Positive DAC Clock Input (DACCLK).
F13	IRQ	Interrupt Request Open Drain Output. Active high. Pull up to VDD33 with a 10 kΩ resistor.
F14	RESET	Reset Input. Active high. Tie to VSS if unused.
G13	$\overline{CS}$	Serial Port Enable Input.
G14	SDIO	Serial Port Data Input/Output.
H13	SCLK	Serial Port Clock Input.
H14	SDO	Serial Port Data Output.
J3, J4, J11, J12	VDD33	3.3 V Digital Supply Input.
G1, G2, G3, G4, G11, G12	VDD	1.8 V Digital Supply Input.
H1, H2, H3, H4, H11, H12, K3, K4, K11, K12	VSS	Digital Supply Ground.
J1, J2	NC	Differential resistor of 200 Ω exists between J1 and J2. Do not connect to this pin.
K1, K2	NC	Differential resistor of 100 Ω exists between K1 and K2. Do not connect to this pin.
J13, J14	DCO_P/DCO_N	Positive/Negative Data Clock Output (DCO).
K13, K14	DCI_P/DCI_N	Positive/Negative Data Clock Input (DCI).

Pin No.	Mnemonic	Description
L1, M1	NC, NC	Do not connect to this pin.
L2, M2	NC, NC	Do not connect to this pin.
L3, M3	NC, NC	Do not connect to this pin.
L4, M4	DB1[0]P/DB1[0]N	Port 1 Positive/Negative Data Input Bit 0.
L5, M5	DB1[1]P/DB1[1]N	Port 1 Positive/Negative Data Input Bit 1.
L6, M6	DB1[2]P/DB1[2]N	Port 1 Positive/Negative Data Input Bit 2.
L7, M7	DB1[3]P/DB1[3]N	Port 1 Positive/Negative Data Input Bit 3.
L8, M8	DB1[4]P/DB1[4]N	Port 1 Positive/Negative Data Input Bit 4.
L9, M9	DB1[5]P/DB1[5]N	Port 1 Positive/Negative Data Input Bit 5.
L10, M10	DB1[6]P/DB1[6]N	Port 1 Positive/Negative Data Input Bit 6.
L11, M11	DB1[7]P/DB1[7]N	Port 1 Positive/Negative Data Input Bit 7.
L12, M12	DB1[8]P/DB1[8]N	Port 1 Positive/Negative Data Input Bit 8.
L13, M13	DB1[9]P/DB1[9]N	Port 1 Positive/Negative Data Input Bit 9.
L14, M14	DB1[10]P/DB1[10]N	Port 1 Positive/Negative Data Input Bit 10.
N1, P1	NC, NC	Do not connect to this pin.
N2, P2	NC, NC	Do not connect to this pin.
N3, P3	NC, NC	Do not connect to this pin.
N4, P4	DB0[0]P/DB0[0]N	Port 0 Positive/Negative Data Input Bit 0.
N5, P5	DB0[1]P/DB0[1]N	Port 0 Positive/Negative Data Input Bit 1.
N6, P6	DB0[2]P/DB0[2]N	Port 0 Positive/Negative Data Input Bit 2.
N7, P7	DB0[3]P/DB0[3]N	Port 0 Positive/Negative Data Input Bit 3.
N8, P8	DB0[4]P/DB0[4]N	Port 0 Positive/Negative Data Input Bit 4.
N9, P9	DB0[5]P/DB0[5]N	Port 0 Positive/Negative Data Input Bit 5.
N10, P10	DB0[6]P/DB0[6]N	Port 0 Positive/Negative Data Input Bit 6.
N11, P11	DB0[7]P/DB0[7]N	Port 0 Positive/Negative Data Input Bit 7.
N12, P12	DB0[8]P/DB0[8]N	Port 0 Positive/Negative Data Input Bit 8.
N13, P13	DB0[9]P/DB0[9]N	Port 0 Positive/Negative Data Input Bit 9.
N14, P14	DB0[10]P/DB0[10]N	Port 0 Positive/Negative Data Input Bit 10.

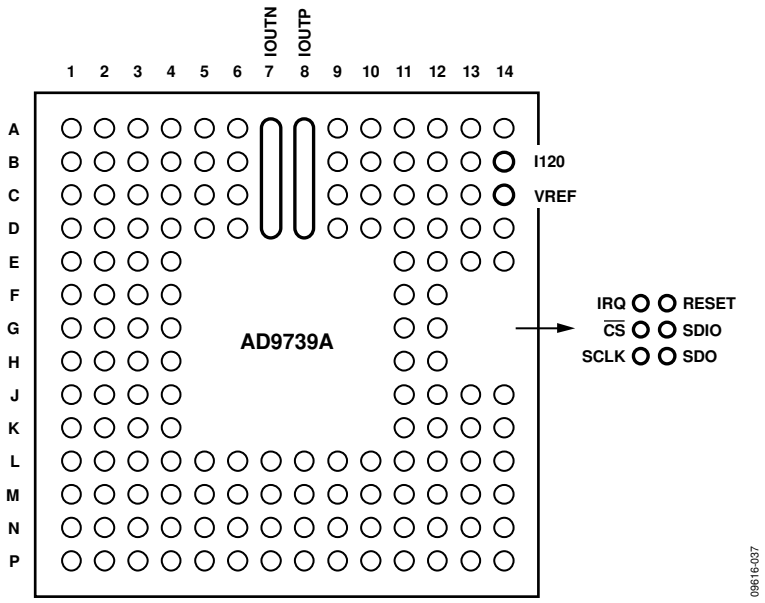

Figure 8. AD9739A Analog I/O and SPI Control Pins (Top View)

Table 8. AD9739A Pin Function Descriptions

Pin No.	Mnemonic	Description
C1, C2, D1, D2, E1, E2, E3, E4	VDDC	1.8 V Clock Supply Input.
A1, A2, A3, A4, A5, B1, B2, B3, B4, B5, C4, C5, D4, D5	VSSC	Clock Supply Ground.
A10, A11, B10, B11, C10, C11, D10, D11	VDDA	3.3 V Analog Supply Input.
A12, A13, B12, B13, C12, C13, D12, D13,	VSSA	Analog Supply Ground.
A6, A9, B6, B9, C6, C9, D6, D9, E11, E12, E13, E14, F1, F2, F3, F4, F11, F12	VSSA Shield	Analog Supply Ground Shield. Tie to VSSA at the DAC.
A14	NC	Do not connect to this pin.
A7, B7, C7, D7	IOUTN	DAC Negative Current Output Source.
A8, B8, C8, D8	IOUTP	DAC Positive Current Output Source.
B14	I120	Nominal 1.2 V Reference. Tie to analog ground via a 10 kΩ resistor to generate a 120 µA reference current.
C14	VREF	Voltage Reference Input/Output. Decouple to VSSA with a 1 nF capacitor.
D14	NC	Factory Test Pin. Do not connect to this pin.
C3, D3	DACCLK_N/DACCLK_P	Negative/Positive DAC Clock Input (DACCLK).
F13	IRQ	Interrupt Request Open Drain Output. Active high. Pull up to VDD33 with a 10 kΩ resistor.
F14	RESET	Reset Input. Active high. Tie to VSS if unused.
G13	$\overline{CS}$	Serial Port Enable Input.
G14	SDIO	Serial Port Data Input/Output.
H13	SCLK	Serial Port Clock Input.
H14	SDO	Serial Port Data Output.
J3, J4, J11, J12	VDD33	3.3 V Digital Supply Input.
G1, G2, G3, G4, G11, G12	VDD	1.8 V Digital Supply Input.
H1, H2, H3, H4, H11, H12, K3, K4, K11, K12	VSS	Digital Supply Ground.
J1, J2	NC	Differential resistor of 200 Ω exists between J1 and J2. Do not connect to this pin.
K1, K2	NC	Differential resistor of 100 Ω exists between K1 and K2. Do not connect to this pin.
J13, J14	DCO_P/DCO_N	Positive/Negative Data Clock Output (DCO).
K13, K14	DCI_P/DCI_N	Positive/Negative Data Clock Input (DCI).

Pin No.	Mnemonic	Description
L1, M1	DB1[0]P/DB1[0]N	Port 1 Positive/Negative Data Input Bit 0.
L2, M2	DB1[1]P/DB1[1]N	Port 1 Positive/Negative Data Input Bit 1.
L3, M3	DB1[2]P/DB1[2]N	Port 1 Positive/Negative Data Input Bit 2.
L4, M4	DB1[3]P/DB1[3]N	Port 1 Positive/Negative Data Input Bit 3.
L5, M5	DB1[4]P/DB1[4]N	Port 1 Positive/Negative Data Input Bit 4.
L6, M6	DB1[5]P/DB1[5]N	Port 1 Positive/Negative Data Input Bit 5.
L7, M7	DB1[6]P/DB1[6]N	Port 1 Positive/Negative Data Input Bit 6.
L8, M8	DB1[7]P/DB1[7]N	Port 1 Positive/Negative Data Input Bit 7.
L9, M9	DB1[8]P/DB1[8]N	Port 1 Positive/Negative Data Input Bit 8.
L10, M10	DB1[9]P/DB1[9]N	Port 1 Positive/Negative Data Input Bit 9.
L11, M11	DB1[10]P/DB1[10]N	Port 1 Positive/Negative Data Input Bit 10.
L12, M12	DB1[11]P/DB1[11]N	Port 1 Positive/Negative Data Input Bit 11.
L13, M13	DB1[12]P/DB1[12]N	Port 1 Positive/Negative Data Input Bit 12.
L14, M14	DB1[13]P/DB1[13]N	Port 1 Positive/Negative Data Input Bit 13.
N1, P1	DB0[0]P/DB0[0]N	Port 0 Positive/Negative Data Input Bit 0.
N2, P2	DB0[1]P/DB0[1]N	Port 0 Positive/Negative Data Input Bit 1.
N3, P3	DB0[2]P/DB0[2]N	Port 0 Positive/Negative Data Input Bit 2.
N4, P4	DB0[3]P/DB0[3]N	Port 0 Positive/Negative Data Input Bit 3.
N5, P5	DB0[4]P/DB0[4]N	Port 0 Positive/Negative Data Input Bit 4.
N6, P6	DB0[5]P/DB0[5]N	Port 0 Positive/Negative Data Input Bit 5.
N7, P7	DB0[6]P/DB0[6]N	Port 0 Positive/Negative Data Input Bit 6.
N8, P8	DB0[7]P/DB0[7]N	Port 0 Positive/Negative Data Input Bit 7.
N9, P9	DB0[8]P/DB0[8]N	Port 0 Positive/Negative Data Input Bit 8.
N10, P10	DB0[9]P/DB0[9]N	Port 0 Positive/Negative Data Input Bit 9.
N11, P11	DB0[10]P/DB0[10]N	Port 0 Positive/Negative Data Input Bit 10.
N12, P12	DB0[11]P/DB0[11]N	Port 0 Positive/Negative Data Input Bit 11.
N13, P13	DB0[12]P/DB0[12]N	Port 0 Positive/Negative Data Input Bit 12.
N14, P14	DB0[13]P/DB0[13]N	Port 0 Positive/Negative Data Input Bit 13.

TYPICAL PERFORMANCE CHARACTERISTICS—AD9737A

STATIC LINEARITY

I_{OUTFS} = 20 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

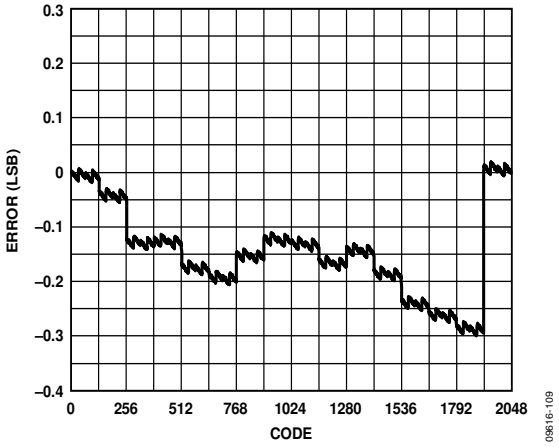

Figure 9. Typical INL, 20 mA at 25°C

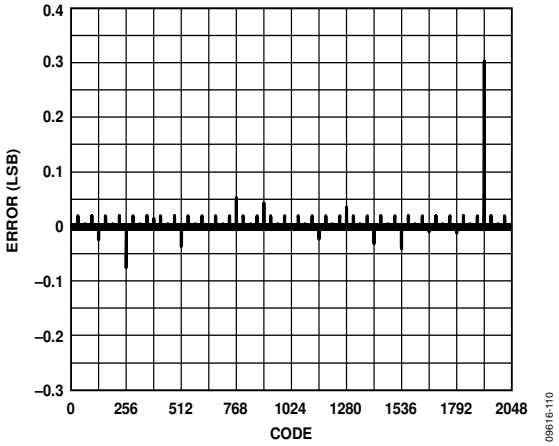

Figure 10. Typical DNL, 20 mA at 25°C

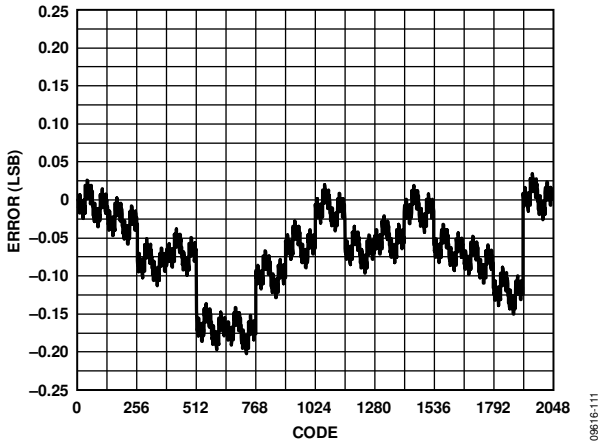

Figure 11. Typical INL, 10 mA at 25°C

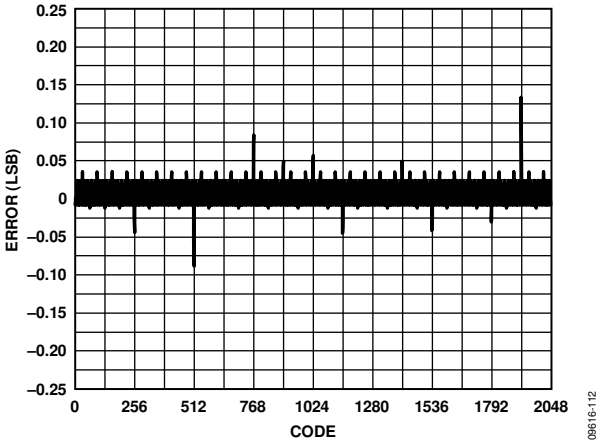

Figure 12. Typical DNL, 10 mA at 25°C

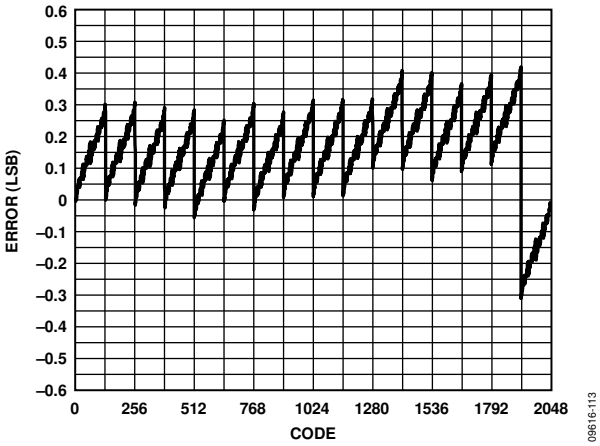

Figure 13. Typical INL, 30 mA at 25°C

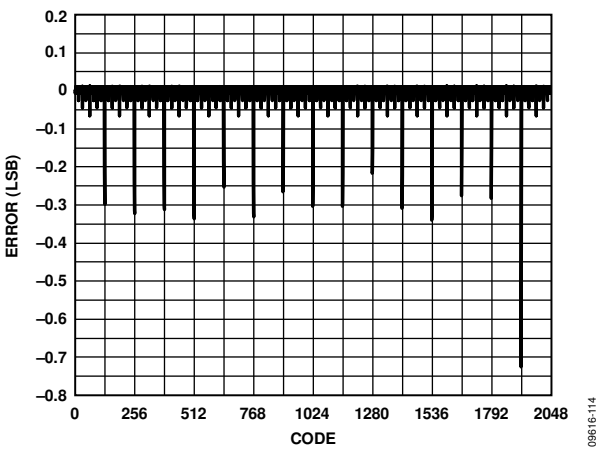

Figure 14. Typical DNL, 30 mA at 25°C

AC (NORMAL MODE)

I_{OUTFS} = 20 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

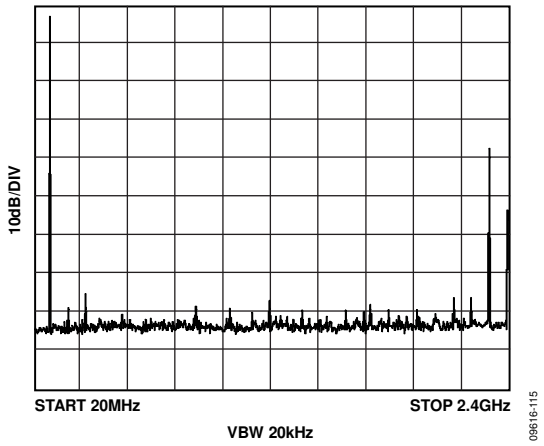

Figure 15. Single Tone Spectrum at f_{OUT} = 91 MHz, f_{DAC} = 2.4 GSPS

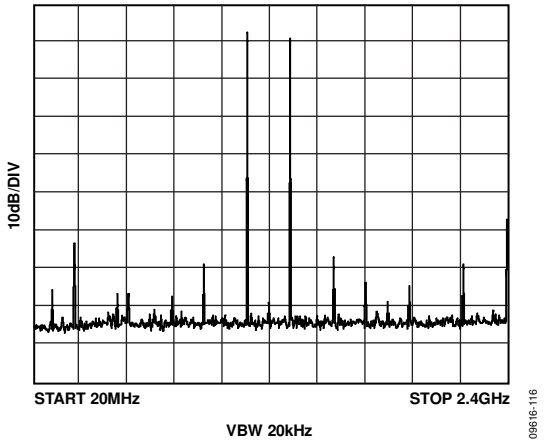

Figure 16. Single-Tone Spectrum at f_{OUT} = 1091 MHz, f_{DAC} = 2.4 GSPS

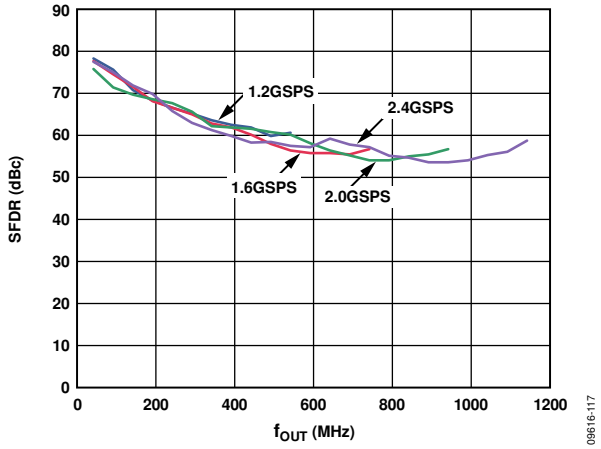

Figure 17. SFDR vs. f_{OUT} over f_{DAC}

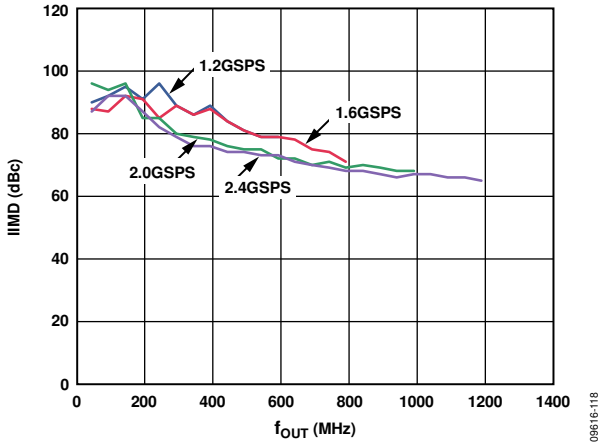

Figure 18. IMD vs. f_{OUT} over f_{DAC}

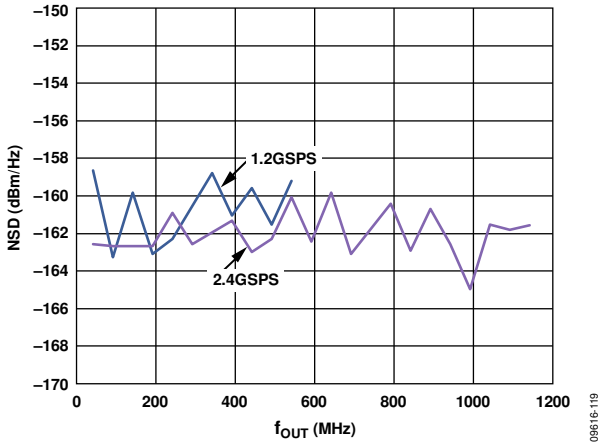

Figure 19. Single-Tone NSD over f_{OUT}

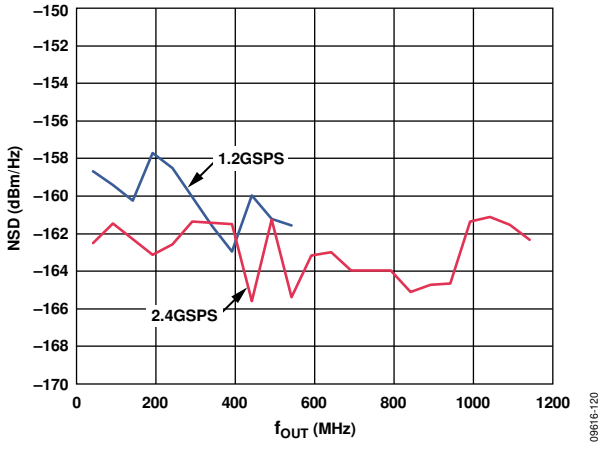

Figure 20. Eight-Tone NSD over f_{OUT}

f_{DAC} = 2 GSPS, I_{OUTFS} = 20 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

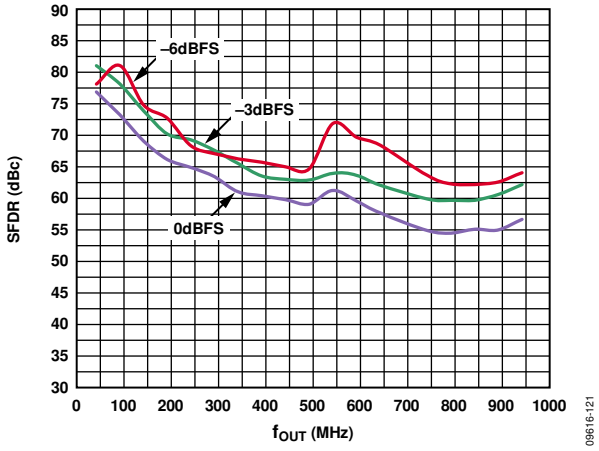

Figure 21. SFDR vs. f_{OUT} over Digital Full Scale

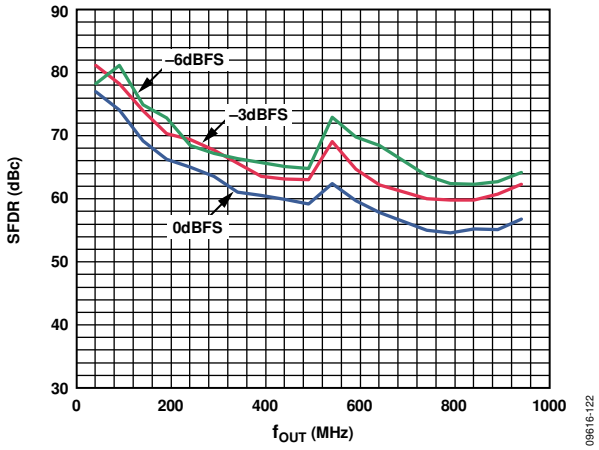

Figure 22. SFDR for Second Harmonic vs. f_{OUT} over Digital Full Scale

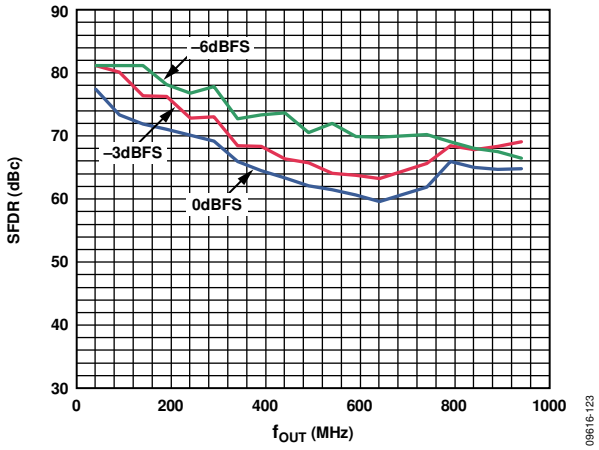

Figure 23. SFDR for Third Harmonic vs. f_{OUT} over Digital Full Scale

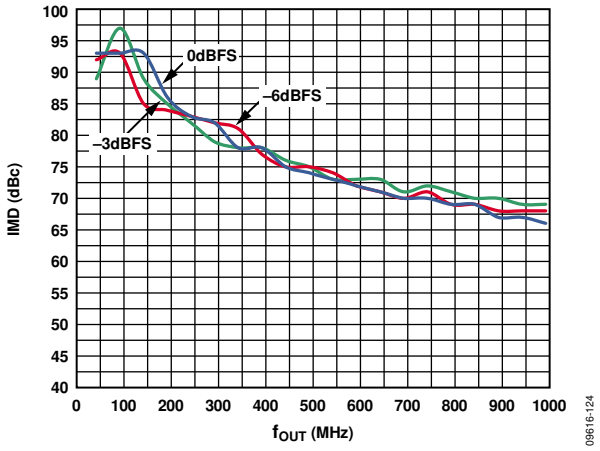

Figure 24. IMD vs. f_{OUT} over Digital Full Scale

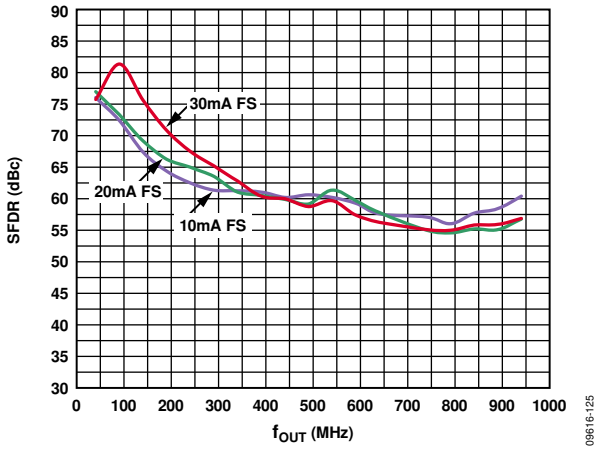

Figure 25. SFDR vs. f_{OUT} over DAC I_{OUTFS}

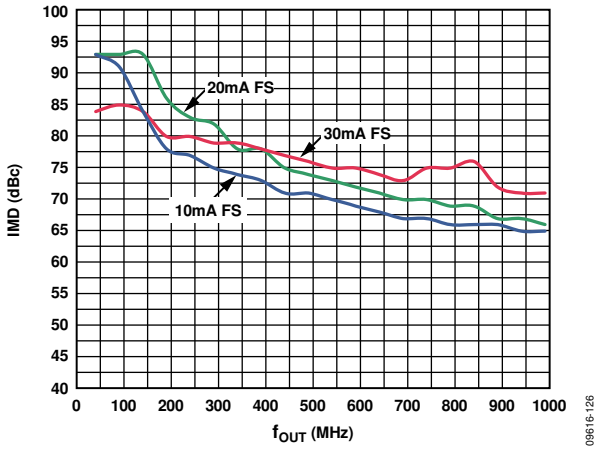

Figure 26. IMD vs. f_{OUT} over DAC I_{OUTFS}

AC (MIX-MODE)

f_{DAC} = 2.1 GSPS, I_{OUTFS} = 20 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

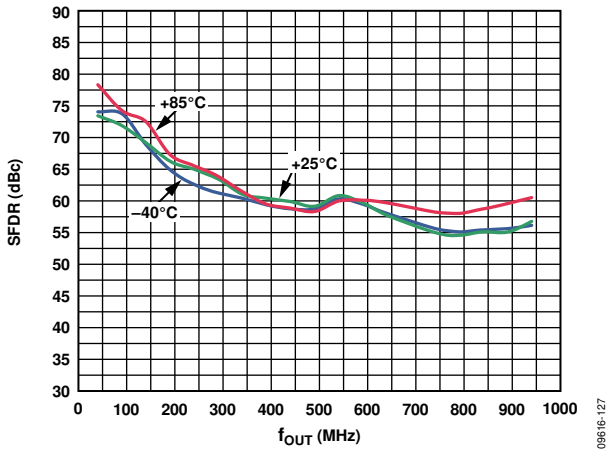

Figure 27. SFDR vs. f_{OUT} over Temperature

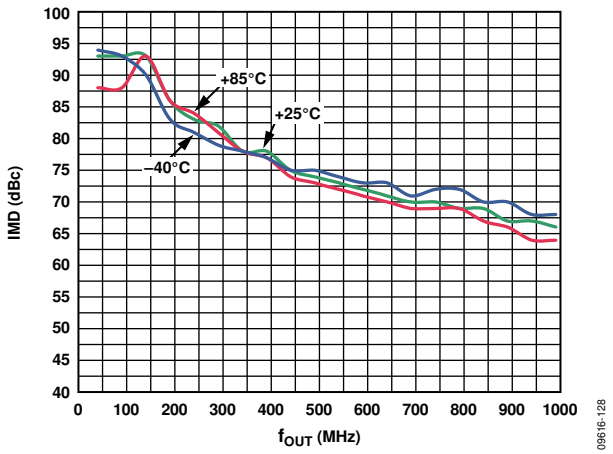

Figure 28. IMD vs. f_{OUT} over Temperature

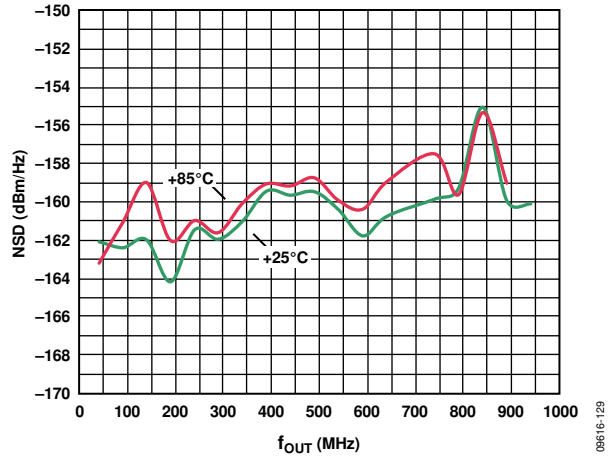

Figure 29. Single-Tone NSD vs. f_{OUT} over Temperature

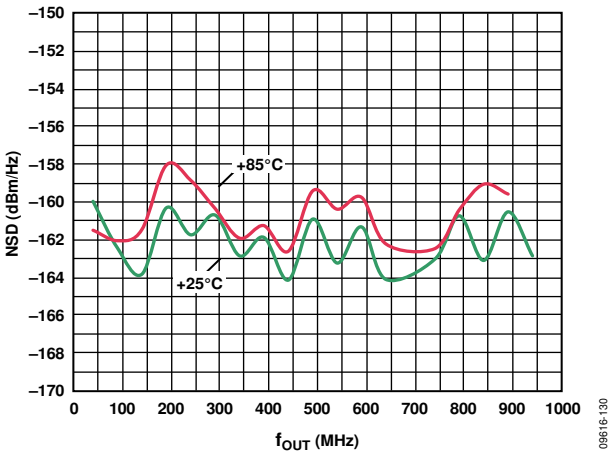

Figure 30. Eight-Tone NSD vs. f_{OUT} over Temperature

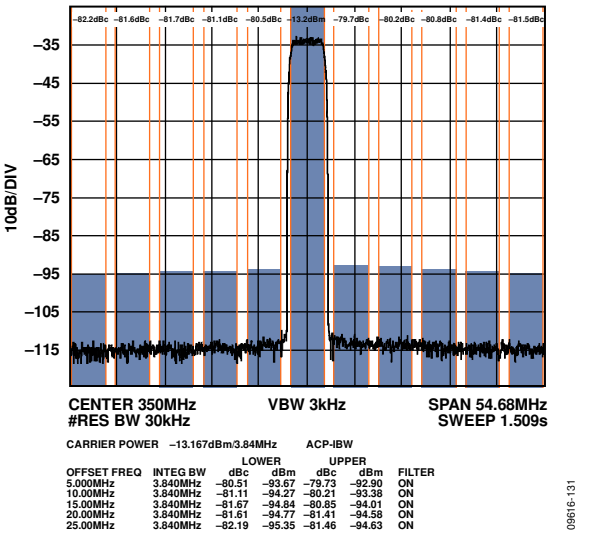

Figure 31. Single-Carrier WCDMA at 350 MHz, f_{DAC} = 2457.6 MSPS

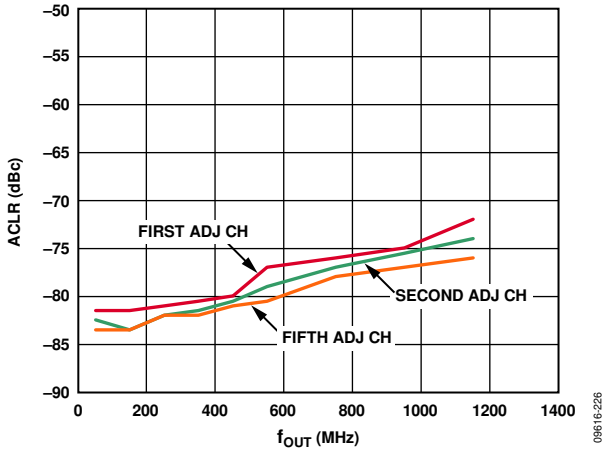

Figure 32. Single-Carrier WCDMA ACLR vs. f_{OUT} at 2457.6 MSPS

f_{DAC} = 2.1 GSPS, I_{OUTFS} = 20 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

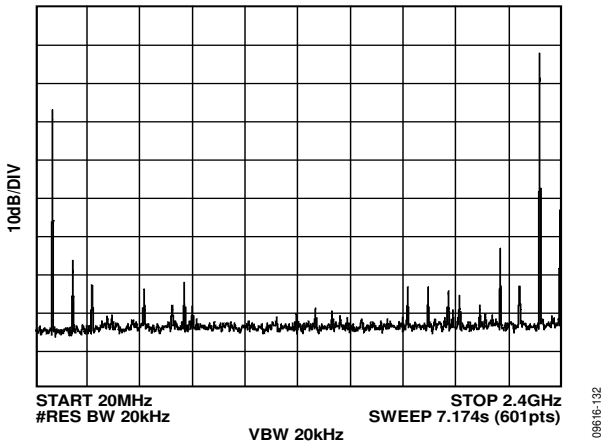

Figure 33. Single-Tone Spectrum at f_{OUT} = 2.31 GHz, f_{DAC} = 2.4 GSPS

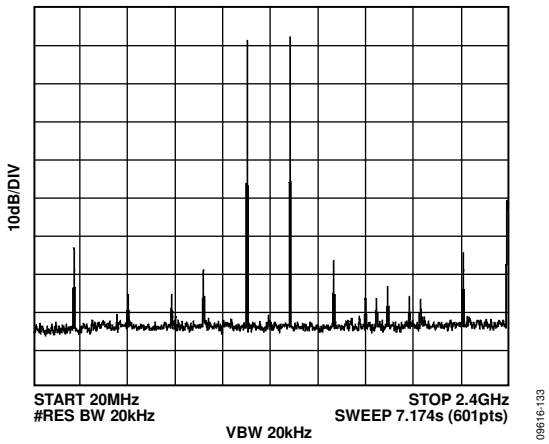

Figure 34. Single-Tone Spectrum at f_{OUT} = 1.31 GHz, f_{DAC} = 2.4 GSPS

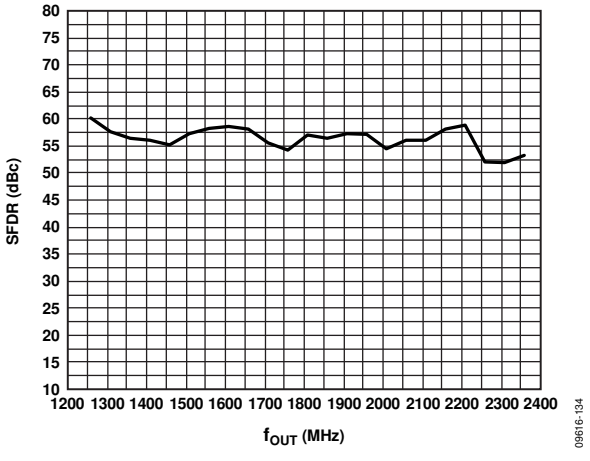

Figure 35. SFDR in Mix-mode vs. f_{OUT} at 2.4 GSPS

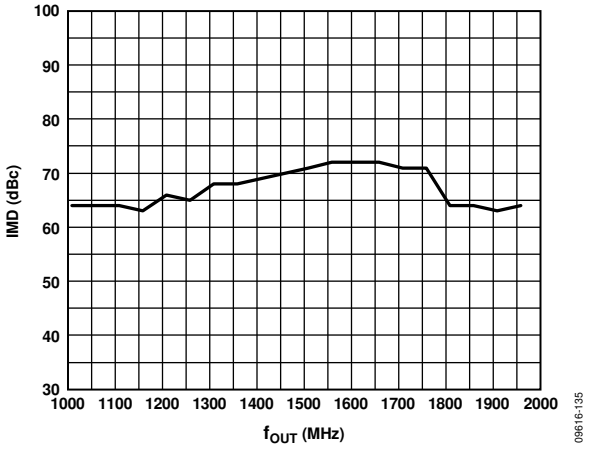

Figure 36. IMD in Mix-Mode vs. f_{OUT} at 2.4 GSPS

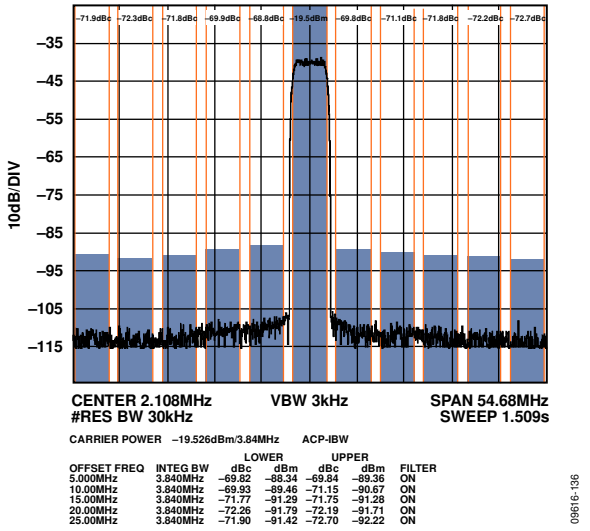

Figure 37. Typical Single-Carrier WCDMA ACLR Performance at 2.1 GHz, f_{DAC} = 2457.6 MSPS (Second Nyquist Zone)

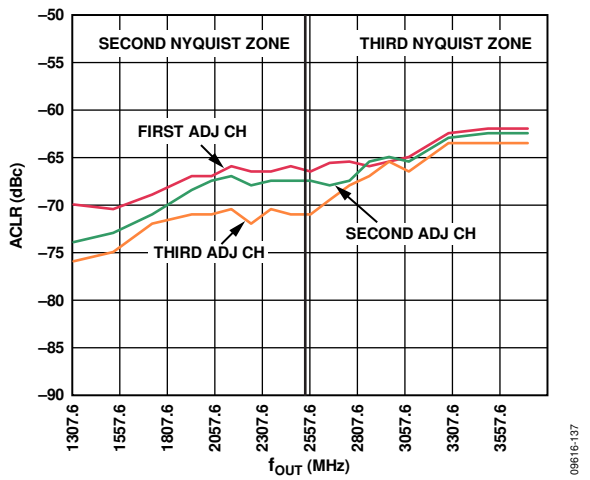

Figure 38. Single-Carrier WCDMA ACLR vs. f_{OUT}, f_{DAC} = 2457.6 MSPS

f_{DAC} = 2.1 GSPS, I_{OUTFS} = 20 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

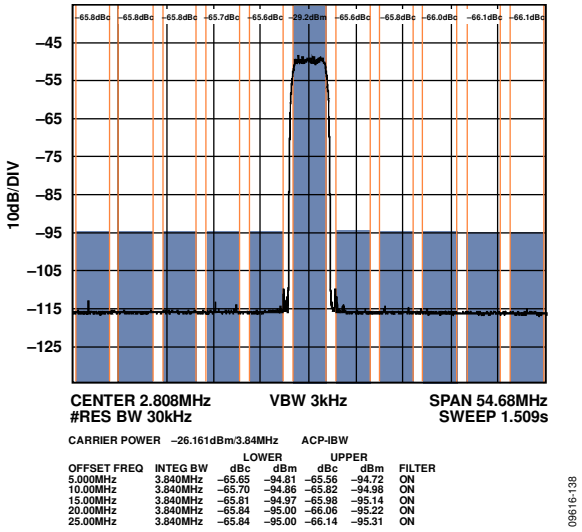

Figure 39. Typical Single-Carrier WCDMA ACLR Performance at 2.8 GHz, f_{DAC} = 2457.6 MSPS (Third Nyquist Zone)

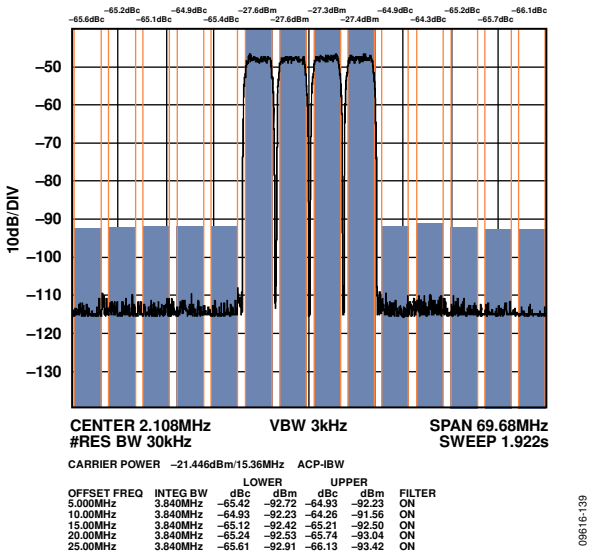

Figure 40. Typical Four-Carrier WCDMA ACLR Performance at 2.1 GHz, f_{DAC} = 2457.6 MSPS (Second Nyquist Zone)

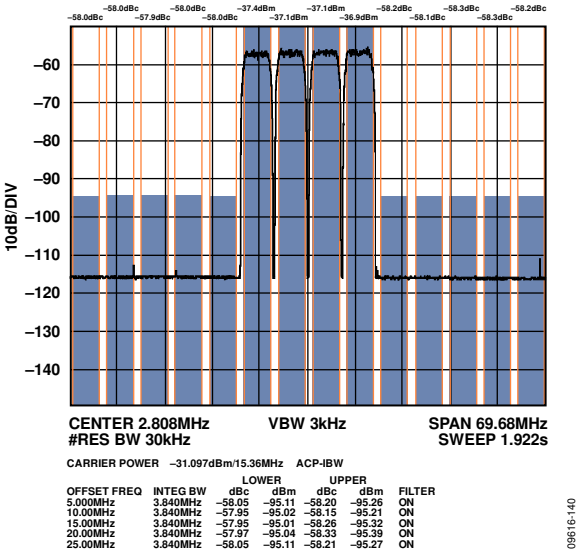

Figure 41. Typical Four-Carrier WCDMA ACLR Performance at 2.8 GHz, f_{DAC} = 2457.6 MSPS (Third Nyquist Zone)

ONE-CARRIER DOCSIS PERFORMANCE (NORMAL MODE)

I_{OUTFS} = 20 mA, f_{DAC} = 2.4576 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

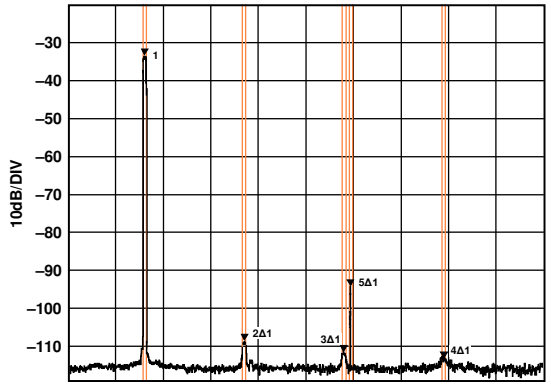

Figure 42. Low Band Wideband ACLR

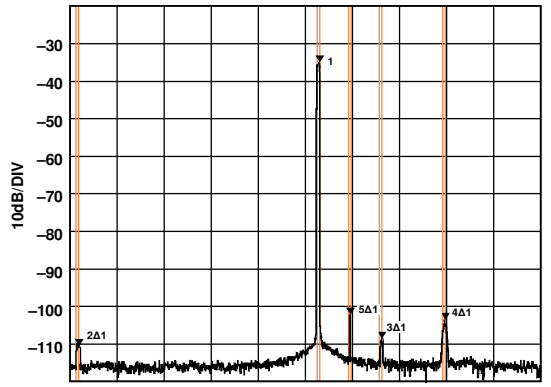

Figure 43. Mid Band Wideband ACLR

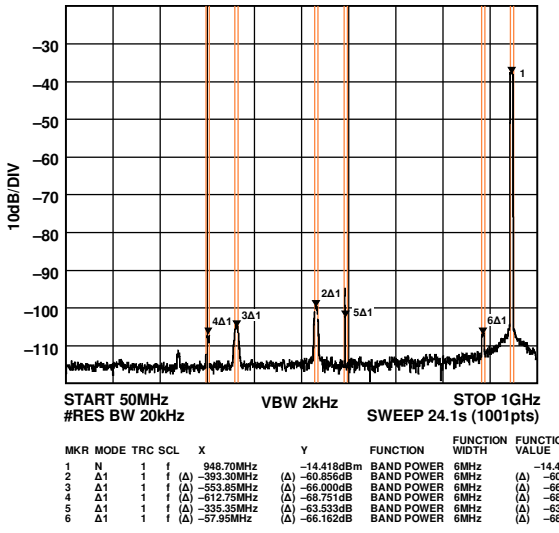

Figure 44. High Band Wideband ACLR

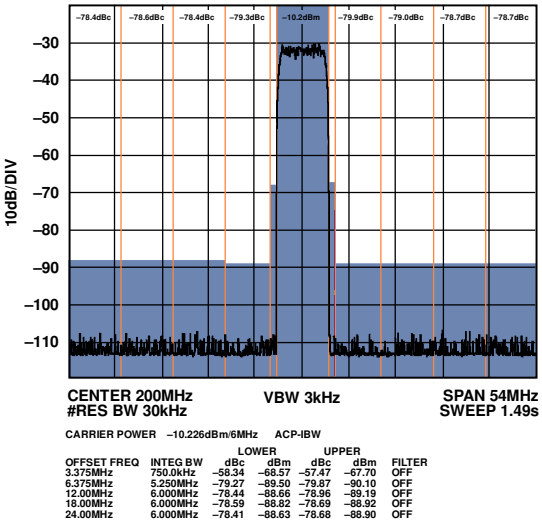

Figure 45. Low Band Narrow-Band ACLR

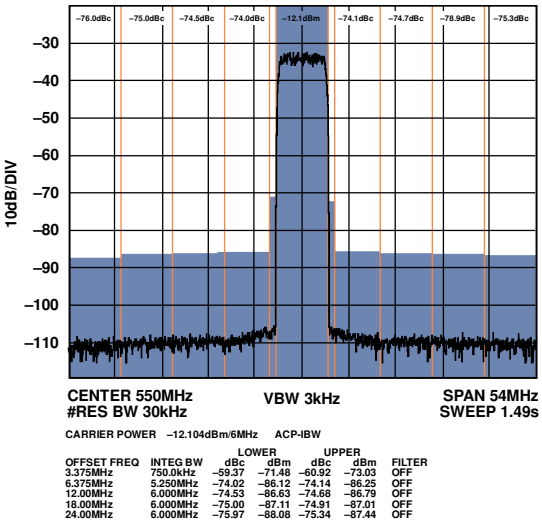

Figure 46. Mid Band Narrow-Band ACLR

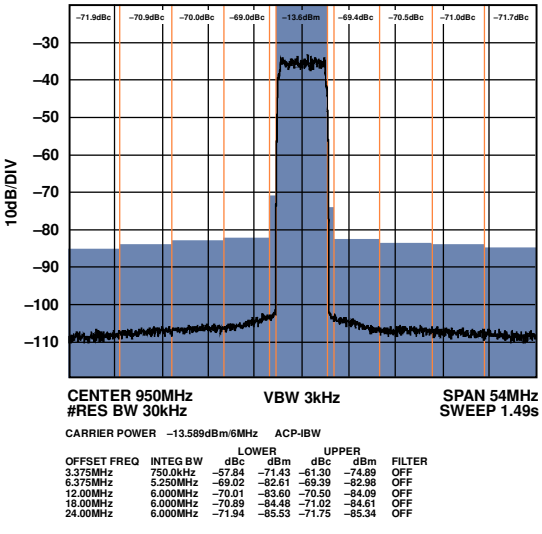

Figure 47. High Band Narrow-Band ACLR

FOUR-CARRIER DOCSIS PERFORMANCE (NORMAL MODE)

I_{OUTFS} = 20 mA, f_{DAC} = 2.4576 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

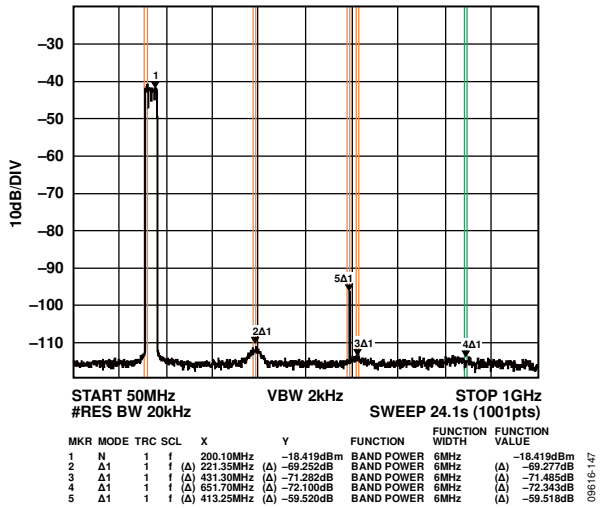

Figure 48. Low Band Wideband ACLR

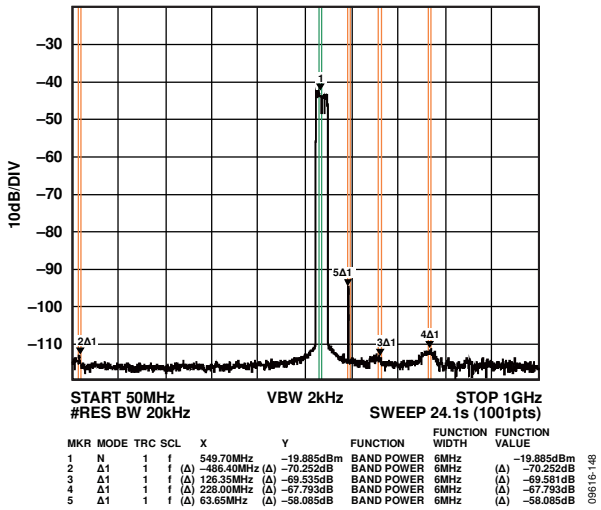

Figure 49. Mid Band Wideband ACLR

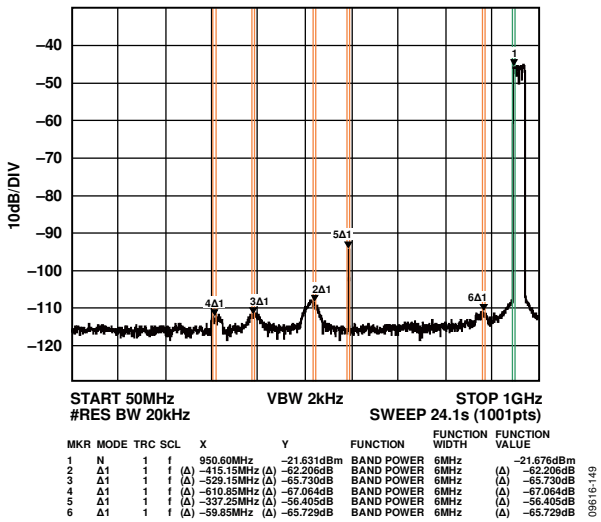

Figure 50. High Band Wideband ACLR

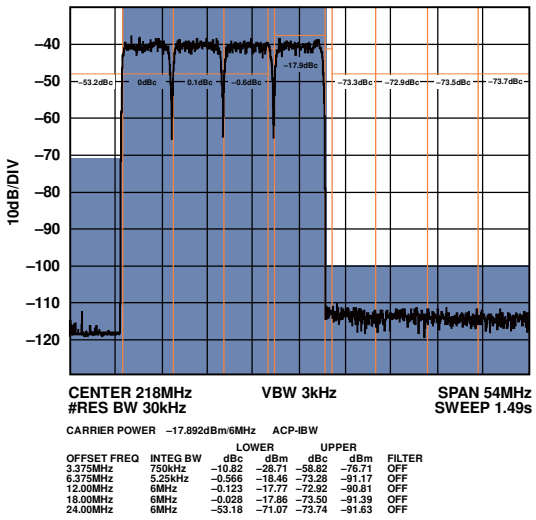

Figure 51. Low Band Narrow-Band ACLR (Worse Side)

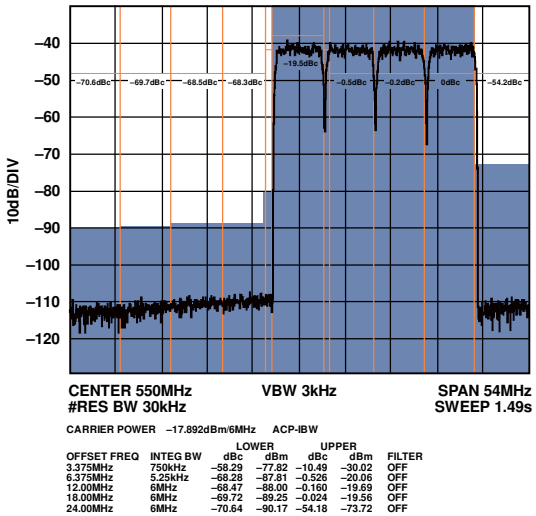

Figure 52. Mid Band Narrow-Band ACLR (Worse Side)

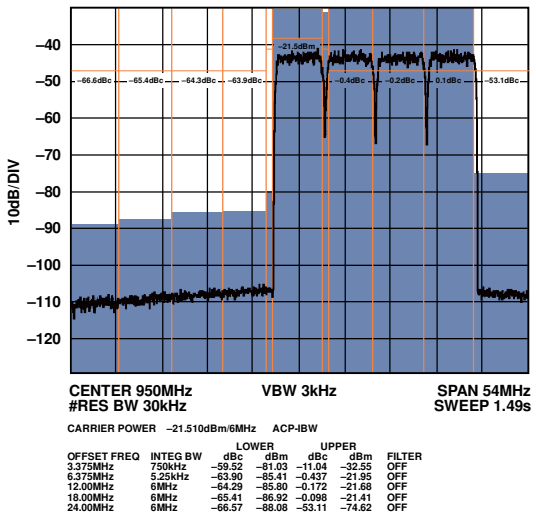

Figure 53. High Band Narrow-Band ACLR (Worse Side)

EIGHT-CARRIER DOCSIS PERFORMANCE (NORMAL MODE)

I_{OUTFS} = 20 mA, f_{DAC} = 2.4576 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

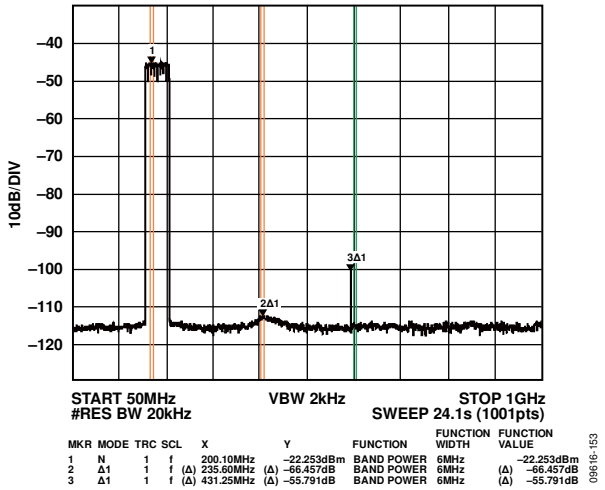

Figure 54. Low Band Wideband ACLR

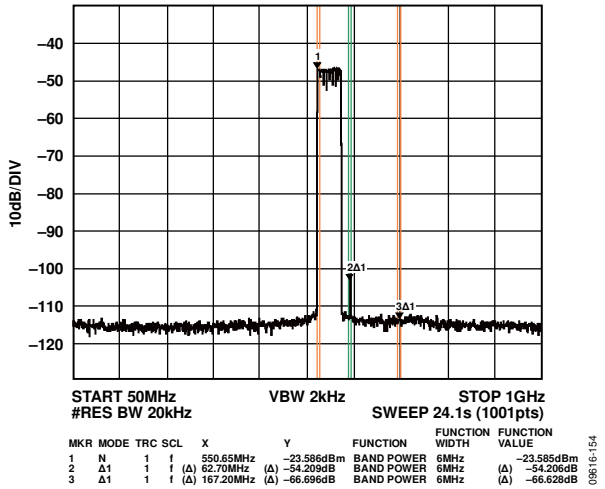

Figure 55. Mid Band Wideband ACLR

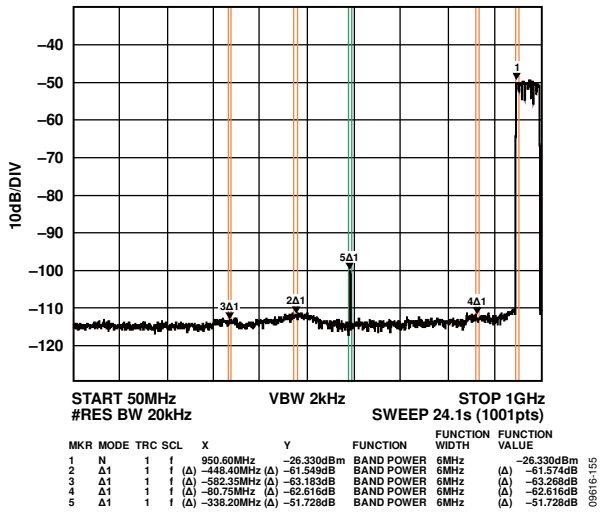

Figure 56. High Band Wideband ACLR

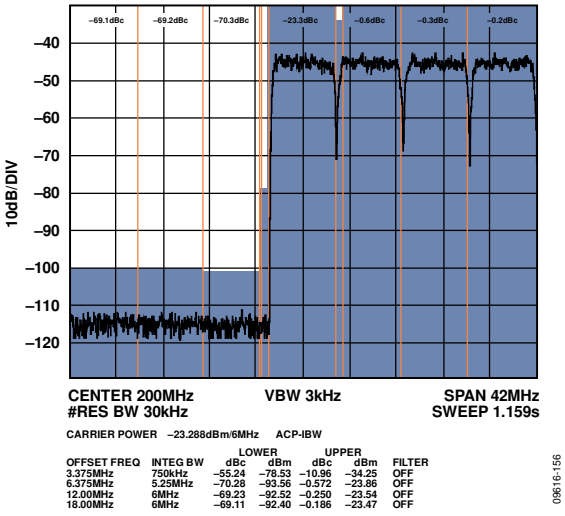

Figure 57. Low Band Narrow-Band ACLR (Worse Side)

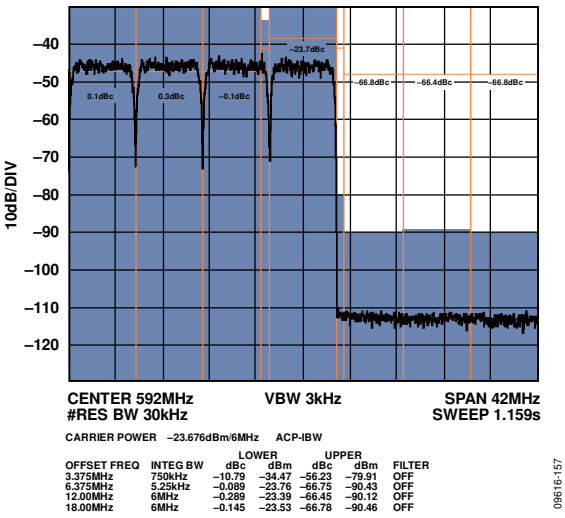

Figure 58. Mid Band Narrow-Band ACLR (Worse Side)

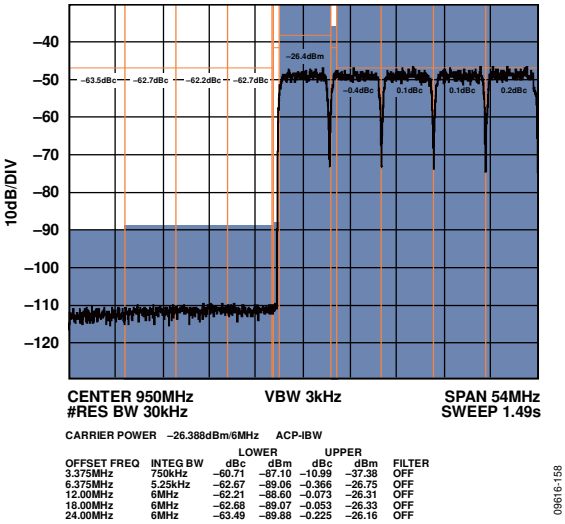

Figure 59. High Band Narrow-Band ACLR

16-CARRIER DOCSIS PERFORMANCE (NORMAL MODE)

I_{OUTFS} = 20 mA, f_{DAC} = 2.4576 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

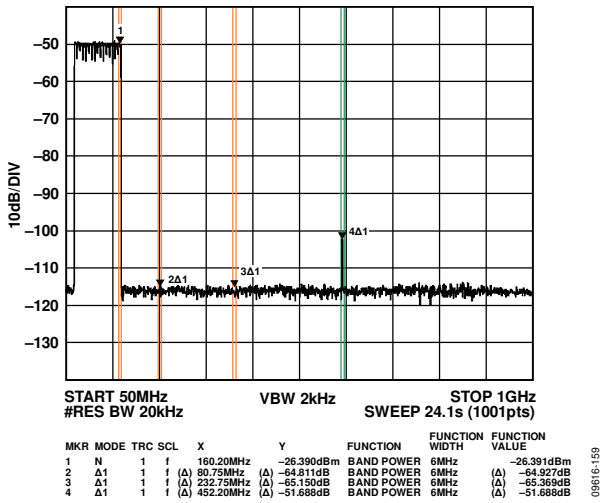

Figure 60. Low Band Wideband ACLR

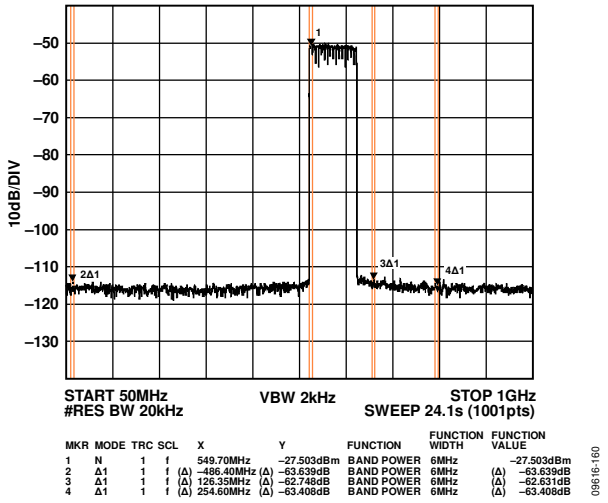

Figure 61. Mid Band Wideband ACLR

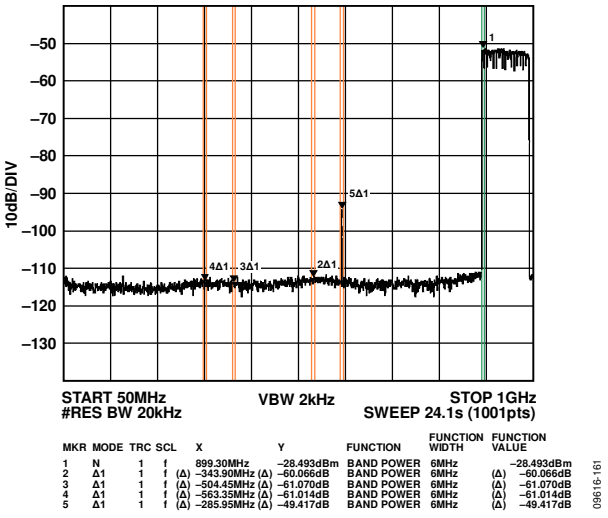

Figure 62. High Band Wideband ACLR

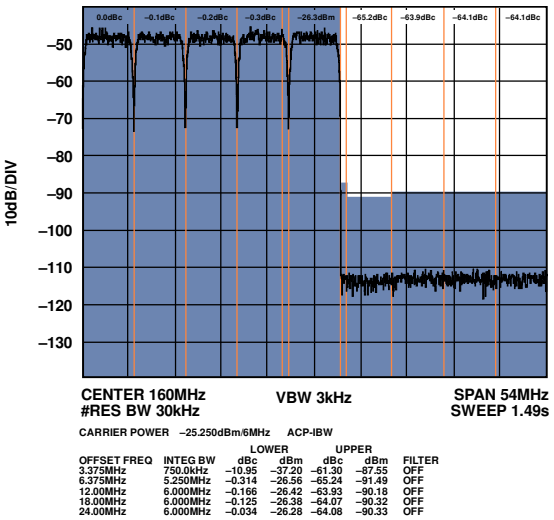

Figure 63. Low Band Narrow-Band ACLR

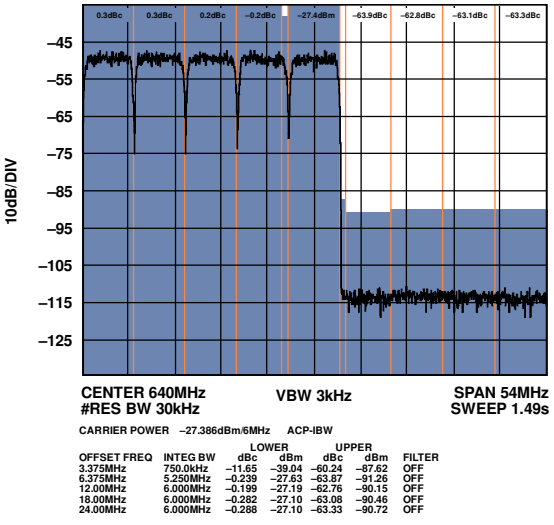

Figure 64. Mid Band Narrow-Band ACLR (Worse Side)

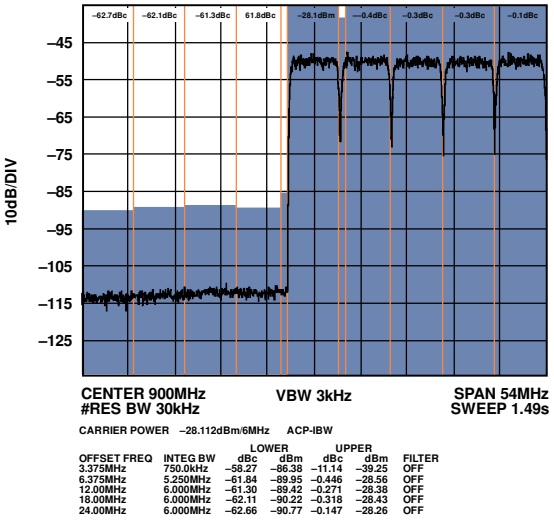

Figure 65. High Band Narrow-Band ACLR

32-CARRIER DOCSIS PERFORMANCE (NORMAL MODE)

I_{OUTFS} = 20 mA, f_{DAC} = 2.4576 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

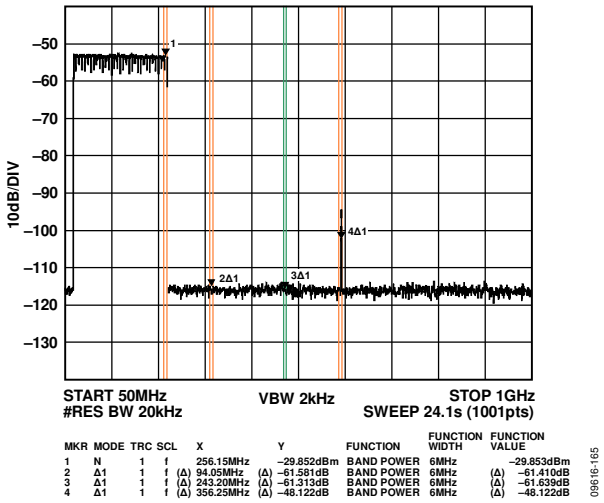

Figure 66. Low Band Wideband ACLR

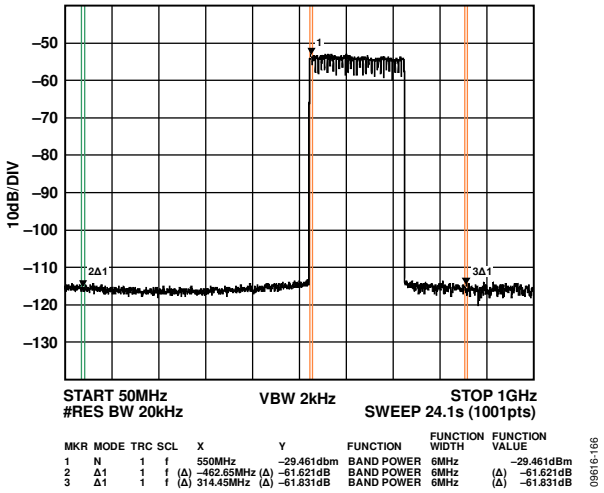

Figure 67. Mid Band Wideband ACLR

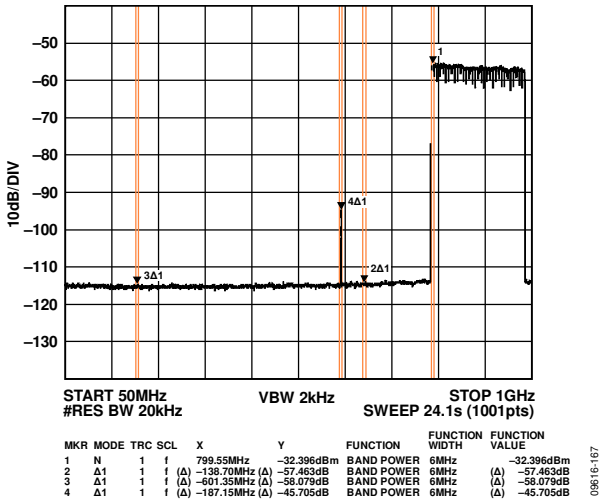

Figure 68. High Band Wideband ACLR

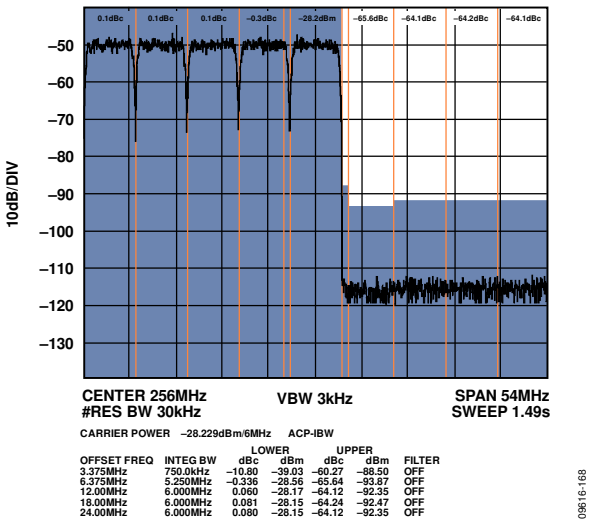

Figure 69. Low Band Narrow-Band ACLR

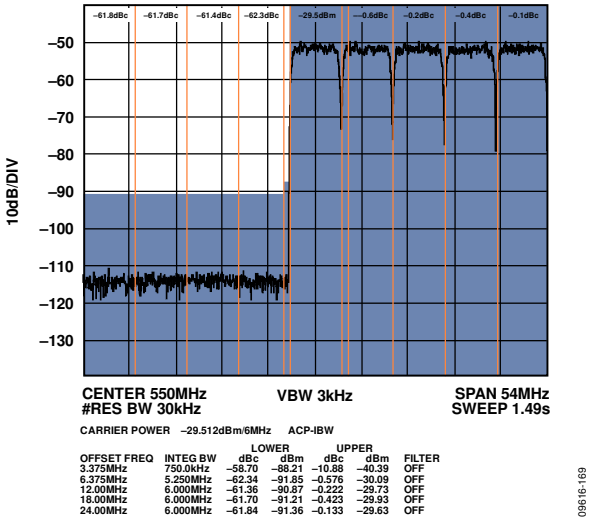

Figure 70. Mid Band Narrow-Band ACLR (Worse Side)

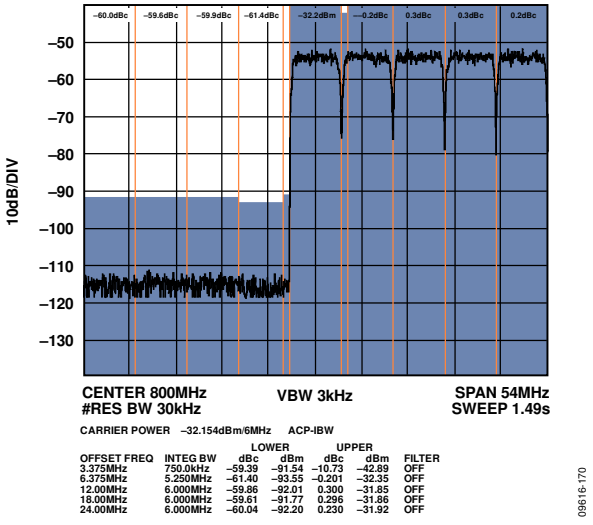

Figure 71. High Band Narrow-Band ACLR

64- AND 128-CARRIER DOCSIS PERFORMANCE (NORMAL MODE)

I_{OUTFS} = 20 mA, f_{DAC} = 2.4576 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

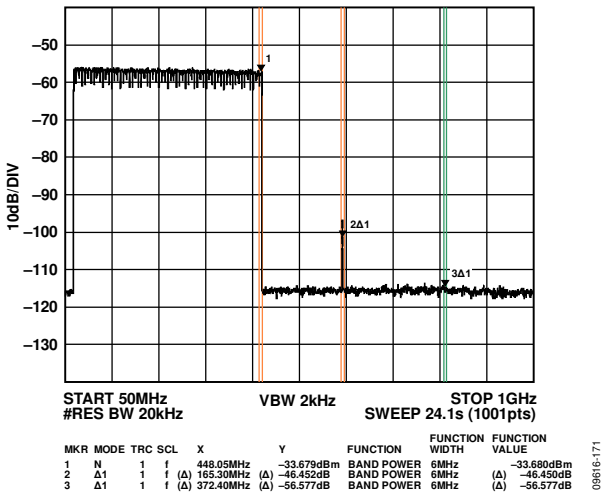

Figure 72. Low Band Wideband ACLR

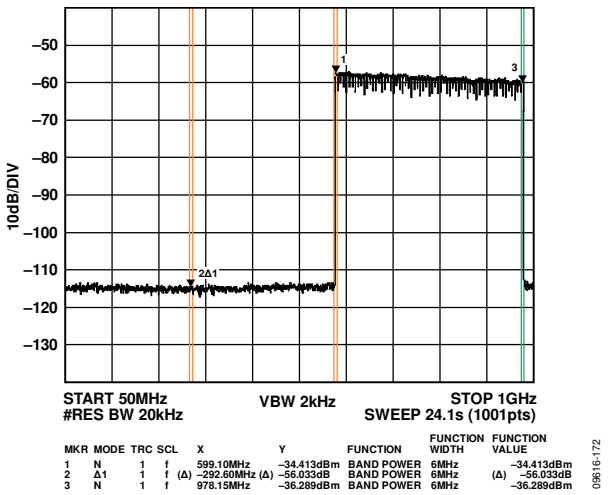

Figure 73. High Band Wideband ACLR

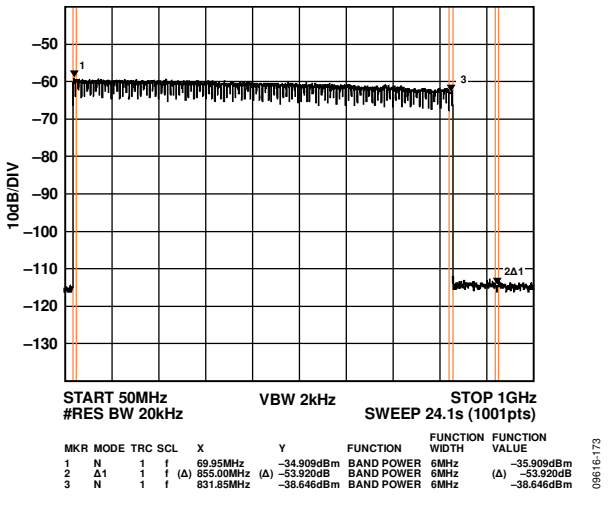

Figure 74. 128-Carrier Low Band Wideband ACLR

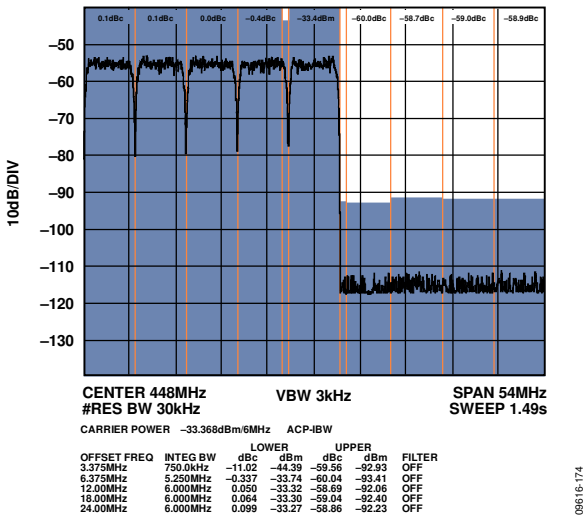

Figure 75. 64-Carrier Low Band Narrow-Band ACLR

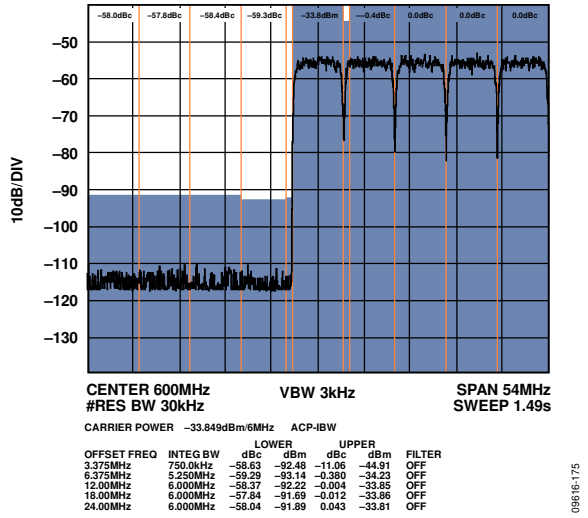

Figure 76. 64-Carrier High Band Narrow-Band ACLR

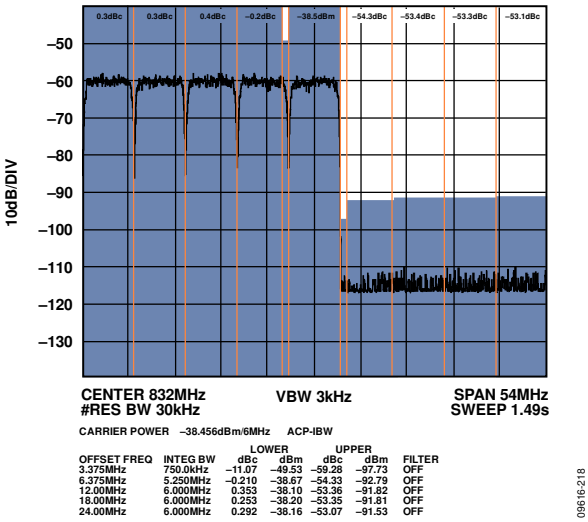

Figure 77. 128-Carrier Narrow-Band ACLR