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14-Bit, 2.5 GSPS, RF Digital-to-Analog Converter

Data Sheet **AD9739**

FEATURES

- **Direct RF synthesis at 2.5 GSPS update rate**
  - **DC to 1.25 GHz in baseband mode**
  - **1.25 GHz to 3.0 GHz in mix mode**
- **Industry leading single/multicarrier IF or RF synthesis**
  - **f_{OUT} = 350 MHz, ACLR =80 dBc**
  - **f_{OUT} = 950 MHz, ACLR = 78 dBc**
  - **f_{OUT} = 2100 MHz, ACLR = 69 dBc**
- **Dual-port LVDS data interface**
  - **Up to 1.25 GSPS operation**
  - **Source synchronous DDR clocking**
- **Pin-compatible with the AD9739A**
- **Multichip synchronization capability**
- **Programmable output current: 8.7 mA to 31.7 mA**
- **Low power: 1.16 W at 2.5 GSPS**

APPLICATIONS

- **Broadband communications systems**
- **Military jammers**
- **Instrumentation, automatic test equipment**
- **Radar, avionics**

FUNCTIONAL BLOCK DIAGRAM

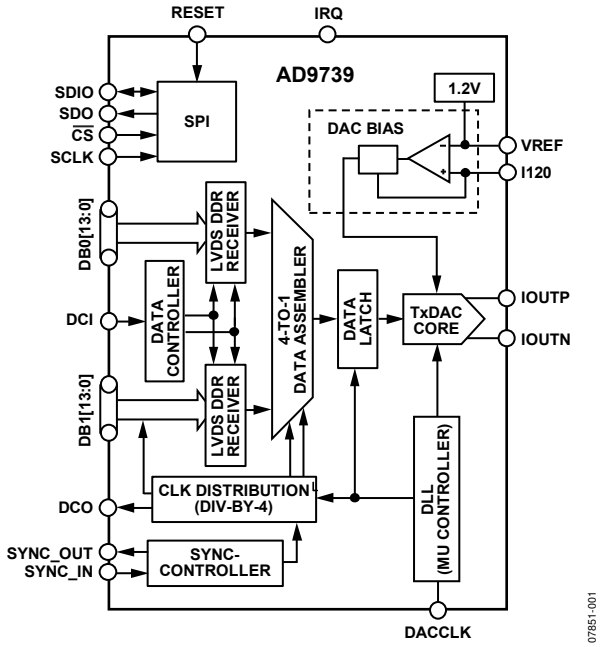


Figure 1.

GENERAL DESCRIPTION

The AD9739 is a 14-bit, 2.5 GSPS high performance RF digital-to-analog converter (DAC) capable of synthesizing wideband signals from dc up to 3.0 GHz. Its DAC core features a quad-switch architecture that provides exceptionally low distortion performance with an industry-leading direct RF synthesis capability. This feature enables multicarrier generation up to the Nyquist frequency in baseband mode as well as second and third Nyquist zones in mix mode. The output current can be programmed over the 8.66 mA to 31.66 mA range.

The inclusion of on-chip controllers simplifies system integration. A dual-port, source synchronous, LVDS interface simplifies the digital interface with existing FGPA/ASIC technology. On-chip controllers are used to manage external and internal clock domain variations over temperature to ensure reliable data transfer from the host to the DAC core. Multichip synchronization is possible with an on-chip synchronization controller. A serial peripheral interface (SPI) is used for device configuration as well as readback of status registers.

The AD9739 is manufactured on a 0.18 µm CMOS process and operates from 1.8 V and 3.3 V supplies. It is supplied in a 160-ball chip scale ball grid array for reduced package parasitics.

PRODUCT HIGHLIGHTS

1. Ability to synthesize high quality wideband signals with bandwidths of up to 1.25 GHz in the first or second Nyquist zone.
2. A proprietary quad-switch DAC architecture provides exceptional ac linearity performance while enabling mix mode operation.
3. A dual-port, double data rate, LVDS interface supports the maximum conversion rate of 2500 MSPS.
4. On-chip controllers manage external and internal clock domain skews.
5. A multichip synchronization capability.
6. Programmable differential current output with an 8.66 mA to 31.66 mA range.

Rev. C **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support **www.analog.com**

AD9739* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9739 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9739: 14-Bit, 2.5 GSPS, RF Digital-to-Analog Converter Data Sheet

TOOLS AND SIMULATIONS

- AD9739 IBIS Models

REFERENCE MATERIALS

Informational

- Advantiv™ Advanced TV Solutions

Press

- Trio of Analog Devices' Best-in-Class High-Speed Transmit D/A Converters Target Aerospace and Defense Applications

Solutions Bulletins & Brochures

- Digital to Analog Converters ICs Solutions Bulletin

DESIGN RESOURCES

- AD9739 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9739 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

2/15—Rev. B to Rev. C

Moved Revision History....3
Changes to Figure 6....11
Changes to Table 19....25
Changes to Theory of Operation Section....28
Changes to Figure 52....36
Changes to Clock Input Considerations Section....40
Deleted Figure 60....40
Changes to Table 32....48

1/12—Rev. A to Rev. B

Changes to Features Section, Applications Section, General Description Section, Figure 1, Product Highlights Section....1
Changes to DC Specifications Section....4
Changed Digital Specifications Section to LVDS Digital Specifications Section....5
Changes to LVDS Digital Specifications Section....5
Added Serial Port Specifications Section and Table 3; Renumbered Sequentially....6
Changes to AC Specifications Section....7
Changes to Table 5....8
Changes to Table 7....10
Deleted Static Linearity Section and Figure 7 to Figure 17; Renumbered Sequentially....11
Changed Dynamic Performance Normal Mode, 20 mA Full Scale (Unless Otherwise Noted) Section to AC (Normal Mode) Section....12
Changes to AC (Normal Mode) Section....12
Changed Dynamic Performance Mix Mode, 20 mA Full Scale Section to AC (Mix Mode) Section....15
Changes to AC (Mix Mode) Section....15
Added Serial Port Interface (SPI) Register Section, SPI Register Map Description Section, Reset Section, Table 8, and SPI Operation Section and Figure 34....18
Deleted DOCSIS Performance Section and Figure 46 to Figure 72 and added Figure 35 through Figure 38; Renumbered Sequentially....19
Changes to SPI Register Map Section and Table 9....20
Added SPI Port Configuration and Software Reset Section, Power-Down LVDS Interface and TxDAC® Section, Controller Clock Disable Section, Interrupt Request (IRQ) Enable/Status Section, and Table 10 to Table 13....22
Added TxDAC Full-Scale Current Setting (I_{OUTFS}) and Sleep Section, TxDAC Quad-Switch Mode of Operation Section, DCI Phase Alignment Status Section, SYNC_IN Phase Alignment Status Section, Data Receiver Controller Configuration Section, and Table 14 to Table 18....23
Added Data Receiver Controller_Data Sample Delay Value Section, Data and Sync Receiver Controller_DCI Delay Value/Window and Phase Rotation Section, Data Receiver Controller_Delay Line Status and Sync Controller SYNC_OUT Status Section, and Table 19 to Table 21....24
Deleted Serial Peripheral Interface Section, General Operation of the Serial Interface Section, Instruction Mode (8-Bit Instruction) Section, and Serial Interface Port Pin Description Section....25
Added Sync and Data Receiver Controller Lock/Tracking Status Section, CLK Input Common Mode Section, Mu Controller Configuration and Status Section, and Table 22 to Table 24....25
Deleted MSB/LSB Transfers Section, Serial Port Configuration Section, and Figure 74 to Figure 79....26
Added Part ID Section and Table 25....26
Changes to Theory of Operation Section....27
Added Figure 39....27
Deleted SPI Registers Section and Table 8 to Table 31....28
Moved and Changes to LVDS Data Port Interface Section....28
Added Figure 40 and Figure 41....28
Changes to Figure 42....29
Moved and Changes to Figure 43....29
Added Data Receiver Controller Initialization Description Section, Table 26, and Data Receiver Operation at Lower Clock Rates Section....30
Added LVDS Driver and Receiver Input Section, Figure 44 to Figure 47, and Table 27....31
Changed and Moved Mu Delay Controller Section to Mu Controller Section....32
Changes to Mu Controller Section, Figure 48, and Figure 49....32
Added Figure 50 and Table 28....32
Added Mu Controller Initialization Description Section....33
Changes to Interrupt Requests Section....34
Added Table 29....34
Changed Synchronization Controller Section to Multiple Device Synchronization Section....35
Added Figure 52....35
Changes to Figure 53....36
Added Sync Controller Initialization Description Section....36
Added Synchronization Limitations Section....37
Changed Applications Information to Analog Interface Considerations Section....38
Changes to Analog Modes of Operation Section....38
Deleted Clocking the AD9739 Section, Figure 85, and Figure 86....39
Added Clock Input Considerations Section, Figure 58 to Figure 60....39
Deleted Clock Phase Noise Affects on AC Performance Section, Table 32 to Table 34, Applying Data to the AD9739 Section, and Figure 87....40
Moved Figure 61....40
Changes to Voltage References Section and Analog Outputs Section....40
Added Equivalent DAC Output and Transfer Function and Figure 63....40
Deleted Mu Control Operation Section, Search Mode Section, and Figure 89....41
Moved Figure 64....41
Added Peak DAC Output Power Capability Section and Figure 65....41
Deleted Figure 90, Figure 91, Track Mode Section, Mu Delay and Phase Readback Section, Operating the Mu Controller

Manually Section, and Calculating Mu Delay Line Step Size Section 42
Added Output Stage Configuration Section and Figure 66 to Figure 70 42
Added Nonideal Spectral Artifacts Section, Figure 71, and Table 30 43
Deleted Operation in Master Mode, Figure 93, and Figure 94 44
Added Lab Evaluation of the AD9739 Section, Power Dissipation and Supply Domains Section, and Figure 72 to Figure 74 44
Deleted Figure 95, Operation in Slave Mode Section, and Data Receiver Operation in Auto Mode Section 45
Changes to Recommended Start-Up Sequence Section 45
Added Figure 75 45
Deleted Figure 97, Data Receiver Operation in Manual Mode Section, Calculating the DCI Delay Line Step Size Section, and Maximum Allowable Data Timing Skew/Jitter Section 46
Added Table 31 46
Deleted Optimizing the Clock Common-Mode Voltage Section, Figure 99, Analog Control Registers Section, Mirror Roll-Off Frequency Control Section, and Figure 101 47
Added Table 32 47
Deleted Figure 103, Figure 104, and Figure 106 48
Updated Outline Dimensions 48
Deleted Figure 107 to Figure 109 49
Deleted Table 35 to Table 44 50

7/11—Rev 0 to Rev A

Changes to Table 2, DAC CLOCK INPUT (DACCLK_P, DACCLK_N), Added DAC Clock Rate 4
Changes to Table 3, Added Dynamic Performance Parameters 5
Change to Ordering Guide 53

2/09—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

VDDA = VDD33 = 3.3 V, VDDC = VDD = 1.8 V, I_{OUTFS} = 20 mA.

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION		14		Bits
ACCURACY				
Integral Nonlinearity (INL)		±1.3		LSB
Differential Nonlinearity (DNL)		±0.8		LSB
ANALOG OUTPUTS				
Gain Error (with Internal Reference)		5.5		%
Full-Scale Output Current	8.66	20.2	31.66	mA
Output Compliance Range	−1.0		+1.0	V
Common-Mode Output Resistance		10		MΩ
Differential Output Resistance		70		Ω
Output Capacitance		1		pF
DAC CLOCK INPUT (DACCLK_P, DACCLK_N)				
Differential Peak-to-Peak Voltage	1.2	1.6	2.0	V
Common-Mode Voltage		900		mV
DAC Clock Rate	0.8		2.5	GHz
TEMPERATURE DRIFT				
Gain		60		ppm/°C
Reference Voltage		20		ppm/°C
REFERENCE				
Internal Reference Voltage	1.15	1.2	1.25	V
Output Resistance		5		kΩ
ANALOG SUPPLY VOLTAGES				
VDDA	3.1	3.3	3.5	V
VDDC	1.70	1.8	1.90	V
DIGITAL SUPPLY VOLTAGES				
VDD33	3.10	3.3	3.5	V
VDD	1.70	1.8	1.90	V
SUPPLY CURRENTS AND POWER DISSIPATION, 2.0 GSPS				
I_{VDDA}		37	38	mA
I_{VDDC}		159	166	mA
I_{VDD33}		34	37	mA
I_{VDD}		233	238	mA
Power Dissipation		0.940	0.975	W
Sleep Mode, I_{VDDA}		2.5	2.75	mA
Power-Down Mode (Register 0x01 = 0x33 and Register 0x02 = 0x80)				
I_{VDDA}		0.02		mA
I_{VDDC}		3.8		mA
I_{VDD33}		0.5		mA
I_{VDD}		0.1		mA
SUPPLY CURRENTS AND POWER DISSIPATION, 2.5 GSPS				
I_{VDDA}		37		mA
I_{VDDC}		223		mA
I_{VDD33}		34		mA
I_{VDD}		290		mA
Power Dissipation		1.16		W

LVDS DIGITAL SPECIFICATIONS

VDDA = VDD33 = 3.3 V, VDDC = VDD = 1.8 V, I_{OUTFS} = 20 mA. LVDS drivers and receivers are compliant to the IEEE Standard 1596.3-1996 reduced range link, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
LVDS DATA INPUTS (DB0[13:0], DB1[13:0])[1]				
Input Common-Mode Voltage Range, V_{COM}	825		1575	mV
Logic High Differential Input Threshold, V_{IH_DTH}	175	400		mV
Logic Low Differential Input Threshold, V_{IL_DTH}	−175	−400		mV
Receiver Differential Input Impedance, R_{IN}	80		120	Ω
Input Capacitance		1.2		pF
LVDS Input Rate	1250			MSPS
LVDS Minimum Data Valid Period, t_{VALID} (See Figure 41)			344	ps
LVDS CLOCK INPUT (DCI and SYNC_IN)[2]				
Input Common-Mode Voltage Range, V_{COM}	825		1575	mV
Logic High Differential Input Threshold, V_{IH_DTH}	175	400		mV
Logic Low Differential Input Threshold, V_{IL_DTH}	−175	−400		mV
Receiver Differential Input Impedance, R_{IN}	80		120	Ω
Input Capacitance		1.2		pF
Maximum Clock Rate	625			MHz
LVDS CLOCK OUTPUT (DCO and SYNC_OUT)[3]				
Output Voltage High (x_P or x_N)			1375	mV
Output Voltage Low (x_P or x_N)	1025			mV
Output Differential Voltage, $\|V_{OD}\|$	150	200	250	mV
Output Offset Voltage, V_{OS}	1150		1250	mV
Output Impedance, Single-Ended, R_O	80	100	120	Ω
R_O Single-Ended Mismatch			10	%
Maximum Clock Rate	625			MHz

[1] DB0[x]P, DB0[x]N, DB1[x]P, and DB1[x]N pins.
[2] DCI_P and DCI_N pins, as well as SYNC_IN_P and SYNC_IN_N pins.
[3] DCO_P and DCO_N pins, as well as SYNC_OUT_P/SYNC_OUT_N pins with 100 Ω differential termination.

SERIAL PORT SPECIFICATIONS

VDDA = VDD33 = 3.3 V, VDDC = VDD = 1.8 V.

Table 3.

Parameter	Min	Typ	Max	Unit
WRITE OPERATION (See Figure 36)				
SCLK Clock Rate, f_{SCLK} (or /t_{SCLK})			20	MHz
SCLK Clock High, t_{HI}	18			ns
SCLK Clock Low, t_{LOW}	18			ns
SDIO to SCLK Setup Time, t_{DS}	2			ns
SCLK to SDIO Hold Time, t_{DH}	1			ns
$\overline{CS}$ to SCLK Setup Time, t_S	3			ns
SCLK to $\overline{CS}$ Hold Time, t_H	2			ns
READ OPERATION (See Figure 37 and Figure 38)				
SCLK Clock Rate, f_{SCLK} (or /t_{SCLK})			20	MHz
SCLK Clock High, t_{HI}	18			ns
SCLK Clock Low, t_{LOW}	18			ns
SDIO to SCLK Setup Time, t_{DS}	2			ns
SCLK to SDIO Hold Time, t_{DH}	1			ns
$\overline{CS}$ to SCLK Setup Time, t_S	3			ns
SCLK to SDIO (or SDO) Data Valid Time, t_{DV}			15	ns
$\overline{CS}$ to SDIO (or SDO) Output Valid to High-Z, t_{EZ}		2		ns
INPUTS (SDIO, SCLK, $\overline{CS}$)				
Voltage in High, V_{IH}	2.0	3.3		V
Voltage in Low, V_{IL}		0	0.8	V
Current in High, I_{IH}	−10		+10	µA
Current in Low, I_{IL}	−10		+10	µA
OUTPUT (SDIO)				
Voltage Out High, V_{OH}	2.4		3.5	V
Voltage Out Low, V_{OL}	0		0.4	V
Current Out High, I_{OH}		4		mA
Current Out Low, I_{OL}		4		mA

AC SPECIFICATIONS

VDDA = VDD33 = 3.3 V, VDDC = VDD = 1.8 V, I_{OUTFS} = 20 mA, f_{DAC} = 2400 MSPS.

Table 4.

Parameter	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE				
DAC Clock Rate	800		2500	MSPS
Adjusted DAC Update Rate[1]	800		2500	MSPS
Output Settling Time (t_{st}) to 0.1%		13		ns
SPURIOUS-FREE DYNAMIC RANGE (SFDR)				
f_{OUT} = 100 MHz		69.5		dBc
f_{OUT} = 350 MHz		58.5		dBc
f_{OUT} = 550 MHz		54		dBc
f_{OUT} = 950 MHz		60		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD), $f_{OUT2} = f_{OUT1} + 1.25$ MHz				
f_{OUT} = 100 MHz		94		dBc
f_{OUT} = 350 MHz		78		dBc
f_{OUT} = 550 MHz		72		dBc
f_{OUT} = 950 MHz		68		dBc
NOISE SPECTRAL DENSITY (NSD), 0 dBFS SINGLE TONE				
f_{OUT} = 100 MHz		−166		dBm/Hz
f_{OUT} = 350 MHz		−161		dBm/Hz
f_{OUT} = 550 MHz		−160		dBm/Hz
f_{OUT} = 850 MHz		−160		dBm/Hz
WCDMA ACLR (SINGLE CARRIER), ADJACENT/ALTERNATE ADJACENT CHANNEL				
f_{DAC} = 2457.6 MSPS f_{OUT} = 350 MHz		80/80		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 950 MHz		78/79		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 1700 MHz (Mix Mode)		74/74		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 2100 MHz (Mix Mode)		69/72		dBc

[1] Adjusted DAC updated rate is calculated as f_{DAC} divided by the minimum required interpolation factor. For the AD9739, the minimum interpolation factor is 1. Thus, with f_{DAC} = 2500 MSPS, f_{DAC} adjusted = 2500 MSPS.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	With Respect To	Rating
VDDA	VSSA	−0.3 V to +3.6 V
VDD33	VSS	−0.3 V to +3.6 V
VDD	VSS	−0.3 V to +1.98 V
VDDC	VSSC	−0.3 V to +1.98 V
VSSA	VSS	−0.3 V to +0.3 V
VSSA	VSSC	−0.3 V to +0.3 V
VSS	VSSC	−0.3 V to +0.3 V
DACCLK_P, DACCLK_N	VSSC	−0.3 V to VDDC + 0.18 V
DCI, DCO, SYNC_IN, SYNC_OUT	VSS	−0.3 V to VDD33 + 0.3 V
LVDS Data Inputs	VSS	−0.3 V to VDD33 + 0.3 V
IOUTP, IOUTN	VSSA	−1.0 V to VDDA + 0.3 V
I120, VREF	VSSA	−0.3 V to VDDA + 0.3 V
IRQ, $\overline{CS}$, SCLK, SDO, SDIO, RESET	VSS	−0.3 V to VDD33 + 0.3 V
Junction Temperature		150°C
Storage Temperature		−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
160-Ball CSP_BGA	31.2	7.0	°C/W[1]

[1] With no airflow movement.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

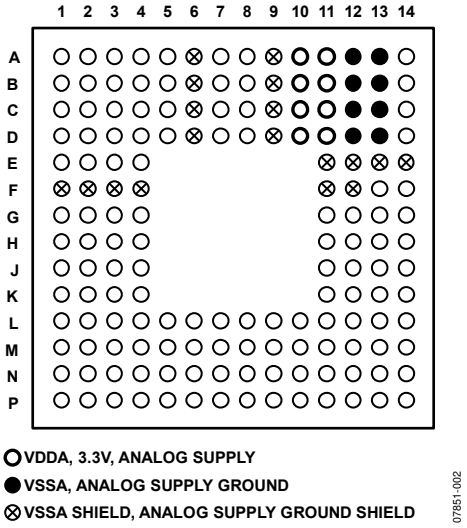


Figure 2. Analog Supply Pins (Top View)

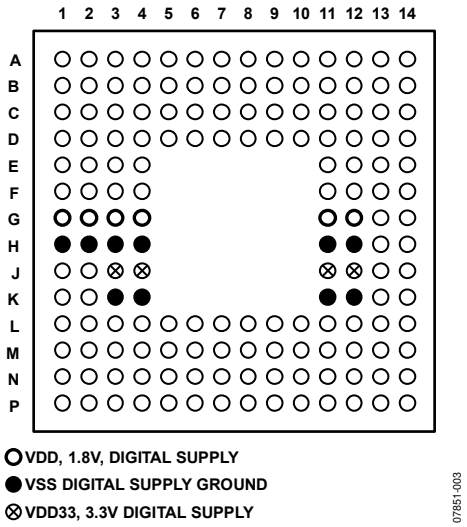


Figure 3. Digital Supply Pins (Top View)

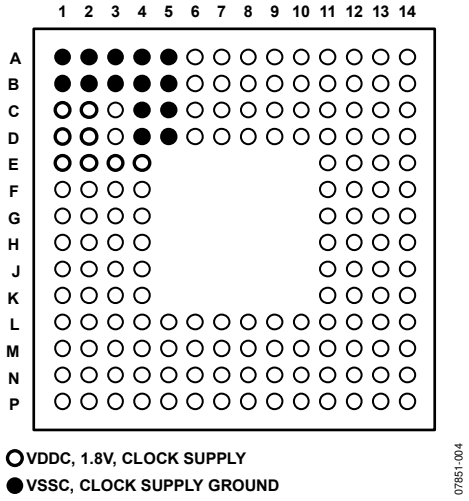


Figure 4. Digital LVDS Clock Supply Pins (Top View)

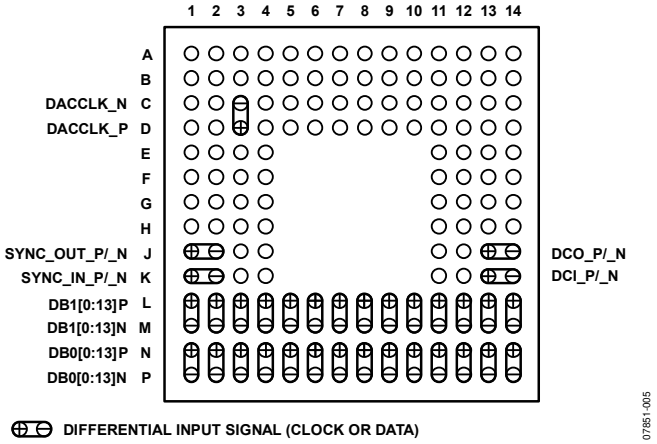


Figure 5. Digital LVDS Input, Clock I/O (Top View)

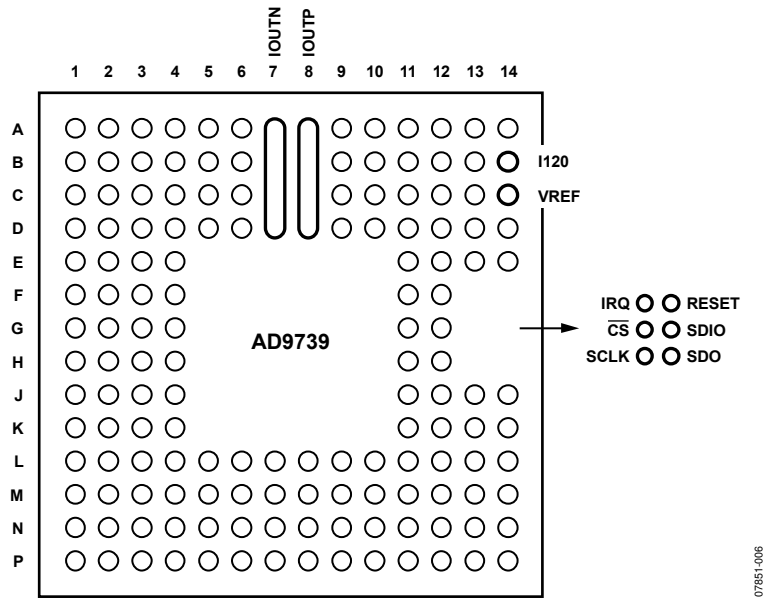


Figure 6. Analog I/O and SPI Control Pins (Top View)

Table 7. AD9739 Pin Function Descriptions

Pin No.	Mnemonic	Description
C1, C2, D1, D2, E1, E2, E3, E4	VDDC	1.8 V Clock Supply Input.
A1, A2, A3, A4, A5, B1, B2, B3, B4, B5, C4, C5, D4, D5	VSSC	Clock Supply Return.
A10, A11, B10, B11, C10, C11, D10, D11	VDDA	3.3 V Analog Supply Input.
A12, A13, B12, B13, C12, C13, D12, D13,	VSSA	Analog Supply Return.
A6, A9, B6, B9, C6, C9, D6, D9, F1, F2, F3, F4, E11, E12, E13, E14, F11, F12	VSSA Shield	Analog Supply Return Shield. Tie to VSSA at the DAC.
A14	NC	No Connect. Do not connect to this pin.
A7, B7, C7, D7	IOUTN	DAC Negative Current Output Source.
A8, B8, C8, D8	IOUTP	DAC Positive Current Output Source.
B14	I120	Nominal 1.2 V Reference. Tie to analog ground via a 10 kΩ resistor to generate a 120 µA reference current.
C14	VREF	Voltage Reference Input/Output. Decouple to VSSA with a 1 nF capacitor.
D14	NC	Factory Test Pin. Do not connect to this pin.
C3, D3	DACCLK_N/DACCLK_P	Negative/Positive DAC Clock Input (DACCLK).
F13	IRQ	Interrupt Request Open Drain Output. Active high. Pull up to VDD33 with a 10 kΩ resistor.
F14	RESET	Reset Input. Active high. Tie to VSS if unused.
G13	$\overline{CS}$	Serial Port Enable Input.
G14	SDIO	Serial Port Data Input/Output.
H13	SCLK	Serial Port Clock Input.
H14	SDO	Serial Port Data Output.
J3, J4, J11, J12	VDD33	3.3 V Digital Supply Input.
G1, G2, G3, G4, G11, G12	VDD	1.8 V Digital Supply. Input.
H1, H2, H3, H4, H11, H12, K3, K4, K11, K12	VSS	Digital Supply Return.
J1, J2	SYNC_OUT_P/SYNC_OUT_N	Positive/Negative SYNC Output (SYNC_OUT)
K1, K2	SYNC_IN_P/SYNC_IN_N	Positive/Negative SYNC Input (SYNC_IN)
J13, J14	DCO_P/DCO_N	Positive/Negative Data Clock Output (DCO).
K13, K14	DCI_P/DCI_N	Positive/Negative Data Clock Input (DCI).
L1, M1	DB1[0]P/DB1[0]N	Port 1 Positive/Negative Data Input Bit 0.
L2, M2	DB1[1]P/DB1[1]N	Port 1 Positive/Negative Data Input Bit 1.
L3, M3	DB1[2]P/DB1[2]N	Port 1 Positive/Negative Data Input Bit 2.

Pin No.	Mnemonic	Description
L4, M4	DB1[3]P/DB1[3]N	Port 1 Positive/Negative Data Input Bit 3.
L5, M5	DB1[4]P/DB1[4]N	Port 1 Positive/Negative Data Input Bit 4.
L6, M6	DB1[5]P/DB1[5]N	Port 1 Positive/Negative Data Input Bit 5.
L7, M7	DB1[6]P/DB1[6]N	Port 1 Positive/Negative Data Input Bit 6.
L8, M8	DB1[7]P/DB1[7]N	Port 1 Positive/Negative Data Input Bit 7.
L9, M9	DB1[8]P/DB1[8]N	Port 1 Positive/Negative Data Input Bit 8.
L10, M10	DB1[9]P/DB1[9]N	Port 1 Positive/Negative Data Input Bit 9.
L11, M11	DB1[10]P/DB1[10]N	Port 1 Positive/Negative Data Input Bit 10.
L12, M12	DB1[11]P/DB1[11]N	Port 1 Positive/Negative Data Input Bit 11.
L13, M13	DB1[12]P/DB1[12]N	Port 1 Positive/Negative Data Input Bit 12.
L14, M14	DB1[13]P/DB1[13]N	Port 1 Positive/Negative Data Input Bit 13.
N1, P1	DB0[0]P/DB0[0]N	Port 0 Positive/Negative Data Input Bit 0.
N2, P2	DB0[1]P/DB0[1]N	Port 0 Positive/Negative Data Input Bit 1.
N3, P3	DB0[2]P/DB0[2]N	Port 0 Positive/Negative Data Input Bit 2.
N4, P4	DB0[3]P/DB0[3]N	Port 0 Positive/Negative Data Input Bit 3.
N5, P5	DB0[4]P/DB0[4]N	Port 0 Positive/Negative Data Input Bit 4.
N6, P6	DB0[5]P/DB0[5]N	Port 0 Positive/Negative Data Input Bit 5.
N7, P7	DB0[6]P/DB0[6]N	Port 0 Positive/Negative Data Input Bit 6.
N8, P8	DB0[7]P/DB0[7]N	Port 0 Positive/Negative Data Input Bit 7.
N9, P9	DB0[8]P/DB0[8]N	Port 0 Positive/Negative Data Input Bit 8.
N10, P10	DB0[9]P/DB0[9]N	Port 0 Positive/Negative Data Input Bit 9.
N11, P11	DB0[10]P/DB0[10]N	Port 0 Positive/Negative Data Input Bit 10.
N12, P12	DB0[11]P/DB0[11]N	Port 0 Positive/Negative Data Input Bit 11.
N13, P13	DB0[12]P/DB0[12]N	Port 0 Positive/Negative Data Input Bit 12.
N14, P14	DB0[13]P/DB0[13]N	Port 0 Positive/Negative Data Input Bit 13.

TYPICAL PERFORMANCE CHARACTERISTICS

AC (NORMAL MODE)

I_{OUTFS} = 20 mA, nominal supplies, 25°C, unless otherwise noted.

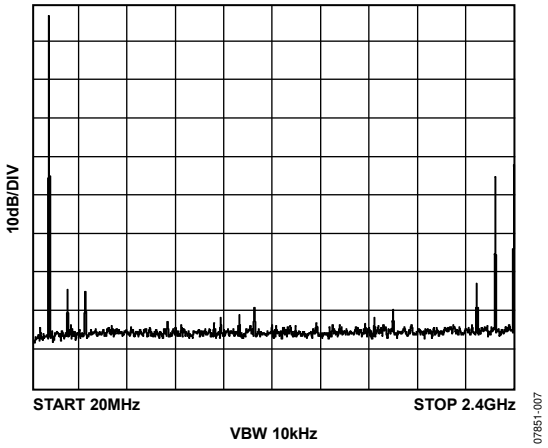


Figure 7. Single-Tone Spectrum at f_{OUT} = 91 MHz, f_{DAC} = 2.4 GSPS

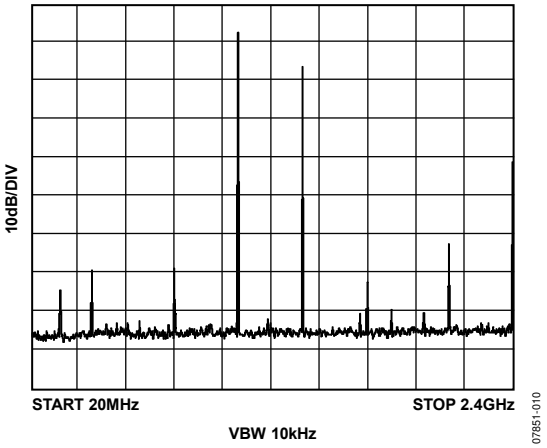


Figure 10. Single-Tone Spectrum at f_{OUT} = 1091 MHz, f_{DAC} = 2.4 GSPS

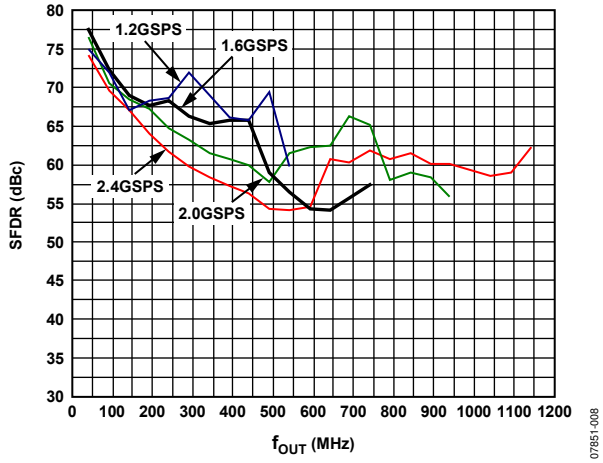


Figure 8. SFDR vs. f_{OUT} over f_{DAC}

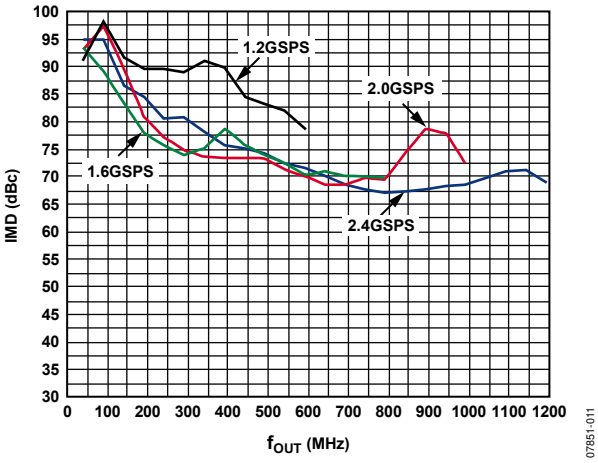


Figure 11. IMD vs. f_{OUT} over f_{DAC}

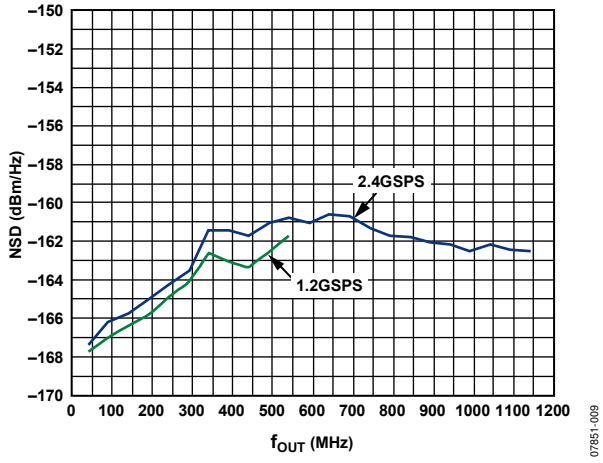


Figure 9. Single-Tone NSD over f_{OUT}

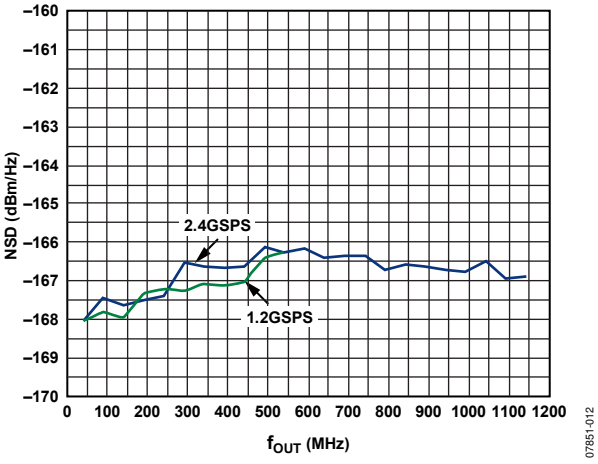


Figure 12. Eight-Tone NSD over f_{OUT}

f_{DAC} = 2 GSPS, I_{OUTFS} = 20 mA, nominal supplies, 25°C, unless otherwise noted.

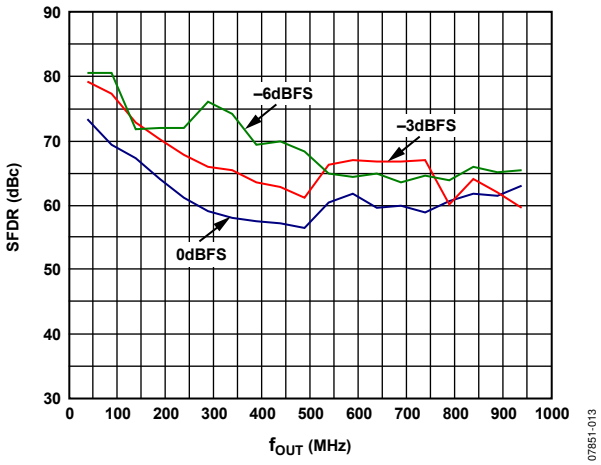


Figure 13. SFDR vs. f_{OUT} over Digital Full Scale

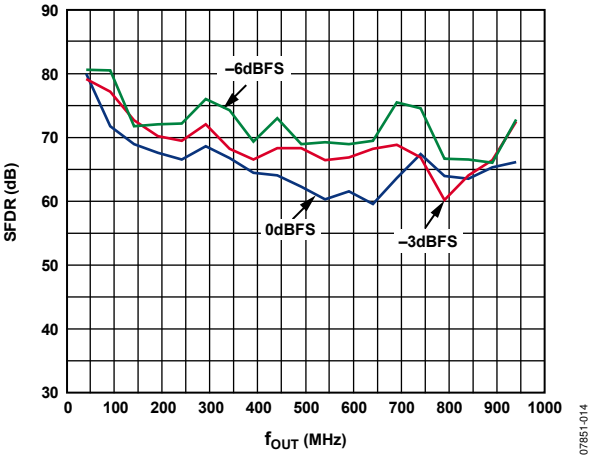


Figure 14. SFDR for Second Harmonic over f_{OUT} vs. Digital Full Scale

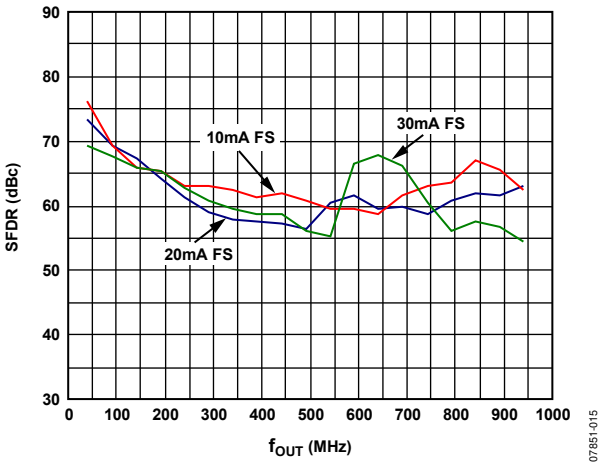


Figure 15. SFDR vs. f_{OUT} over DAC I_{OUTFS}

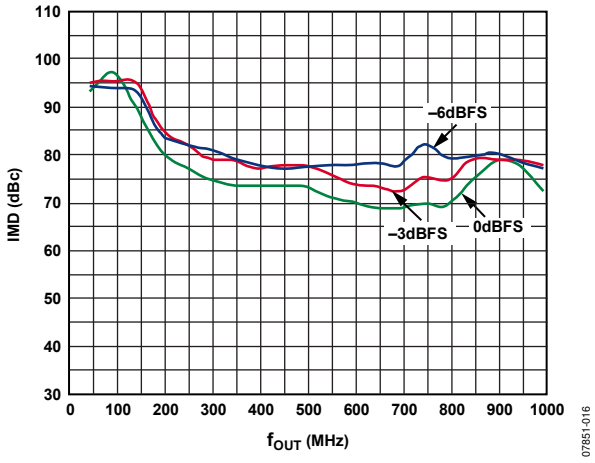


Figure 16. IMD vs. f_{OUT} over Digital Full Scale

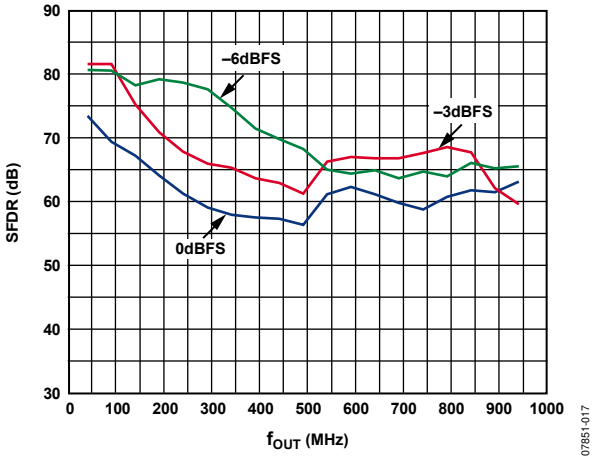


Figure 17. SFDR for Third Harmonic over f_{OUT} vs. Digital Full Scale

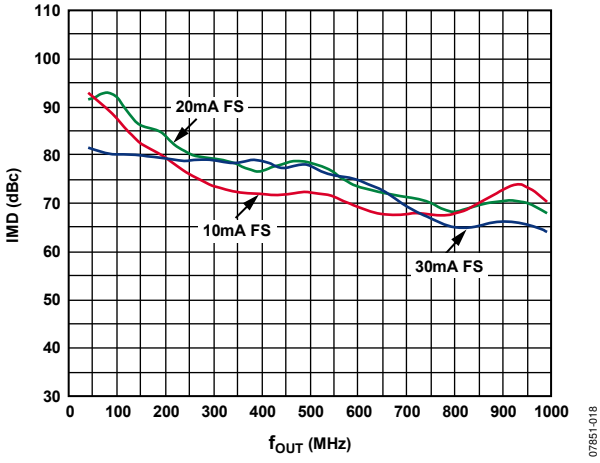


Figure 18. IMD vs. f_{OUT} over DAC I_{OUTFS}

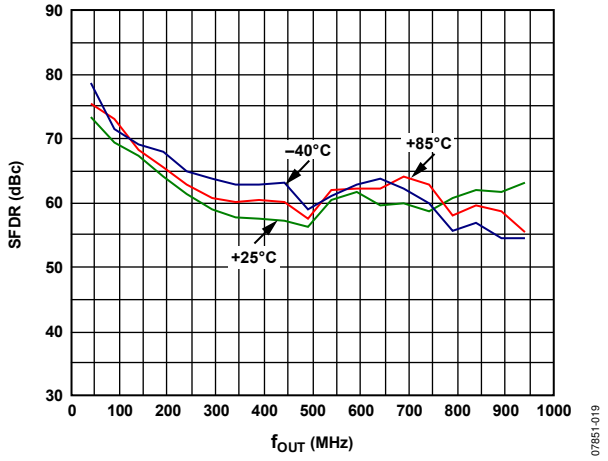


Figure 19. SFDR vs. f_{OUT} over Temperature

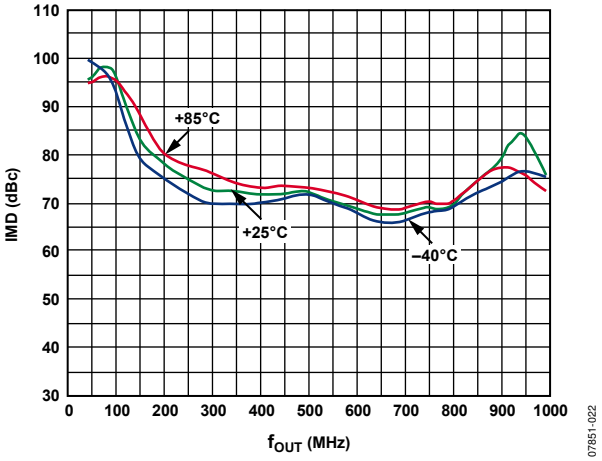


Figure 22. IMD vs. f_{OUT} over Temperature

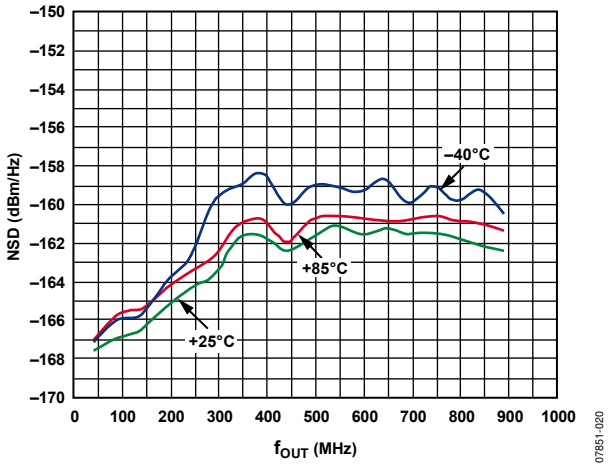


Figure 20. Single-Tone NSD vs. f_{OUT} over Temperature

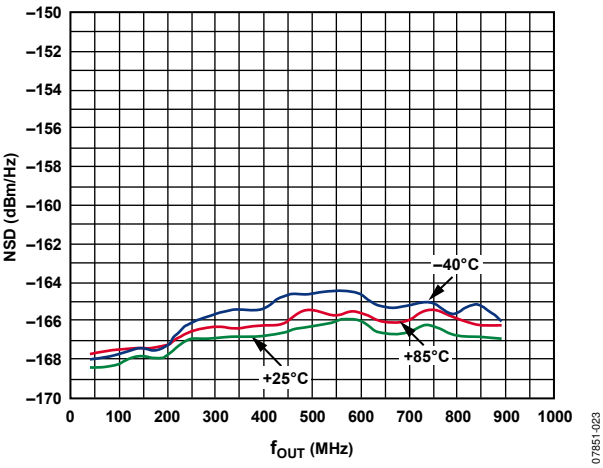
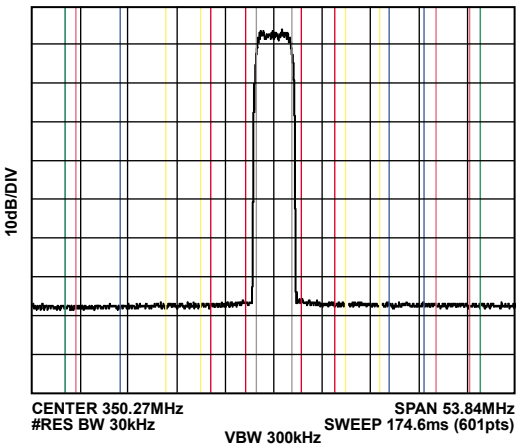


Figure 23. Eight-Tone NSD vs. f_{OUT} over Temperature



RMS RESULTS CARRIER POWER	FREQ OFFSET (MHz)	REF BW (MHz)	LOWER (dBc)	LOWER (dBm)	UPPER (dBc)	UPPER (dBm)
–14.54dBm/ 3.84MHz	5	3.84	–79.90	–94.44	–79.03	–93.57
	10	3.84	–80.60	–95.14	–79.36	–94.40
	15	3.84	–80.90	–95.45	–80.73	–95.27
	20	3.84	–80.62	–95.16	–80.97	–95.51
	25	3.84	–80.76	–95.30	–80.95	–95.49

Figure 21. Single-Carrier WCDMA at 350 MHz, f_{DAC} = 2457.6 MSPS

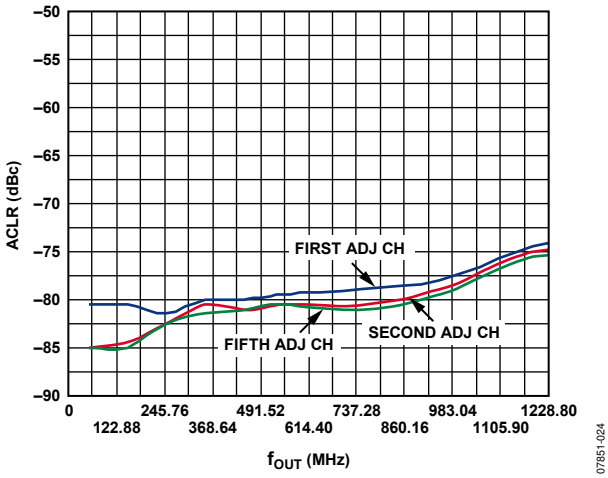


Figure 24. Four-Carrier WCDMA at 350 MHz, f_{DAC} = 2457.6 MSPS

AC (MIX MODE)

f_{DAC} = 2.4 GSPS, I_{OUTFS} = 20 mA, nominal supplies, 25°C, unless otherwise noted.

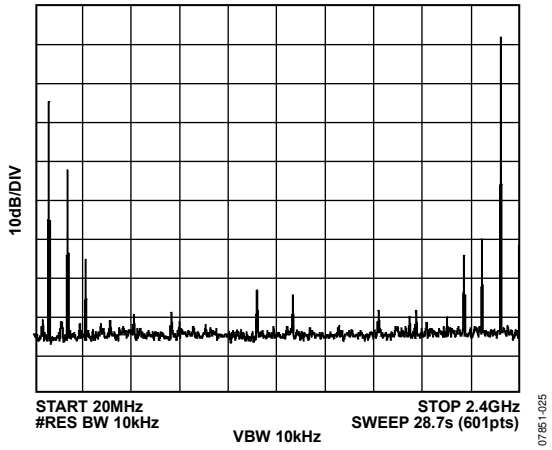


Figure 25. Single-Tone Spectrum at f_{OUT} = 2.31 GHz, f_{DAC} = 2.4 GSPS

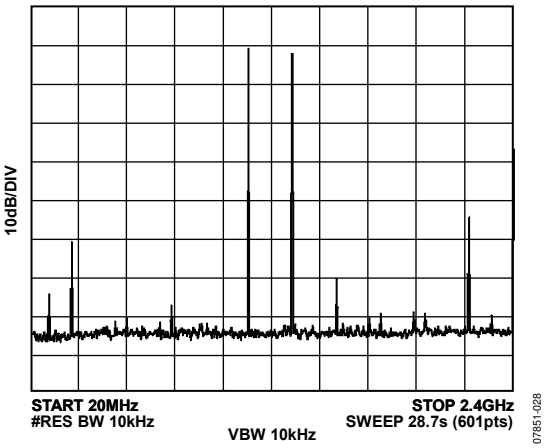


Figure 28. Single-Tone Spectrum in Mix Mode at f_{OUT} = 1.31 GHz, f_{DAC} = 2.4 GSPS

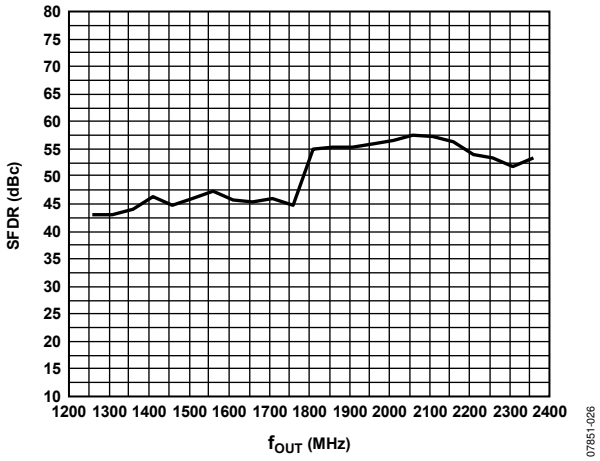


Figure 26. SFDR in Mix Mode vs. f_{OUT} at 2.4 GSPS

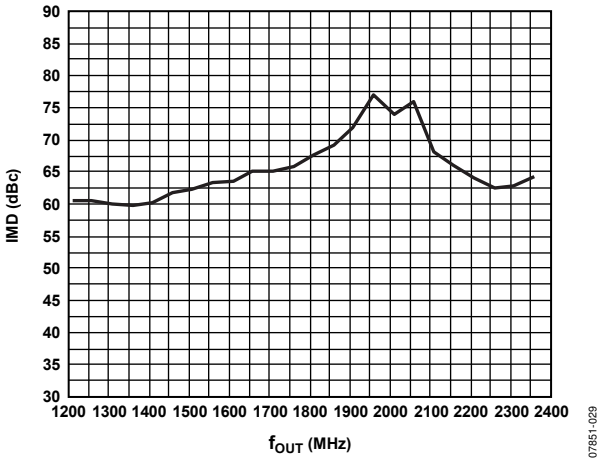


Figure 29. IMD in Mix Mode vs. f_{OUT} at 2.4 GSPS

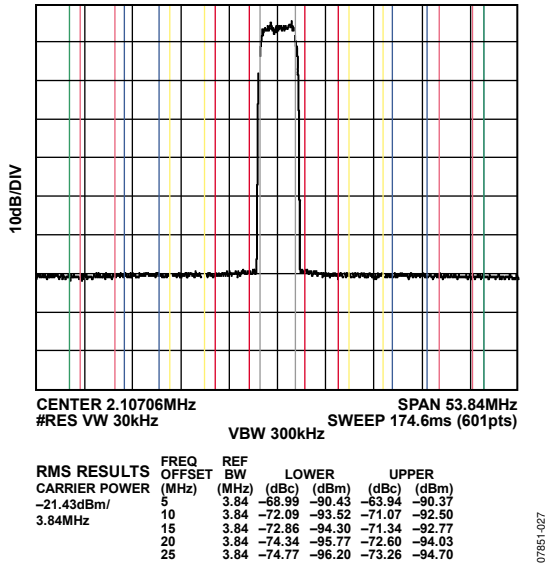


Figure 27. Typical Single-Carrier WCDMA ACLR Performance at 2.1 GHz, f_{DAC} = 2457.6 MSPS (Second Nyquist Zone)

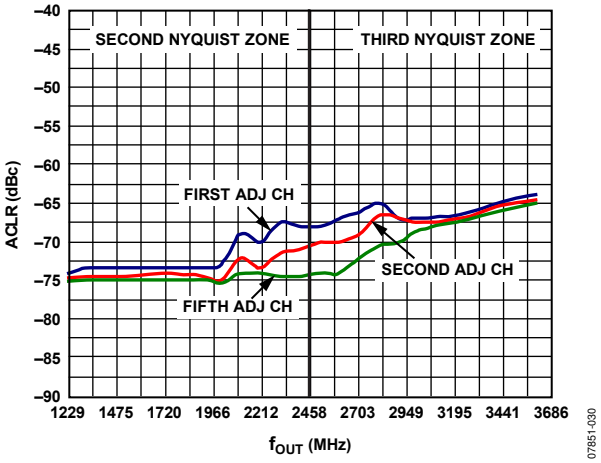
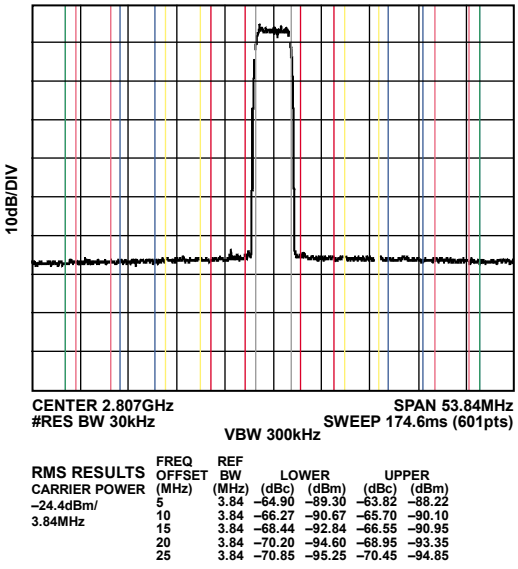
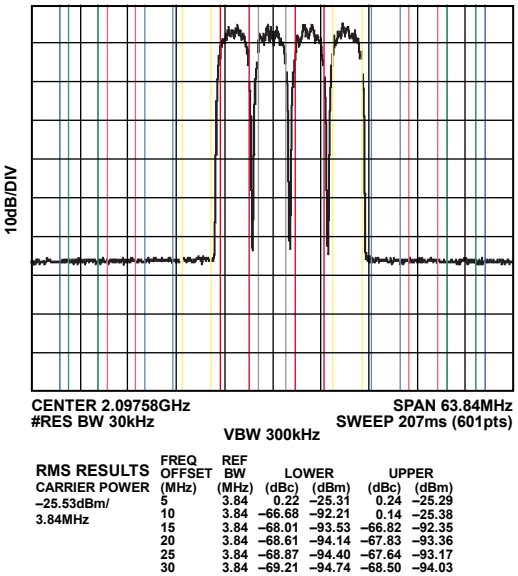


Figure 30. Single-Carrier WCDMA ACLR vs. f_{OUT} at 2457.6 MSPS



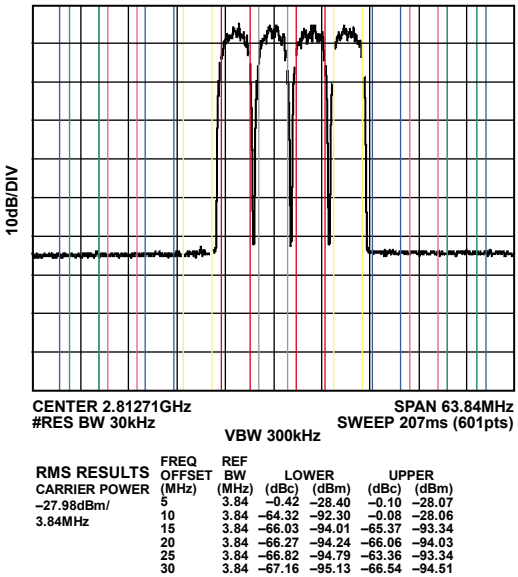
RMS RESULTS CARRIER POWER	FREQ OFFSET (MHz)	REF BW (MHz)	LOWER (dBc)	LOWER (dBm)	UPPER (dBc)	UPPER (dBm)
–24.4dBm/ 3.84MHz	5	3.84	–64.90	–89.30	–63.82	–88.22
	10	3.84	–66.27	–90.67	–65.70	–90.10
	15	3.84	–68.44	–92.84	–66.55	–90.95
	20	3.84	–70.20	–94.60	–68.95	–93.35
	25	3.84	–70.85	–95.25	–70.45	–94.85

Figure 31. Typical Single-Carrier WCDMA ACLR Performance at 2.8 GHz, f_{DAC} = 2457.6 MSPS (Third Nyquist Zone)



RMS RESULTS CARRIER POWER	FREQ OFFSET (MHz)	REF BW (MHz)	LOWER (dBc)	LOWER (dBm)	UPPER (dBc)	UPPER (dBm)
–25.53dBm/ 3.84MHz	5	3.84	0.22	–25.31	0.24	–25.29
	10	3.84	–66.68	–92.21	0.14	–25.38
	15	3.84	–68.01	–93.53	–66.82	–92.35
	20	3.84	–68.61	–94.14	–67.83	–93.36
	25	3.84	–68.87	–94.40	–67.64	–93.17
	30	3.84	–69.21	–94.74	–68.50	–94.03

Figure 32. Typical Four-Carrier WCDMA ACLR Performance at 2.1 GHz, f_{DAC} = 2457.6 MSPS (Second Nyquist Zone)



RMS RESULTS CARRIER POWER	FREQ OFFSET (MHz)	REF BW (MHz)	LOWER (dBc)	LOWER (dBm)	UPPER (dBc)	UPPER (dBm)
–27.98dBm/ 3.84MHz	5	3.84	–0.42	–28.40	–0.10	–28.07
	10	3.84	–64.32	–92.30	–0.08	–28.06
	15	3.84	–66.03	–94.01	–65.37	–93.34
	20	3.84	–66.27	–94.24	–66.06	–94.03
	25	3.84	–66.82	–94.79	–63.36	–93.34
	30	3.84	–67.16	–95.13	–66.54	–94.51

Figure 33. Typical Four-Carrier WCDMA ACLR Performance at 2.8 GHz, f_{DAC} = 2457.6 MSPS (Third Nyquist Zone)

TERMINOLOGY

Linearity Error (Integral Nonlinearity or INL)
The maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from 0 to full scale.

Differential Nonlinearity (DNL)
The measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of 0 is called the offset error. For IOUTP, 0 mA output is expected when the inputs are all 0s. For IOUTN, 0 mA output is expected when all inputs are set to 1.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1 minus the output when all inputs are set to 0.

Output Compliance Range
The range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Power Supply Rejection (PSR)
The maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Spurious-Free Dynamic Range (SFDR)
The difference, in decibels (dB), between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion (THD)
The ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal. It is expressed as a percentage or in decibels (dB).

Noise Spectral Density (NSD)
NSD is the converter noise power per unit of bandwidth. This is usually specified in dBm/Hz in the presence of a 0 dBm full-scale signal.

Adjacent Channel Leakage Ratio (ACLR)
The adjacent channel leakage (power) ratio is a ratio, in dBc, of the measured power within a channel relative to its adjacent channels.

Modulation Error Ratio (MER)
Modulated signals create a discrete set of output values referred to as a constellation. Each symbol creates an output signal corresponding to one point on the constellation. MER is a measure of the discrepancy between the average output symbol magnitude and the rms error magnitude of the individual symbol.

Intermodulation Distortion (IMD)
IMD is the result of two or more signals at different frequencies mixing together. Many products are created according to the formula, aF1 ± bF2, where a and b are integer values.

SERIAL PORT INTERFACE (SPI) REGISTER

SPI REGISTER MAP DESCRIPTION

The AD9739 contains a set of programmable registers described in Table 10 that are used to configure and monitor various internal parameters. Note the following points when programming the AD9739 SPI registers:

- Registers pertaining to similar functions are grouped together and assigned adjacent addresses.
- Bits that are undefined within a register should be assigned a 0 when writing to that register.
- Registers that are undefined should not be written to.
- A hardware or software reset is recommended upon power-up to place SPI registers in a known state.
- A SPI initialization routine is required as part of the boot process. See Table 31 and Table 32 for example procedures.

Reset

Issuing a hardware or software reset places the AD9739 SPI registers in a known state. All SPI registers (excluding 0x00) are set to their default states as described in Table 10 upon issuing a reset. After issuing a reset, the SPI initialization process need only write to registers that are required for the boot process as well as any other register settings that must be modified, depending on the target application.

Although the AD9739 does feature an internal power-on-reset (POR), it is still recommended that a software or hardware reset be implemented shortly after power-up. The internal reset signal is derived from a logical OR operation from the internal POR signal, the RESET pin, and the software reset state. A software reset can be issued via the reset bit (Register 0x00, Bit 5) by toggling the bit high then low. Note that, because the MSB/LSB format may still be unknown upon initial power-up (that is, internal POR is unsuccessful), it is also recommended that the bit settings for Bits[7:5] be mirrored onto Bits[2:0] for the instruction cycle that issues a software reset. A hardware reset can be issued from a host or external supervisory IC by applying a high pulse with a minimum width of 40 ns to the RESET pin (that is, Pin F14). RESET should be tied to VSS if unused.

Table 8. SPI Registers Pertaining to SPI Options

Address (Hex)	Bit	Description
0x00	7	Enable 3-wire SPI
	6	Enable SPI LSB first
	5	Software reset

SPI OPERATION

The serial port of the AD9739 shown in Figure 34 has a 3- or 4-wire SPI capability, allowing read/write access to all registers that configure the device's internal parameters. It provides a flexible, synchronous serial communications port, allowing easy interface to many industry-standard microcontrollers and microprocessors. The 3.3 V serial I/O is compatible with most synchronous transfer formats, including the Motorola® SPI and the Intel® SSR protocols.

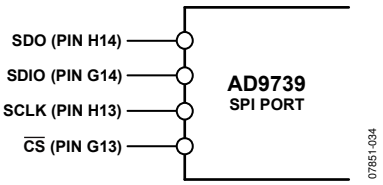


Figure 34. AD9739 SPI Port

The default 4-wire SPI interface consists of a clock (SCLK), serial port enable ($\overline{CS}$), serial data input (SDIO), and serial data output (SDO). The inputs to SCLK, $\overline{CS}$, and SDIO contain a Schmitt trigger with a nominal hysteresis of 0.4 V centered about VDD33/2. The maximum frequency for SCLK is 20 MHz. The SDO pin is active only during the transmission of data and remains three-stated at any other time.

A 3-wire SPI interface can be enabled by setting the SDIO_DIR bit (Register 0x00, Bit 7). This causes the SDIO pin to become bidirectional such that output data only appears on the SDIO pin during a read operation. The SDO pin remains three-stated in a 3-wire SPI interface.

Instruction Header Information

MSB							LSB
17	16	15	14	13	12	11	10
R/$\overline{W}$	A6	A5	A4	A3	A2	A1	A0

An 8-bit instruction header must accompany each read and write operation. The MSB is a R/$\overline{W}$ indicator bit with logic high indicating a read operation. The remaining seven bits specify the address bits to be accessed during the data transfer portion. The eight data bits immediately follow the instruction header for both read and write operations. For write operations, registers change immediately upon writing to the last bit of each transfer byte. $\overline{CS}$ can be raised after each sequence of eight bits (except the last byte) to stall the bus. The serial transfer resumes when $\overline{CS}$ is lowered. Stalling on nonbyte boundaries resets the SPI.

The AD9739 serial port can support both most significant bit (MSB) first and least significant bit (LSB) first data formats. Figure 35 illustrates how the serial port words are formed for the MSB first and LSB first modes. The bit order is controlled by the SDIO_DIR bit (Register 0x00, Bit 7). The default value is 0, MSB first. When the LSB first bit is set high, the serial port interprets both instruction and data bytes LSB first.

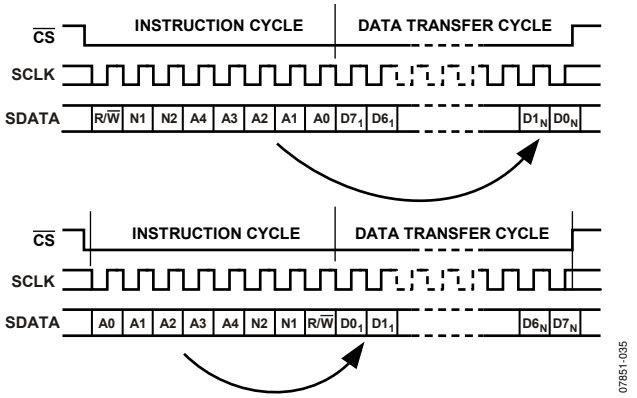


Figure 35. SPI Timing, MSB First (Upper) and LSB First (Lower)

Figure 36 illustrates the timing requirements for a write operation to the SPI port. After the serial port enable ($\overline{CS}$) signal goes low, data (SDIO) pertaining to the instruction header is read on the rising edges of the clock (SCLK). To initiate a write operation, the read/not-write bit is set low. After the instruction header is read, the eight data bits pertaining to the specified register are shifted into the SDIO pin on the rising edge of the next eight clock cycles.

Figure 37 illustrates the timing for a 3-wire read operation to the SPI port. After $\overline{CS}$ goes low, data (SDIO) pertaining to the instruction header is read on the rising edges of SCLK. A read operation occurs if the read/not-write indicator is set high. After the address bits of the instruction header are read, the eight data bits pertaining to the specified register are shifted out of the SDIO pin on the falling edges of the next eight clock cycles.

Figure 38 illustrates the timing for a 4-wire read operation to the SPI port. The timing is similar to the 3-wire read operation with the exception that data appears at the SDO pin only, while the SDIO pin remains at high impedance throughout the operation. The SDO pin is an active output only during the data transfer phase and remains three-stated at all other times.

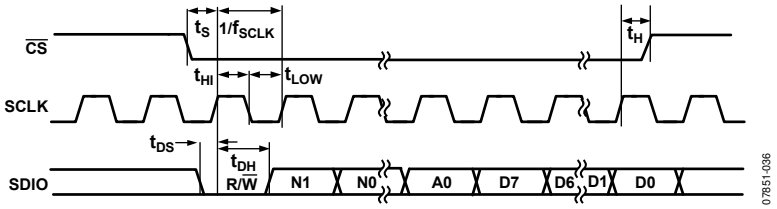


Figure 36. SPI Write Operation Timing

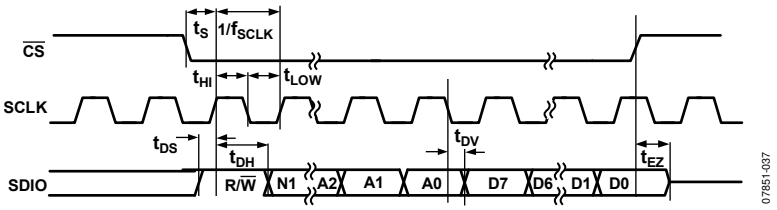


Figure 37. SPI 3-Wire Read Operation Timing

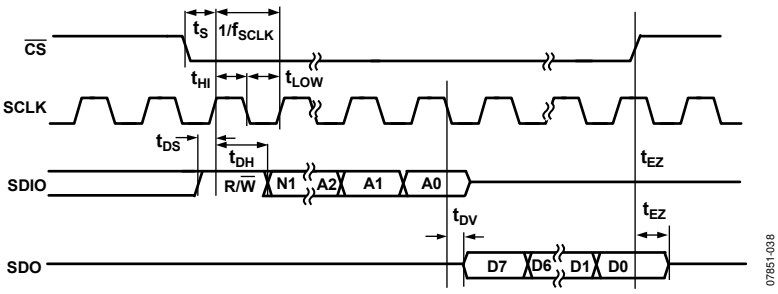


Figure 38. SPI 4-Wire Read Operation Timing

SPI REGISTER MAP

Table 9. Full Register Map (N/A = Not Applicable)

Name	Hex Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
Mode	00	SDIO_DIR	LSB/MSB	Reset	N/A	N/A	N/A	N/A	N/A	0x00
Power-Down	01	N/A	N/A	LVDS_ DRVR_PD	LVDS_ RCVR_PD	N/A	N/A	CLK_ RCVR_PD	DAC_ BIAS_PD	0x00
CNT_ CLK_DIS	02	N/A	N/A	N/A	N/A	CLKGEN_PD	N/A	REC_CNT_ CLK	MU_CNT_ CLK	0x03
IRQ_EN	03	N/A	N/A	SYNC_ LST_EN	SYNC_ LCK_EN	MU_LST_EN	MU_LCK_EN	RCV_ LST_EN	RCV_ LCK_EN	0x00
IRQ_REQ	04	N/A	N/A	SYNC_ LST_IRQ	SYNC_ LCK_IRQ	MU_LST_ IRQ	MU_LCK_ IRQ	RCVLST_ IRQ	RCVLCK_ IRQ	0x00
RSVD	05	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
FSC_1	06	FSC[7]	FSC[6]	FSC[5]	FSC[4]	FSC[3]	FSC[2]	FSC[1]	FSC[0]	0x00
FSC_2	07	Sleep	N/A	N/A	N/A	N/A	N/A	FSC[9]	FSC[8]	0x02
DEC_ CNT	08	N/A	N/A	N/A	N/A	N/A	N/A	DAC_DEC[1]	DAC_DEC[0]	0x00
RSVD	09	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
LVDS_ CNT	0A	N/A	N/A	N/A	N/A	HNDOFF_ CHK_RST	N/A	LVDS_ Bias[1]	LVDS_ Bias[0]	0x00
DIG_ STAT	0B	HNDOFF_ Fall[3]	HNDOFF_ Fall[2]	HNDOFF_ Fall[1]	HNDOFF_ Fall[0]	HNDOFF_ Rise[3]	HNDOFF_ Rise[2]	HNDOFF_ Rise[1]	HNDOFF_ Rise[0]	RNDM
LVDS_ STAT1	0C	SUP/HLD_ Edge1	N/A	DCI_ PHS3	DCI_ PHS1	DCI_PRE_ PH2	DCI_PRE_ PH0	DCI_PST_ PH2	DCI_PST_ PH0	RNDM
LVDS_ STAT2	0D	SUP/HLD_ SYNC	SUP/HLD_ Edge0	SYNC_ SAMP1	SYNC_ SAMP0	LVDS1_HI	LVDS1_LO	LVDS0_HI	LVDS0_LO	RNDM/0
RSVD	0E	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
RSVD	0F	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
LVDS_ REC_ CNT1	10	SYNC_ FLG_RST	SYNC_ LOOP_ON	SYNC_ MST/SLV	SYNC_ CNT_ENA	N/A	RCVR_ FLG_RST	RCVR_ LOOP_ON	RCVR_ CNT_ENA	0x42
LVDS_ REC_ CNT2	11	SMP_DEL[1]	SMP_ DEL[0]	FINE_ DEL_ MID[3]	FINE_ DEL_ MID[2]	FINE_DEL_ MID[1]	FINE_DEL_ MID[0]	RCVR_ GAIN[1]	RCVR_ GAIN[0]	0xDD
LVDS_ REC_ CNT3	12	SMP_DEL[9]	SMP_ DEL[8]	SMP_ DEL[7]	SMP_ DEL[6]	SMP_ DEL[5]	SMP_ DEL[4]	SMP_ DEL[3]	SMP_ DEL[2]	0x29
LVDS_ REC_ CNT4	13	DCI_DEL[3]	DCI_ DEL[2]	DCI_ DEL[1]	DCI_ DEL[0]	FINE_DEL_ SKW[3]	FINE_DEL_ SKW[2]	FINE_DEL_ SKW[1]	FINE_DEL_ SKW[0]	0x71
LVDS_ REC_ CNT5	14	CLKDIVPH[1]	CLKDIVPH[0]	DCI_ DEL[9]	DCI_ DEL[8]	DCI_ DEL[7]	DCI_ DEL[6]	DCI_ DEL[5]	DCI_ DEL[4]	0x0A
LVDS_ REC_ CNT6	15	SYNC_ GAIN[1]	SYNC_ GAIN[0]	SYNCOUT_ PH[1]	SYNCOUT_ PH[0]	LCKTHR[3]	LCKTHR[2]	LCKTHR[1]	LCKTHR[0]	0x42
LVDS_ REC_ CNT7	16	N/A	SYNCO_ DEL[6]	SYNCO_ DEL[5]	SYNCO_ DEL[4]	SYNCO_ DEL[3]	SYNCO_ DEL[2]	SYNCO_ DEL[1]	SYNCO_ DEL[0]	0x00
LVDS_ REC_ CNT8	17	SYNCSH_ DEL[0]	N/A	N/A	N/A	N/A	N/A	N/A	N/A	0x00
LVDS_ REC_ CNT9	18	SYNCSH_ DEL[8]	SYNCSH_ DEL[7]	SYNCSH_ DEL[6]	SYNCSH_ DEL[5]	SYNCSH_ DEL[4]	SYNCSH_ DEL[3]	SYNCSH_ DEL[2]	SYNCSH_ DEL[1]	0x00
LVDS_ REC_ STAT1	19	SMP_DEL[1]	SMP_DEL[0]	N/A	N/A	SMP_ FINE_ DEL[3]	SMP_ FINE_ DEL[2]	SMP_ FINE_ DEL[1]	SMP_ FINE_ DEL[0]	0xC7
LVDS_ REC_ STAT2	1A	SMP_DEL[9]	SMP_ DEL[8]	SMP_ DEL[7]	SMP_ DEL[6]	SMP_ DEL[5]	SMP_ DEL[4]	SMP_ DEL[3]	SMP_ DEL[2]	0x29

Name	Hex Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
LVDS_ REC_ STAT3	1B	DCI_DEL[1]	DCI_DEL[0]	N/A	N/A	SYNCOUT PH[1]	SYNCOUT PH[0]	CLKDIV PH[1]	CLKDIV PH[0]	0xC0
LVDS_ REC_ STAT4	1C	DCI_DEL[9]	DCI_ DEL[8]	DCI_ DEL[7]	DCI_ DEL[6]	DCI_ DEL[5]	DCI_ DEL[4]	DCI_ DEL[3]	DCI_ DEL[2]	0x29
LVDS_ REC_ STAT5	1D	FINE_DEL_ PST[3]	FINE_DEL_ PST[2]	FINE_DEL_ PST[1]	FINE_DEL_ PST[0]	FINE_DEL_ PRE[3]	FINE_DEL_ PRE[2]	FINE_DEL_ PRE[1]	FINE_DEL_ PRE[0]	0x86
LVDS_ REC_ STAT6	1E	N/A	SYNCO_ DEL[6]	SYNCO_ DEL[5]	SYNCO_ DEL[4]	SYNCO_ DEL[3]	SYNCO_ DEL[2]	SYNCO_ DEL[1]	SYNCO_ DEL[0]	0x00
LVDS_ REC_ STAT7	1F	SYNCSH_ DEL[0]	N/A	N/A	N/A	N/A	N/A	N/A	N/A	0x00
LVDS_ REC_ STAT8	20	SYNCSH_ DEL[8]	SYNCSH_ DEL[7]	SYNCSH_ DEL[6]	SYNCSH_ DEL[5]	SYNCSH_ DEL[4]	SYNCSH_ DEL[3]	SYNCSH_ DEL[2]	SYNCSH_ DEL[1]	0x00
LVDS_ REC_ STAT9	21	SYNC_ TRK_ON	SYNC_ INIT_ON	SYNC_ LST_LCK	SYNC_LCK	RCVR_ TRK_ON	RCVR_ FE_ON	RCVR_LST	RCVR_LCK	0x00
CROSS_ CNT1	22	N/A	N/A	N/A	DIR_P	CLKP_ OFFSET[3]	CLKP_ OFFSET[2]	CLKP_ OFFSET[1]	CLKP_ OFFSET[0]	0x00
CROSS_ CNT2	23	N/A	N/A	N/A	DIR_N	CLKN_ OFFSET[3]	CLKN_ OFFSET[2]	CLKN_ OFFSET[1]	CLKN_ OFFSET[0]	0x00
PHS_ DET	24	N/A	N/A	CMP_BST	PHS_DET AUTO_EN	Bias[3]	Bias[2]	Bias[1]	Bias[0]	0x00
MU_ DUTY	25	MU_ DUTYAUTO_EN	POS/NEG	ADJ[5]	ADJ[4]	ADJ[3]	ADJ[2]	ADJ[1]	ADJ[0]	0x00
MU_ CNT1	26	N/A	Slope	Mode[1]	Mode[0]	Read	Gain[1]	Gain[0]	Enable	0x42
MU_ CNT2	27	MUDEL[0]	SRCH_MODE [1]	SRCH_MODE [0]	SET_PHS[4]	SET_PHS[3]	SET_PHS[2]	SET_PHS[1]	SETPHS[0]	0x40
MU_ CNT3	28	MUDEL[8]	MUDEL[7]	MUDEL[6]	MUDEL[5]	MUDEL[4]	MUDEL[3]	MUDEL[2]	MUDEL[1]	0x00
MU_ CNT4	29	SEARCH_TOL	Retry	CONTRST	Guard[4]	Guard[3]	Guard[2]	Guard[1]	Guard[0]	0x0B
MU_ STAT1	2A	N/A	N/A	N/A	N/A	N/A	N/A	MU_LOST	MU_LKD	0x00
RSVD	2B	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
RSVD	2C	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
ANA_ CNT1	32	HDRM[7]	HDRM[6]	HDRM[5]	HDRM[4]	HDRM[3]	HDRM[2]	HDRM[1]	HDRM[0]	0xCA
ANA_ CNT2	33	N/A	N/A	N/A	N/A	N/A	N/A	MSEL[1]	MSEL[0]	0x03
RSVD	34	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
PART ID	35	ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	0x20

SPI PORT CONFIGURATION AND SOFTWARE RESET

Table 10. SPI Port Configuration and Software Reset Register

Address (Hex)	Name	Bit	R/W	Default Setting	Comments
0x00	SDIO_DIR	7	R/W	0	0 = 4-wire SPI, 1 = 3-wire SPI.
	LSB/MSB	6	R/W	0	0 = MSB first, 1 = LSB first.
	Reset	5	R/W	0	Software reset is recommended before modification of other SPI registers from the default setting. Setting the bit to 1 causes all registers (except 0x00) to be set to the default setting. Setting the bit to 0 corresponds to the inactive state, allowing the user to modify registers from the default setting.

POWER-DOWN LVDS INTERFACE AND TXDAC®

Table 11. Power-Down LVDS Interface and TxDAC Register

Address (Hex)	Name	Bit	R/W	Default Setting	Comments
0x01	LVDS_DRVR_PD	5	R/W	0	Power-down of the LVDS drivers/receivers and TxDAC. 0 = enable, 1 = disable.
	LVDS_RCVR_PD	4	R/W	0	
	CLK_RCVR_PD	1	R/W	0	
	DAC_BIAS_PD	0	R/W	0	

CONTROLLER CLOCK DISABLE

Table 12. Controller Clock Disable Register

Address (Hex)	Name	Bit	R/W	Default Setting	Comments
0x02	CLKGEN_PD	3	R/W	0	Internal CLK distribution enable: 0 = enable, 1 = disable.
	REC_CNT_CLK	1	R/W	1	LVDS receiver and Mu controller clock disable. 0 = disable, 1 = enable.
	MU_CNT_CLK	0	R/W	1	

INTERRUPT REQUEST (IRQ) ENABLE/STATUS

Table 13. Interrupt Request (IRQ) Enable/Status Register

Address (Hex)	Name	Bit	R/W	Default Setting	Comments
0x03	SYNC_LST_EN	5	W	0	This register enables the sync, mu, and LVDS Rx controllers to update their corresponding IRQ status bits in Register 0x04, which defines whether the controller is locked (LCK) or unlocked (LST). 0 = disable (resets the status bit). 1 = enable.
	SYNC_LCK_EN	4	W	0	
	MU_LST_EN	3	W	0	
	MU_LCK_EN	2	W	0	
	RCV_LST_EN	1	W	0	
	RCV_LCK_EN	0	W	0	
0x04	SYNC_LST_IRQ	5	R	0	This register indicates the status of the controllers. For LCK_IQR bits: 0 = lost locked, 1 = locked. For LST_IQR bits: 0 = not lost locked, 1 = unlocked. Note that, if the controller IRQ is serviced, the relevant bits in Register 0x03 should be reset by writing 0, followed by another write of 1 to enable.
	SYNC_LCK_IRQ	4	R	0	
	MU_LST_IRQ	3	R	0	
	MU_LCK_IRQ	2	R	0	
	RCV_LST_IRQ	1	R	0	
	RCV_LCK_IRQ	0	R	0	

TxDAC FULL-SCALE CURRENT SETTING (I_{OUTFS}) AND SLEEP

Table 14. TxDAC Full-Scale Current Setting (I_{OUTFS}) and Sleep Register

Address (Hex)	Name	Bit	R/W	Default Setting	Comments
0x06	FSC_1	[7:0]	R/W	0x00	Sets the TxDAC I_{OUTFS} current between 8 mA and 31 mA (default = 20 mA). I_{OUTFS} = 0.0226 × FSC[9:0] + 8.58, where FSC = 0 to 1023.
0x07	FSC_2	[1:0]	R/W	0x02	
	Sleep	7	R/W		0 = enable DAC output, 1 = disable DAC output (sleep).

TxDAC QUAD-SWITCH MODE OF OPERATION

Table 15. TxDAC Quad-Switch Mode of Operation Register

Address (Hex)	Name	Bit	R/W	Default Setting	Comments
0x08	DAC-DEC	[1:0]	R/W	0x00	0x00 = normal baseband mode. 0x01 = return-to-zero mode. 0x02 = mix mode.

DCI PHASE ALIGNMENT STATUS

Table 16. DCI Phase Alignment Status Register

Address (Hex)	Name	Bit	R/W	Default Setting	Comments
0x0C	DCI_PRE_PH0	2	R	0	0 = DCI rising edge is after the PRE delayed version of the Phase 0 sampling edge. 1 = DCI rising edge is before the PRE delayed version of the Phase 0 sampling edge.
	DCI_PST_PH0	0	R	0	0 = DCI rising edge is after the POST delayed version of the Phase 0 sampling edge. 1 = DCI rising edge is before the POST delayed version of the Phase 0 sampling edge.

SYNC_IN PHASE ALIGNMENT STATUS

Table 17. SYNC_IN Phase Alignment Status Register

Address (Hex)	Name	Bit	R/W	Default Setting	Comments
0x0D	SYNC_IN_PH90	5	R	0	0 = SYNCIN rising edge is after Phase 90 sampling edge. 1 = SYNCIN rising edge is before Phase 90 sampling edge.
	SYNC_IN_PH0	4	R	0	0 = SYNCIN rising edge is after Phase 0 sampling edge. 1 = SYNCIN rising edge is before Phase 0 sampling edge.

DATA RECEIVER CONTROLLER CONFIGURATION

Table 18. Data Receiver Controller Configuration Register

Address (Hex)	Name	Bit	R/W	Default Setting	Comments
0x10	SYNC_FLG_RST	7	W	0	Sync controller flag reset. Write 1 followed by 0 to reset flags.
	SYNC_LOOP_ON	6	R/W	1	0 = disable, 1 = enable. Enable for master only. When enabled, sync controller generates an IRQ when master falls out of lock and automatically begins search/track routine.
	SYNC_MST/SLV	5	R/W	0	Sync controller configuration. 0 = slave, 1 = master.
	SYNC_CNT_ENA	4	R/W	0	Sync controller enable. 0 = disable, 1 = enable
	RCVR_FLG_RST	2	W	0	Data receiver controller flag reset. Write 1 followed by 0 to reset flags.
	RCVR_LOOP_ON	1	R/W	1	0 = disable, 1 = enable. When enabled, the data receiver controller generates an IRQ; it falls out of lock and automatically begins a search/track routine.
	RCVR_CNT_ENA	0	R/W	0	Data receiver controller enabled. 0 = disable, 1 = enable.