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Dual, 12-/14-/16-Bit,1 GSPS Digital-to-Analog Converters

AD9776A/AD9778A/AD9779A

FEATURES

Low power: 1.0 W @ 1 GSPS, 600 mW @ 500 MSPS, full operating conditions
Single carrier W-CDMA ACLR = 80 dBc @ 80 MHz IF
Analog output: adjustable 8.7 mA to 31.7 mA, R_L = 25 Ω to 50 Ω
Novel 2×, 4×, and 8× interpolator/coarse complex modulator allows carrier placement anywhere in DAC bandwidth
Auxiliary DACs allow control of external VGA and offset control
Multiple chip synchronization interface
High performance, low noise PLL clock multiplier
Digital inverse sinc filter
100-lead, exposed paddle TQFP

APPLICATIONS

Wireless infrastructure
W-CDMA, CDMA2000, TD-SCDMA, WiMax, GSM, LTE
Digital high or low IF synthesis
Internal digital upconversion capability
Transmit diversity
Wideband communications: LMDS/MMDS, point-to-point

GENERAL DESCRIPTION

The AD9776A/AD9778A/AD9779A are dual, 12-/14-/16-bit, high dynamic range digital-to-analog converters (DACs) that provide a sample rate of 1 GSPS, permitting a multicarrier generation up to the Nyquist frequency. They include features optimized for direct conversion transmission applications, including complex digital modulation and gain and offset compensation. The DAC outputs are optimized to interface seamlessly with analog quadrature modulators such as the ADL537x FMOD series from Analog Devices, Inc. A 3-wire interface provides for programming/readback of many internal parameters. Full-scale output current can be programmed over a range of 10 mA to 30 mA. The devices are manufactured on an advanced 0.18 μm CMOS process and operate on 1.8 V and 3.3 V supplies for a total power consumption of 1.0 W. They are enclosed in a 100-lead thin quad flat package (TQFP).

PRODUCT HIGHLIGHTS

1. Ultralow noise and intermodulation distortion (IMD) enable high quality synthesis of wideband signals from baseband to high intermediate frequencies.
2. A proprietary DAC output switching technique enhances dynamic performance.
3. The current outputs are easily configured for various single-ended or differential circuit topologies.
4. CMOS data input interface with adjustable setup and hold.
5. Novel 2×, 4×, and 8× interpolator/coarse complex modulator allows carrier placement anywhere in DAC bandwidth.

TYPICAL SIGNAL CHAIN

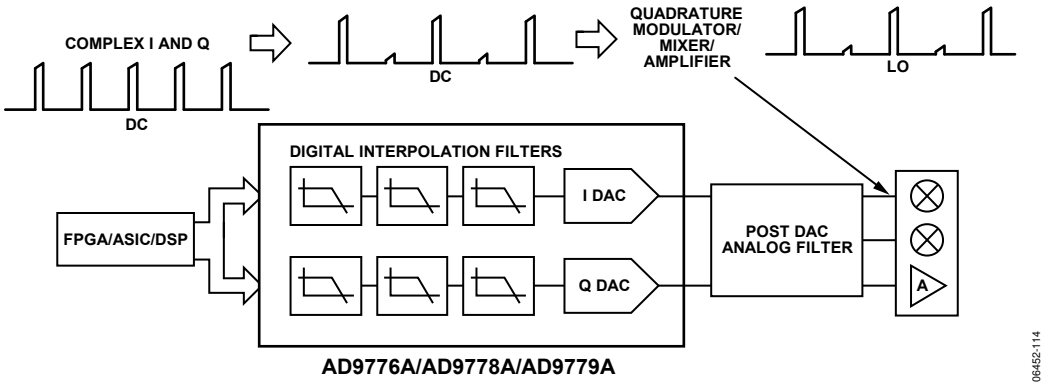

Figure 1.

Rev. B

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Fax: 781.461.3113

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9/08—Rev. A to Rev. B

3/08—Rev. 0 to Rev. A

8/07—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

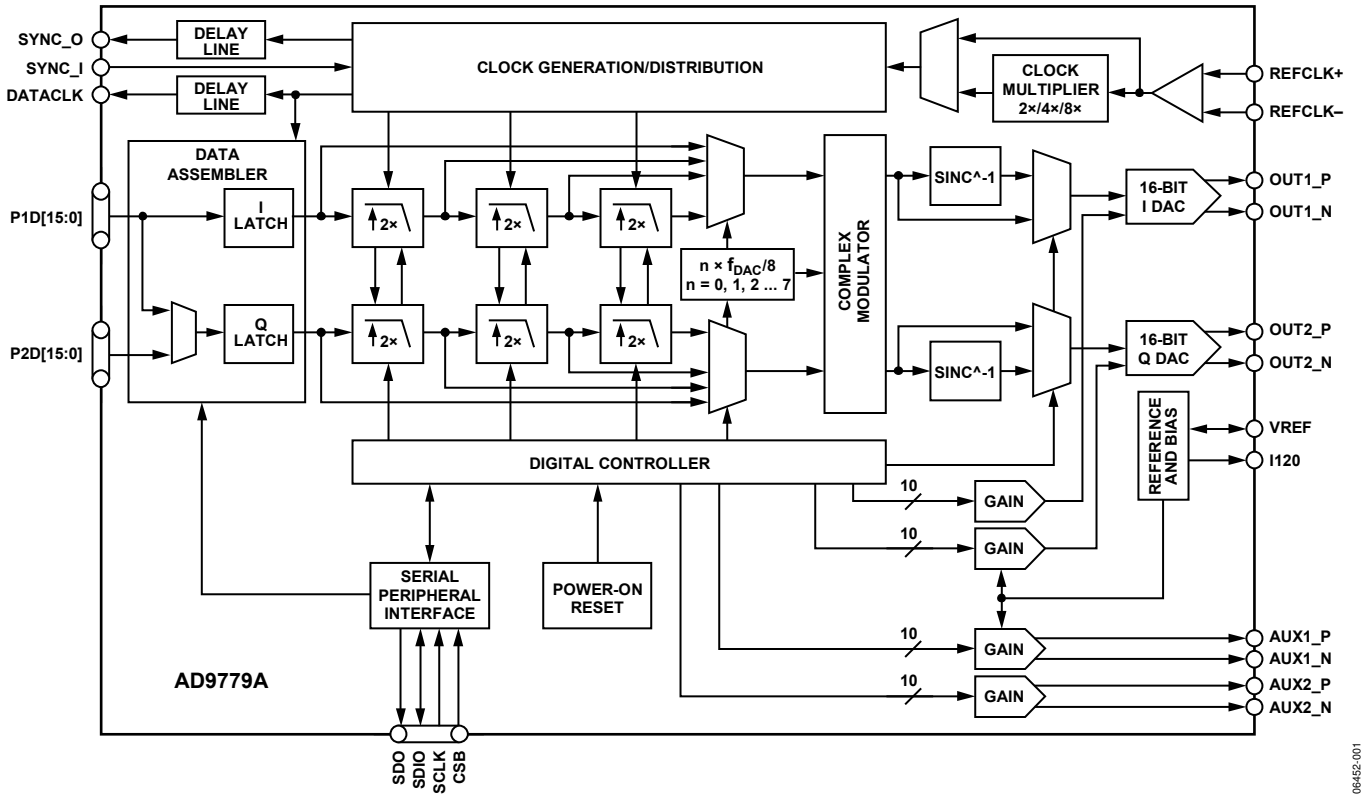

Figure 2. AD9779A Functional Block Diagram

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 1.

	AD9776A			AD9778A			AD9779A			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		12			14			16		Bits
ACCURACY										
Differential Nonlinearity (DNL)		±0.1			±0.65			±2.1		LSB
Integral Nonlinearity (INL)		±0.86			±1.5			±6.0		LSB
MAIN DAC OUTPUTS										
Offset Error	−0.001	0	+0.001	−0.001	0	+0.001	−0.001	0	+0.001	% FSR
Gain Error (with Internal Reference)		±2			±2			±2		% FSR
Full-Scale Output Current[1]	8.66	20.2	31.66	8.66	20.2	31.66	8.66	20.2	31.66	mA
Output Compliance Range	−1.0		+1.0	−1.0		+1.0	−1.0		+1.0	V
Output Resistance		10			10			10		MΩ
Gain DAC Monotonicity		Guaranteed			Guaranteed			Guaranteed		
MAIN DAC TEMPERATURE DRIFT										
Offset		0.04			0.04			0.04		ppm/°C
Gain		100			100			100		ppm/°C
Reference Voltage		30			30			30		ppm/°C
AUXILIARY DAC OUTPUTS										
Resolution		10			10			10		Bits
Full-Scale Output Current[1]	−1.998		+1.998	−1.998		+1.998	−1.998		+1.998	mA
Output Compliance Range (Source)	0		1.6	0		1.6	0		1.6	V
Output Compliance Range (Sink)	0.8		1.6	0.8		1.6	0.8		1.6	V
Output Resistance		1			1			1		MΩ
Auxiliary DAC Monotonicity		Guaranteed			Guaranteed			Guaranteed		
REFERENCE										
Internal Reference Voltage		1.2			1.2			1.2		V
Output Resistance		5			5			5		kΩ
ANALOG SUPPLY VOLTAGES										
AVDD33	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
CVDD18	1.70	1.8	2.05	1.70	1.8	2.05	1.70	1.8	2.05	V
DIGITAL SUPPLY VOLTAGES										
DVDD33	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
DVDD18	1.70	1.8	2.05	1.70	1.8	2.05	1.70	1.8	2.05	V
POWER CONSUMPTION[2]										
1× Mode, f_{DAC} = 100 MSPS, IF = 1 MHz		250	300		250	300		250	300	mW
2× Mode, f_{DAC} = 320 MSPS, IF = 16 MHz, PLL Off		498			498			498		mW
2× Mode, f_{DAC} = 320 MSPS, IF = 16 MHz, PLL On		588			588			588		mW
4× Mode, $f_{DAC}/4$ Modulation, f_{DAC} = 500 MSPS, IF = 137.5 MHz, Q DAC Off		572			572			572		mW
8× Mode, $f_{DAC}/4$ Modulation, f_{DAC} = 1 GSPS, IF = 262.5 MHz		980			980			980		mW
Power-Down Mode		2.5	9.8		2.5	9.8		2.5	9.8	mW
Power Supply Rejection Ratio, AVDD33	−0.3		+0.3	−0.3		+0.3	−0.3		+0.3	% FSR/V
OPERATING RANGE	−40	+25	+85	−40	+25	+85	−40	+25	+85	°C

[1] Based on a 10 kΩ external resistor.
[2] See the Power Dissipation section for more details.

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted. LVDS driver and receiver are compliant to the IEEE-1596 reduced range link, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL					
Input V_{IN} Logic High		2.0			V
Input V_{IN} Logic Low				0.8	V
Maximum Input Data Rate at Interpolation					
1×		300			MSPS
2×		250			MSPS
4×		200			MSPS
8×	DVDD18, CVDD18 = 1.8 V ± 5%	112.5			MSPS
	DVDD18, CVDD18 = 1.9 V ± 5%	125			MSPS
	DVDD18, CVDD18 = 2.0 V ± 2%	137.5			MSPS
CMOS OUTPUT LOGIC LEVEL (DATACLK, PIN 37)[1]					
Output V_{OUT} Logic High		2.4			V
Output V_{OUT} Logic Low				0.4	V
DATACLK Output Duty Cycle	At 250 MHz, into 5 pF load	40	50	60	%
LVDS RECEIVER INPUTS (SYNC_I+, SYNC_I–)	SYNC_I+ = V_{IA}, SYNC_I– = V_{IB}				
Input Voltage Range, V_{IA} or V_{IB}		825		1575	mV
Input Differential Threshold, V_{IDTH}		−100		+100	mV
Input Differential Hysteresis, $V_{IDTHH} - V_{IDTHL}$			20		mV
Receiver Differential Input Impedance, R_{IN}		80		120	Ω
LVDS Input Rate	Additional limits on f_{SYNC_I} apply; see description of Register 0x05, Bits[3:1], in Table 14			250	MSPS
Setup Time, SYNC_I to REFCLK		0.4			ns
Hold Time, SYNC_I to REFCLK		0.55			ns
LVDS DRIVER OUTPUTS (SYNC_O+, SYNC_O–)	SYNC_O+ = V_{OA}, SYNC_O– = V_{OB}, 100 Ω termination				
Output Voltage High, V_{OA} or V_{OB}				1375	mV
Output Voltage Low, V_{OA} or V_{OB}		1025			mV
Output Differential Voltage, $\|V_{OD}\|$		150	200	250	mV
Output Offset Voltage, V_{OS}		1150		1250	mV
Output Impedance, R_O	Single-ended	80	100	120	Ω
DAC CLOCK INPUT (REFCLK+, REFCLK–)					
Differential Peak-to-Peak Voltage		400	800	2000	mV
Common-Mode Voltage		300	400	500	mV
Maximum Clock Rate	DVDD18, CVDD18 = 1.8 V ± 5%, PLL off	900			MHz
	DVDD18, CVDD18 = 1.9 V ± 5%, PLL off	1000			MHz
	DVDD18, CVDD18 = 2.0 V ± 2%, PLL off	1100			MHz
	DVDD18, CVDD18 = 2.0 V ± 2%, PLL on	250			MHz

[1] Specification is at a DATACLK frequency of 100 MHz into a 1 kΩ load, with maximum drive capability of 8 mA. At higher speeds or greater loads, best practice suggests using an external buffer for this signal.

DIGITAL INPUT DATA TIMING SPECIFICATIONS

All modes, −40°C to +85°C.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
INPUT DATA[1]					
Setup Time	Input data to DATACLK	3.0			ns
Hold Time	Input data to DATACLK	−0.05			ns
Setup Time	Input data to REFCLK	−0.80			ns
Hold Time	Input data to REFCLK	3.80			ns
LATENCY					
1× Interpolation	With or without modulation		25		DACCLK cycles
2× Interpolation	With or without modulation		70		DACCLK cycles
4× Interpolation	With or without modulation		146		DACCLK cycles
8× Interpolation	With or without modulation		297		DACCLK cycles
Inverse Sync			18		DACCLK cycles
3-WIRE INTERFACE					
Maximum Clock Rate (SCLK)		40			MHz
Minimum Pulse Width High, t_{PWH}				12.5	ns
Minimum Pulse Width Low, t_{PWL}				12.5	ns
Setup Time, t_{DS}	SDIO to SCLK	2.8			ns
Hold Time, t_{DH}	SDIO to SCLK	0.0			ns
Setup Time, t_{DS}	CSB to SCLK	2.8			ns
Data Valid, t_{DV}	SDO to SCLK	2.0			ns
POWER-UP TIME[2]			260		ms
RESET					
Minimum Pulse Width, High				2	DACCLK cycles

[1] Specified values are with PLL disabled. Timing vs. temperature and data valid keep out windows (that is, the minimum amount of time valid data must be presented to the device to ensure proper sampling) are delineated in Table 28.
[2] Measured from CSB rising edge when Register 0x00, Bit 4, is written from 1 to 0 with the VREF decoupling capacitor equal to 0.1 µF.

AC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 4.

	AD9776A			AD9778A			AD9779A			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SPURIOUS-FREE DYNAMIC RANGE (SFDR)										
f_{DAC} = 100 MSPS, f_{OUT} = 20 MHz		82			82			82		dBc
f_{DAC} = 200 MSPS, f_{OUT} = 50 MHz		81			81			82		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 70 MHz		80			80			80		dBc
f_{DAC} = 800 MSPS, f_{OUT} = 70 MHz		85			85			87		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)										
f_{DAC} = 200 MSPS, f_{OUT} = 50 MHz		87			87			91		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 60 MHz		80			85			85		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 80 MHz		75			81			81		dBc
f_{DAC} = 800 MSPS, f_{OUT} = 100 MHz		75			80			81		dBc
NOISE SPECTRAL DENSITY (NSD), EIGHT-TONE, 500 kHz TONE SPACING										
f_{DAC} = 200 MSPS, f_{OUT} = 80 MHz		−152			−155			−158		dBm/Hz
f_{DAC} = 400 MSPS, f_{OUT} = 80 MHz		−155			−159			−160		dBm/Hz
f_{DAC} = 800 MSPS, f_{OUT} = 80 MHz		−157.5			−160			−161		dBm/Hz
W-CDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER										
f_{DAC} = 491.52 MSPS, f_{OUT} = 100 MHz		76			78			79		dBc
f_{DAC} = 491.52 MSPS, f_{OUT} = 200 MHz		69			73			74		dBc
W-CDMA SECOND ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER										
f_{DAC} = 491.52 MSPS, f_{OUT} = 100 MHz		77.5			80			81		dBc
f_{DAC} = 491.52 MSPS, f_{OUT} = 200 MHz		76			78			78		dBc

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	With Respect To	Rating
AVDD33, DVDD33	AGND, DGND, CGND	−0.3 V to +3.6 V
DVDD18, CVDD18	AGND, DGND, CGND	−0.3 V to +2.1 V
AGND	DGND, CGND	−0.3 V to +0.3 V
DGND	AGND, CGND	−0.3 V to +0.3 V
CGND	AGND, DGND	−0.3 V to +0.3 V
I120, VREF, IPTAT	AGND	−0.3 V to AVDD33 + 0.3 V
OUT1_P, OUT1_N, OUT2_P, OUT2_N, AUX1_P, AUX1_N, AUX2_P, AUX2_N	AGND	−1.0 V to AVDD33 + 0.3 V
P1D[15:0], P2D[15:0]	DGND	−0.3 V to DVDD33 + 0.3 V
DATACLK, TXENABLE	DGND	−0.3 V to DVDD33 + 0.3 V
REFCLK+, REFCLK−	CGND	−0.3 V to CVDD18 + 0.3 V
RESET, IRQ, PLL_LOCK, SYNC_O+, SYNC_O−, SYNC_I+, SYNC_I−, CSB, SCLK, SDIO, SDO	DGND	−0.3 V to DVDD33 + 0.3 V
Junction Temperature		+125°C
Storage Temperature Range		−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

For optimal thermal performance, the exposed paddle (EPAD) should be soldered to the ground plane for the 100-lead, thermally enhanced TQFP package.

Typical θ_{JA} and θ_{JC} are specified for a 4-layer board in still air. Airflow increases heat dissipation, effectively reducing θ_{JA}.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
100-Lead TQFP				
EPAD Soldered	19.1	12.4	7.1	°C/W
EPAD Not Soldered	27.4			°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

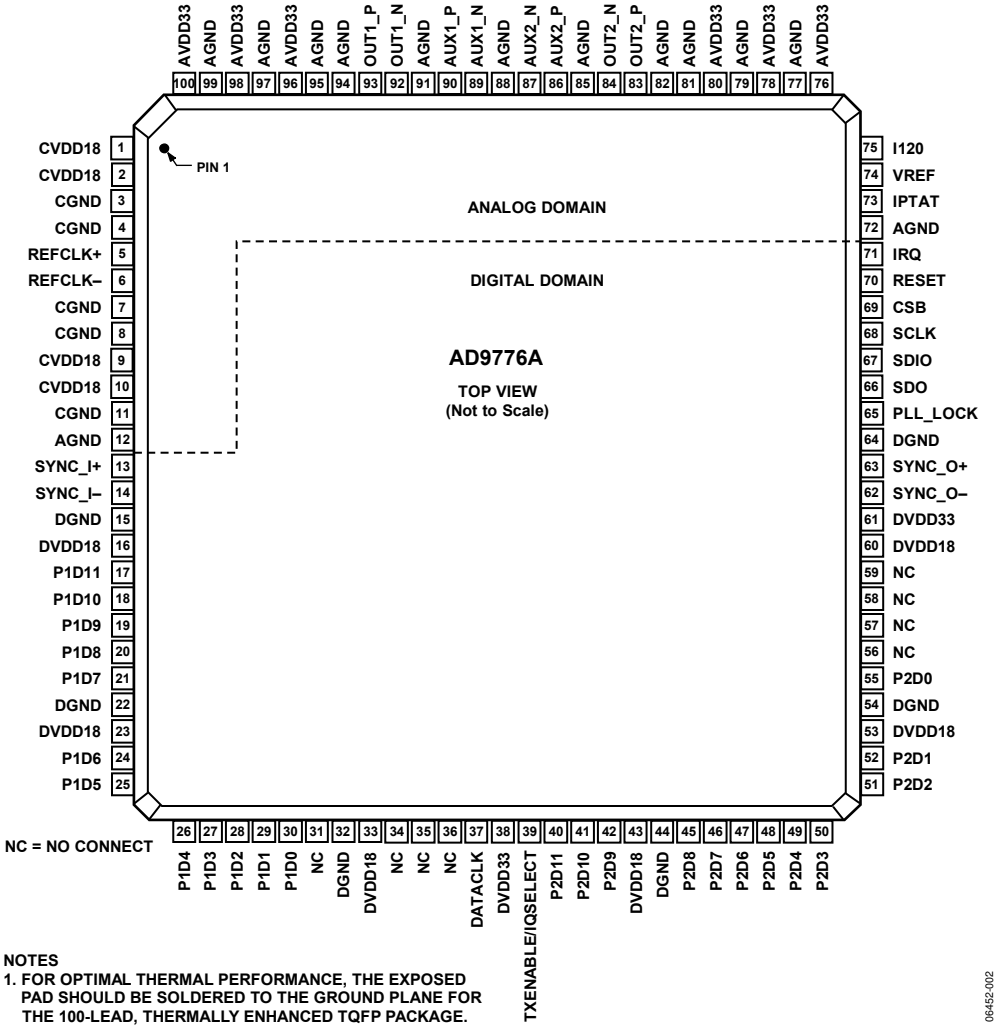

Figure 3. AD9776A Pin Configuration

Table 7. AD9776A Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CVDD18	1.8 V Clock Supply.
2	CVDD18	1.8 V Clock Supply.
3	CGND	Clock Ground.
4	CGND	Clock Ground.
5	REFCLK+	Differential Clock Input.
6	REFCLK–	Differential Clock Input.
7	CGND	Clock Ground.
8	CGND	Clock Ground.
9	CVDD18	1.8 V Clock Supply.
10	CVDD18	1.8 V Clock Supply.
11	CGND	Clock Ground.
12	AGND	Analog Ground.
13	SYNC_I+	Differential Synchronization Input.
14	SYNC_I–	Differential Synchronization Input.
15	DGND	Digital Ground.
16	DVDD18	1.8 V Digital Supply.
17	P1D11	Port 1, Data Input D11 (MSB).
18	P1D10	Port 1, Data Input D10.
19	P1D9	Port 1, Data Input D9.
20	P1D8	Port 1, Data Input D8.
21	P1D7	Port 1, Data Input D7.
22	DGND	Digital Ground.
23	DVDD18	1.8 V Digital Supply.
24	P1D6	Port 1, Data Input D6.
25	P1D5	Port 1, Data Input D5.
26	P1D4	Port 1, Data Input D4.
27	P1D3	Port 1, Data Input D3.
28	P1D2	Port 1, Data Input D2.
29	P1D1	Port 1, Data Input D1.
30	P1D0	Port 1, Data Input D0 (LSB).
31	NC	No Connect.
32	DGND	Digital Ground.

Pin No.	Mnemonic	Description
33	DVDD18	1.8 V Digital Supply.
34	NC	No Connect.
35	NC	No Connect.
36	NC	No Connect.
37	DATACLK	Data Clock Output.
38	DVDD33	3.3 V Digital Supply.
39	TXENABLE/ IQSELECT	Transmit Enable. In single port mode, this pin also functions as IQSELECT.
40	P2D11	Port 2, Data Input D11 (MSB).
41	P2D10	Port 2, Data Input D10.
42	P2D9	Port 2, Data Input D9.
43	DVDD18	1.8 V Digital Supply.
44	DGND	Digital Ground.
45	P2D8	Port 2, Data Input D8.
46	P2D7	Port 2, Data Input D7.
47	P2D6	Port 2, Data Input D6.
48	P2D5	Port 2, Data Input D5.
49	P2D4	Port 2, Data Input D4.
50	P2D3	Port 2, Data Input D3.
51	P2D2	Port 2, Data Input D2.
52	P2D1	Port 2, Data Input D1.
53	DVDD18	1.8 V Digital Supply.
54	DGND	Digital Ground.
55	P2D0	Port 2, Data Input D0 (LSB).
56	NC	No Connect.
57	NC	No Connect.
58	NC	No Connect.
59	NC	No Connect.
60	DVDD18	1.8 V Digital Supply.
61	DVDD33	3.3 V Digital Supply.
62	SYNC_O–	Differential Synchronization Output.
63	SYNC_O+	Differential Synchronization Output.
64	DGND	Digital Ground.
65	PLL_LOCK	PLL Lock Indicator.
66	SDO	3-Wire Interface Port Data Output.
67	SDIO	3-Wire Interface Port Data Input/Output.
68	SCLK	3-Wire Interface Port Clock.
69	CSB	3-Wire Interface Port Chip Select Bar.
70	RESET	Reset, Active High.
71	IRQ	Interrupt Request.
72	AGND	Analog Ground.
73	IPTAT	Factory Test Pin. Output current is proportional to absolute temperature, approximately 14 µA at 25°C with approximately 20 nA/°C slope. This pin should remain floating.
74	VREF	Voltage Reference Output.
75	I120	120 µA Reference Current.
76	AVDD33	3.3 V Analog Supply.
77	AGND	Analog Ground.
78	AVDD33	3.3 V Analog Supply.
79	AGND	Analog Ground.
80	AVDD33	3.3 V Analog Supply.
81	AGND	Analog Ground.
82	AGND	Analog Ground.
83	OUT2_P	Differential DAC Current Output, Channel 2.
84	OUT2_N	Differential DAC Current Output, Channel 2.
85	AGND	Analog Ground.
86	AUX2_P	Auxiliary DAC Current Output, Channel 2.
87	AUX2_N	Auxiliary DAC Current Output, Channel 2.
88	AGND	Analog Ground.
89	AUX1_N	Auxiliary DAC Current Output, Channel 1.
90	AUX1_P	Auxiliary DAC Current Output, Channel 1.
91	AGND	Analog Ground.
92	OUT1_N	Differential DAC Current Output, Channel 1.
93	OUT1_P	Differential DAC Current Output, Channel 1.
94	AGND	Analog Ground.
95	AGND	Analog Ground.
96	AVDD33	3.3 V Analog Supply.
97	AGND	Analog Ground.
98	AVDD33	3.3 V Analog Supply.
99	AGND	Analog Ground.
100	AVDD33	3.3 V Analog Supply.

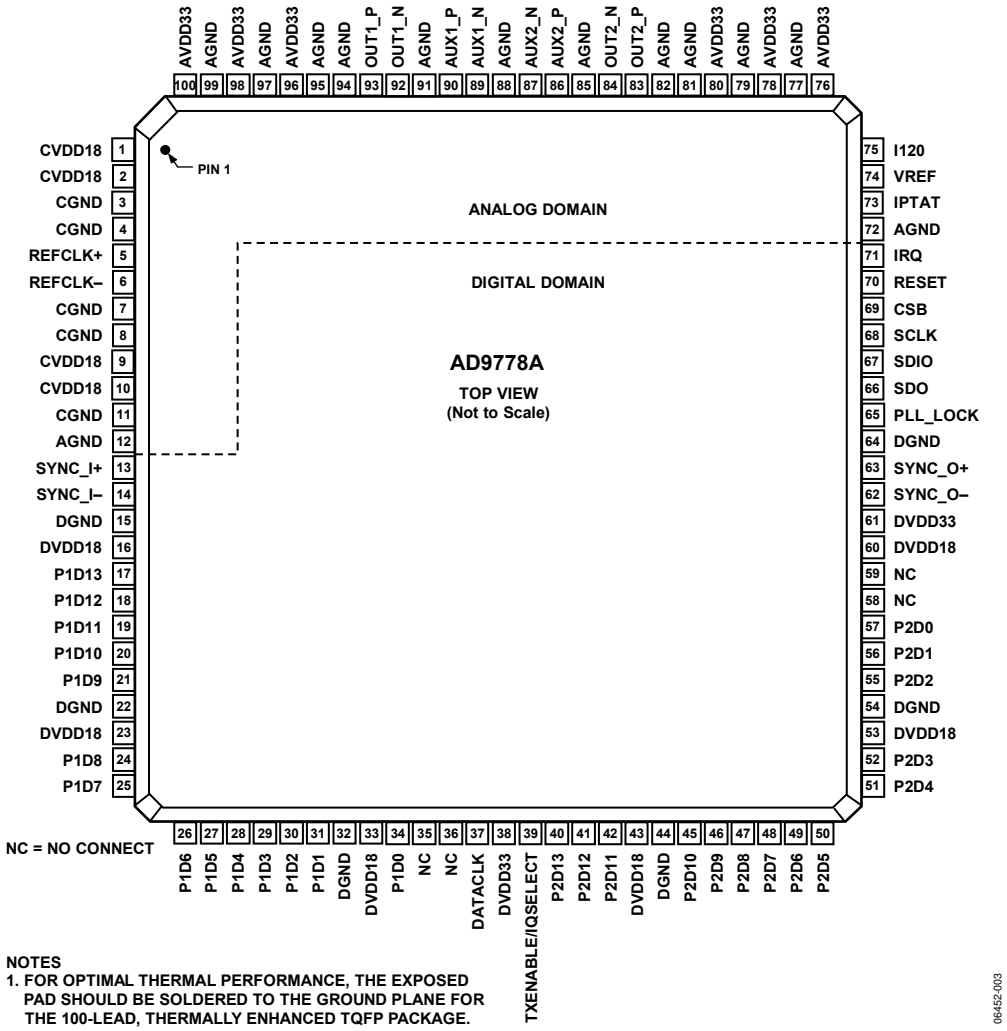

Figure 4. AD9778A Pin Configuration

Table 8. AD9778A Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CVDD18	1.8 V Clock Supply.
2	CVDD18	1.8 V Clock Supply.
3	CGND	Clock Ground.
4	CGND	Clock Common.
5	REFCLK+	Differential Clock Input.
6	REFCLK–	Differential Clock Input.
7	CGND	Clock Ground.
8	CGND	Clock Ground.
9	CVDD18	1.8 V Clock Supply.
10	CVDD18	1.8 V Clock Supply.
11	CGND	Clock Ground.
12	AGND	Analog Ground.
13	SYNC_I+	Differential Synchronization Input.
14	SYNC_I–	Differential Synchronization Input.
15	DGND	Digital Ground.
16	DVDD18	1.8 V Digital Supply.
17	P1D13	Port 1, Data Input D13 (MSB).
18	P1D12	Port 1, Data Input D12.
19	P1D11	Port 1, Data Input D11.
20	P1D10	Port 1, Data Input D10.
21	P1D9	Port 1, Data Input D9.
22	DGND	Digital Ground.
23	DVDD18	1.8 V Digital Supply.
24	P1D8	Port 1, Data Input D8.
25	P1D7	Port 1, Data Input D7.
26	P1D6	Port 1, Data Input D6.
27	P1D5	Port 1, Data Input D5.
28	P1D4	Port 1, Data Input D4.
29	P1D3	Port 1, Data Input D3.
30	P1D2	Port 1, Data Input D2.
31	P1D1	Port 1, Data Input D1.
32	DGND	Digital Ground.
33	DVDD18	1.8 V Digital Supply.
34	P1D0	Port 1, Data Input D0 (LSB).
35	NC	No Connect.
36	NC	No Connect.

Pin No.	Mnemonic	Description
37	DATACLK	Data Clock Output.
38	DVDD33	3.3 V Digital Supply.
39	TXENABLE/ IQSELECT	Transmit Enable. In single port mode, this pin also functions as IQSELECT.
40	P2D13	Port 2, Data Input D13 (MSB).
41	P2D12	Port 2, Data Input D12.
42	P2D11	Port 2, Data Input D11.
43	DVDD18	1.8 V Digital Supply.
44	DGND	Digital Ground.
45	P2D10	Port 2, Data Input D10.
46	P2D9	Port 2, Data Input D9.
47	P2D8	Port 2, Data Input D8.
48	P2D7	Port 2, Data Input D7.
49	P2D6	Port 2, Data Input D6.
50	P2D5	Port 2, Data Input D5.
51	P2D4	Port 2, Data Input D4.
52	P2D3	Port 2, Data Input D3.
53	DVDD18	1.8 V Digital Supply.
54	DGND	Digital Ground.
55	P2D2	Port 2, Data Input D2.
56	P2D1	Port 2, Data Input D1.
57	P2D0	Port 2, Data Input D0 (LSB).
58	NC	No Connect.
59	NC	No Connect.
60	DVDD18	1.8 V Digital Supply.
61	DVDD33	3.3 V Digital Supply.
62	SYNC_O–	Differential Synchronization Output.
63	SYNC_O+	Differential Synchronization Output.
64	DGND	Digital Ground.
65	PLL_LOCK	PLL Lock Indicator.
66	SDO	3-Wire Interface Port Data Output.
67	SDIO	3-Wire Interface Port Data Input/Output.
68	SCLK	3-Wire Interface Port Clock.
69	CSB	3-Wire Interface Port Chip Select Bar.
70	RESET	Reset, Active High.
71	IRQ	Interrupt Request.
72	AGND	Analog Ground.
73	IPTAT	Factory Test Pin. Output current is proportional to absolute temperature, approximately 14 µA at 25°C with approximately 20 nA/°C slope. This pin should remain floating.
74	VREF	Voltage Reference Output.
75	I120	120 µA Reference Current.
76	AVDD33	3.3 V Analog Supply.
77	AGND	Analog Ground.
78	AVDD33	3.3 V Analog Supply.
79	AGND	Analog Ground.
80	AVDD33	3.3 V Analog Supply.
81	AGND	Analog Ground.
82	AGND	Analog Ground.
83	OUT2_P	Differential DAC Current Output, Channel 2.
84	OUT2_N	Differential DAC Current Output, Channel 2.
85	AGND	Analog Ground.
86	AUX2_P	Auxiliary DAC Current Output, Channel 2.
87	AUX2_N	Auxiliary DAC Current Output, Channel 2.
88	AGND	Analog Ground.
89	AUX1_N	Auxiliary DAC Current Output, Channel 1.
90	AUX1_P	Auxiliary DAC Current Output, Channel 1.
91	AGND	Analog Ground.
92	OUT1_N	Differential DAC Current Output, Channel 1.
93	OUT1_P	Differential DAC Current Output, Channel 1.
94	AGND	Analog Ground.
95	AGND	Analog Ground.
96	AVDD33	3.3 V Analog Supply.
97	AGND	Analog Ground.
98	AVDD33	3.3 V Analog Supply.
99	AGND	Analog Ground.
100	AVDD33	3.3 V Analog Supply.

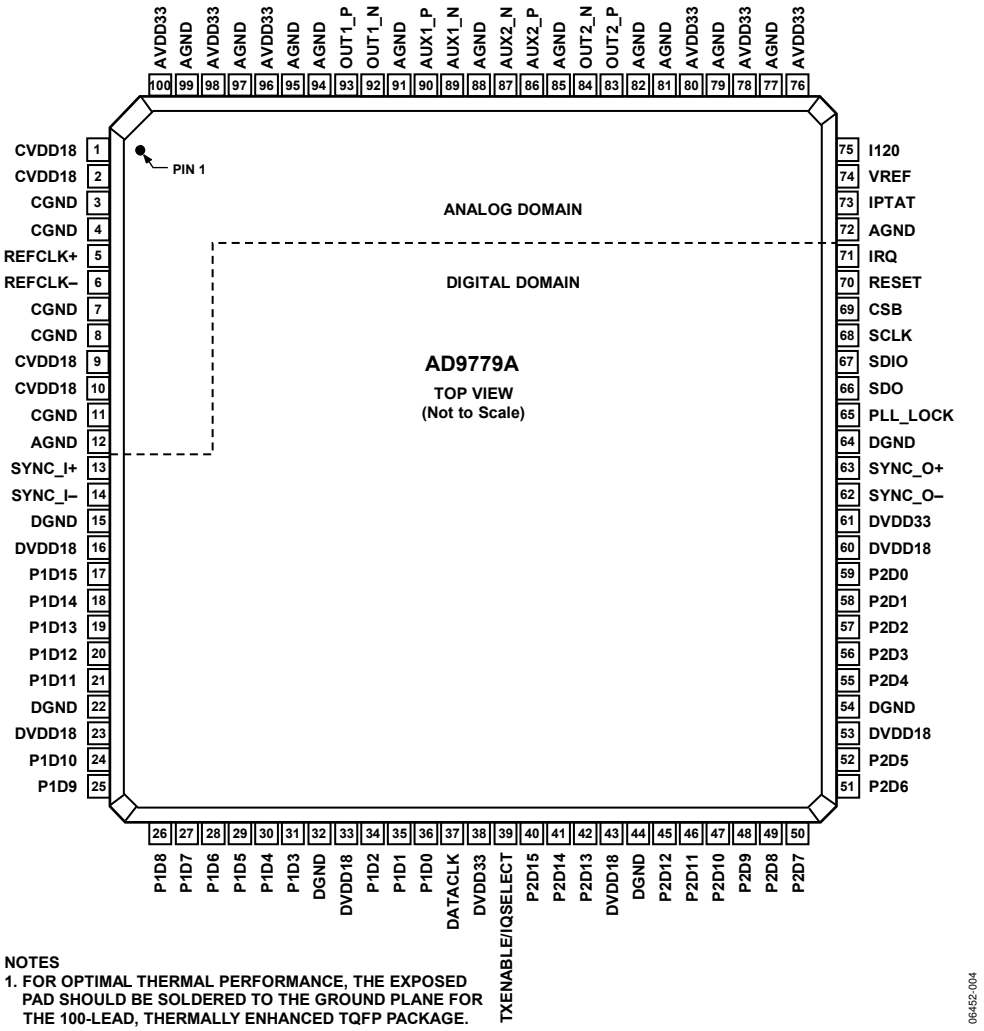

Figure 5. AD9779A Pin Configuration

Table 9. AD9779A Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CVDD18	1.8 V Clock Supply.
2	CVDD18	1.8 V Clock Supply.
3	CGND	Clock Ground.
4	CGND	Clock Ground.
5	REFCLK+	Differential Clock Input.
6	REFCLK–	Differential Clock Input.
7	CGND	Clock Ground.
8	CGND	Clock Ground.
9	CVDD18	1.8 V Clock Supply.
10	CVDD18	1.8 V Clock Supply.
11	CGND	Clock Ground.
12	AGND	Analog Ground.
13	SYNC_I+	Differential Synchronization Input.
14	SYNC_I–	Differential Synchronization Input.
15	DGND	Digital Ground.
16	DVDD18	1.8 V Digital Supply.
17	P1D15	Port 1, Data Input D15 (MSB).
18	P1D14	Port 1, Data Input D14.
19	P1D13	Port 1, Data Input D13.
20	P1D12	Port 1, Data Input D12.
21	P1D11	Port 1, Data Input D11.
22	DGND	Digital Ground.
23	DVDD18	1.8 V Digital Supply.
24	P1D10	Port 1, Data Input D10.
25	P1D9	Port 1, Data Input D9.
26	P1D8	Port 1, Data Input D8.
27	P1D7	Port 1, Data Input D7.
28	P1D6	Port 1, Data Input D6.
29	P1D5	Port 1, Data Input D5.
30	P1D4	Port 1, Data Input D4.
31	P1D3	Port 1, Data Input D3.
32	DGND	Digital Ground.
33	DVDD18	1.8 V Digital Supply.
34	P1D2	Port 1, Data Input D2.
35	P1D1	Port 1, Data Input D1.
36	P1D0	Port 1, Data Input D0 (LSB).

Pin No.	Mnemonic	Description
37	DATACLK	Data Clock Output.
38	DVDD33	3.3 V Digital Supply.
39	TXENABLE/ IQSELECT	Transmit Enable. In single port mode, this pin also functions as IQSELECT.
40	P2D15	Port 2, Data Input D15 (MSB).
41	P2D14	Port 2, Data Input D14.
42	P2D13	Port 2, Data Input D13.
43	DVDD18	1.8 V Digital Supply.
44	DGND	Digital Ground.
45	P2D12	Port 2, Data Input D12.
46	P2D11	Port 2, Data Input D11.
47	P2D10	Port 2, Data Input D10.
48	P2D9	Port 2, Data Input D9.
49	P2D8	Port 2, Data Input D8.
50	P2D7	Port 2, Data Input D7.
51	P2D6	Port 2, Data Input D6.
52	P2D5	Port 2, Data Input D5.
53	DVDD18	1.8 V Digital Supply.
54	DGND	Digital Ground.
55	P2D4	Port 2, Data Input D4.
56	P2D3	Port 2, Data Input D3.
57	P2D2	Port 2, Data Input D2.
58	P2D1	Port 2, Data Input D1.
59	P2D0	Port 2, Data Input D0 (LSB).
60	DVDD18	1.8 V Digital Supply.
61	DVDD33	3.3 V Digital Supply.
62	SYNC_O–	Differential Synchronization Output.
63	SYNC_O+	Differential Synchronization Output.
64	DGND	Digital Ground.
65	PLL_LOCK	PLL Lock Indicator.
66	SDO	3-Wire Interface Port Data Output.
67	SDIO	3-Wire Interface Port Data Input/Output.
68	SCLK	3-Wire Interface Port Clock.
69	CSB	3-Wire Interface Port Chip Select Bar.
70	RESET	Reset, Active High.
71	IRQ	Interrupt Request.
72	AGND	Analog Ground.
73	IPTAT	Factory Test Pin. Output current is proportional to absolute temperature, approximately 14 µA at 25°C with approximately 20 nA/°C slope. This pin should remain floating.
74	VREF	Voltage Reference Output.
75	I120	120 µA Reference Current.
76	AVDD33	3.3 V Analog Supply.
77	AGND	Analog Ground.
78	AVDD33	3.3 V Analog Supply.
79	AGND	Analog Ground.
80	AVDD33	3.3 V Analog Supply.
81	AGND	Analog Ground.
82	AGND	Analog Ground.
83	OUT2_P	Differential DAC Current Output, Channel 2.
84	OUT2_N	Differential DAC Current Output, Channel 2.
85	AGND	Analog Ground.
86	AUX2_P	Auxiliary DAC Current Output, Channel 2.
87	AUX2_N	Auxiliary DAC Current Output, Channel 2.
88	AGND	Analog Ground.
89	AUX1_N	Auxiliary DAC Current Output, Channel 1.
90	AUX1_P	Auxiliary DAC Current Output, Channel 1.
91	AGND	Analog Ground.
92	OUT1_N	Differential DAC Current Output, Channel 1.
93	OUT1_P	Differential DAC Current Output, Channel 1.
94	AGND	Analog Ground.
95	AGND	Analog Ground.
96	AVDD33	3.3 V Analog Supply.
97	AGND	Analog Ground.
98	AVDD33	3.3 V Analog Supply.
99	AGND	Analog Ground.
100	AVDD33	3.3 V Analog Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

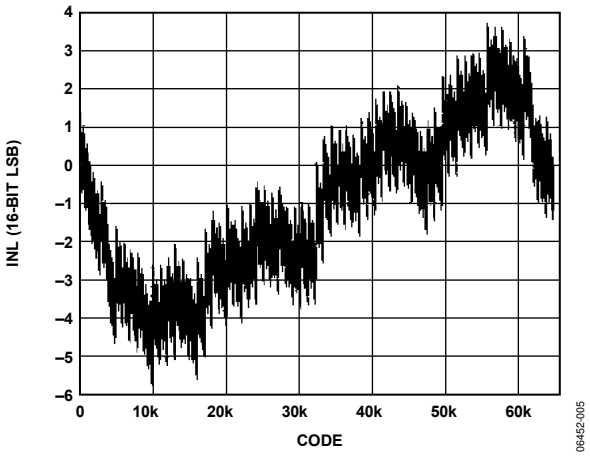

Figure 6. AD9779A Typical INL

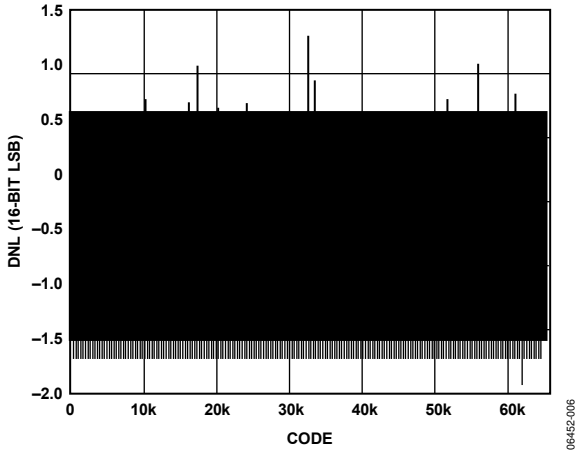

Figure 7. AD9779A Typical DNL

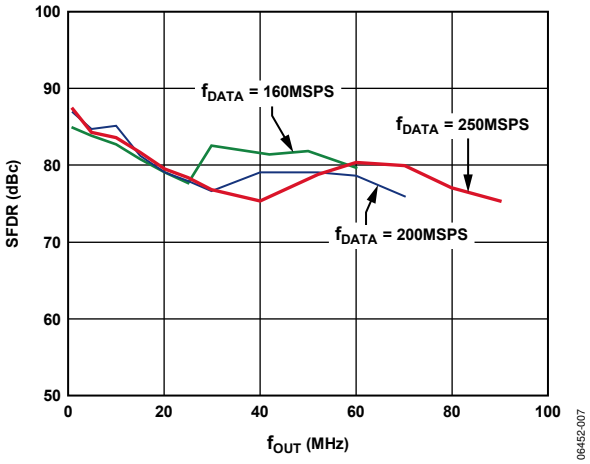

Figure 8. AD9779A In-Band SFDR vs. f_{OUT}, 1× Interpolation

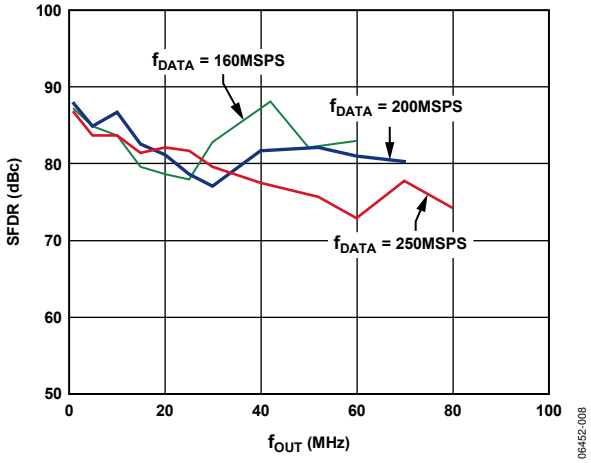

Figure 9. AD9779A In-Band SFDR vs. f_{OUT}, 2× Interpolation

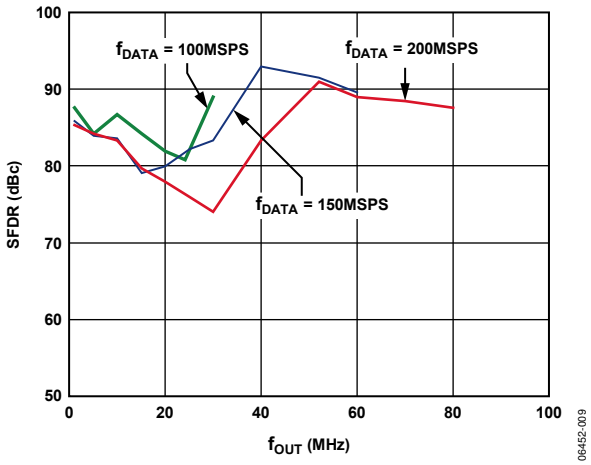

Figure 10. AD9779A In-Band SFDR vs. f_{OUT}, 4× Interpolation

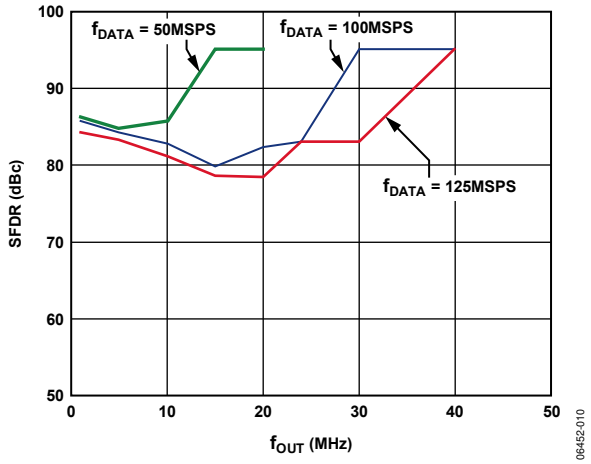

Figure 11. AD9779A In-Band SFDR vs. f_{OUT}, 8× Interpolation

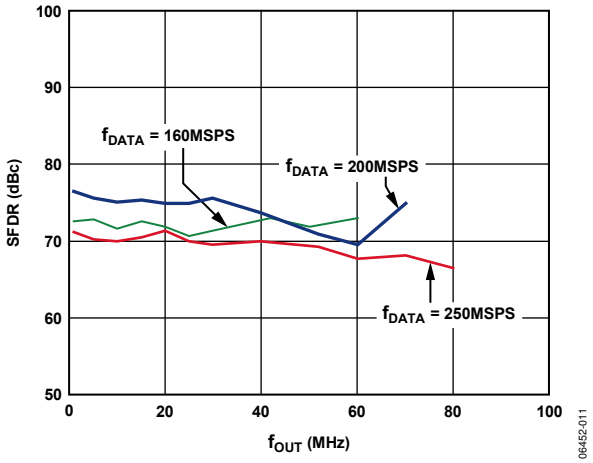

Figure 12. AD9779A Out-of-Band SFDR vs. f_{OUT}, 2× Interpolation

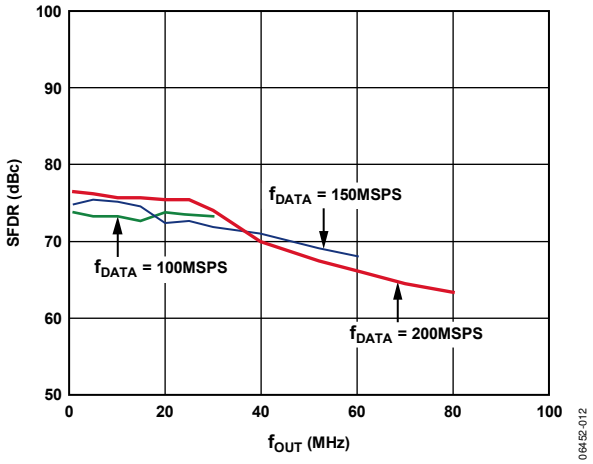

Figure 13. AD9779A Out-of-Band SFDR vs. f_{OUT}, 4× Interpolation

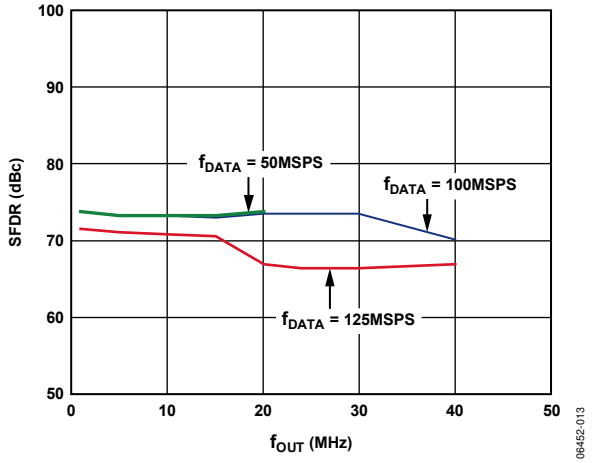

Figure 14. AD9779A Out-of-Band SFDR vs. f_{OUT}, 8× Interpolation

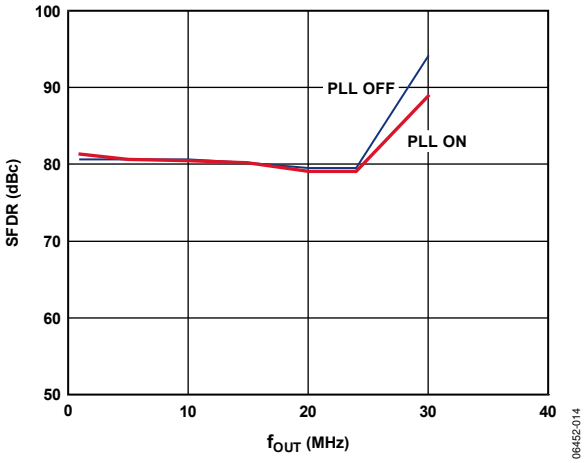

Figure 15. AD9779A In-Band SFDR vs. f_{OUT}, 4× Interpolation, f_{DATA} = 100 MSPS, PLL On/Off

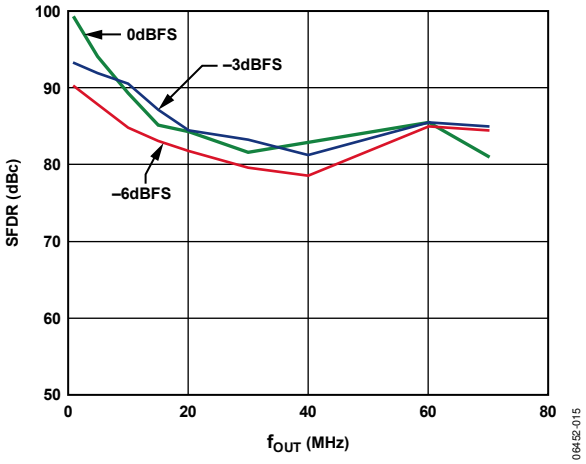

Figure 16. AD9779A In-Band SFDR vs. f_{OUT}, Digital Full Scale

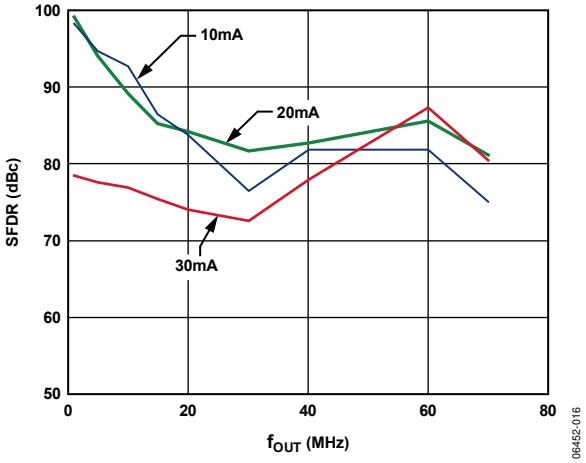

Figure 17. AD9779A In-Band SFDR vs. f_{OUT}, Output Full-Scale Current

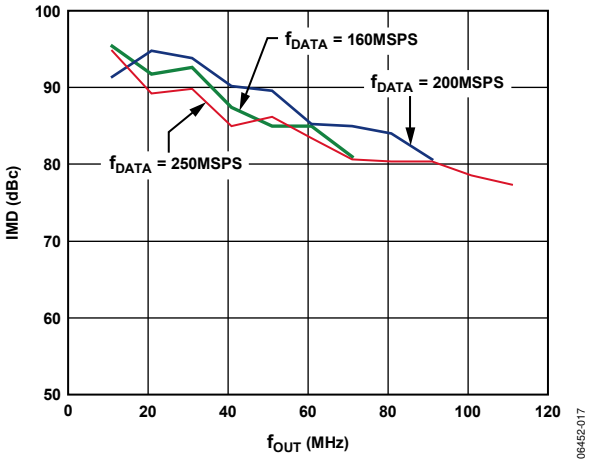

Figure 18. AD9779A Third-Order IMD vs. f_{OUT}, 1× Interpolation

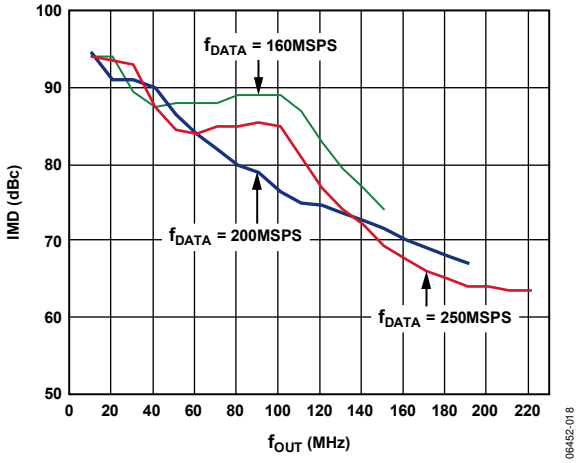

Figure 19. AD9779A Third-Order IMD vs. f_{OUT}, 2× Interpolation

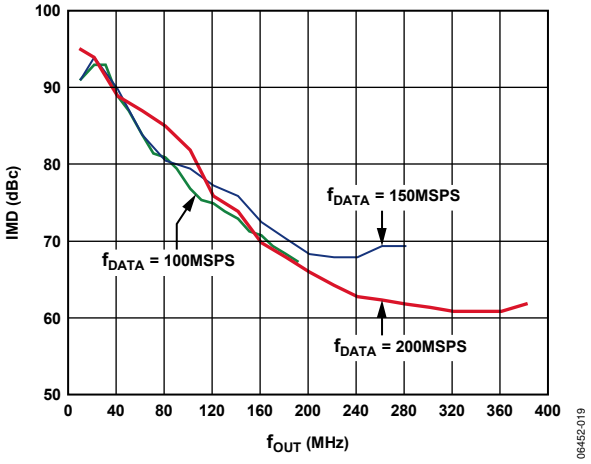

Figure 20. AD9779A Third-Order IMD vs. f_{OUT}, 4× Interpolation

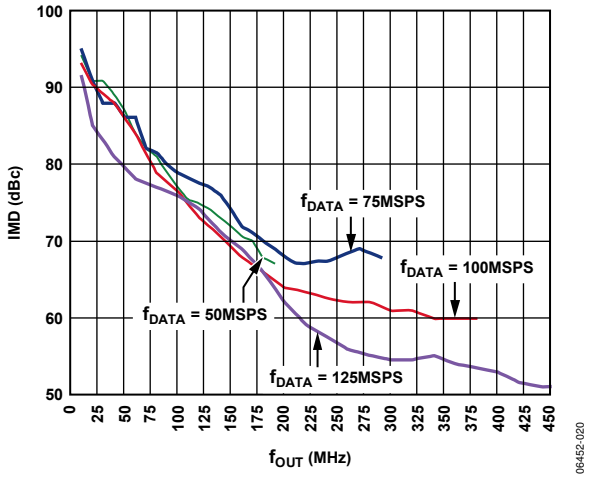

Figure 21. AD9779A Third-Order IMD vs. f_{OUT}, 8× Interpolation

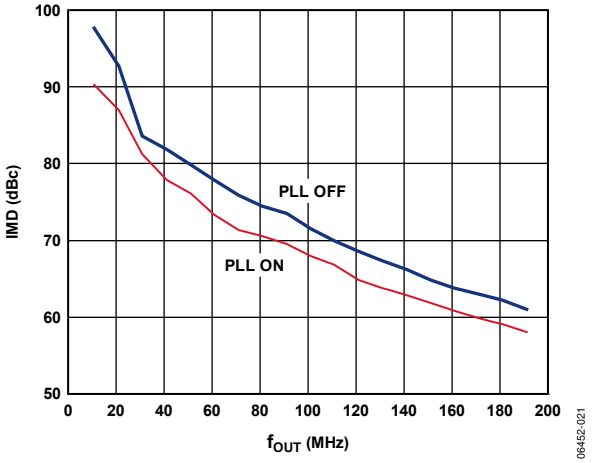

Figure 22. AD9779A Third-Order IMD vs. f_{OUT}, 4× Interpolation, f_{DATA} = 100 MSPS, PLL On/Off

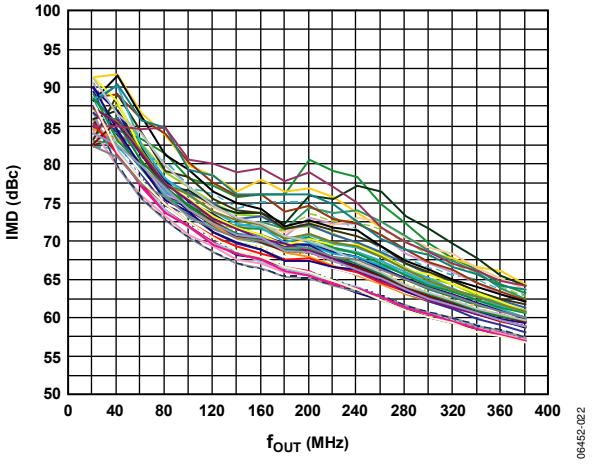

Figure 23. AD9779A Third-Order IMD vs. f_{OUT}, Over 50 Parts, 4× Interpolation, f_{DATA} = 200 MSPS

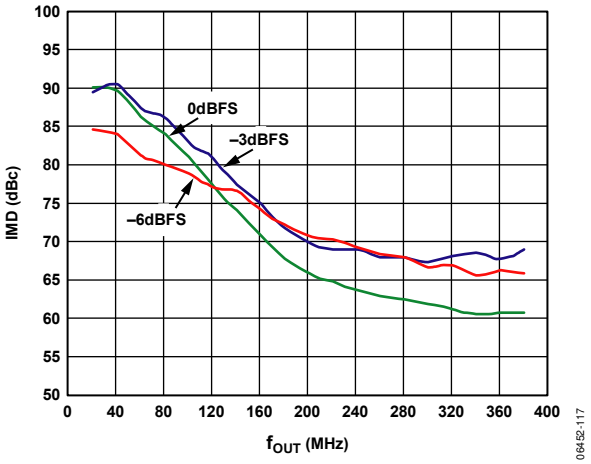

Figure 24. AD9779A IMD Performance vs. f_{OUT}, Digital Full-Scale Input Over Output Frequency, 4× Interpolation, f_{DATA} = 200 MSPS

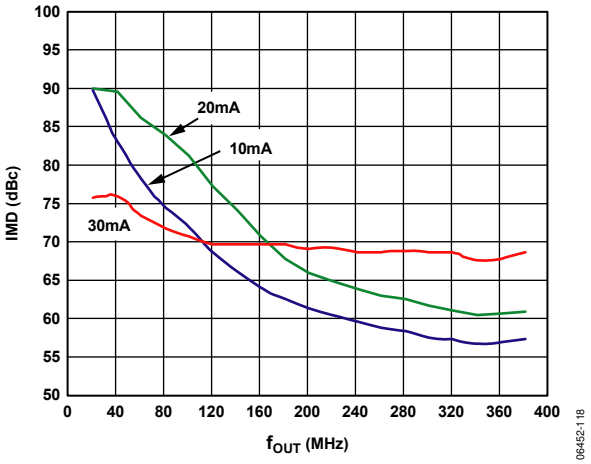

Figure 25. AD9779A IMD Performance vs. f_{OUT}, Full-Scale Output Current Over Output Frequency, 4× Interpolation, f_{DATA} = 200 MSPS

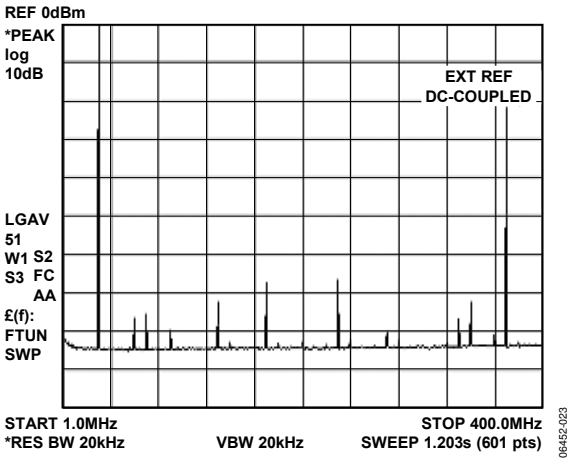

Figure 26. AD9779A Single Tone, 4× Interpolation, f_{DATA} = 100 MSPS, f_{OUT} = 30 MHz

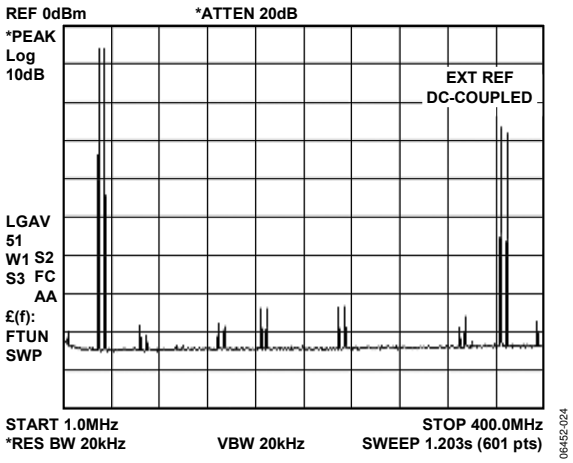

Figure 27. AD9779A Two-Tone Spectrum, 4× Interpolation, f_{DATA} = 100 MSPS, f_{OUT} = 30 MHz, 35 MHz

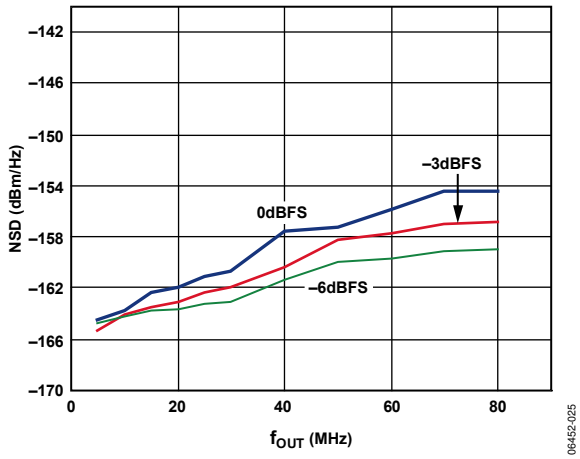

Figure 28. AD9779A Noise Spectral Density vs. f_{OUT}, Digital Full-Scale Over Output Frequency of Single-Tone Input, 2× Interpolation, f_{DATA} = 200 MSPS

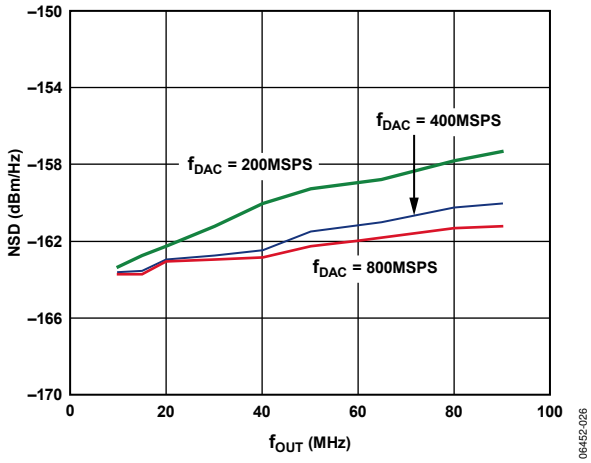

Figure 29. AD9779A Noise Spectral Density vs. f_{OUT}, f_{DAC} Over Output Frequency for Eight-Tone Input with 500 kHz Spacing, f_{DATA} = 200 MSPS

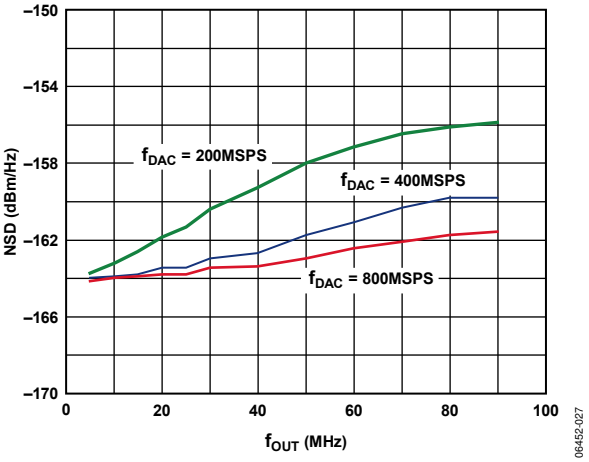

Figure 30. AD9779A Noise Spectral Density vs. f_{OUT}, f_{DAC} Over Output Frequency with a Single-Tone Input at −6 dBFS

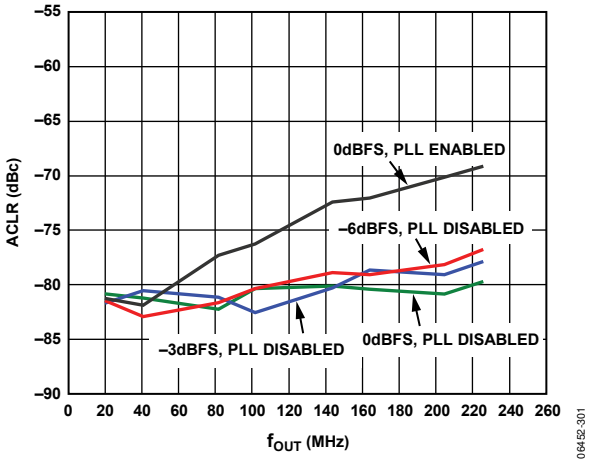

Figure 33. AD9779A ACLR for Second Adjacent Band W-CDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, On-Chip Modulation Translates Baseband Signal to IF

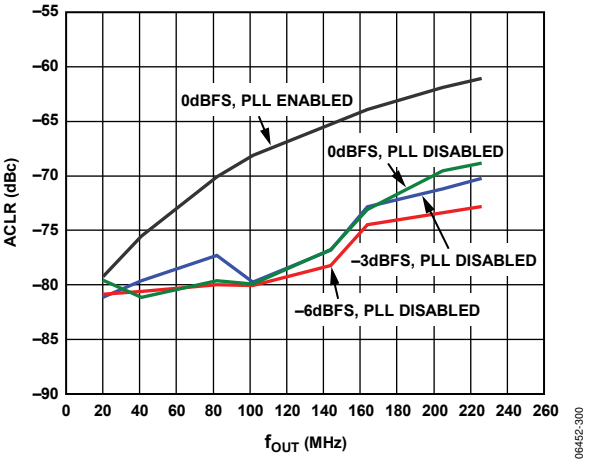

Figure 31. AD9779A ACLR for First Adjacent Band W-CDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, On-Chip Modulation Translates Baseband Signal to IF

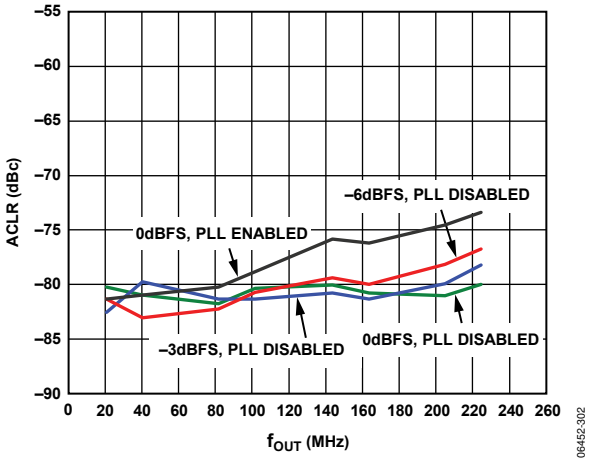

Figure 34. AD9779A ACLR for Third Adjacent Band W-CDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, On-Chip Modulation Translates Baseband Signal to IF

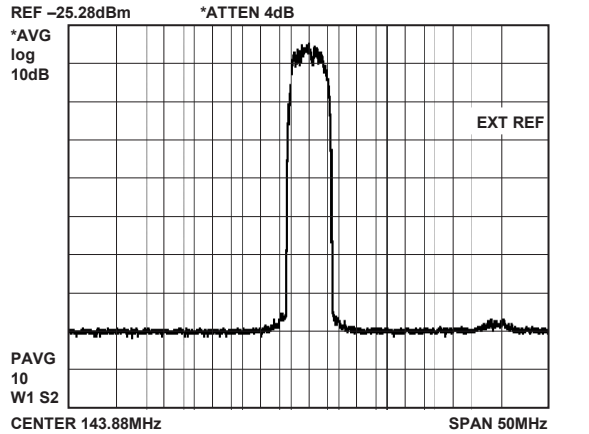

Figure 32. AD9779A W-CDMA Signal, 4× Interpolation, f_{DATA} = 122.88 MSPS, f_{DAC}/4 Modulation

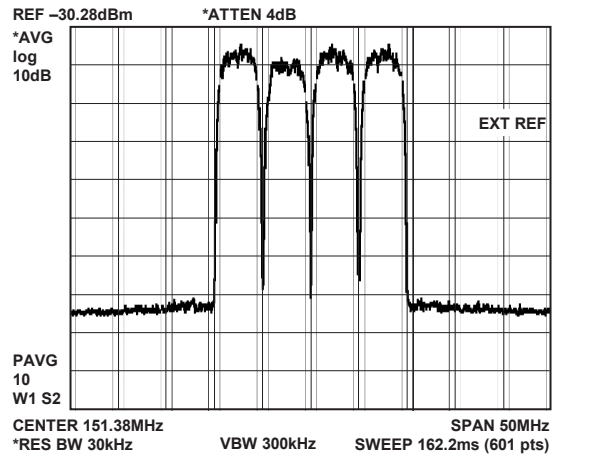

Figure 35. AD9779A Multicarrier W-CDMA Signal, 4× Interpolation, f_{DAC} = 122.88 MSPS, f_{DAC}/4 Modulation

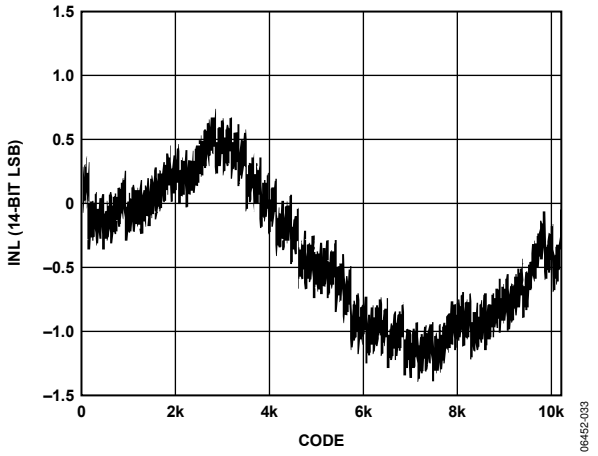

Figure 36. AD9778A Typical INL

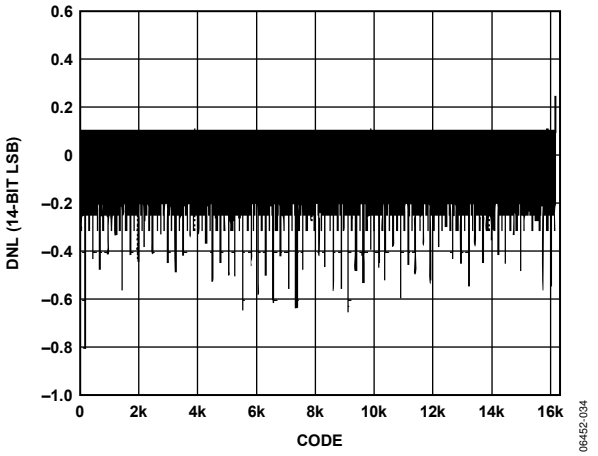

Figure 37. AD9778A Typical DNL

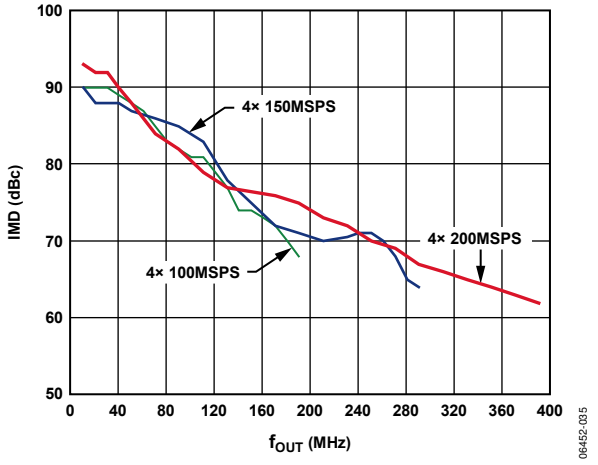

Figure 38. AD9778A IMD vs. f_{OUT}, 4× Interpolation

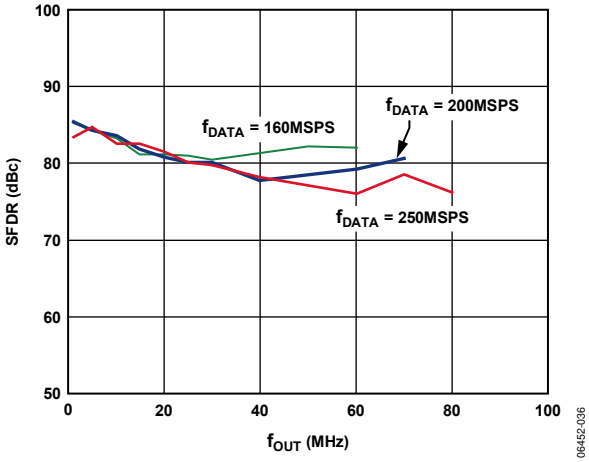

Figure 39. AD9778A In-Band SFDR vs. f_{OUT}, 2× Interpolation

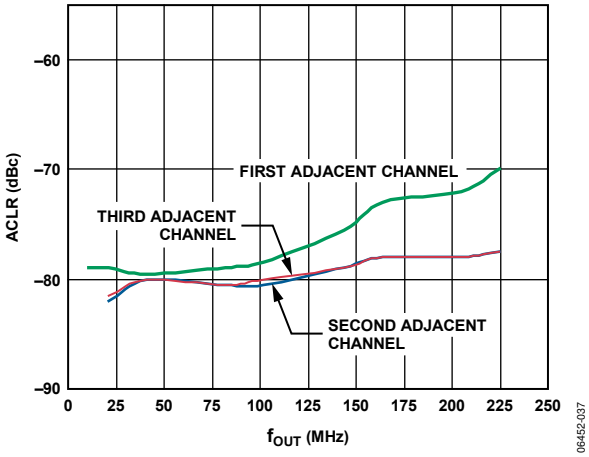

Figure 40. AD9778A ACLR, Single Carrier W-CDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, Amplitude = –3 dBFS

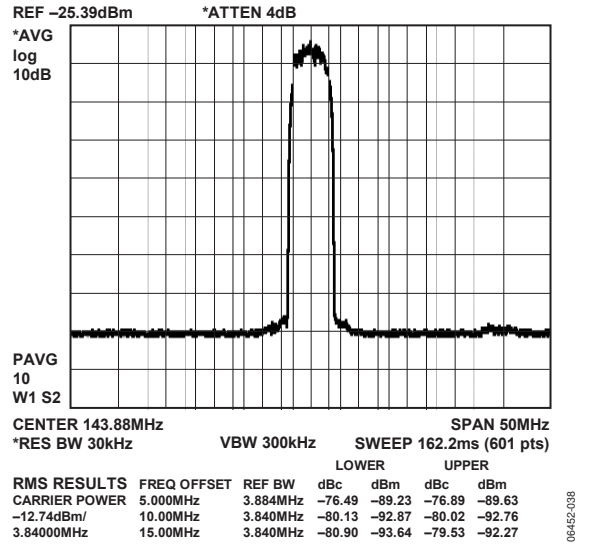

Figure 41. AD9778A ACLR, f_{DATA} = 122.88 MSPS, 4× Interpolation, $f_{DAC}/4$ Modulation

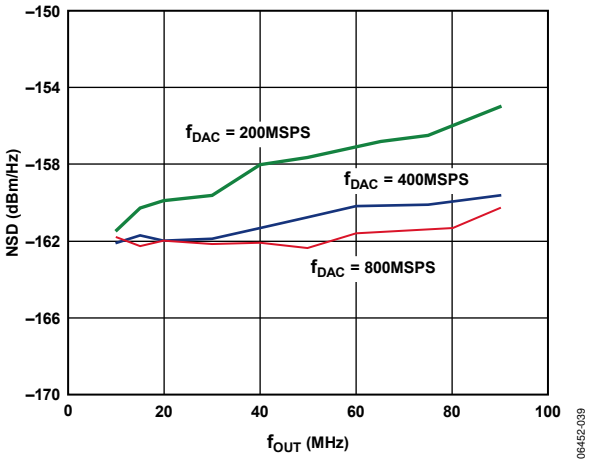

Figure 42. AD9778A Noise Spectral Density vs. f_{OUT} for Eight-Tone Input with 500 kHz Spacing, f_{DATA} = 200 MSPS

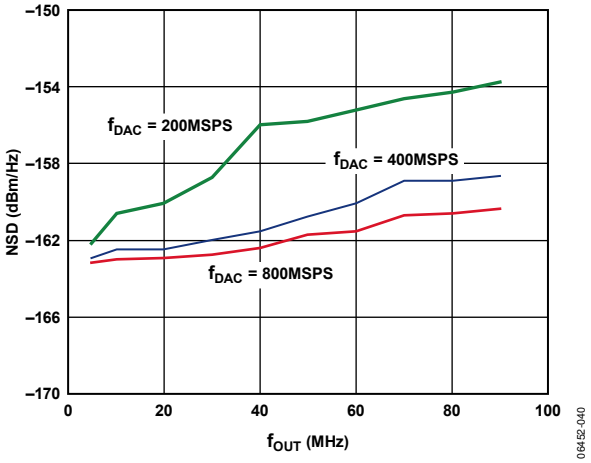

Figure 43. AD9778A Noise Spectral Density vs. f_{OUT} with Single-Tone Input at –6 dBFS, f_{DATA} = 200 MSPS

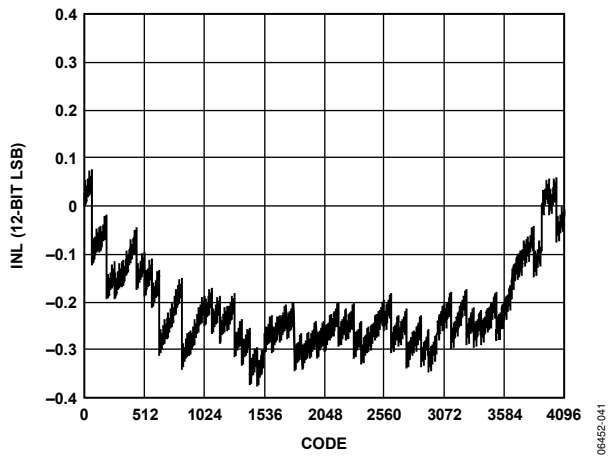

Figure 44. AD9776A Typical INL

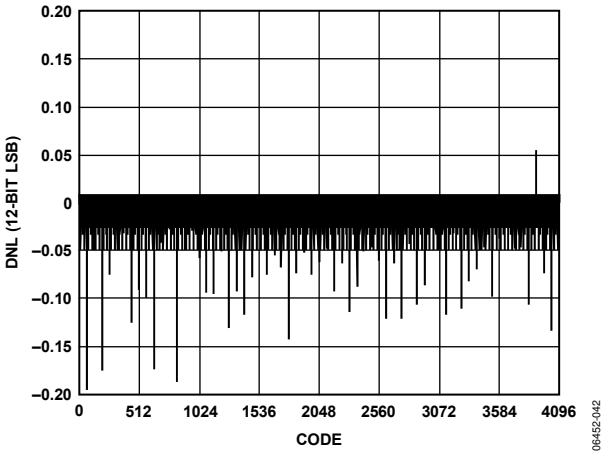

Figure 45. AD9776A Typical DNL

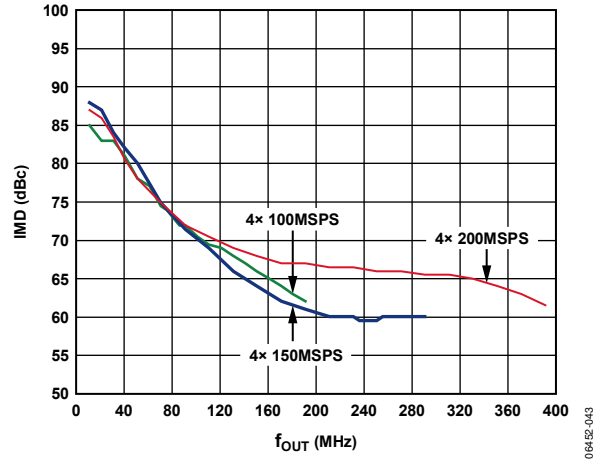

Figure 46. AD9776A IMD vs. f_{OUT}, 4× Interpolation

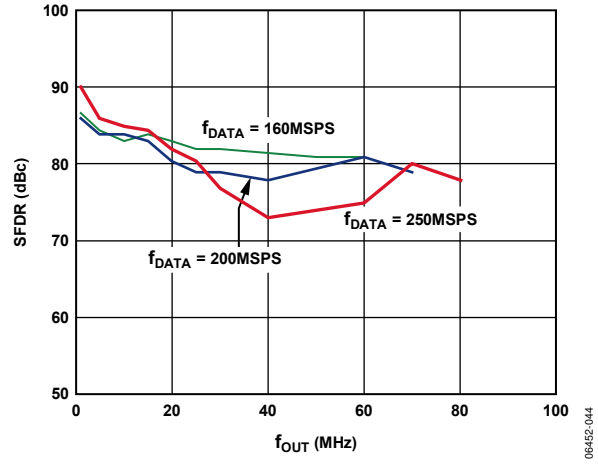

Figure 47. AD9776A In-Band SFDR vs. f_{OUT}, 2× Interpolation

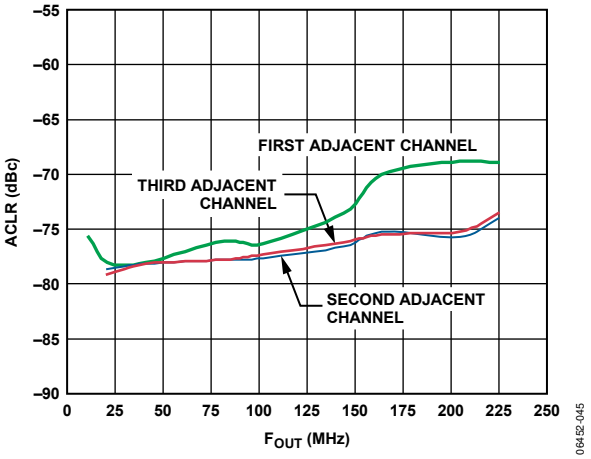

Figure 48. AD9776A ACLR vs. f_{OUT}, f_{DATA} = 122.88 MSPS, 4× Interpolation, $f_{DAC}/4$ Modulation

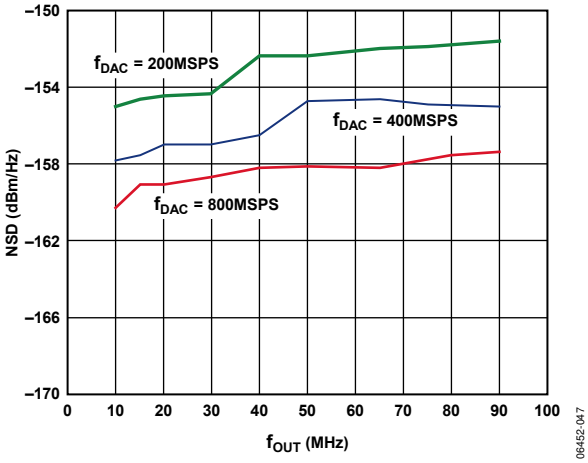

Figure 50. AD9776A Noise Spectral Density vs. f_{OUT}, Eight-Tone Input with 500 kHz Spacing, f_{DATA} = 200 MSPS

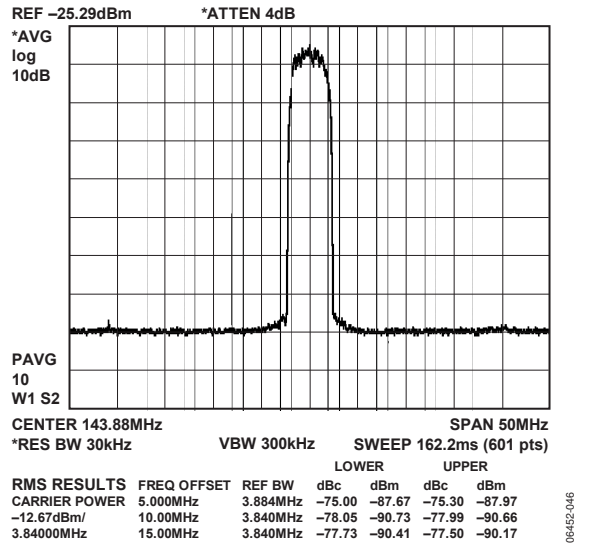

Figure 49. AD9776A Single Carrier W-CDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, Amplitude = −3 dBFS

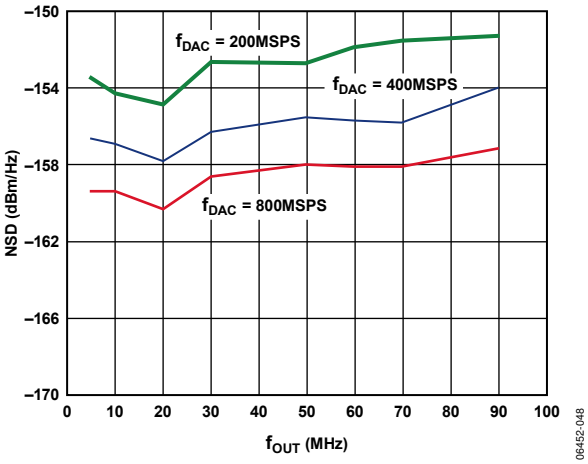

Figure 51. AD9776A Noise Spectral Density vs. f_{OUT}, Single-Tone Input at −6 dBFS, f_{DATA} = 200 MSPS

TERMINOLOGY

Integral Nonlinearity (INL)
INL is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current at Code 0 from the ideal of zero is called offset error. For I_{OUTA}, 0 mA output is expected when the inputs are all 0s. For I_{OUTB}, 0 mA output is expected when all inputs are set to 1s.

Gain Error
Gain error is the difference between the actual and the ideal output spans. The actual span is determined by the difference between the full-scale output and the bottom-scale output.

Output Compliance Range
Output compliance range is the range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree Celsius. For reference drift, the drift is reported in ppm per degree Celsius.

Power Supply Rejection (PSR)
PSR is the maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

In-Band Spurious-Free Dynamic Range (SFDR)
In-band SFDR is the difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal between dc and the frequency equal to half the input data rate.

Out-of-Band Spurious-Free Dynamic Range (SFDR)
Out-of-band SFDR is the difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal within the band that starts at the frequency of the input data rate and ends at the Nyquist frequency of the DAC output sample rate. Normally, energy in this band is rejected by the interpolation filters. This specification, therefore, defines how well the interpolation filters work and the effect of other parasitic coupling paths to the DAC output.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured fundamental. It is expressed as a percentage or in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Interpolation Filter
If the digital inputs to the DAC are sampled at a multiple rate of f_{DATA} (interpolation rate), a digital filter can be constructed that has a sharp transition band near $f_{DATA}/2$. Images that typically appear around f_{DAC} (output data rate) can be greatly suppressed.

Adjacent Channel Leakage Ratio (ACLR)
ACLR is the ratio in dBc of the measured power within a channel relative to its adjacent channel.

Complex Image Rejection
In a traditional two-part upconversion, two images are created around the second IF frequency. These images have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

THEORY OF OPERATION

The AD9776A/AD9778A/AD9779A have many features that make them highly suited for wired and wireless communications systems. The dual digital signal path and dual DAC structure allow an easy interface with common quadrature modulators when designing single sideband transmitters. The speed and performance of the parts allow wider bandwidths and more carriers to be synthesized than in previously available DACs. The digital engine uses an innovative filter architecture that combines the interpolation with a digital quadrature modulator. This allows the parts to perform digital quadrature frequency upconversions. The on-chip synchronization circuitry enables multiple devices to be synchronized to each other, or to a system clock.

DIFFERENCES BETWEEN AD9776/AD9778/AD9779 AND AD9776A/AD9778A/AD9779A

REFCLK Maximum Frequency vs. Supply

With some restrictions on the DVDD18 and CVDD18 power supplies, the AD9776A/AD9778A/AD9779A support a maximum sample rate of 1100 MHz. Table 2 lists the valid operating frequencies vs. power supply voltage.

REFCLK Amplitude

With a differential sinusoidal clock applied to REFCLK, the PLL on the AD9776/AD9778/AD9779 does not achieve optimal noise performance unless the REFCLK differential amplitude is increased to 2 V p-p. Note that if an LVPECL driver is used on the AD9776/AD9778/AD9779, the PLL exhibits optimal performance if the REFCLK amplitude is well within LVPECL specifications (<1.6 V p-p differential). The design of the PLL on the AD9779A has been improved so that even with a sinusoidal clock, the PLL still achieves optimal amplitude if the swing is 1.6 V p-p.

PLL Lock Ranges

The individual lock ranges for the AD9776A/AD9778A/AD9779A PLL are wider than those for the AD9776/AD9778/AD9779. This means that the AD9776A/AD9778A/AD9779A PLL remains in lock in a given range over a wider temperature range than the AD9776/AD9778/AD9779. See Table 23 for PLL lock ranges for the AD9776A/AD9778A/AD9779A.

PLL Optimal Settings

The optimal settings for the AD9776/AD9778/AD9779 differ from the AD9776A/AD9778A/AD9779A. Refer to the PLL Bias Settings section for complete details.

Input Data Delay Line, Manual and Automatic Correction Modes

The AD9776A/AD9778A/AD9779A can be programmed to not only sense when the timing margin on the input data falls below a preset threshold but to also take action. The device can be programmed to either set the IRQ (pin and register) or automatically reoptimize the timing input data timing.

Input Data Timing

See Table 28 for timing specifications vs. temperature. The input data timing specifications (setup and hold) are different for the AD9776A/AD9778A/AD9779A than they are for the AD9776/AD9778/AD9779.

DATACLK Delay Range

In the AD9776/AD9778/AD9779, the input data delay was controlled by Register 0x04, Bits[7:4]. At 25°C, the delay was stepped by approximately 180 ps/increment. In the AD9776A/AD9778A/AD9779A, an extra bit has been added, which effectively doubles the delay range. This bit is now located at Register 0x01, Bit 1. The increment/step on the AD9776A/AD9778A/AD9779A remains at ~180 ps.

Version Register

The version register (Register 0x1F) of the AD9776A/AD9778A/AD9779A reads a value of 0x07. The version register of the AD9776/AD9778/AD9779 reads a value of 0x03.

Table 10. Register Value Differences Between AD9776/AD9778/AD9779 and AD9776A/AD9778A/AD9779A

Part No.	PLL Loop Bandwidth, Register 0x0A, Bits[4:0]	PLL Bias, Register 0x09, Bits[2:0]	VCO Control Voltage, Register 0x0A, Bits[7:5]	PLL VCO Drive, Register 0x08, Bits[1:0]
AD9776/AD9778/AD9779	11111	111	010	00
AD9776A/AD9778A/AD9779A	01111	011	011	11