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# Dual 12-/14-/16-Bit, 1 GSPS, Digital-to-Analog Converters

# AD9776/AD9778/AD9779

## FEATURES

- **Low power: 1.0 W @ 1 GSPS, 600 mW @ 500 MSPS, full operating conditions**
- **SFDR = 78 dBc to $f_{OUT}$ = 100 MHz**
- **Single carrier WCDMA ACLR = 79 dBc @ 80 MHz IF**
- **Analog output: adjustable 8.7 mA to 31.7 mA, $R_L$ = 25 Ω to 50 Ω**
- **Novel 2×, 4×, and 8× interpolator/coarse complex modulator allows carrier placement anywhere in DAC bandwidth**
- **Auxiliary DACs allow control of external VGA and offset control**
- **Multiple chip synchronization interface**
- **High performance, low noise PLL clock multiplier**
- **Digital inverse sinc filter**
- **100-lead, exposed paddle TQFP package**

## APPLICATIONS

- **Wireless infrastructure**
  - **WCDMA, CDMA2000, TD-SCDMA, WiMax, GSM**
- **Digital high or low IF synthesis**
- **Internal digital upconversion capability**
- **Transmit diversity**
- **Wideband communications: LMDS/MMDS, point-to-point**

## GENERAL DESCRIPTION

The AD9776/AD9778/AD9779 are dual, 12-/14-/16-bit, high dynamic range, digital-to-analog converters (DACs) that provide a sample rate of 1 GSPS, permitting multicarrier generation up to the Nyquist frequency. They include features optimized for direct conversion transmit applications, including complex digital modulation, and gain and offset compensation. The DAC outputs are optimized to interface seamlessly with analog quadrature modulators such as the AD8349. A serial peripheral interface (SPI®) provides for programming/readback of many internal parameters. Full-scale output current can be programmed over a range of 10 mA to 30 mA. The devices are manufactured on an advanced 0.18 µm CMOS process and operate on 1.8 V and 3.3 V supplies for a total power consumption of 1.0 W. They are enclosed in 100-lead TQFP packages.

## PRODUCT HIGHLIGHTS

1. Ultralow noise and intermodulation distortion (IMD) enable high quality synthesis of wideband signals from baseband to high intermediate frequencies.
2. A proprietary DAC output switching technique enhances dynamic performance.
3. The current outputs are easily configured for various single-ended or differential circuit topologies.
4. CMOS data input interface with adjustable set up and hold.
5. Novel 2×, 4×, and 8× interpolator/coarse complex modulator allows carrier placement anywhere in DAC bandwidth.

## TYPICAL SIGNAL CHAIN

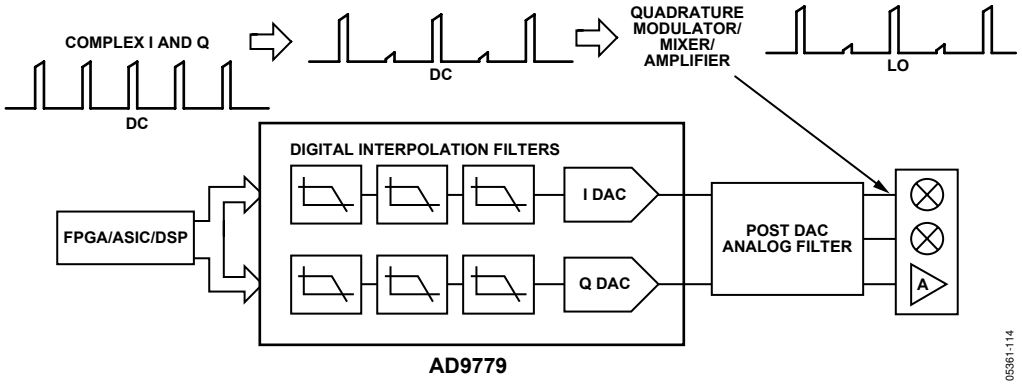


*Figure 1.*

**Rev. A**



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# FUNCTIONAL BLOCK DIAGRAM

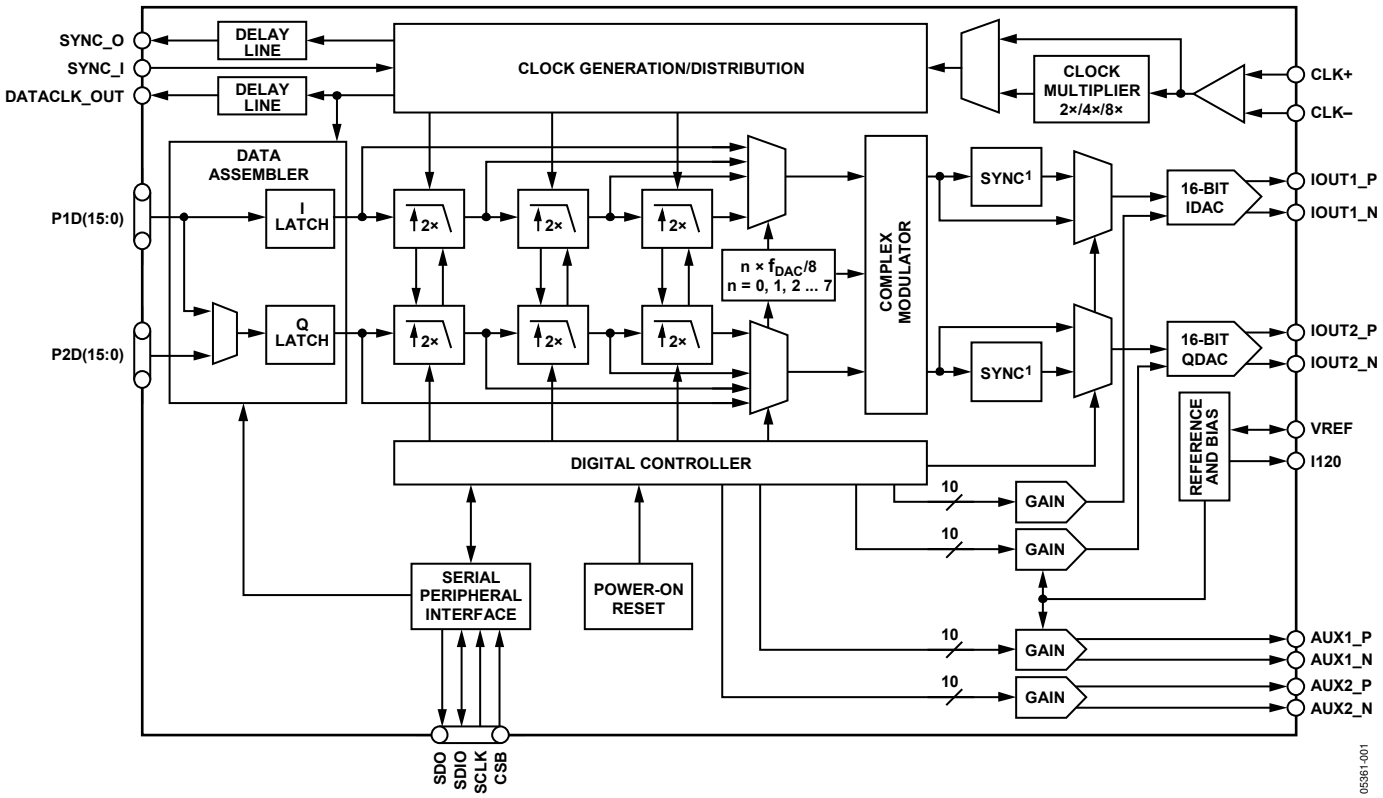



*Figure 2. Functional Block Diagram*

# SPECIFICATIONS

## DC SPECIFICATIONS

$T_{MIN}$ to $T_{MAX}$, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 =1.8 V, $I_{OUTFS}$ = 20 mA, maximum sample rate, unless otherwise noted.

**Table 1. AD9776, AD9778, and AD9779 DC Specifications**

| | AD9776 | | | AD9778 | | | AD9779 | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| RESOLUTION | | 12 | | | 14 | | | 16 | | Bits |
| ACCURACY | | | | | | | | | | |
| Differential Nonlinearity (DNL) | | ±0.1 | | | ±0.65 | | | ±2.1 | | LSB |
| Integral Nonlinearity (INL) | | ±0.6 | | | ±1 | | | ±3.7 | | LSB |
| MAIN DAC OUTPUTS | | | | | | | | | | |
| Offset Error | −0.001 | 0 | +0.001 | −0.001 | 0 | +0.001 | −0.001 | 0 | +0.001 | % FSR |
| Gain Error (with Internal Reference) | | ±2 | | | ±2 | | | ±2 | | % FSR |
| Full-Scale Output Current[1] | 8.66 | 20.2 | 31.66 | 8.66 | 20.2 | 31.66 | 8.66 | 20.2 | 31.66 | mA |
| Output Compliance Range | −1.0 | | +1.0 | −1.0 | | +1.0 | −1.0 | | +1.0 | V |
| Output Resistance | | 10 | | | 10 | | | 10 | | MΩ |
| Gain DAC Monotonicity | | Guaranteed | | | Guaranteed | | | Guaranteed | | |
| MAIN DAC TEMPERATURE DRIFT | | | | | | | | | | |
| Offset | | 0.04 | | | 0.04 | | | 0.04 | | ppm/°C |
| Gain | | 100 | | | 100 | | | 100 | | ppm/°C |
| Reference Voltage | | 30 | | | 30 | | | 30 | | ppm/°C |
| AUX DAC OUTPUTS | | | | | | | | | | |
| Resolution | | 10 | | | 10 | | | 10 | | Bits |
| Full-Scale Output Current[1] | −1.998 | | +1.998 | −1.998 | | +1.998 | −1.998 | | +1.998 | mA |
| Output Compliance Range (Source) | 0 | | 1.6 | 0 | | 1.6 | 0 | | 1.6 | V |
| Output Compliance Range (Sink) | 0.8 | | 1.6 | 0.8 | | 1.6 | 0.8 | | 1.6 | V |
| Output Resistance | | 1 | | | 1 | | | 1 | | MΩ |
| Aux DAC Monotonicity Guaranteed | | | | | | | | | | |
| REFERENCE | | | | | | | | | | |
| Internal Reference Voltage | | 1.2 | | | 1.2 | | | 1.2 | | V |
| Output Resistance | | 5 | | | 5 | | | 5 | | kΩ |
| ANALOG SUPPLY VOLTAGES | | | | | | | | | | |
| AVDD33 | 3.13 | 3.3 | 3.47 | 3.13 | 3.3 | 3.47 | 3.13 | 3.3 | 3.47 | V |
| CVDD18 | 1.70 | 1.8 | 1.90 | 1.70 | 1.8 | 1.90 | 1.70 | 1.8 | 1.90 | V |
| DIGITAL SUPPLY VOLTAGES | | | | | | | | | | |
| DVDD33 | 3.13 | 3.3 | 3.47 | 3.13 | 3.3 | 3.47 | 3.13 | 3.3 | 3.47 | V |
| DVDD18 | 1.70 | 1.8 | 1.90 | 1.70 | 1.8 | 1.90 | 1.70 | 1.8 | 1.90 | V |
| POWER CONSUMPTION | | | | | | | | | | |
| 1× Mode, $f_{DAC}$ = 100 MSPS, IF = 1 MHz | | 250 | 300 | | 250 | 300 | | 250 | 300 | mW |
| 2× Mode, $f_{DAC}$ = 320 MSPS, IF = 16 MHz, PLL Off | | 498 | | | 498 | | | 498 | | mW |
| 2× Mode, $f_{DAC}$ = 320 MSPS, IF = 16 MHz, PLL On | | 588 | | | 588 | | | 588 | | mW |
| 4× Mode, $f_{DAC}/4$ Modulation, $f_{DAC}$ = 500 MSPS, IF = 137.5 MHz, Q DAC Off | | 572 | | | 572 | | | 572 | | mW |

| Parameter | AD9776 | | | AD9778 | | | AD9779 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| 8× Mode, $f_{DAC}/4$ Modulation, $f_{DAC}$ = 1 GSPS, IF = 262.5 MHz | | 980 | | | 980 | | | 980 | | mW |
| Power-Down Mode | | 2 | 3.7 | | 2 | 3.7 | | 2 | 3.7 | mW |
| Power Supply Rejection Ratio, AVDD33 | −0.3 | | +0.3 | −0.3 | | +0.3 | −0.3 | | +0.3 | % FSR/V |
| OPERATING RANGE | −40 | +25 | +85 | −40 | +25 | +85 | −40 | +25 | +85 | °C |

[1] Based on a 10 kΩ external resistor.

## DIGITAL SPECIFICATIONS

$T_{MIN}$ to $T_{MAX}$, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, $I_{OUTFS}$ = 20 mA, maximum sample rate, unless otherwise noted. LVDS driver and receiver are compliant to the IEEE-1596 reduced range link, unless otherwise noted.

**Table 2. AD9776, AD9778, and AD9779 Digital Specifications**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| CMOS INPUT LOGIC LEVEL | | | | | |
| Input $V_{IN}$ Logic High | | 2.0 | | | V |
| Input $V_{IN}$ Logic Low | | | | 0.8 | V |
| Maximum Input Data Rate at Interpolation | | | | | |
| 1× | | 300 | | | MSPS |
| 2× | | 250 | | | MSPS |
| 4× | | 200 | | | MSPS |
| 8× | | 125 | | | MSPS |
| CMOS OUTPUT LOGIC LEVEL (DATACLK, PIN 37)[1] | | | | | |
| Output $V_{OUT}$ Logic High | | 2.4 | | | V |
| Output $V_{OUT}$ Logic Low | | | | 0.4 | V |
| LVDS RECEIVER INPUTS (SYNC_I+, SYNC_I–) | SYNC_I+ = $V_{IA}$, SYNC_I– = $V_{IB}$ | | | | |
| Input Voltage Range, $V_{IA}$ or $V_{IB}$ | | 825 | | 1575 | mV |
| Input Differential Threshold, $V_{IDTH}$ | | −100 | | +100 | mV |
| Input Differential Hysteresis, $V_{IDTHH} - V_{IDTHL}$ | | | 20 | | mV |
| Receiver Differential Input Impedance, $R_{IN}$[2] | | 80 | | 120 | Ω |
| LVDS Input Rate | | | | 125 | MSPS |
| Set-Up Time, SYNC_I to DAC Clock | | −0.2 | | | ns |
| Hold Time, SYNC_I to DAC Clock | | 1 | | | ns |
| LVDS DRIVER OUTPUTS (SYNC_O+, SYNC_O–) | SYNC_O+ = $V_{OA}$, SYNC_O– = $V_{OB}$, 100 Ω termination | | | | |
| Output Voltage High, $V_{OA}$ or $V_{OB}$ | | 825 | | 1575 | mV |
| Output Voltage Low, $V_{OA}$ or $V_{OB}$ | | 1025 | | | mV |
| Output Differential Voltage, $\|V_{OD}\|$ | | 150 | 200 | 250 | mV |
| Output Offset Voltage, $V_{OS}$ | | 1150 | | 1250 | mV |
| Output Impedance, $R_O$ | Single-ended | 80 | 100 | 120 | Ω |
| Maximum Clock Rate | | 1 | | | GHz |
| DAC CLOCK INPUT (CLK+, CLK–) | | | | | |
| Differential Peak-to-Peak Voltage (CLK+, CLK–)[3] | | 400 | 800 | 2000 | mV |
| Common-Mode Voltage | | 300 | 400 | 500 | mV |
| Maximum Clock Rate[4] | | 1 | | | GSPS |
| SERIAL PERIPHERAL INTERFACE | | | | | |
| Maximum Clock Rate (SCLK) | | 40 | | | MHz |
| Minimum Pulse Width High | | | | 12.5 | ns |
| Minimum Pulse Width Low | | | | 12.5 | ns |

[1] Specification is at a DATACLK frequency of 100 MHz into a 1 kΩ load; maximum drive capability of 8 mA. At higher speeds or greater loads, best practice suggests using an external buffer for this signal.
[2] Guaranteed at 25°C. Can drift above 120 Ω at temperatures above 25°C.
[3] When using the PLL, a differential swing of 2 V p-p is recommended.
[4] Typical maximum clock rate when DVDD18 = CVDD18 = 1.9 V.

## DIGITAL INPUT DATA TIMING SPECIFICATIONS

**Table 3. AD9776, AD9778, and AD9779 Digital Input Data Timing Specifications**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| INPUT DATA (ALL MODES, −40°C to +85°C)[1] | | | | |
| Set-Up Time, Input Data to DATACLK | +2.5 | | | ns |
| Hold Time, Input Data to DATACLK | −0.4 | | | ns |
| Set-Up Time, Input Data to REFCLK | −0.8 | | | ns |
| Hold Time, Input Data to REFCLK | +2.9 | | | ns |

[1] Timing vs. temperature and data valid keep out windows are delineated in Table 19.

## AC SPECIFICATIONS

$T_{MIN}$ to $T_{MAX}$, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, $I_{OUTFS}$ = 20 mA, maximum sample rate, unless otherwise noted.

**Table 4. AD9776, AD9778, and AD9779 AC Specifications**

| | AD9776 | | | AD9778 | | | AD9779 | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Unit |
| SPURIOUS FREE DYNAMIC RANGE (SFDR) | | | | | | | | | | |
| $f_{DAC}$ = 100 MSPS, $f_{OUT}$ = 20 MHz | | 82 | | | 82 | | | 82 | | dBc |
| $f_{DAC}$ = 200 MSPS, $f_{OUT}$ = 50 MHz | | 81 | | | 81 | | | 82 | | dBc |
| $f_{DAC}$ = 400 MSPS, $f_{OUT}$ = 70 MHz | | 80 | | | 80 | | | 80 | | dBc |
| $f_{DAC}$ = 800 MSPS, $f_{OUT}$ = 70 MHz | | 85 | | | 85 | | | 87 | | dBc |
| TWO-TONE INTERMODULATION DISTORTION (IMD) | | | | | | | | | | |
| $f_{DAC}$ = 200 MSPS, $f_{OUT}$ = 50 MHz | | 87 | | | 87 | | | 91 | | dBc |
| $f_{DAC}$ = 400 MSPS, $f_{OUT}$ = 60 MHz | | 80 | | | 85 | | | 85 | | dBc |
| $f_{DAC}$ = 400 MSPS, $f_{OUT}$ = 80 MHz | | 75 | | | 81 | | | 81 | | dBc |
| $f_{DAC}$ = 800 MSPS, $f_{OUT}$ = 100 MHz | | 75 | | | 80 | | | 81 | | dBc |
| NOISE SPECTRAL DENSITY (NSD) EIGHT-TONE, 500 kHz TONE SPACING | | | | | | | | | | |
| $f_{DAC}$ = 200 MSPS, $f_{OUT}$ = 80 MHz | | −152 | | | −155 | | | −158 | | dBm/Hz |
| $f_{DAC}$ = 400 MSPS, $f_{OUT}$ = 80 MHz | | −155 | | | −159 | | | −160 | | dBm/Hz |
| $f_{DAC}$ = 800 MSPS, $f_{OUT}$ = 80 MHz | | −157.5 | | | −160 | | | −161 | | dBm/Hz |
| WCDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER | | | | | | | | | | |
| $f_{DAC}$ = 491.52 MSPS, $f_{OUT}$ = 100 MHz | | 76 | | | 78 | | | 79 | | dBc |
| $f_{DAC}$ = 491.52 MSPS, $f_{OUT}$ = 200 MHz | | 69 | | | 73 | | | 74 | | dBc |
| WCDMA SECOND ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER | | | | | | | | | | |
| $f_{DAC}$ = 491.52 MSPS, $f_{OUT}$ = 100 MHz | | 77.5 | | | 80 | | | 81 | | dBc |
| $f_{DAC}$ = 491.52 MSPS, $f_{OUT}$ = 200 MHz | | 76 | | | 78 | | | 78 | | dBc |

# ABSOLUTE MAXIMUM RATINGS

**Table 5.**

| Parameter | With Respect To | Rating |
|---|---|---|
| AVDD33, DVDD33 | AGND, DGND, CGND | −0.3 V to +3.6 V |
| DVDD18, CVDD18 | AGND, DGND, CGND | −0.3 V to +1.98 V |
| AGND | DGND, CGND | −0.3 V to +0.3 V |
| DGND | AGND, CGND | −0.3 V to +0.3 V |
| CGND | AGND, DGND | −0.3 V to +0.3 V |
| I120, VREF, IPTAT | AGND | −0.3 V to AVDD33 + 0.3 V |
| $I_{OUT1-P}$, $I_{OUT1-N}$, $I_{OUT2-P}$, $I_{OUT2-N}$, $Aux_{1-P}$, $Aux_{1-N}$, $Aux_{2-P}$, $Aux_{2-N}$ | AGND | −1.0 V to AVDD33 + 0.3 V |
| P1D15 to P1D0, P2D15 to P2D0 | DGND | −0.3 V to DVDD33 + 0.3 V |
| DATACLK, TXENABLE | DGND | −0.3 V to DVDD33 + 0.3 V |
| CLK+, CLK− | CGND | −0.3 V to CVDD18 + 0.3 V |
| RESET, IRQ, PLL_LOCK, SYNC_O+, SYNC_O−, SYNC_I+, SYNC_I−, CSB, SCLK, SDIO, SDO | DGND | −0.3 V to DVDD33 + 0.3 V |
| Junction Temperature | | +125°C |
| Storage Temperature Range | | −65°C to +150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

100-lead, thermally enhanced TQFP_EP package, $\theta_{JA}$ = 19.1°C/W with the bottom EPAD soldered to the PCB. With the bottom EPAD not soldered to the PCB, $\theta_{JA}$ = 27.4°C/W. These specifications are valid with no airflow movement.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

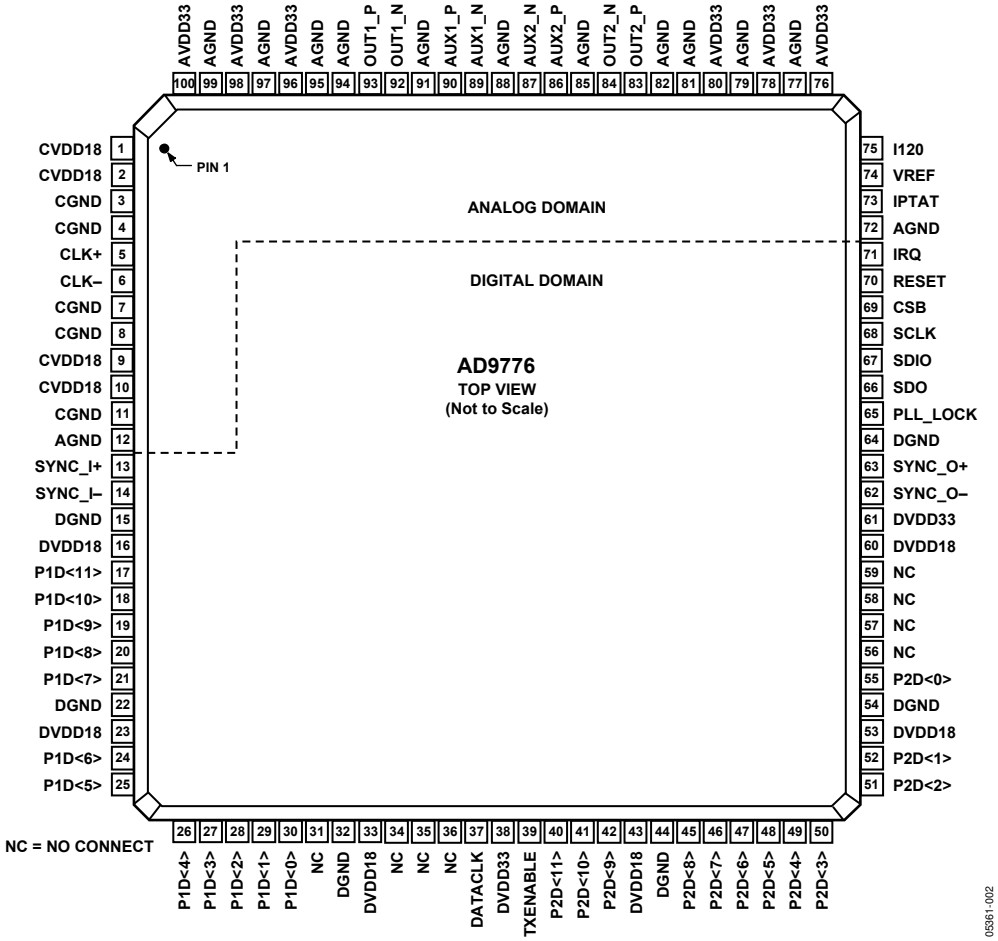



*Figure 3. AD9776 Pin Configuration*

**Table 6. AD9776 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | CVDD18 | 1.8 V Clock Supply. |
| 2 | CVDD18 | 1.8 V Clock Supply. |
| 3 | CGND | Clock Common. |
| 4 | CGND | Clock Common. |
| 5 | CLK+[1] | Differential Clock Input. |
| 6 | CLK–[1] | Differential Clock Input. |
| 7 | CGND | Clock Common. |
| 8 | CGND | Clock Common. |
| 9 | CVDD18 | 1.8 V Clock Supply. |
| 10 | CVDD18 | 1.8 V Clock Supply. |
| 11 | CGND | Clock Common. |
| 12 | AGND | Analog Common. |
| 13 | SYNC_I+ | Differential Synchronization Input. |
| 14 | SYNC_I– | Differential Synchronization Input. |
| 15 | DGND | Digital Common. |
| 16 | DVDD18 | 1.8 V Digital Supply. |
| 17 | P1D<11> | Port 1, Data Input D11 (MSB). |
| 18 | P1D<10> | Port 1, Data Input D10. |
| 19 | P1D<9> | Port 1, Data Input D9. |
| 20 | P1D<8> | Port 1, Data Input D8. |
| 21 | P1D<7> | Port 1, Data Input D7. |
| 22 | DGND | Digital Common. |
| 23 | DVDD18 | 1.8 V Digital Supply. |
| 24 | P1D<6> | Port 1, Data Input D6. |
| 25 | P1D<5> | Port 1, Data Input D5. |
| 26 | P1D<4> | Port 1, Data Input D4. |
| 27 | P1D<3> | Port 1, Data Input D3. |
| 28 | P1D<2> | Port 1, Data Input D2. |
| 29 | P1D<1> | Port 1, Data Input D1. |
| 30 | P1D<0> | Port 1, Data Input D0 (LSB). |
| 31 | NC | No Connect. |
| 32 | DGND | Digital Common. |
| 33 | DVDD18 | 1.8 V Digital Supply. |
| 34 | NC | No Connect. |
| 35 | NC | No Connect. |
| 36 | NC | No Connect. |
| 37 | DATACLK | Data Clock Output. |
| 38 | DVDD33 | 3.3 V Digital Supply. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 39 | TXENABLE | Transmit Enable. |
| 40 | P2D<11> | Port 2, Data Input D11 (MSB). |
| 41 | P2D<10> | Port 2, Data Input D10. |
| 42 | P2D<9> | Port 2, Data Input D9. |
| 43 | DVDD18 | 1.8 V Digital Supply. |
| 44 | DGND | Digital Common. |
| 45 | P2D<8> | Port 2, Data Input D8. |
| 46 | P2D<7> | Port 2, Data Input D7. |
| 47 | P2D<6> | Port 2, Data Input D6. |
| 48 | P2D<5> | Port 2, Data Input D5. |
| 49 | P2D<4> | Port 2, Data Input D4. |
| 50 | P2D<3> | Port 2, Data Input D3. |
| 51 | P2D<2> | Port 2, Data Input D2. |
| 52 | P2D<1> | Port 2, Data Input D1. |
| 53 | DVDD18 | 1.8 V Digital Supply. |
| 54 | DGND | Digital Common. |
| 55 | P2D<0> | Port 2, Data Input D0 (LSB). |
| 56 | NC | No Connect. |
| 57 | NC | No Connect. |
| 58 | NC | No Connect. |
| 59 | NC | No Connect. |
| 60 | DVDD18 | 1.8 V Digital Supply. |
| 61 | DVDD33 | 3.3 V Digital Supply. |
| 62 | SYNC_O– | Differential Synchronization Output. |
| 63 | SYNC_O+ | Differential Synchronization Output |
| 64 | DGND | Digital Common |
| 65 | PLL_LOCK | PLL Lock Indicator |
| 66 | SDO | SPI Port Data Output |
| 67 | SDIO | SPI Port Data Input/Output |
| 68 | SCLK | SPI Port Clock |
| 69 | CSB | SPI Port Chip Select Bar. |
| 70 | RESET | Reset, Active High. |
| 71 | IRQ | Interrupt Request. |
| 72 | AGND | Analog Common. |
| 73 | IPTAT | Factory Test Pin. Output current is proportional to absolute temperature, approximately 10 µA at 25°C with approximately 20 nA/°C slope. This pin should remain floating. |
| 74 | VREF | Voltage Reference Output. |
| 75 | I120 | 120 µA Reference Current. |
| 76 | AVDD33 | 3.3 V Analog Supply. |
| 77 | AGND | Analog Common. |
| 78 | AVDD33 | 3.3 V Analog Supply. |
| 79 | AGND | Analog Common. |
| 80 | AVDD33 | 3.3 V Analog Supply. |
| 81 | AGND | Analog Common. |
| 82 | AGND | Analog Common. |
| 83 | OUT2_P | Differential DAC Current Output, Channel 2. |
| 84 | OUT2_N | Differential DAC Current Output, Channel 2. |
| 85 | AGND | Analog Common. |
| 86 | AUX2_P | Auxiliary DAC Current Output, Channel 2. |
| 87 | AUX2_N | Auxiliary DAC Current Output, Channel 2. |
| 88 | AGND | Analog Common. |
| 89 | AUX1_N | Auxiliary DAC Current Output, Channel 1. |
| 90 | AUX1_P | Auxiliary DAC Current Output, Channel 1. |
| 91 | AGND | Analog Common. |
| 92 | OUT1_N | Differential DAC Current Output, Channel 1. |
| 93 | OUT1_P | Differential DAC Current Output, Channel 1. |
| 94 | AGND | Analog Common. |
| 95 | AGND | Analog Common. |
| 96 | AVDD33 | 3.3 V Analog Supply. |
| 97 | AGND | Analog Common. |
| 98 | AVDD33 | 3.3 V Analog Supply. |
| 99 | AGND | Analog Common. |
| 100 | AVDD33 | 3.3 V Analog Supply. |

[1] The combined differential clock input at the CLK+ and CLK– pins are referred to as REFCLK.

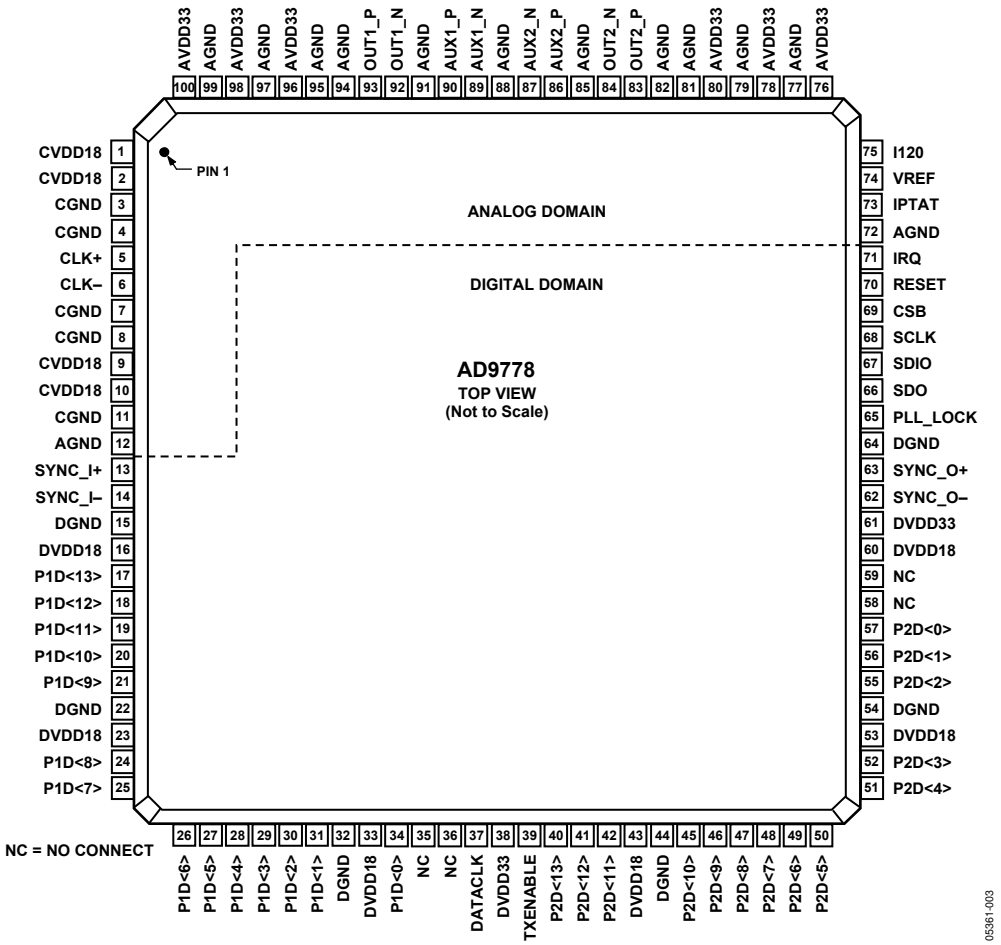



*Figure 4. AD9778 Pin Configuration*

**Table 7. AD9778 Pin Function Description**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | CVDD18 | 1.8 V Clock Supply. |
| 2 | CVDD18 | 1.8 V Clock Supply. |
| 3 | CGND | Clock Common. |
| 4 | CGND | Clock Common. |
| 5 | CLK+[1] | Differential Clock Input. |
| 6 | CLK–[1] | Differential Clock Input. |
| 7 | CGND | Clock Common. |
| 8 | CGND | Clock Common. |
| 9 | CVDD18 | 1.8 V Clock Supply. |
| 10 | CVDD18 | 1.8 V Clock Supply. |
| 11 | CGND | Clock Common. |
| 12 | AGND | Analog Common. |
| 13 | SYNC_I+ | Differential Synchronization Input. |
| 14 | SYNC_I– | Differential Synchronization Input. |
| 15 | DGND | Digital Common. |
| 16 | DVDD18 | 1.8 V Digital Supply. |
| 17 | P1D<13> | Port 1, Data Input D13 (MSB). |
| 18 | P1D<12> | Port 1, Data Input D12. |
| 19 | P1D<11> | Port 1, Data Input D11. |
| 20 | P1D<10> | Port 1, Data Input D10. |
| 21 | P1D<9> | Port 1, Data Input D9. |
| 22 | DGND | Digital Common. |
| 23 | DVDD18 | 1.8 V Digital Supply. |
| 24 | P1D<8> | Port 1, Data Input D8. |
| 25 | P1D<7> | Port 1, Data Input D7. |
| 26 | P1D<6> | Port 1, Data Input D6. |
| 27 | P1D<5> | Port 1, Data Input D5. |
| 28 | P1D<4> | Port 1, Data Input D4. |
| 29 | P1D<3> | Port 1, Data Input D3. |
| 30 | P1D<2> | Port 1, Data Input D2. |
| 31 | P1D<1> | Port 1, Data Input D1. |
| 32 | DGND | Digital Common. |
| 33 | DVDD18 | 1.8 V Digital Supply. |
| 34 | P1D<0> | Port 1, Data Input D0 (LSB). |
| 35 | NC | No Connect. |
| 36 | NC | No Connect. |
| 37 | DATACLK | Data Clock Output. |
| 38 | DVDD33 | 3.3 V Digital Supply. |
| 39 | TXENABLE | Transmit Enable. |
| 40 | P2D<13> | Port 2, Data Input D13 (MSB). |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 41 | P2D<12> | Port 2, Data Input D12. |
| 42 | P2D<11> | Port 2, Data Input D11. |
| 43 | DVDD18 | 1.8 V Digital Supply. |
| 44 | DGND | Digital Common. |
| 45 | P2D<10> | Port 2, Data Input D10. |
| 46 | P2D<9> | Port 2, Data Input D9. |
| 47 | P2D<8> | Port 2, Data Input D8. |
| 48 | P2D<7> | Port 2, Data Input D7. |
| 49 | P2D<6> | Port 2, Data Input D6. |
| 50 | P2D<5> | Port 2, Data Input D5. |
| 51 | P2D<4> | Port 2, Data Input D4. |
| 52 | P2D<3> | Port 2, Data Input D3. |
| 53 | DVDD18 | 1.8 V Digital Supply. |
| 54 | DGND | Digital Common. |
| 55 | P2D<2> | Port 2, Data Input D2. |
| 56 | P2D<1> | Port 2, Data Input D1. |
| 57 | P2D<0> | Port 2, Data Input D0 (LSB). |
| 58 | NC | No Connect. |
| 59 | NC | No Connect. |
| 60 | DVDD18 | 1.8 V Digital Supply. |
| 61 | DVDD33 | 3.3 V Digital Supply. |
| 62 | SYNC_O– | Differential Synchronization Output. |
| 63 | SYNC_O+ | Differential Synchronization Output. |
| 64 | DGND | Digital Common. |
| 65 | PLL_LOCK | PLL Lock Indicator. |
| 66 | SDO | SPI Port Data Output. |
| 67 | SDIO | SPI Port Data Input/Output. |
| 68 | SCLK | SPI Port Clock. |
| 69 | CSB | SPI Port Chip Select Bar. |
| 70 | RESET | Reset, Active High. |
| 71 | IRQ | Interrupt Request. |
| 72 | AGND | Analog Common. |
| 73 | IPTAT | Factory Test Pin. Output current is proportional to absolute temperature, approximately 10 µA at 25°C with approximately 20 nA/°C slope. This pin should remain floating. |
| 74 | VREF | Voltage Reference Output. |
| 75 | I120 | 120 µA Reference Current. |
| 76 | AVDD33 | 3.3 V Analog Supply. |
| 77 | AGND | Analog Common. |
| 78 | AVDD33 | 3.3 V Analog Supply. |
| 79 | AGND | Analog Common. |
| 80 | AVDD33 | 3.3 V Analog Supply. |
| 81 | AGND | Analog Common. |
| 82 | AGND | Analog Common. |
| 83 | OUT2_P | Differential DAC Current Output, Channel 2. |
| 84 | OUT2_N | Differential DAC Current Output, Channel 2. |
| 85 | AGND | Analog Common. |
| 86 | AUX2_P | Auxiliary DAC Current Output, Channel 2. |
| 87 | AUX2_N | Auxiliary DAC Current Output, Channel 2. |
| 88 | AGND | Analog Common. |
| 89 | AUX1_N | Auxiliary DAC Current Output, Channel 1. |
| 90 | AUX1_P | Auxiliary DAC Current Output, Channel 1. |
| 91 | AGND | Analog Common. |
| 92 | OUT1_N | Differential DAC Current Output, Channel 1. |
| 93 | OUT1_P | Differential DAC Current Output, Channel 1. |
| 94 | AGND | Analog Common. |
| 95 | AGND | Analog Common. |
| 96 | AVDD33 | 3.3 V Analog Supply. |
| 97 | AGND | Analog Common. |
| 98 | AVDD33 | 3.3 V Analog Supply. |
| 99 | AGND | Analog Common. |
| 100 | AVDD33 | 3.3 V Analog Supply. |

[1] The combined differential clock input at the CLK+ and CLK– pins are referred to as REFCLK.

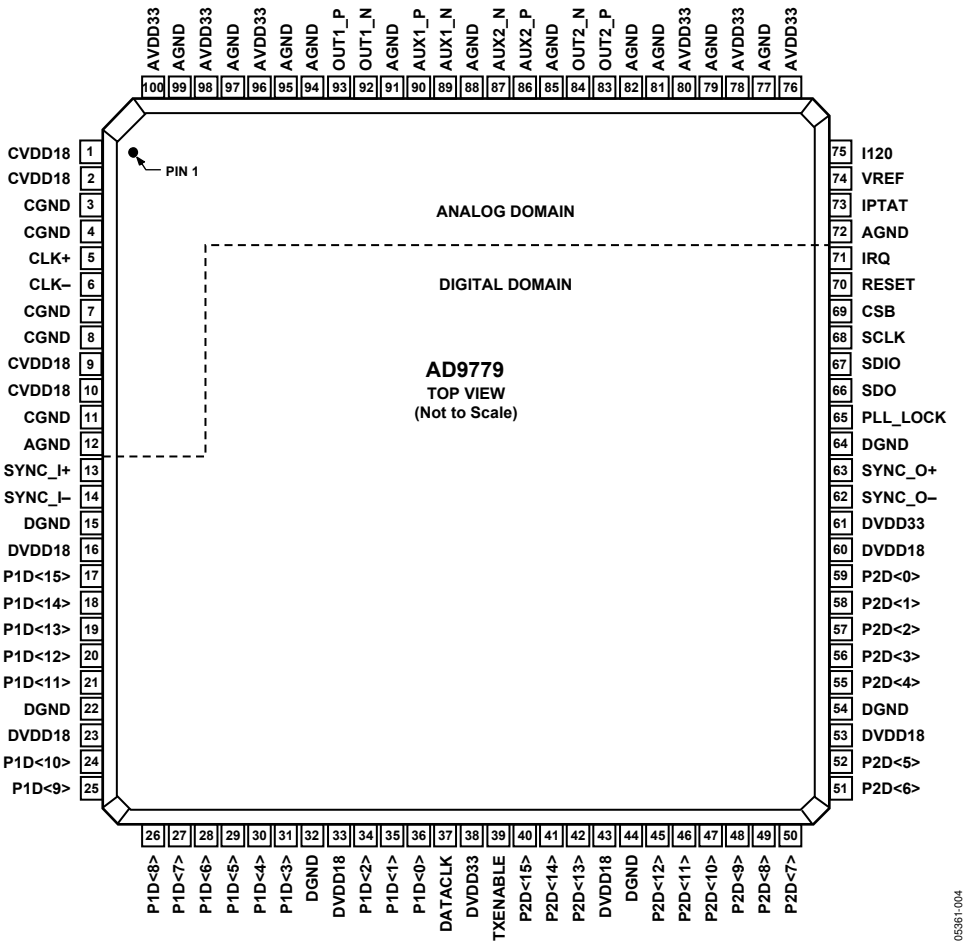



*Figure 5. AD9779 Pin Configuration*

**Table 8. AD9779 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | CVDD18 | 1.8 V Clock Supply. |
| 2 | CVDD18 | 1.8 V Clock Supply. |
| 3 | CGND | Clock Common. |
| 4 | CGND | Clock Common. |
| 5 | CLK+[1] | Differential Clock Input. |
| 6 | CLK–[1] | Differential Clock Input. |
| 7 | CGND | Clock Common. |
| 8 | CGND | Clock Common. |
| 9 | CVDD18 | 1.8 V Clock Supply. |
| 10 | CVDD18 | 1.8 V Clock Supply. |
| 11 | CGND | Clock Common. |
| 12 | AGND | Analog Common. |
| 13 | SYNC_I+ | Differential Synchronization Input. |
| 14 | SYNC_I– | Differential Synchronization Input. |
| 15 | DGND | Digital Common. |
| 16 | DVDD18 | 1.8 V Digital Supply. |
| 17 | P1D<15> | Port 1, Data Input D15 (MSB). |
| 18 | P1D<14> | Port 1, Data Input D14. |
| 19 | P1D<13> | Port 1, Data Input D13. |
| 20 | P1D<12> | Port 1, Data Input D12. |
| 21 | P1D<11> | Port 1, Data Input D11. |
| 22 | DGND | Digital Common. |
| 23 | DVDD18 | 1.8 V Digital Supply. |
| 24 | P1D<10> | Port 1, Data Input D10. |
| 25 | P1D<9> | Port 1, Data Input D9. |
| 26 | P1D<8> | Port 1, Data Input D8. |
| 27 | P1D<7> | Port 1, Data Input D7. |
| 28 | P1D<6> | Port 1, Data Input D6. |
| 29 | P1D<5> | Port 1, Data Input D5. |
| 30 | P1D<4> | Port 1, Data Input D4. |
| 31 | P1D<3> | Port 1, Data Input D3. |
| 32 | DGND | Digital Common. |
| 33 | DVDD18 | 1.8 V Digital Supply. |
| 34 | P1D<2> | Port 1, Data Input D2. |
| 35 | P1D<1> | Port 1, Data Input D1. |
| 36 | P1D<0> | Port 1, Data Input D0 (LSB). |
| 37 | DATACLK | Data Clock Output. |
| 38 | DVDD33 | 3.3 V Digital Supply. |
| 39 | TXENABLE | Transmit Enable. |
| 40 | P2D<15> | Port 2, Data Input D15 (MSB). |
| 41 | P2D<14> | Port 2, Data Input D14. |
| 42 | P2D<13> | Port 2, Data Input D13. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 43 | DVDD18 | 1.8 V Digital Supply. |
| 44 | DGND | Digital Common. |
| 45 | P2D<12> | Port 2, Data Input D12. |
| 46 | P2D<11> | Port 2, Data Input D11. |
| 47 | P2D<10> | Port 2, Data Input D10. |
| 48 | P2D<9> | Port 2, Data Input D9. |
| 49 | P2D<8> | Port 2, Data Input D8. |
| 50 | P2D<7> | Port 2, Data Input D7. |
| 51 | P2D<6> | Port 2, Data Input D6. |
| 52 | P2D<5> | Port 2, Data Input D5. |
| 53 | DVDD18 | 1.8 V Digital Supply. |
| 54 | DGND | Digital Common. |
| 55 | P2D<4> | Port 2, Data Input D4. |
| 56 | P2D<3> | Port 2, Data Input D3. |
| 57 | P2D<2> | Port 2, Data Input D2. |
| 58 | P2D<1> | Port 2, Data Input D1. |
| 59 | P2D<0> | Port 2, Data Input D0 (LSB). |
| 60 | DVDD18 | 1.8 V Digital Supply. |
| 61 | DVDD33 | 3.3 V Digital Supply. |
| 62 | SYNC_O– | Differential Synchronization Output. |
| 63 | SYNC_O+ | Differential Synchronization Output. |
| 64 | DGND | Digital Common. |
| 65 | PLL_LOCK | PLL Lock Indicator. |
| 66 | SPI_SDO | SPI Port Data Output. |
| 67 | SPI_SDIO | SPI Port Data Input/Output. |
| 68 | SCLK | SPI Port Clock. |
| 69 | SPI_CSB | SPI Port Chip Select Bar. |
| 70 | RESET | Reset, Active High. |
| 71 | IRQ | Interrupt Request. |
| 72 | AGND | Analog Common. |
| 73 | IPTAT | Factory Test Pin. Output current is proportional to absolute temperature, approximately 10 µA at 25°C with approximately 20 nA/°C slope. This pin should remain floating. |
| 74 | VREF | Voltage Reference Output. |
| 75 | I120 | 120 µA Reference Current. |
| 76 | AVDD33 | 3.3 V Analog Supply. |
| 77 | AGND | Analog Common. |
| 78 | AVDD33 | 3.3 V Analog Supply. |
| 79 | AGND | Analog Common. |
| 80 | AVDD33 | 3.3 V Analog Supply. |
| 81 | AGND | Analog Common. |
| 82 | AGND | Analog Common. |
| 83 | OUT2_P | Differential DAC Current Output, Channel 2. |
| 84 | OUT2_N | Differential DAC Current Output, Channel 2. |
| 85 | AGND | Analog Common. |
| 86 | AUX2_P | Auxiliary DAC Current Output, Channel 2. |
| 87 | AUX2_N | Auxiliary DAC Current Output, Channel 2. |
| 88 | AGND | Analog Common. |
| 89 | AUX1_N | Auxiliary DAC Current Output, Channel 1. |
| 90 | AUX1_P | Auxiliary DAC Current Output, Channel 1. |
| 91 | AGND | Analog Common. |
| 92 | OUT1_N | Differential DAC Current Output, Channel 1. |
| 93 | OUT1_P | Differential DAC Current Output, Channel 1. |
| 94 | AGND | Analog Common. |
| 95 | AGND | Analog Common. |
| 96 | AVDD33 | 3.3 V Analog Supply. |
| 97 | AGND | Analog Common. |
| 98 | AVDD33 | 3.3 V Analog Supply. |
| 99 | AGND | Analog Common. |
| 100 | AVDD33 | 3.3 V Analog Supply. |

[1] The combined differential clock input at the CLK+ and CLK– pins are referred to as REFCLK.

# TYPICAL PERFORMANCE CHARACTERISTICS

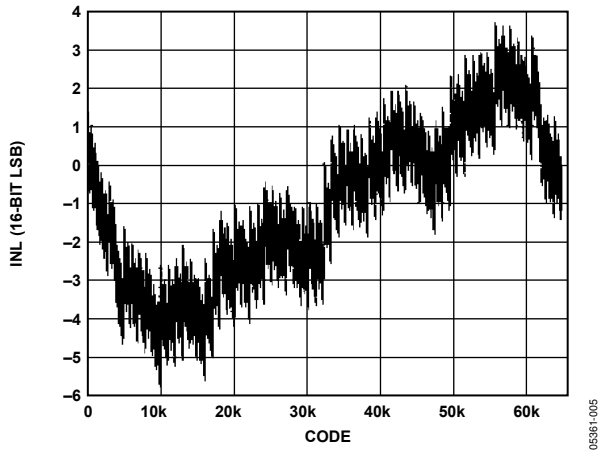



Figure 6. AD9779 Typical INL

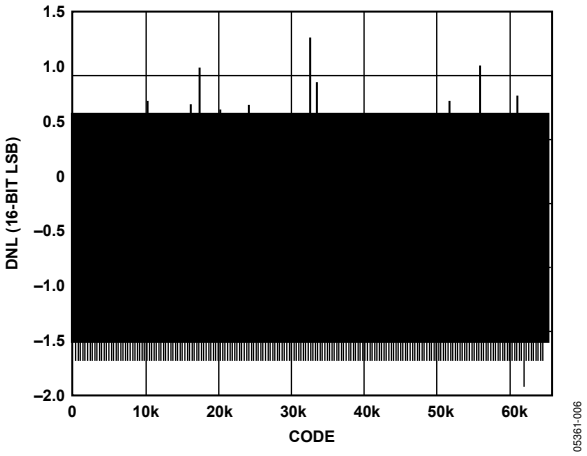



Figure 7. AD9779 Typical DNL

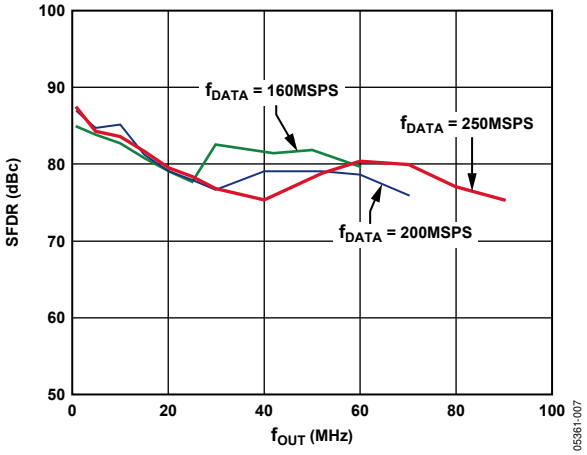



Figure 8. AD9779 In-Band SFDR vs. $f_{OUT}$, 1x Interpolation

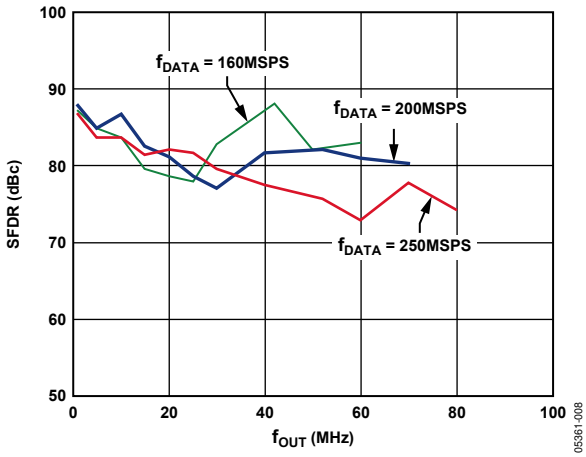



Figure 9. AD9779 In-Band SFDR vs. $f_{OUT}$, 2× Interpolation

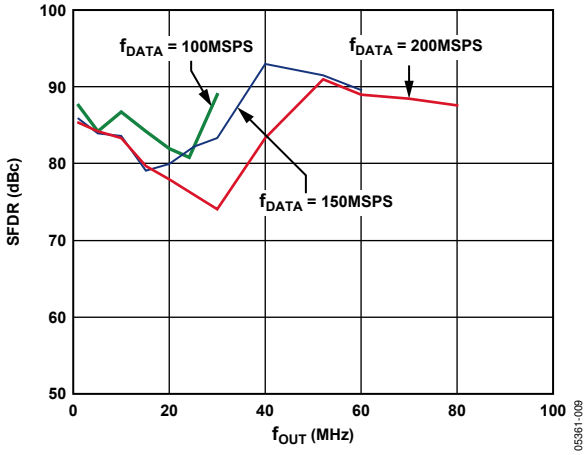



Figure 10. AD9779 In-Band SFDR vs. $f_{OUT}$, 4× Interpolation

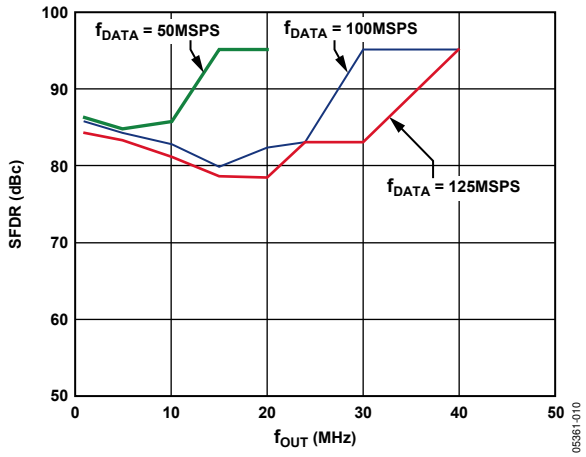



Figure 11. AD9779 In-Band SFDR vs. $f_{OUT}$, 8× Interpolation

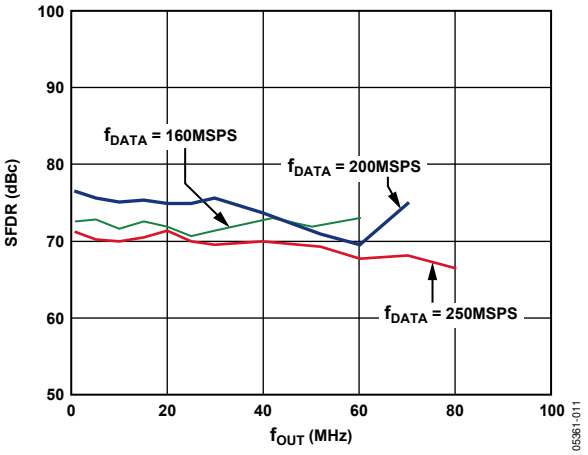



Figure 12. AD9779 Out-of-Band SFDR vs. $f_{OUT}$, 2× Interpolation

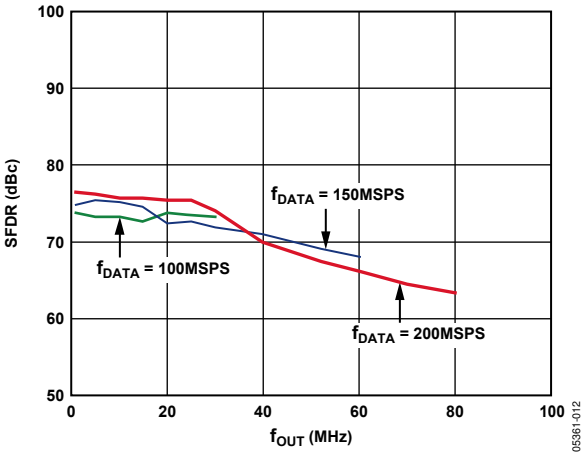



Figure 13. AD9779 Out-of-Band SFDR vs. $f_{OUT}$, 4× Interpolation

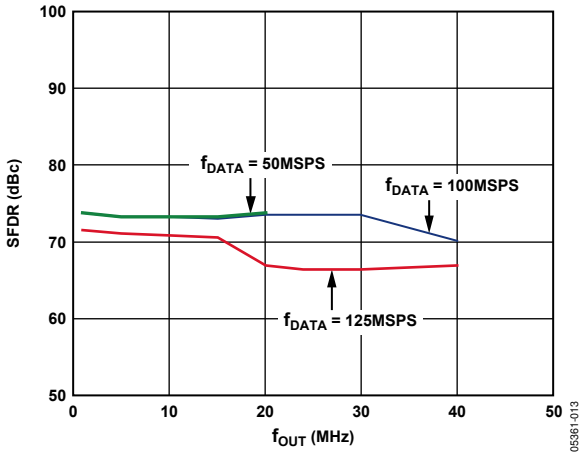



Figure 14. AD9779 Out-of-Band SFDR vs. $f_{OUT}$, 8× Interpolation

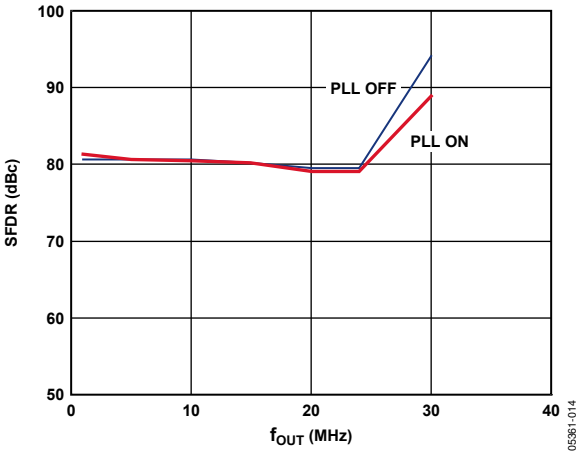



Figure 15. AD9779 In-Band SFDR, 4× Interpolation, $f_{DATA}$ = 100 MSPS, PLL On/Off

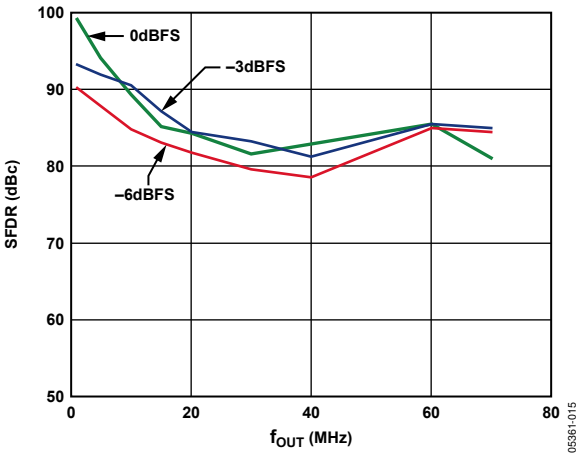



Figure 16. AD9779 In-Band SFDR vs. Digital Full-Scale Input

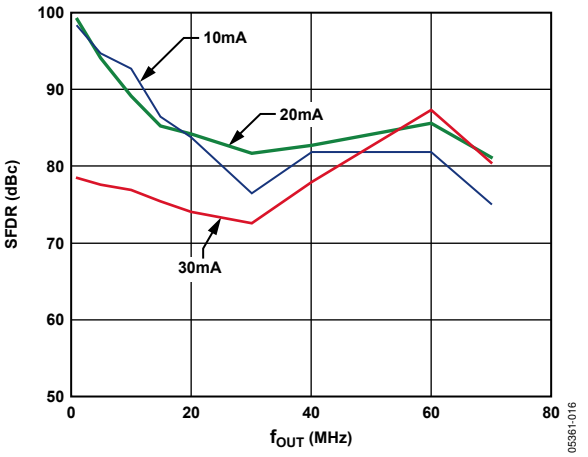



Figure 17. AD9779 In-Band SFDR vs. Output Full-Scale Current

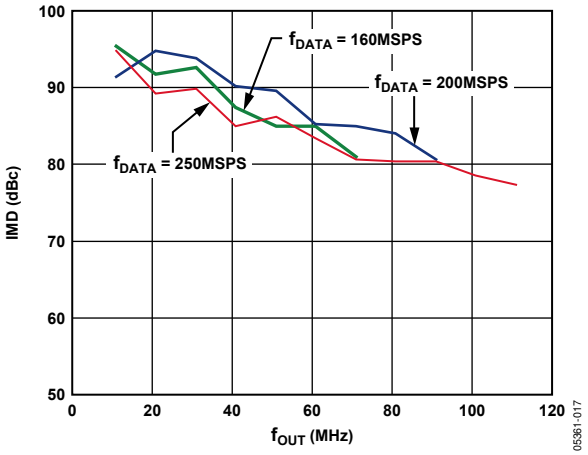



Figure 18. AD9779 Third-Order IMD vs. $f_{OUT}$, 1× Interpolation

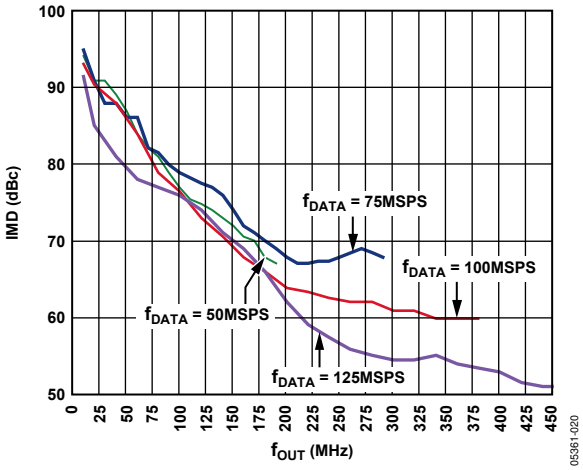



Figure 21. AD9779 Third-Order IMD vs. $f_{OUT}$, 8× Interpolation

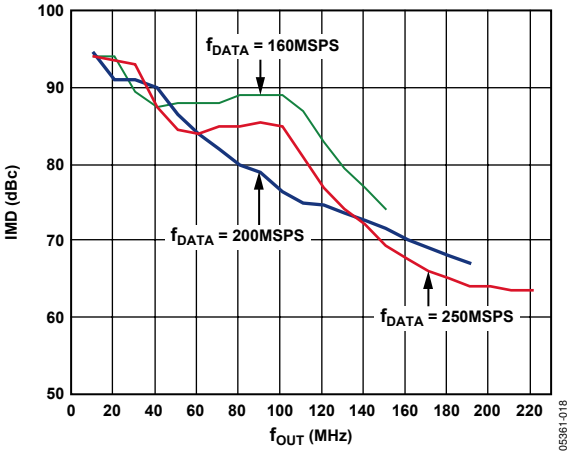



Figure 19. AD9779 Third-Order IMD vs. $f_{OUT}$, 2× Interpolation

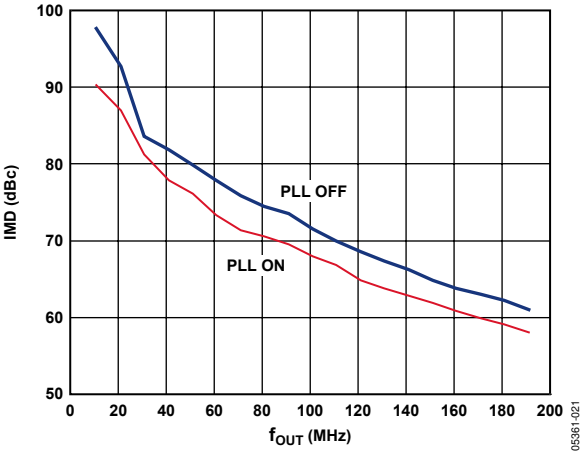



Figure 22. AD9779 Third-Order IMD vs. $f_{OUT}$, 4× Interpolation, $f_{DATA}$ = 100 MSPS, PLL On vs. PLL Off

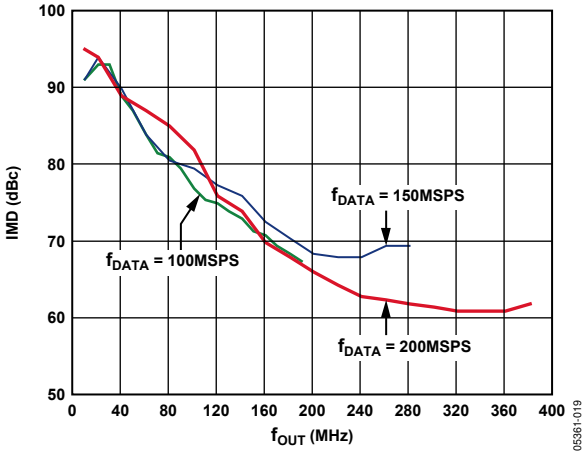



Figure 20. AD9779 Third-Order IMD vs. $f_{OUT}$, 4× Interpolation

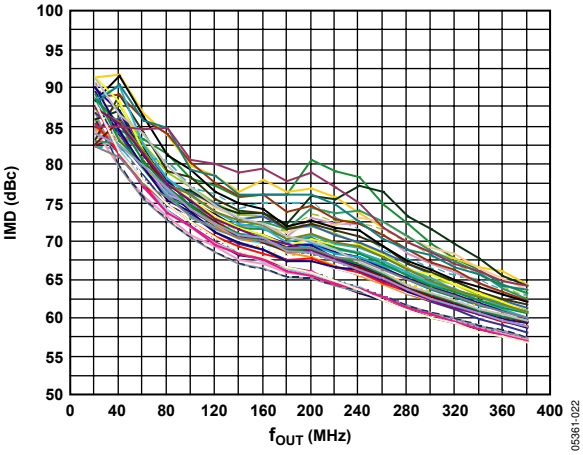



Figure 23. AD9779 Third-Order IMD vs. $f_{OUT}$, over 50 Parts,4× Interpolation, $f_{DATA}$ = 200 MSPS

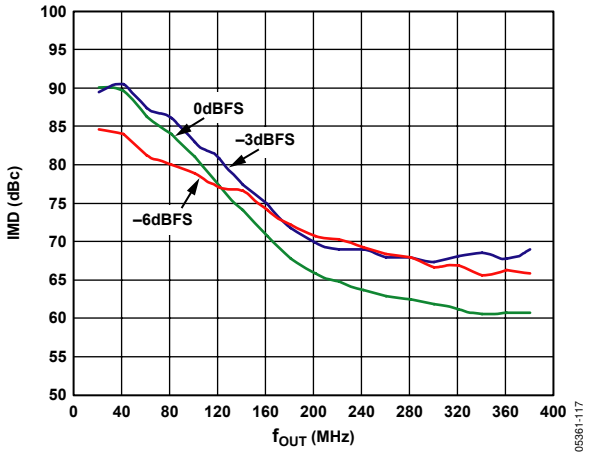



Figure 24. IMD Performance vs. Digital Full-Scale Input, 4× Interpolation, $f_{DATA}$ = 200 MSPS

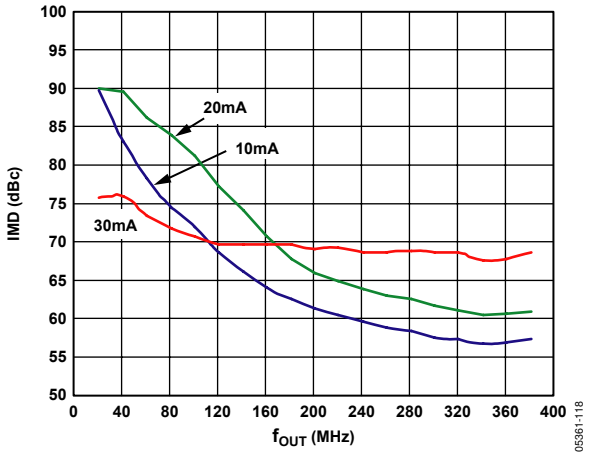



Figure 25. IMD Performance vs. Full-Scale Output Current, 4× Interpolation, $f_{DATA}$ = 200 MSPS

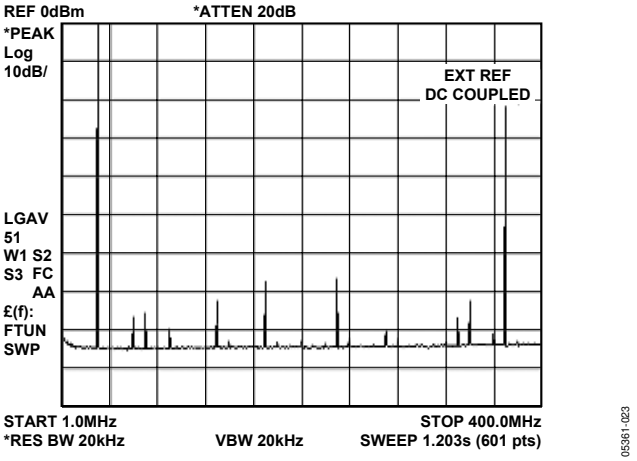



Figure 26. AD9779 Single Tone, 4× Interpolation, $f_{DATA}$ = 100 MSPS, $f_{OUT}$ = 30 MHz

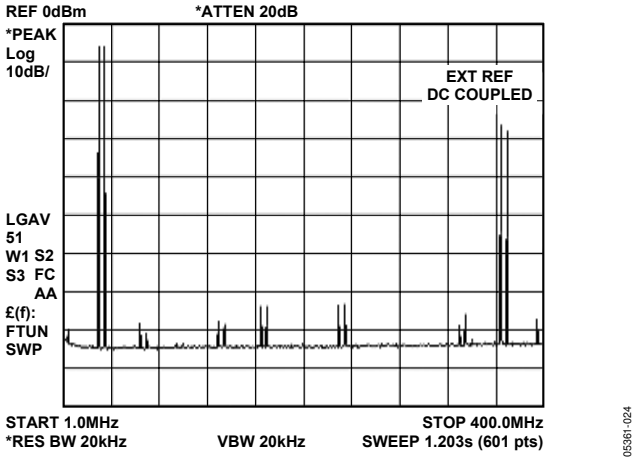



Figure 27. AD9779 Two-Tone Spectrum, 4× Interpolation, $f_{DATA}$ = 100 MSPS, $f_{OUT}$ = 30 MHz, 35 MHz

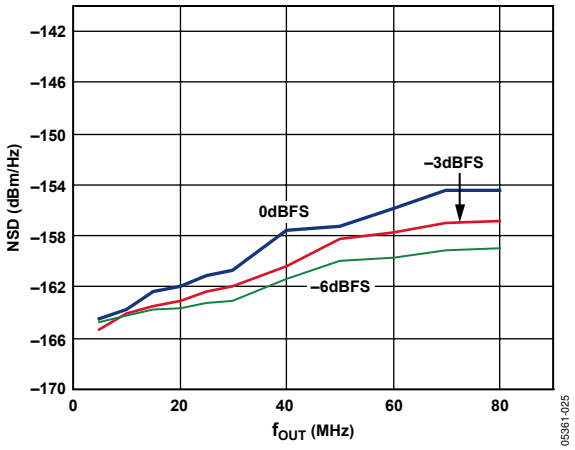



Figure 28. AD9779 Noise Spectral Density vs. Digital Full-Scale of Single-Tone Input, $f_{DATA}$ = 200 MSPS, 2× Interpolation

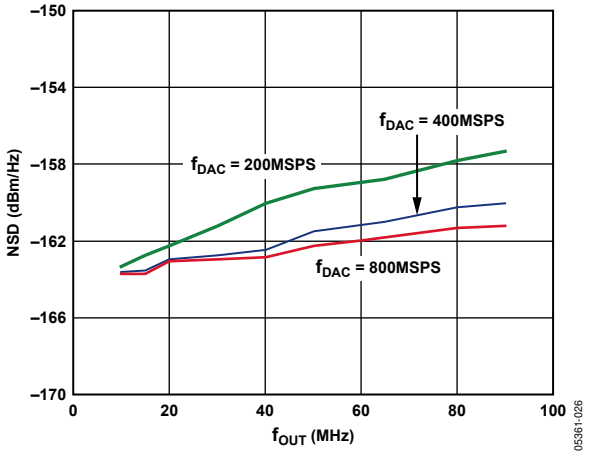



Figure 29. AD9779 Noise Spectral Density vs. $f_{DAC}$, Eight-Tone Input with 500 kHz Spacing, $f_{DATA}$ = 200 MSPS

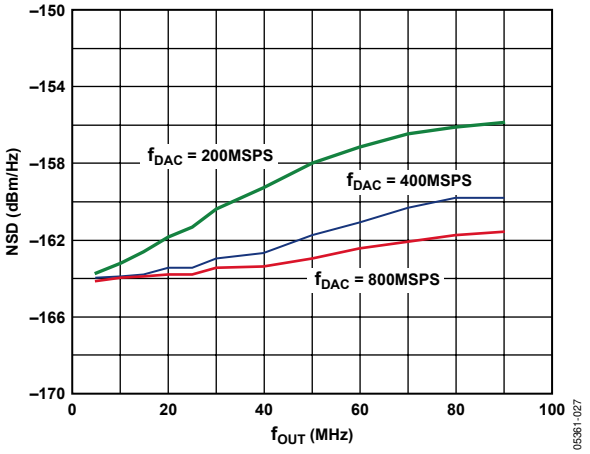



*Figure 30. AD9779 Noise Spectral Density vs. $f_{DAC}$, Single-Tone Input at –6 dBFS*

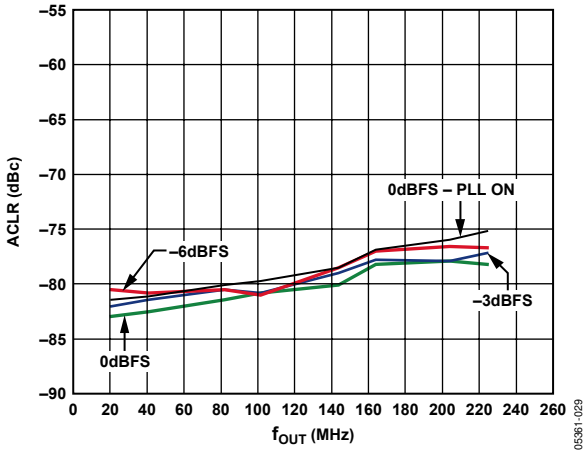



*Figure 32. AD9779 ACLR for Second Adjacent Band WCDMA, 4× Interpolation, $f_{DATA}$ = 122.88 MSPS. On-Chip Modulation Translates Baseband Signal to IF*

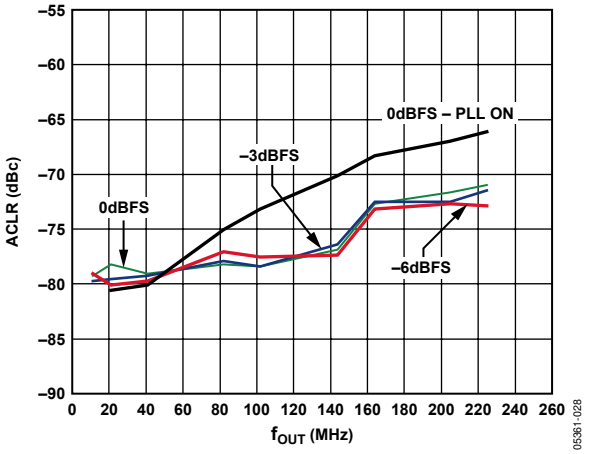



*Figure 31. AD9779 ACLR for First Adjacent Band WCDMA, 4× Interpolation, $f_{DATA}$ = 122.88 MSPS, On-Chip Modulation Translates Baseband Signal to IF*

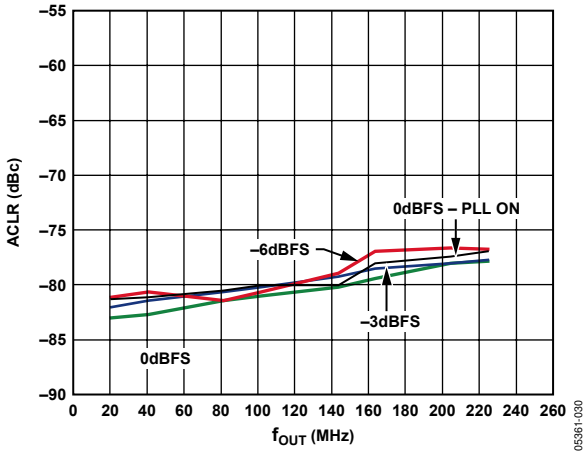
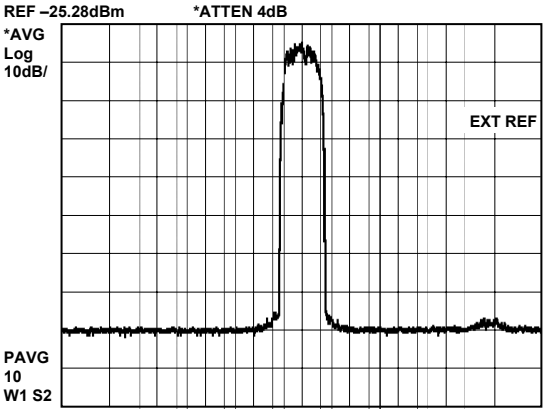



*Figure 33. AD9779 ACLR for Third Adjacent Band WCDMA, 4× Interpolation, $f_{DATA}$ = 122.88 MSPS, On-Chip Modulation Translates Baseband Signal to IF*




| | | | LOWER | | UPPER | |
|---|---|---|---|---|---|---|
| RMS RESULTS | FREQ OFFSET | REF BW | dBc | dBm | dBc | dBm |
| CARRIER POWER | 5.000MHz | 3.840MHz | –76.75 | –89.23 | –77.42 | –89.91 |
| –12.49dBm/ | 10.00MHz | 3.840MHz | –80.94 | –93.43 | –80.47 | –92.96 |
| 3.84000MHz | 15.00MHz | 3.840MHz | –79.95 | –92.44 | –78.96 | –91.45 |

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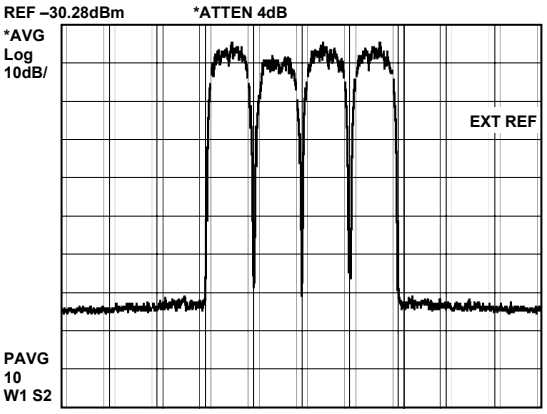
*Figure 34. AD9779 WCDMA Signal, 4× Interpolation, $f_{DATA}$ =122.88 MSPS, $f_{DAC}$/4 Modulation*




| | | | LOWER | | UPPER | |
|---|---|---|---|---|---|---|
| | FREQ OFFSET | INTEG BW | dBc | dBm | dBc | dBm |
| 1 –17.87dBm | 5.000MHz | 3.840MHz | –67.70 | –85.57 | –67.70 | –85.57 |
| 2 –20.65dBm | 10.00MHz | 3.840MHz | –70.00 | –97.87 | –69.32 | –87.19 |
| 3 –18.26dBm | 15.00MHz | 3.840MHz | –71.65 | –99.52 | –71.00 | –88.88 |
| 4 –18.23dBm | | | | | | |

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*Figure 35. AD9779 Multicarrier WCDMA Signal, 4× Interpolation, $f_{DAC}$ =122.88 MSPS, $f_{DAC}$/4 Modulation*

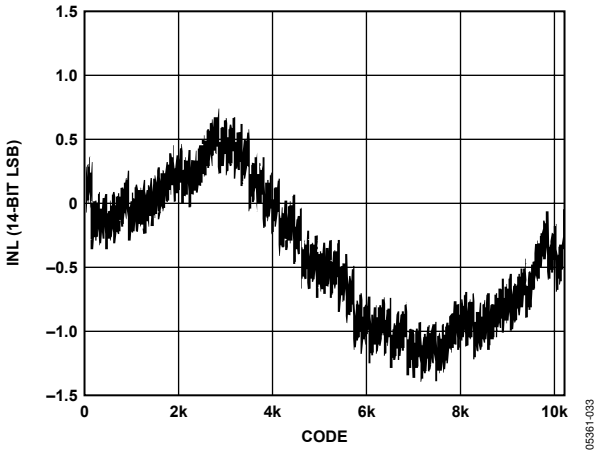


*Figure 36. AD9778 Typical INL*

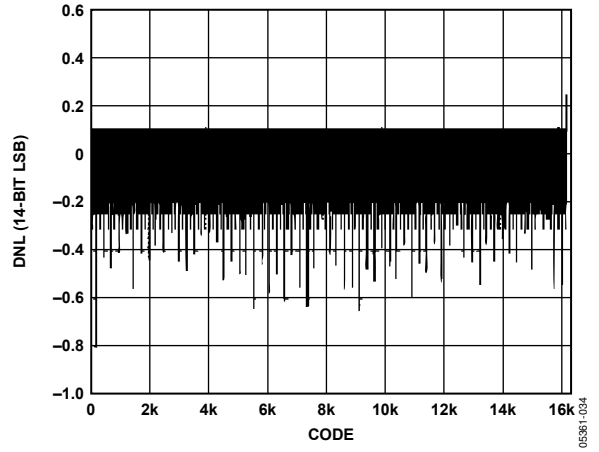


*Figure 37. AD9778 Typical DNL*

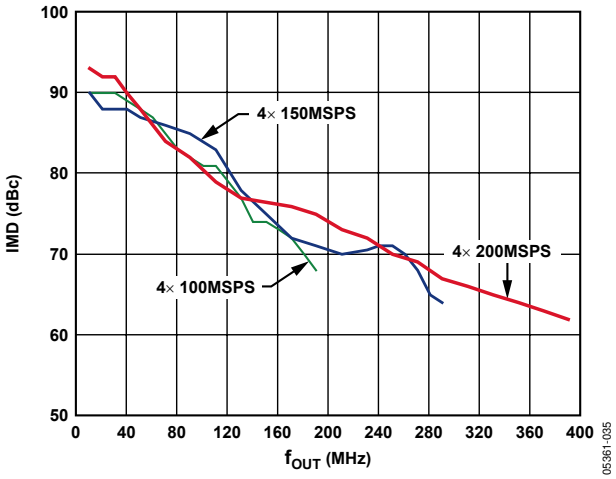


Figure 38. AD9778 IMD, 4× Interpolation

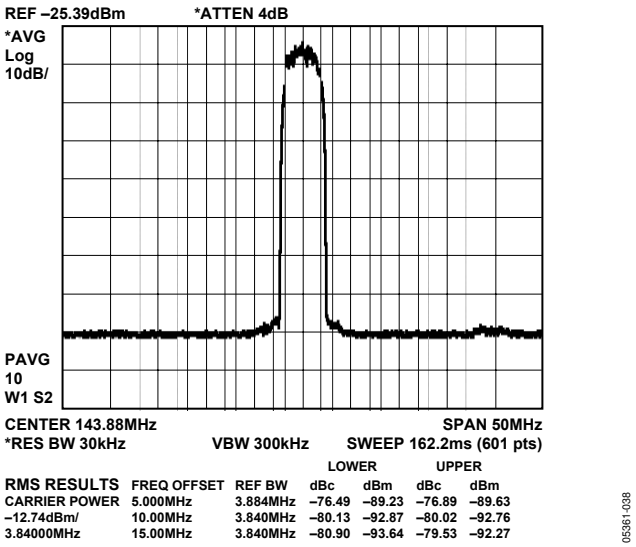


Figure 41. AD9778 ACLR, $f_{DATA}$ = 122.88 MSPS, 4× Interpolation, $f_{DAC}/4$ Modulation

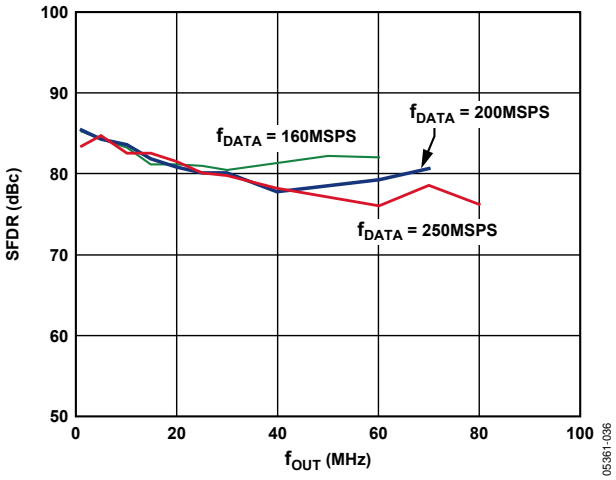


Figure 39. AD9778 In-Band SFDR, 2× Interpolation

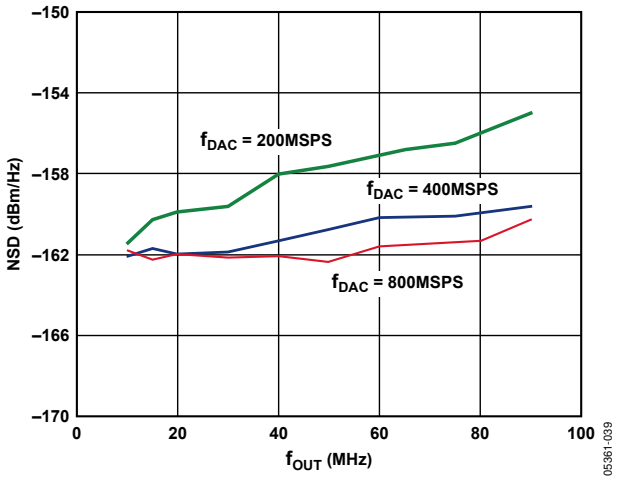


Figure 42. AD9778 Noise Spectral Density vs. $f_{DAC}$ Eight-Tone Input with 500 kHz Spacing, $f_{DATA}$ = 200 MSPS

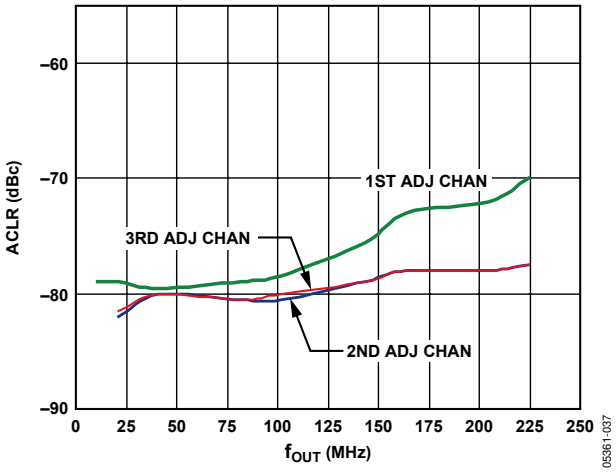


Figure 40. AD9778 ACLR, Single-Carrier WCDMA, 4× Interpolation, $f_{DATA}$ = 122.88 MSPS, Amplitude = –3 dBFS

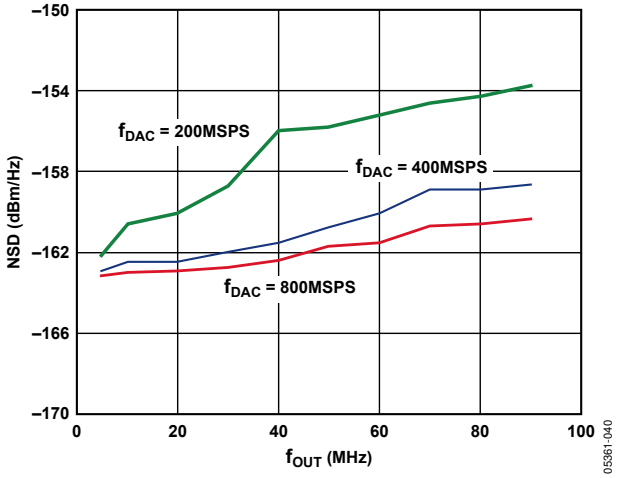


Figure 43. AD9778 Noise Spectral Density vs. $f_{DAC}$ Single-Tone Input at –6 dBFS, $f_{DATA}$ = 200 MSPS

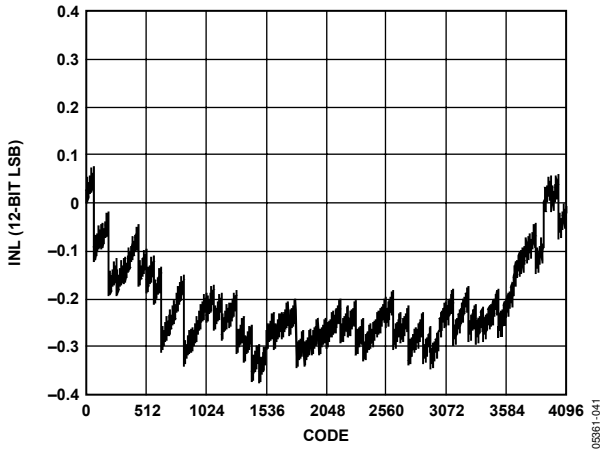


Figure 44. AD9776 Typical INL

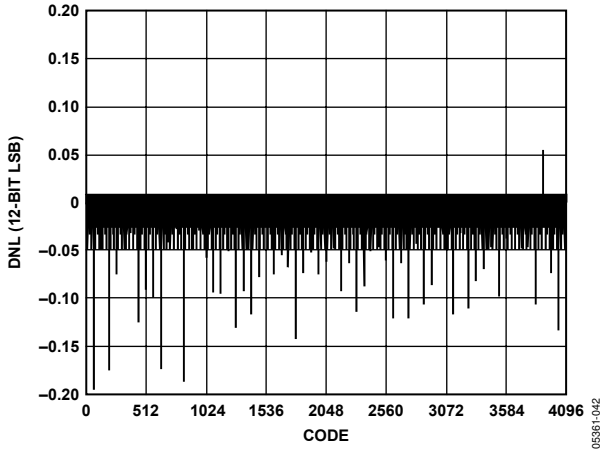


Figure 45. AD9776 Typical DNL

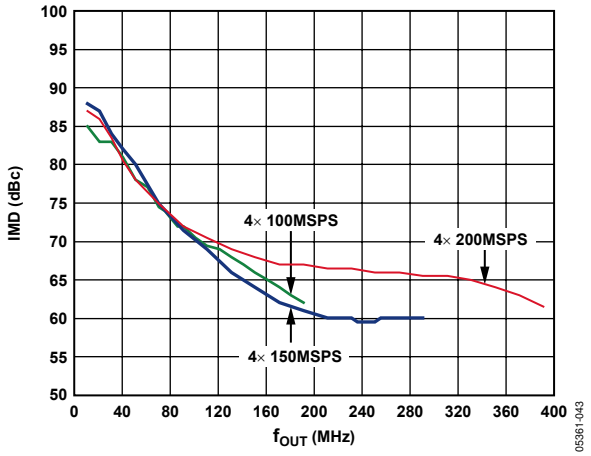


Figure 46. AD9776 IMD, 4× Interpolation

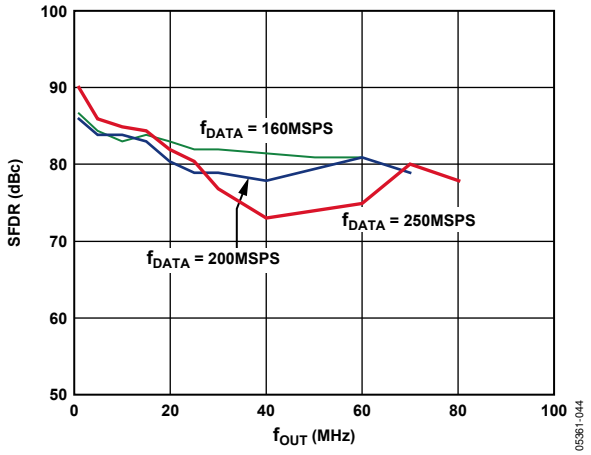


Figure 47. AD9776 In-Band SFDR, 2× Interpolation

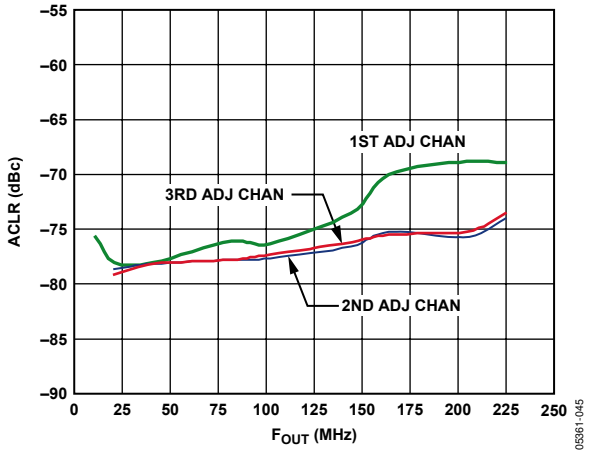


Figure 48. AD9776 ACLR, $f_{DATA}$ = 122.88 MSPS, 4× Interpolation, $f_{DAC}/4$ Modulation

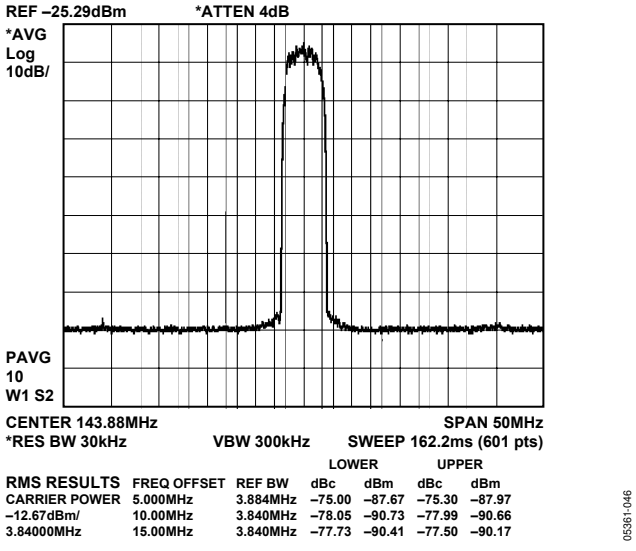


Figure 49. AD9776, Single Carrier WCDMA, 4× Interpolation, $f_{DATA}$ = 122.88 MSPS, Amplitude = –3 dBFS

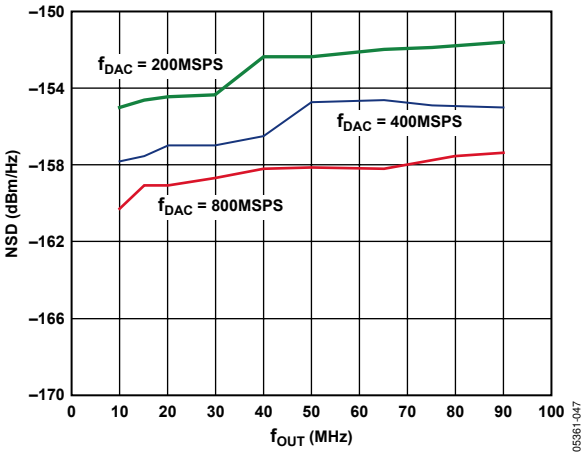


*Figure 50. AD9776 Noise Spectral Density vs. $f_{DAC}$, Eight-Tone Input with 500 kHz Spacing, $f_{DATA}$ = 200 MSPS*

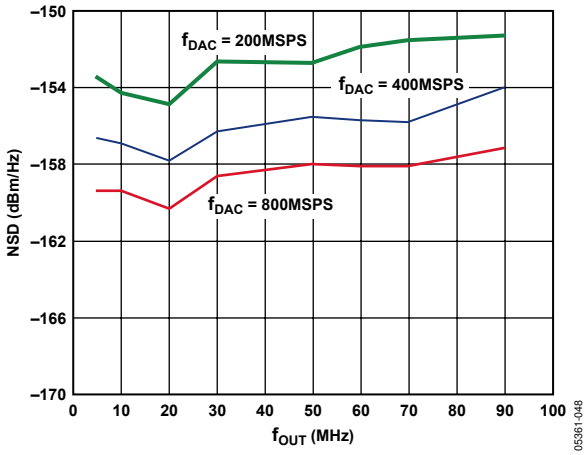


*Figure 51. AD9776 Noise Spectral Density vs. $f_{DAC}$, Single-Tone Input at –6 dBFS, $f_{DATA}$ = 200 MSPS*

# TERMINOLOGY

**Integral Nonlinearity (INL)**

INL is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

**Differential Nonlinearity (DNL)**
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

**Monotonicity**
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

**Offset Error**
The deviation of the output current from the ideal of zero is called offset error. For $I_{OUTA}$, 0 mA output is expected when the inputs are all 0s. For $I_{OUTB}$, 0 mA output is expected when all inputs are set to 1.

**Gain Error**
The difference between the actual and ideal output span. The actual span is determined by the difference between the output when all inputs are set to 1 and the output when all inputs are set to 0.

**Output Compliance Range**
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

**Temperature Drift**
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either $T_{MIN}$ or $T_{MAX}$. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree Celsius. For reference drift, the drift is reported in ppm per degree Celsius.

**Power Supply Rejection (PSR)**
The maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

**Settling Time**
The time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

**In-Band Spurious Free Dynamic Range (SFDR)**
The difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal between dc and the frequency equal to half the input data rate.

**Out-of-Band Spurious Free Dynamic Range (SFDR)**
The difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal within the band that starts at the frequency of the input data rate and ends at the Nyquist frequency of the DAC output sample rate. Normally, energy in this band is rejected by the interpolation filters. This specification, therefore, defines how well the interpolation filters work and the effect of other parasitic coupling paths to the DAC output.

**Total Harmonic Distortion (THD)**
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured fundamental. It is expressed as a percentage or in decibels.

**Signal-to-Noise Ratio (SNR)**
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

**Interpolation Filter**
If the digital inputs to the DAC are sampled at a multiple rate of $f_{DATA}$ (interpolation rate), a digital filter can be constructed that has a sharp transition band near $f_{DATA}/2$. Images that typically appear around $f_{DAC}$ (output data rate) can be greatly suppressed.

**Adjacent Channel Leakage Ratio (ACLR)**
The ratio in dBc between the measured power within a channel relative to its adjacent channel.

**Complex Image Rejection**
In a traditional two-part upconversion, two images are created around the second IF frequency. These images have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

# THEORY OF OPERATION

The AD9776/AD9778/AD9779 combine many features that make them very attractive DACs for wired and wireless communications systems. The dual digital signal path and dual DAC structure allow an easy interface with common quadrature modulators when designing single sideband transmitters. The speed and performance of the parts allow wider bandwidths and more carriers to be synthesized than in previously available DACs. The digital engine uses a breakthrough filter architecture that combines the interpolation with a digital quadrature modulator. This allows the parts to conduct digital quadrature frequency upconversion. They also have features that allow simplified synchronization with incoming data and between multiple parts.

The serial port configuration is controlled by Register 0x00, Bits<6:7>. It is important to note that the configuration changes immediately upon writing to the last bit of the byte. For multibyte transfers, writing to this register can occur during the middle of a communication cycle. Care must be taken to compensate for this new configuration for the remaining bytes of the current communication cycle.

The same considerations apply to setting the software reset, RESET (Register 0x00, Bit 5) or pulling the RESET pin (Pin 70) high. All registers are set to their default values, except Register 0x00 and Register 0x04, which remain unchanged.

Use of only single-byte transfers when changing serial port configurations or initiating a software reset is recommended to prevent unexpected device behavior.

As described in this section, all serial port data is transferred to/from the device in synchronization to the SCLK pin. If synchronization is lost, the device has the ability to asynchronously terminate an I/O operation, putting the serial port controller into a known state and, thereby, regaining synchronization.

## SERIAL PERIPHERAL INTERFACE

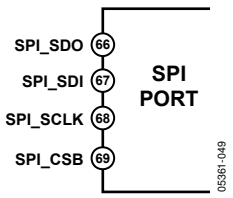


*Figure 52. SPI Port*

The serial port is a flexible, synchronous serial communications port allowing easy interface to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola SPI® and Intel® SSR protocols. The interface allows read/write access to all registers that configure the AD9776/AD9778/AD9779. Single or multiple byte transfers are supported, as well as MSB-first or LSB-first transfer formats. The serial interface ports can be configured as a single pin I/O (SDIO) or two unidirectional pins for input/output (SDIO/SDO).

### *General Operation of the Serial Interface*

There are two phases to a communication cycle with the AD977x. Phase 1 is the instruction cycle (the writing of an instruction byte into the device), coincident with the first eight SCLK rising edges. The instruction byte provides the serial port controller with information regarding the data transfer cycle, Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is a read or write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the device.

A logic high on the CSB pin followed by a logic low resets the SPI port timing to the initial state of the instruction cycle. From this state, the next eight rising SCLK edges represent the instruction bits of the current I/O operation, regardless of the state of the internal registers or the other signal levels at the inputs to the SPI port. If the SPI port is in an instruction cycle or a data transfer cycle, none of the present data is written.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the device and the system controller. Phase 2 of the communication cycle is a transfer of one, two, three, or four data bytes as determined by the instruction byte. Using one multibyte transfer is preferred. Single-byte data transfers are useful in reducing CPU overhead when register access requires only one byte. Registers change immediately upon writing to the last bit of each transfer byte.

### *Instruction Byte*

The instruction byte contains the information shown in Table 9.

**Table 9. SPI Instruction Byte**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| **I7** | **I6** | **I5** | **I4** | **I3** | **I2** | **I1** | **I0** |
| R/$\overline{W}$ | N1 | N0 | A4 | A3 | A2 | A1 | A0 |

R/$\overline{W}$, Bit 7 of the instruction byte, determines whether a read or a write data transfer occurs after the instruction byte write. Logic high indicates a read operation. Logic 0 indicates a write operation.

N1 and N0, Bit 6 and Bit 5 of the instruction byte, determine the number of bytes to be transferred during the data transfer cycle. The bit decodes are listed in Table 10.

A4, A3, A2, A1, and A0—Bit 4, Bit 3, Bit 2, Bit 1, and Bit 0, respectively, of the instruction byte determine the register that is accessed during the data transfer portion of the communication cycle.