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Dual 12-/14-/16-Bit 800 MSPS DAC with Low Power 32-Bit Complex NCO

Data Sheet

AD9785/AD9787/AD9788

FEATURES

Analog output: adjustable 8.7 mA to 31.7 mA, R_L = 25 Ω to 50 Ω
Low power, fine complex NCO allows carrier placement anywhere in DAC bandwidth while adding <300 mW power
Auxiliary DACs allow I and Q gain matching and offset control
Includes programmable I and Q phase compensation
Internal digital upconversion capability
Multiple chip synchronization interface
High performance, low noise PLL clock multiplier
Digital inverse sinc filter
100-lead, exposed pad TQFP package

APPLICATIONS

Wireless infrastructure
W-CDMA, CDMA2000, TD-SCDMA, WiMAX, GSM
Digital high or low IF synthesis
Transmit diversity
Wideband communications
LMDS/MMDS, point-to-point

GENERAL DESCRIPTION

The AD9785/AD9787/AD9788 are 12-bit, 14-bit, and 16-bit, high dynamic range TxDAC® devices, respectively, that provide a sample rate of 800 MSPS, permitting multicarrier generation up to the Nyquist frequency. Features are included for optimizing direct conversion transmit applications, including complex digital modulation, as well as gain, phase, and offset compensation. The DAC outputs are optimized to interface seamlessly with analog quadrature modulators, such as the ADL5375 family from Analog Devices, Inc. A serial peripheral interface (SPI) provides for programming and readback of many internal parameters. Full-scale output current can be programmed over a range of 10 mA to 30 mA. The AD9785/AD9787/AD9788 family is manufactured on a 0.18 µm CMOS process and operates from 1.8 V and 3.3 V supplies. It is enclosed in a 100-lead TQFP package.

PRODUCT HIGHLIGHTS

1. Low noise and intermodulation distortion (IMD) enable high quality synthesis of wideband signals from baseband to high intermediate frequencies.
2. Proprietary DAC output switching technique enhances dynamic performance.
3. CMOS data input interface with adjustable setup and hold.
4. Low power complex 32-bit numerically controlled oscillators (NCOs).

TYPICAL SIGNAL CHAIN

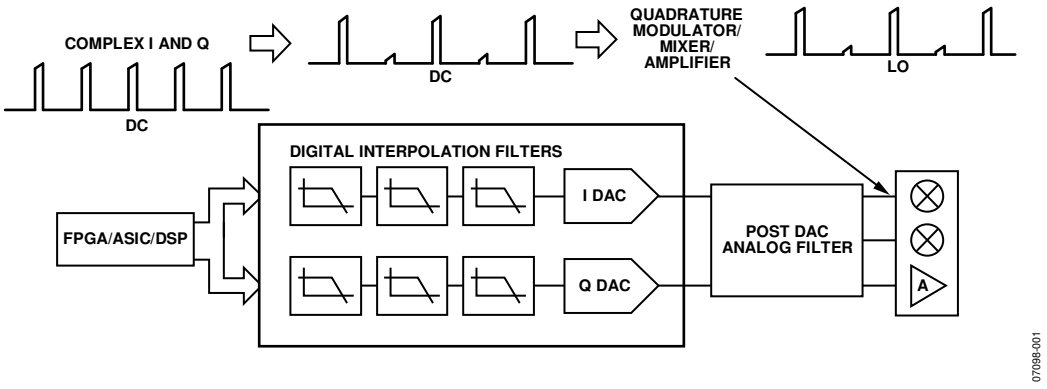

Figure 1.

Rev. B Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

2/16—Rev. A to Rev. B

Changed SPI_CSB to SPI_CS ... Throughout
Changes to General Description Section ... 1
Changes to Figure 2 and Table 6 ... 7
Changes to Figure 3 and Table 7 ... 9
Changes to Figure 4 and Table 8 ... 11
Changes to Figure 52 ... 36
Updated Outline Dimensions ... 62
Changes to Ordering Guide ... 62

2/09—Rev. 0 to Rev. A

Added Settling Time, to Within ±0.5 LSBs Parameter, Table 1 ... 3
Added REFCLK Frequency Range, PLL Enabled Parameter, Table 2 ... 4
Changes to SPI_SDIO—Serial Data I/O Section ... 23
Changes to Table 9 ... 24
Changes to Table 11 ... 26
Changes to Table 12 ... 27
Changes to Table 13 ... 28
Changes to Table 22 ... 32
Changes to Dual-Port Mode Section ... 33
Changes to Input Data RAM Section ... 37
Changes to Digital Amplitude and Offset Control Section ... 41
Changes to Direct Clocking Section ... 47

1/08—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted. LVDS driver and receiver are compliant to the IEEE 1596 reduced range link, unless otherwise noted.

Table 1.

	AD9785			AD9787			AD9788			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		12			14			16		Bits
ACCURACY										
Differential Nonlinearity (DNL)		±0.2			±0.5			±2.1		LSB
Integral Nonlinearity (INL)		±0.3			±1.0			±3.7		LSB
MAIN DAC OUTPUTS										
Offset Error	−0.001	0	+0.001	−0.001	0	+0.001	−0.001	0	+0.001	% FSR
Gain Error (with Internal Reference)		±2			±2			±2		% FSR
Full-Scale Output Current	8.66	20.2	31.66	8.66	20.2	31.66	8.66	20.2	31.66	mA
Output Compliance Range	−1.0		+1.0	−1.0		+1.0	−1.0		+1.0	V
Output Resistance		10			10			10		MΩ
Gain DAC Monotonicity Guaranteed		10			10			10		Bits
Settling Time, to Within ±0.5 LSBs		20			20			20		ns
MAIN DAC TEMPERATURE DRIFT										
Offset		0.04			0.04			0.04		ppm/°C
Gain		100			100			100		ppm/°C
Reference Voltage		30			30			30		ppm/°C
AUX DAC OUTPUTS										
Resolution		10			10			10		Bits
Full-Scale Output Current[1]	−1.998		+1.998	−1.998		+1.998	−1.998		+1.998	mA
Output Compliance Range (Source)	0		1.6	0		1.6	0		1.6	V
Output Compliance Range (Sink)	0.8		1.6	0.8		1.6	0.8		1.6	V
Output Resistance		1			1			1		MΩ
Aux DAC Monotonicity Guaranteed		10			10			10		Bits
REFERENCE										
Internal Reference Voltage		1.2			1.2			1.2		V
Output Resistance		5			5			5		kΩ
ANALOG SUPPLY VOLTAGES										
AVDD33	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
CVDD18	1.70	1.8	1.90	1.70	1.8	1.90	1.70	1.8	1.90	V
DIGITAL SUPPLY VOLTAGES										
DVDD33	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
DVDD18	1.70	1.8	1.90	1.70	1.8	1.90	1.70	1.8	1.90	V
POWER CONSUMPTION										
1× Mode, f_{DATA} = 100 MSPS, PLL Off, IF = 2 MHz		375	450		375	450		375	450	mW
2× Mode, f_{DATA} = 100 MSPS, Inverse Sinc Off, PLL Off		533			533			533		mW
4× Mode, f_{DATA} = 100 MSPS, Inverse Sinc Off, PLL Off		754			754			754		mW
8× Mode, f_{DATA} = 100 MSPS, Inverse Sinc Off, PLL Off		1054			1054			1054		mW
Power-Down Mode		2.5	9.0		2.5	9.0		2.5	9.0	mW
OPERATING RANGE	−40	+25	+85	−40	+25	+85	−40	+25	+85	°C

[1] Based on a 10 Ω external resistor.

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL					
Input V_{IN} Logic High		2.0			V
Input V_{IN} Logic Low				0.8	V
LVDS INPUT (SYNC_I+, SYNC_I–)	SYNC_I+ = V_{1A}, SYNC_I– = V_{1B}				
Input Voltage Range, V_{IA} or V_{IB}		825		1575	mV
Input Differential Threshold, V_{IDTH}		–100		+100	mV
Input Differential Hysteresis, $V_{IDTHH} - V_{IDTHL}$			20		mV
Receiver Differential Input Impedance, R_{IN}		80		120	Ω
LVDS Input Rate ($f_{SYNC\_I} = f_{DATA}$)		30			MHz
Setup Time, SYNC_I to DAC Clock		0.45			ns
Hold Time, SYNC _I to DAC Clock		0.25			ns
LVDS DRIVER OUTPUTS (SYNC_O+, SYNC_O–)	SYNC_O+ = V_{OA}, SYNC_O– = V_{OB}, 100 Ω termination				
Output Voltage High, V_{OA} or V_{OB}		825		1575	mV
Output Voltage Low, V_{OA} or V_{OB}		1025			mV
Output Differential Voltage, $\|V_{OD}\|$		150	200	250	mV
Output Offset Voltage, V_{OS}		1150		1250	mV
Output Impedance, Single-Ended, R_O		80	100	120	Ω
DAC CLOCK INPUT (REFCLK+, REFCLK–)					
Differential Peak-to-Peak Voltage		400	800	1600	mV
Common-Mode Voltage		300	400	500	mV
Maximum Clock Rate					
DVDD18 = 1.8 V ± 5%		800			MHz
DVDD18 = 1.9 V ± 5%		900			MHz
REFCLK Frequency Range, PLL Enabled		30		250	MHz
MAXIMUM INPUT DATA RATE					
1× Interpolation			250		MSPS
2× Interpolation			250		MSPS
4× Interpolation					
DVDD18 = 1.8 V ± 5%		200			MSPS
DVDD18 = 1.9 V ± 5%		225			MSPS
8× Interpolation					
DVDD18 = 1.8 V ±5%		100			MSPS
DVDD18 = 1.9 V ± 5%		112.5			MSPS
SERIAL PERIPHERAL INTERFACE					
Maximum Clock Rate (SCLK)		40			MHz
Minimum Pulse Width High		12.5			ns
Minimum Pulse Width Low		12.5			ns
Setup Time, SPI_SDIO to SCLK		2.8			ns
Hold Time, SPI_SDIO to SCLK		0.0			ns
Setup Time, $\overline{\text{SPI\_CS}}$ to SCLK		3.0			ns
Data Valid, SPI_SDO to SCLK		10.0			ns
INPUT DATA	All modes, –40°C to +85°C[1]				
Setup Time, Input Data to DATACLK		460			ns
Hold Time, Input Data to DATACLK		–1.5			ns
Setup Time, Input Data to REFCLK		–0.25			ns
Hold Time, Input Data to REFCLK		2.4			ns

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LATENCY (DACCLK CYCLES)					
1× Interpolation	With or without modulation		40		Cycles
2× Interpolation	With or without modulation		83		Cycles
4× Interpolation	With or without modulation		155		Cycles
8× Interpolation	With or without modulation		294		Cycles
Inverse Sinc			18		Cycles
POWER-UP TIME[2]			260		ms
DAC Wake-Up Time[3]	I_{OUT} current settling to 1%		22		ms
DAC Sleep Time[4]	I_{OUT} current to less than 1% of full scale		22		ms

[1] Timing vs. temperature and data valid windows are delineated in Table 25.
[2] Measured from $\overline{SPI\_CS}$ rising edge on Register 0x00; toggle Bit 4 from 0 to 1. VREF decoupling capacitor = 0.1 µF.
[3] Measured from $\overline{SPI\_CS}$ rising edge on Register 0x05 or Register 0x07; toggle Bit 15 or Bit 14 from 0 to 1.
[4] Measured from $\overline{SPI\_CS}$ rising edge on Register 0x05 or Register 0x07; toggle Bit 15 or Bit 14 from 1 to 0.

AC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 3.

	AD9785			AD9787			AD9788			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SPURIOUS-FREE DYNAMIC RANGE (IN-BAND SFDR)										
f_{DACCLK} = 200 MSPS, f_{OUT} = 70 MHz 1× Interpolation		80			82			83		dBc
f_{DACCLK} = 200 MSPS, f_{OUT} = 70 MHz 2× Interpolation		80			82			83		dBc
f_{DACCLK} = 200 MSPS, f_{OUT} = 70 MHz 4× Interpolation		78			80			81		dBc
f_{DACCLK} = 800 MSPS, f_{OUT} = 40 MHz 8× Interpolation		85			87			90		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)										
f_{DATA} = 200 MSPS, f_{OUT} = 50 MHz 1× Interpolation		80			82			83		dBc
f_{DATA} = 200 MSPS, f_{OUT} = 50 MHz 2× Interpolation		78			79			80		dBc
f_{DATA} = 200 MSPS, f_{OUT} = 100 MHz 4× Interpolation		78			79			80		dBc
f_{DATA} = 100 MSPS, f_{OUT} = 100 MHz 8× Interpolation		70			70			70		dBc
NOISE SPECTRAL DENSITY (NSD), EIGHT TONE, 500 kHz TONE SPACING										
f_{DACCLK} = 200 MSPS, f_{OUT} = 80 MHz		−154			−157			−158		dBm/Hz
f_{DACCLK} = 400 MSPS, f_{OUT} = 80 MHz		−154			−158			−161		dBm/Hz
f_{DACCLK} = 800 MSPS, f_{OUT} = 80 MHz		−154			−159			−162		dBm/Hz
WCDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER										
f_{DACCLK} = 491.52 MSPS, f_{OUT} = 100 MHz 4× Interpolation		78			80			82		dBc
f_{DACCLK} = 491.52 MSPS, f_{OUT} = 200 MHz 4× Interpolation		72			74			76		dBc
WCDMA SECOND ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER										
f_{DACCLK} = 491.52 MSPS, f_{OUT} = 100 MHz 4× Interpolation		80			82			88		dBc
f_{DACCLK} = 491.52 MSPS, f_{OUT} = 200 MHz 4× Interpolation		78			80			82		dBc

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
AVDD33 to AGND, DGND, CGND	−0.3 V to +3.6 V
DVDD33, DVDD18, CVDD18 to AGND, DGND, CGND	−0.3 V to +2.1 V
AGND to DGND, CGND	−0.3 V to +0.3 V
DGND to AGND, CGND	−0.3 V to +0.3 V
CGND to AGND, DGND	−0.3 V to +0.3 V
I120, VREF, IPTAT to AGND	−0.3 V to AVDD33 + 0.3 V
OUT1_P, OUT1_N, OUT2_P, OUT2_N, AUX1_P, AUX1_N, AUX2_P, AUX2_N to AGND	−1.0 V to AVDD33 + 0.3 V
P1D[15] to P1D[0], P2D[15] to P2D[0] to DGND	−0.3 V to DVDD33 + 0.3 V
DATACLK, TXENABLE to DGND	−0.3 V to DVDD33 + 0.3 V
REFCLK+, REFCLK−, RESET, IRQ, PLL_LOCK, SYNC_O+, SYNC_O−, SYNC_I+, SYNC_I− to CGND	−0.3 V to CVDD18 + 0.3 V
RESET, IRQ, PLL_LOCK, SYNC_O+, $\overline{\text{SYNC\_O}}$−, SYNC_I+, $\overline{\text{SYNC\_I}}$−, $\overline{\text{SPI\_CS}}$, SCLK, SPI_SDIO, SPI_SDO to DGND	−0.3 V to DVDD33 + 0.3 V
Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

For this 100-lead, thermally enhanced TQFP, the exposed pad (EPAD) must be soldered to the ground plane. Note that these specifications are valid with no airflow movement.

Table 5. Thermal Resistance

Resistance	Unit	Conditions
θ_{JA}	19.1°C/W	EPAD soldered. No airflow.
θ_{JB}	12.4°C/W	EPAD soldered. No airflow.
θ_{JC}	7.1°C/W	EPAD soldered. No airflow.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

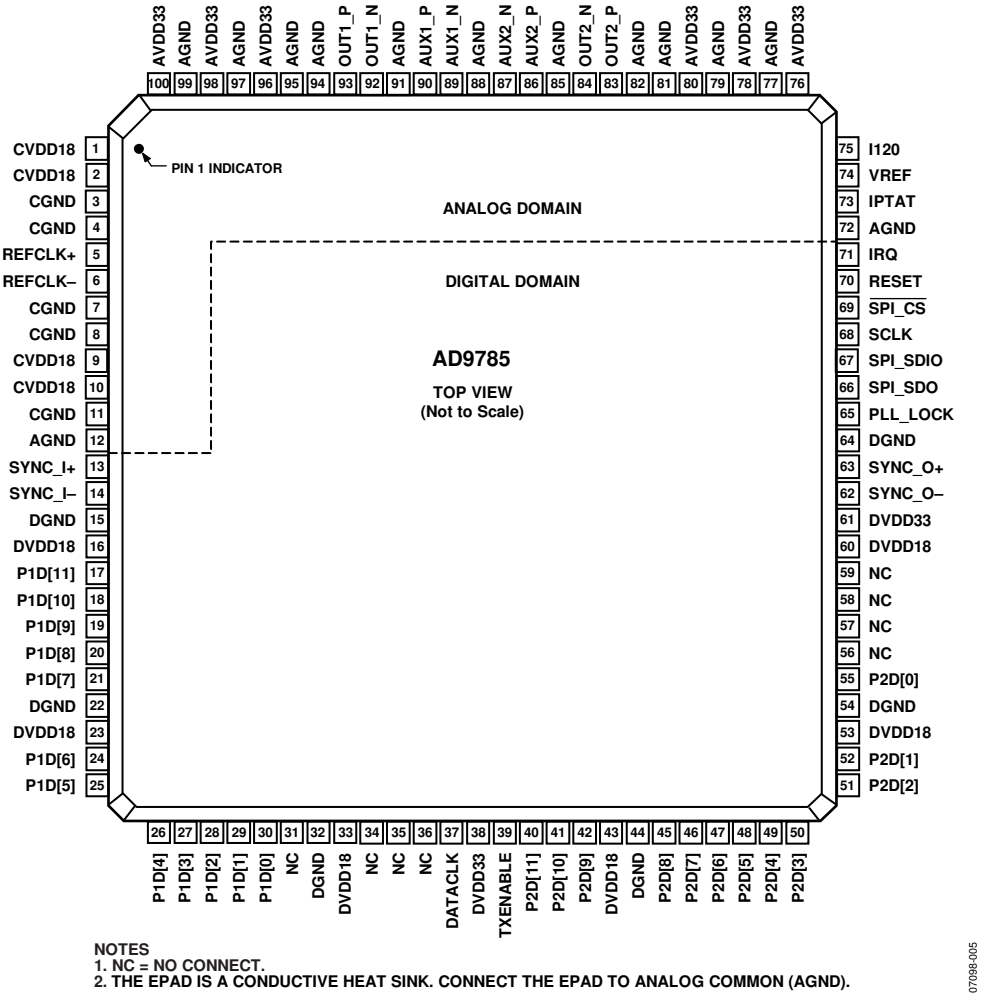

Figure 2. AD9785 Pin Configuration

Table 6. AD9785 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 9, 10	CVDD18	1.8 V Clock Supply.
3, 4, 7, 8, 11	CGND	Clock Common.
5	REFCLK+	Differential Clock Input, Positive.
6	REFCLK–	Differential Clock Input, Negative.
12, 72, 77, 79, 81, 82, 85, 88, 91, 94, 95, 97, 99	AGND	Analog Common.
13	SYNC_I+	Differential Synchronization Input, Positive.
14	SYNC_I–	Differential Synchronization Input, Negative.
15, 22, 32, 44, 54, 64	DGND	Digital Common.
16, 23, 33, 43, 53, 60	DVDD18	1.8 V Digital Supply.
17	P1D[11]	Port 1, Data Input D11 (MSB).
18	P1D[10]	Port 1, Data Input D10.
19	P1D[9]	Port 1, Data Input D9.
20	P1D[8]	Port 1, Data Input D8.
21	P1D[7]	Port 1, Data Input D7.
24	P1D[6]	Port 1, Data Input D6.
25	P1D[5]	Port 1, Data Input D5.
26	P1D[4]	Port 1, Data Input D4.

Pin No.	Mnemonic	Description
27	P1D[3]	Port 1, Data Input D3.
28	P1D[2]	Port 1, Data Input D2.
29	P1D[1]	Port 1, Data Input D1.
30	P1D[0]	Port 1, Data Input D0 (LSB).
31, 34 to 36, 56 to 59	NC	No Connection Necessary. The NC pins are internally connected as digital inputs. They can be connected directly to ground.
37	DATACLK	Data Clock Output.
38, 61	DVDD33	3.3 V Digital Supply.
39	TXENABLE	Transmit Enable.
40	P2D[11]	Port 2, Data Input D11 (MSB).
41	P2D[10]	Port 2, Data Input D10.
42	P2D[9]	Port 2, Data Input D9.
45	P2D[8]	Port 2, Data Input D8.
46	P2D[7]	Port 2, Data Input D7.
47	P2D[6]	Port 2, Data Input D6.
48	P2D[5]	Port 2, Data Input D5.
49	P2D[4]	Port 2, Data Input D4.
50	P2D[3]	Port 2, Data Input D3.
51	P2D[2]	Port 2, Data Input D2.
52	P2D[1]	Port 2, Data Input D1.
55	P2D[0]	Port 2, Data Input D0 (LSB).
62	SYNC_O–	Differential Synchronization Output, Negative.
63	SYNC_O+	Differential Synchronization Output, Positive.
65	PLL_LOCK	PLL Lock Indicator.
66	SPI_SDO	SPI Port Data Output.
67	SPI_SDIO	SPI Port Data Input/Output.
68	SCLK	SPI Port Clock.
69	$\overline{\text{SPI\_CS}}$	SPI Port Chip Select Bar.
70	RESET	Reset, Active High.
71	IRQ	Interrupt Request.
73	IPTAT	Factory Test Pin. Output current is proportional to absolute temperature, approximately 10 µA at 25°C with approximately 20 nA/°C slope. This pin should remain floating.
74	VREF	Voltage Reference Output.
75	I120	120 µA Reference Current.
76, 78, 80, 96, 98, 100	AVDD33	3.3 V Analog Supply.
83	OUT2_P	Differential DAC Current Output, Positive, Channel 2.
84	OUT2_N	Differential DAC Current Output, Negative, Channel 2.
86	AUX2_P	Auxiliary DAC Current Output, Positive, Channel 2.
87	AUX2_N	Auxiliary DAC Current Output, Negative, Channel 2.
89	AUX1_N	Auxiliary DAC Current Output, Negative, Channel 1.
90	AUX1_P	Auxiliary DAC Current Output, Positive, Channel 1.
92	OUT1_N	Differential DAC Current Output, Negative, Channel 1.
93	OUT1_P	Differential DAC Current Output, Positive, Channel 1.
	EPAD	Exposed Pad. The EPAD is a conductive heat sink. Connect the EPAD to analog common (AGND).

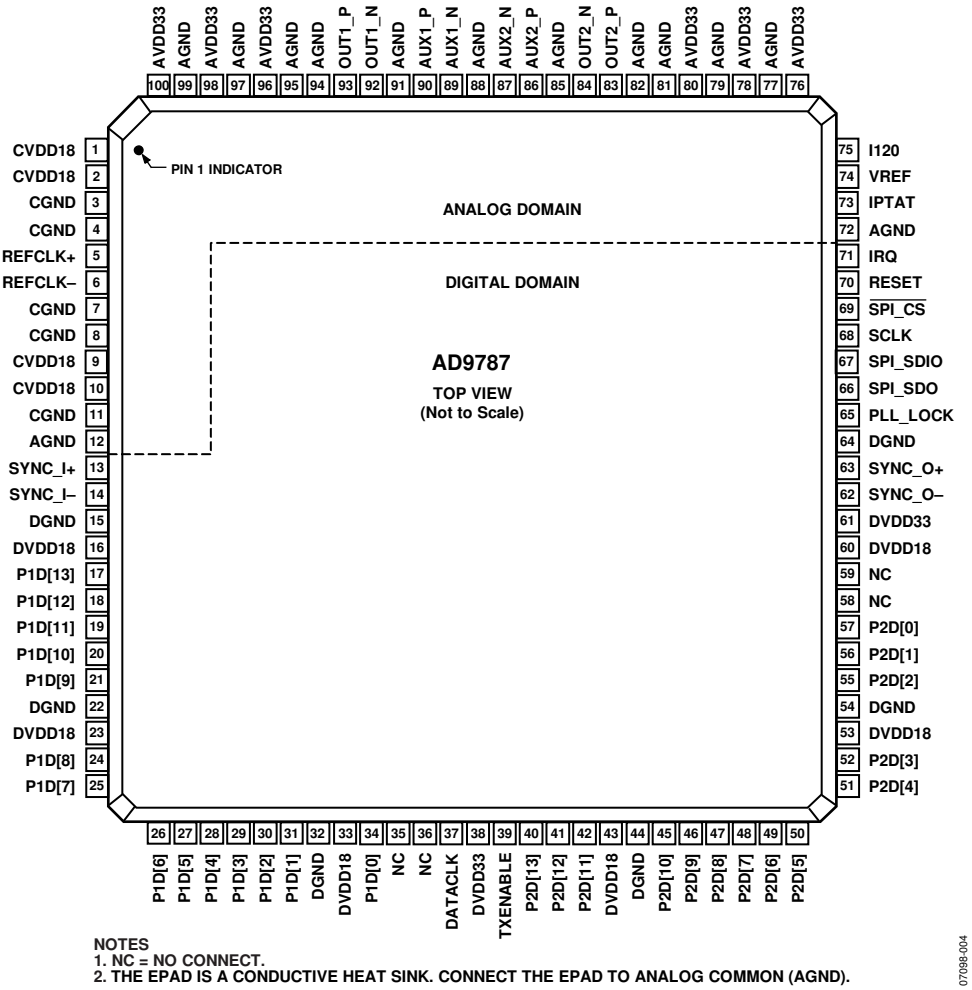

Figure 3. AD9787 Pin Configuration

Table 7. AD9787 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 9, 10	CVDD18	1.8 V Clock Supply.
3, 4, 7, 8, 11	CGND	Clock Common.
5	REFCLK+	Differential Clock Input, Positive.
6	REFCLK–	Differential Clock Input, Negative.
12, 72, 77, 79, 81, 82, 85, 88, 91, 94, 95, 97, 99	AGND	Analog Common.
13	SYNC_I+	Differential Synchronization Input, Positive.
14	SYNC_I–	Differential Synchronization Input, Negative.
15, 22, 32, 44, 54, 64	DGND	Digital Common.
16, 23, 33, 43, 53, 60	DVDD18	1.8 V Digital Supply.
17	P1D[13]	Port 1, Data Input D13 (MSB).
18	P1D[12]	Port 1, Data Input D12.
19	P1D[11]	Port 1, Data Input D11.
20	P1D[10]	Port 1, Data Input D10.
21	P1D[9]	Port 1, Data Input D9.
24	P1D[8]	Port 1, Data Input D8.
25	P1D[7]	Port 1, Data Input D7.
26	P1D[6]	Port 1, Data Input D6.
27	P1D[5]	Port 1, Data Input D5.

Pin No.	Mnemonic	Description
28	P1D[4]	Port 1, Data Input D4.
29	P1D[3]	Port 1, Data Input D3.
30	P1D[2]	Port 1, Data Input D2.
31	P1D[1]	Port 1, Data Input D1.
34	P1D[0]	Port 1, Data Input D0 (LSB).
35, 36, 58, 59	NC	No Connection Necessary. The NC pins are internally connected as digital inputs. They can be connected directly to ground.
37	DATACLK	Data Clock Output.
38, 61	DVDD33	3.3 V Digital Supply.
39	TXENABLE	Transmit Enable.
40	P2D[13]	Port 2, Data Input D13 (MSB).
41	P2D[12]	Port 2, Data Input D12.
42	P2D[11]	Port 2, Data Input D11.
45	P2D[10]	Port 2, Data Input D10.
46	P2D[9]	Port 2, Data Input D9.
47	P2D[8]	Port 2, Data Input D8.
48	P2D[7]	Port 2, Data Input D7.
49	P2D[6]	Port 2, Data Input D6.
50	P2D[5]	Port 2, Data Input D5.
51	P2D[4]	Port 2, Data Input D4.
52	P2D[3]	Port 2, Data Input D3.
55	P2D[2]	Port 2, Data Input D2.
56	P2D[1]	Port 2, Data Input D1.
57	P2D[0]	Port 2, Data Input D0 (LSB).
62	SYNC_O–	Differential Synchronization Output, Negative.
63	SYNC_O+	Differential Synchronization Output, Positive.
65	PLL_LOCK	PLL Lock Indicator.
66	SPI_SDO	SPI Port Data Output.
67	SPI_SDIO	SPI Port Data Input/Output.
68	SCLK	SPI Port Clock.
69	$\overline{\text{SPI\_CS}}$	SPI Port Chip Select Bar.
70	RESET	Reset, Active High.
71	IRQ	Interrupt Request.
73	IPTAT	Factory Test Pin. Output current is proportional to absolute temperature, approximately 10 µA at 25°C with approximately 20 nA/°C slope. This pin should remain floating.
74	VREF	Voltage Reference Output.
75	I120	120 µA Reference Current.
76, 78, 80, 96, 98, 100	AVDD33	3.3 V Analog Supply.
83	OUT2_P	Differential DAC Current Output, Positive, Channel 2.
84	OUT2_N	Differential DAC Current Output, Negative, Channel 2.
86	AUX2_P	Auxiliary DAC Current Output, Positive, Channel 2.
87	AUX2_N	Auxiliary DAC Current Output, Negative, Channel 2.
89	AUX1_N	Auxiliary DAC Current Output, Negative, Channel 1.
90	AUX1_P	Auxiliary DAC Current Output, Positive, Channel 1.
92	OUT1_N	Differential DAC Current Output, Negative, Channel 1.
93	OUT1_P	Differential DAC Current Output, Positive, Channel 1.
	EPAD	Exposed Paddle. The EPAD is a conductive heat sink. Connect the EPAD to analog common (AGND).

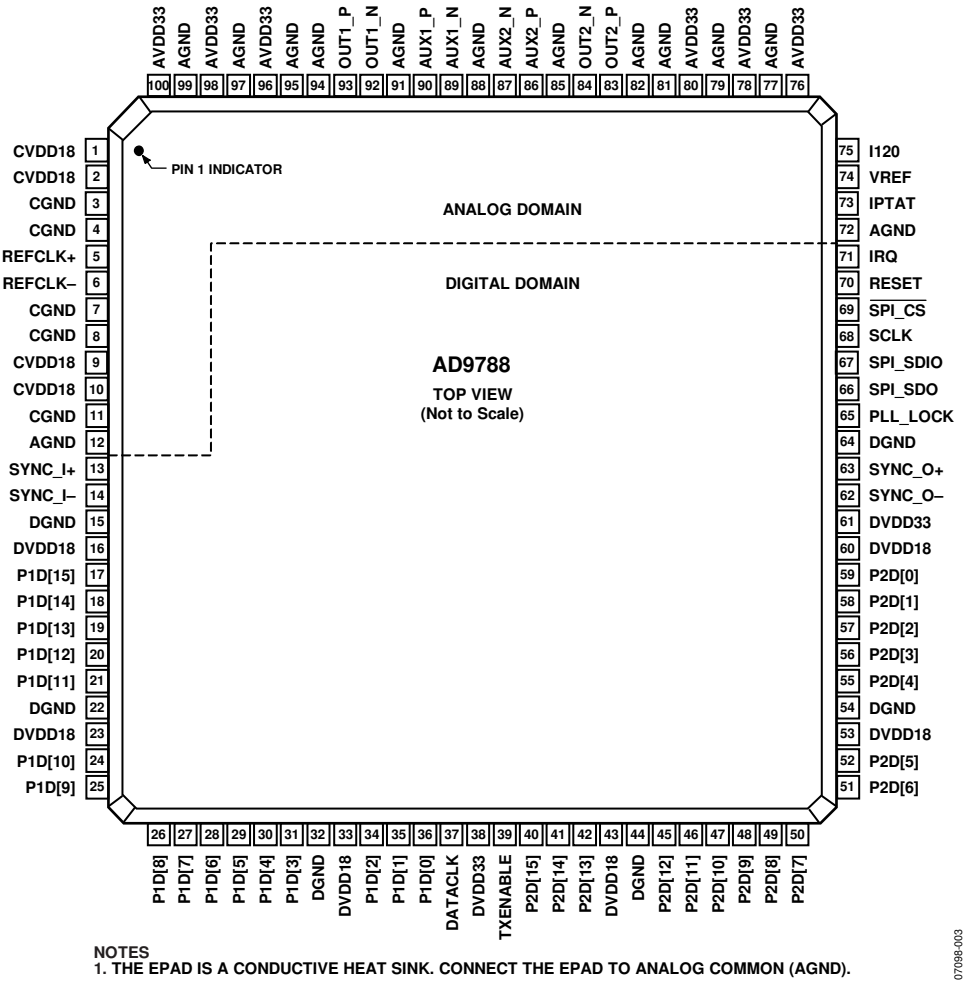

Figure 4. AD9788 Pin Configuration

Table 8. AD9788 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 9, 10	CVDD18	1.8 V Clock Supply.
3, 4, 7, 8, 11	CGND	Clock Common.
5	REFCLK+	Differential Clock Input, Positive.
6	REFCLK–	Differential Clock Input, Negative.
12, 72, 77, 79, 81, 82, 85, 88, 91, 94, 95, 97, 99	AGND	Analog Common.
13	SYNC_I+	Differential Synchronization Input, Positive.
14	SYNC_I–	Differential Synchronization Input, Negative.
15, 22, 32, 44, 54, 64	DGND	Digital Common.
16, 23, 33, 43, 53, 60	DVDD18	1.8 V Digital Supply.
17	P1D[15]	Port 1, Data Input D15 (MSB).
18	P1D[14]	Port 1, Data Input D14.
19	P1D[13]	Port 1, Data Input D13.
20	P1D[12]	Port 1, Data Input D12.
21	P1D[11]	Port 1, Data Input D11.
24	P1D[10]	Port 1, Data Input D10.
25	P1D[9]	Port 1, Data Input D9.
26	P1D[8]	Port 1, Data Input D8.
27	P1D[7]	Port 1, Data Input D7.
28	P1D[6]	Port 1, Data Input D6.
29	P1D[5]	Port 1, Data Input D5.

Pin No.	Mnemonic	Description
30	P1D[4]	Port 1, Data Input D4.
31	P1D[3]	Port 1, Data Input D3.
34	P1D[2]	Port 1, Data Input D2.
35	P1D[1]	Port 1, Data Input D1.
36	P1D[0]	Port 1, Data Input D0 (LSB).
37	DATACLK	Data Clock Output.
38, 61	DVDD33	3.3 V Digital Supply.
39	TXENABLE	Transmit Enable.
40	P2D[15]	Port 2, Data Input D15 (MSB).
41	P2D[14]	Port 2, Data Input D14.
42	P2D[13]	Port 2, Data Input D13.
45	P2D[12]	Port 2, Data Input D12.
46	P2D[11]	Port 2, Data Input D11.
47	P2D[10]	Port 2, Data Input D10.
48	P2D[9]	Port 2, Data Input D9.
49	P2D[8]	Port 2, Data Input D8.
50	P2D[7]	Port 2, Data Input D7.
51	P2D[6]	Port 2, Data Input D6.
52	P2D[5]	Port 2, Data Input D5.
55	P2D[4]	Port 2, Data Input D4.
56	P2D[3]	Port 2, Data Input D3.
57	P2D[2]	Port 2, Data Input D2.
58	P2D[1]	Port 2, Data Input D1.
59	P2D[0]	Port 2, Data Input D0 (LSB).
62	SYNC_O–	Differential Synchronization Output, Negative.
63	SYNC_O+	Differential Synchronization Output, Positive.
65	PLL_LOCK	PLL Lock Indicator.
66	SPI_SDO	SPI Port Data Output.
67	SPI_SDIO	SPI Port Data Input/Output.
68	SCLK	SPI Port Clock.
69	$\overline{\text{SPI\_CS}}$	SPI Port Chip Select Bar.
70	RESET	Reset, Active High.
71	IRQ	Interrupt Request.
73	IPTAT	Factory Test Pin. Output current is proportional to absolute temperature, approximately 10 µA at 25°C with approximately 20 nA/°C slope. This pin should remain floating.
74	VREF	Voltage Reference Output.
75	I120	120 µA Reference Current.
76, 78, 80, 96, 98, 100	AVDD33	3.3 V Analog Supply.
83	OUT2_P	Differential DAC Current Output, Positive, Channel 2.
84	OUT2_N	Differential DAC Current Output, Negative, Channel 2.
86	AUX2_P	Auxiliary DAC Current Output, Positive, Channel 2.
87	AUX2_N	Auxiliary DAC Current Output, Negative, Channel 2.
89	AUX1_N	Auxiliary DAC Current Output, Negative, Channel 1.
90	AUX1_P	Auxiliary DAC Current Output, Positive, Channel 1.
92	OUT1_N	Differential DAC Current Output, Negative, Channel 1.
93	OUT1_P	Differential DAC Current Output, Positive, Channel 1.
	EPAD	Exposed Paddle. The EPAD is a conductive heat sink. Connect the EPAD to analog common (AGND).

TYPICAL PERFORMANCE CHARACTERISTICS

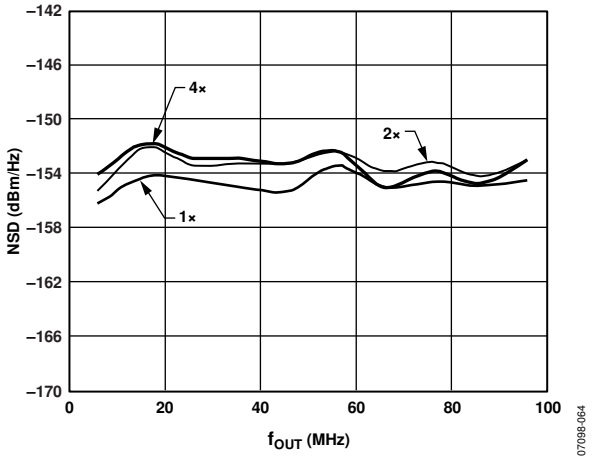

Figure 5. AD9785 Noise Spectral Density vs. f_{OUT}, Multitone Input, f_{DATA} = 200 MSPS

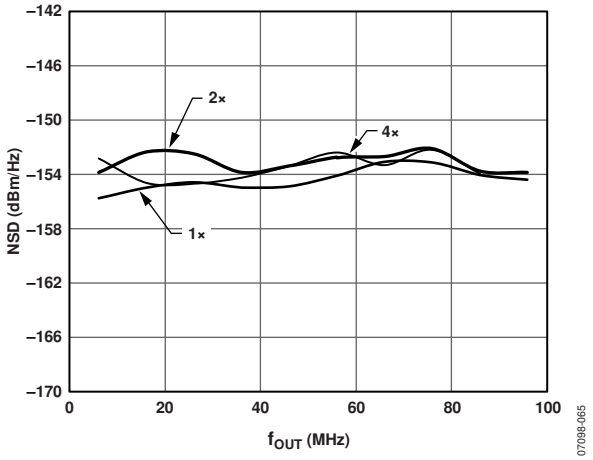

Figure 6. AD9785 Noise Spectral Density vs. f_{OUT}, Single-Tone Input, f_{DATA} = 200 MSPS

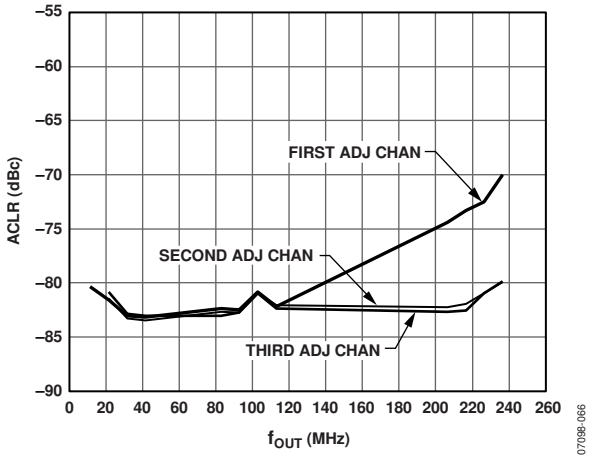

Figure 7. AD9785 ACLR, 4× Interpolation, f_{DATA} = 122.88 MSPS

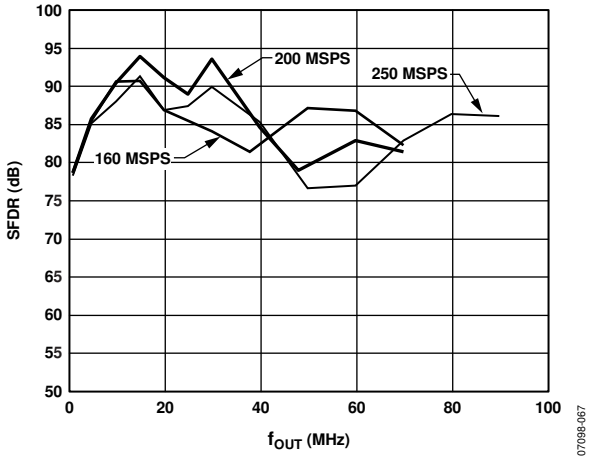

Figure 8. AD9785 In-Band SFDR vs. f_{OUT}, 2× Interpolation

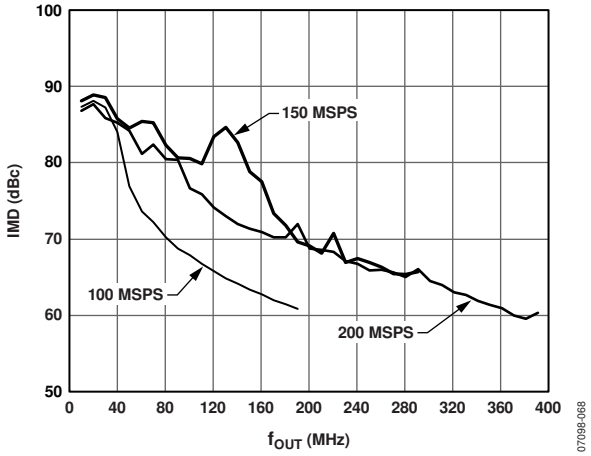

Figure 9. AD9785 IMD vs. f_{OUT}, 4× Interpolation

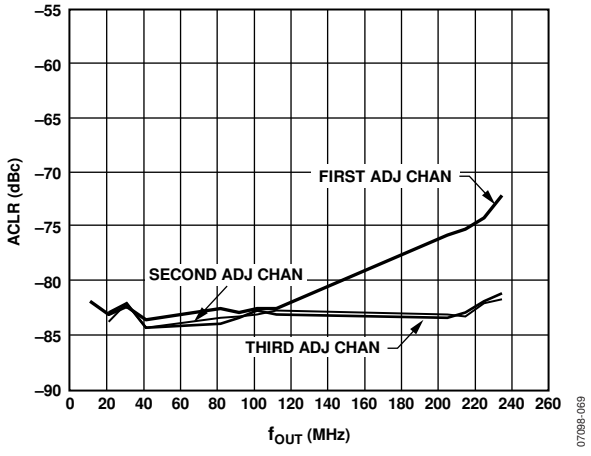

Figure 10. AD9787 ACLR, 4× Interpolation, f_{DATA} = 122.88 MSPS

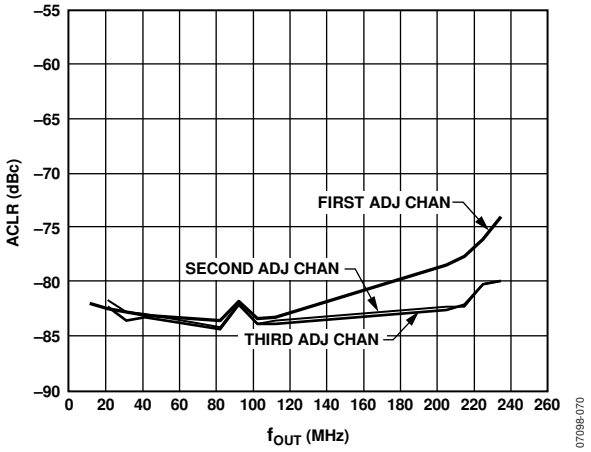

Figure 11. AD9787 ACLR, 4× Interpolation, f_{DATA} = 122.88 MSPS, Amplitude = −3 dB

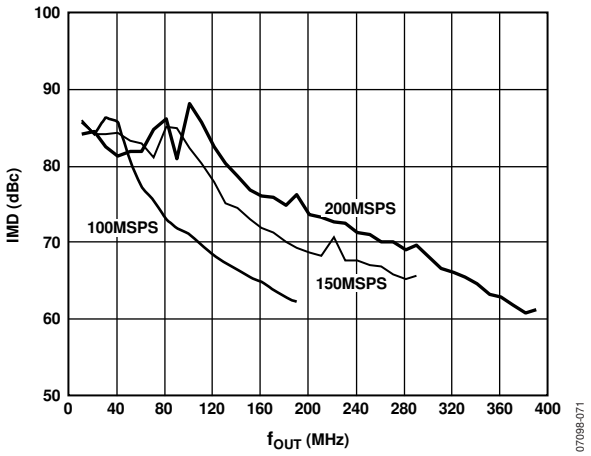

Figure 12. AD9787 IMD vs. f_{OUT}, 4× Interpolation

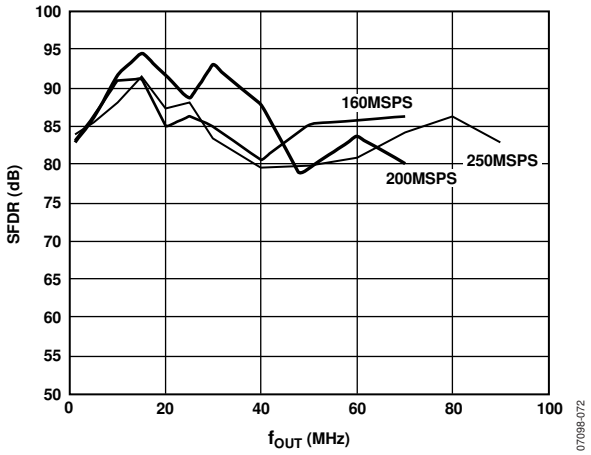

Figure 13. AD9787 In-Band SFDR vs. f_{OUT}, 2× Interpolation

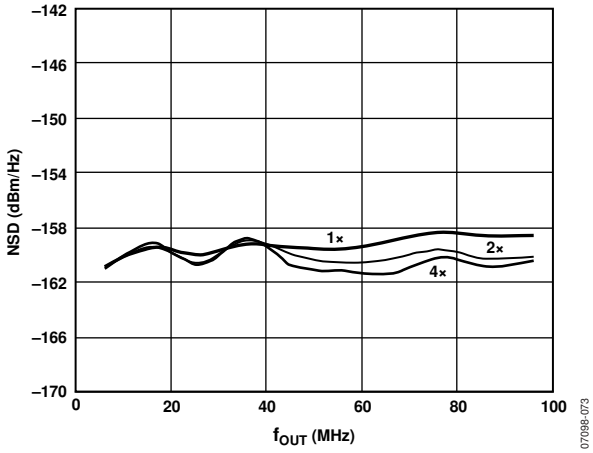

Figure 14. AD9787 Noise Spectral Density vs. f_{OUT} over Output Frequency of Multitone Input, f_{DATA} = 200 MSPS

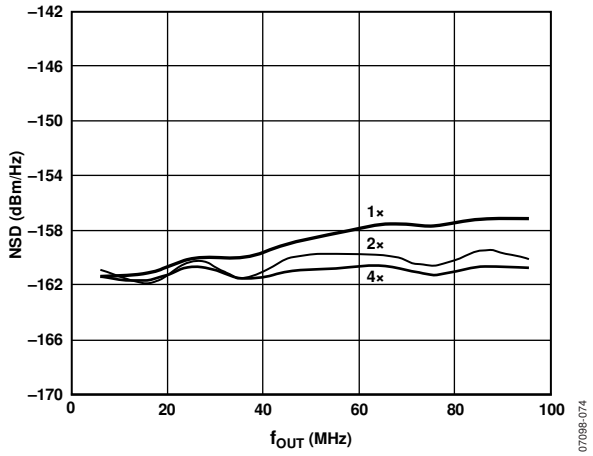

Figure 15. AD9787 Noise Spectral Density vs. f_{OUT}, Single-Tone Input, f_{DATA} = 200 MSPS

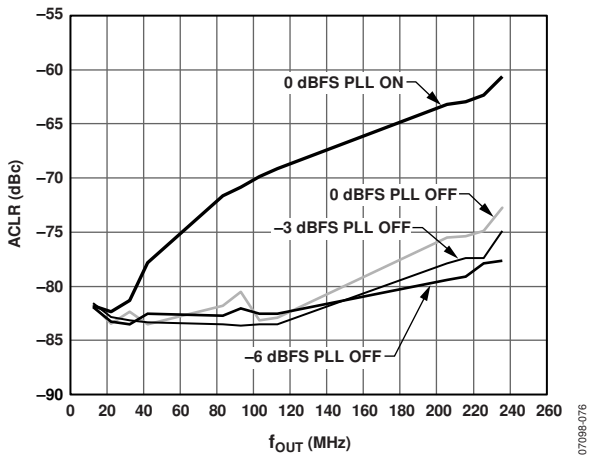

Figure 16. AD9788 ACLR for First Adjacent Band WCDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, NCO Translates Baseband Signal to IF

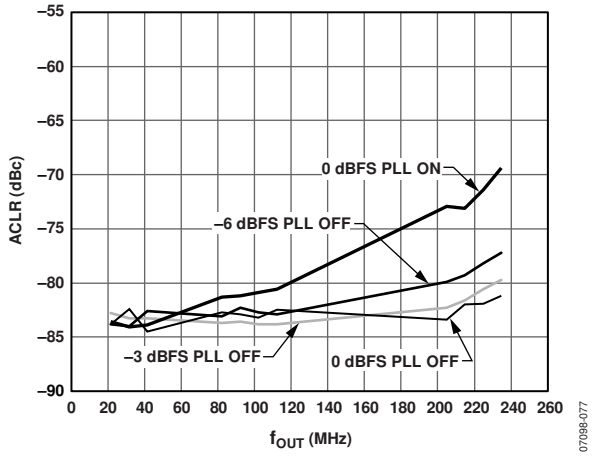

Figure 17. AD9788 ACLR for Second Adjacent Band WCDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, NCO Translates Baseband Signal to IF

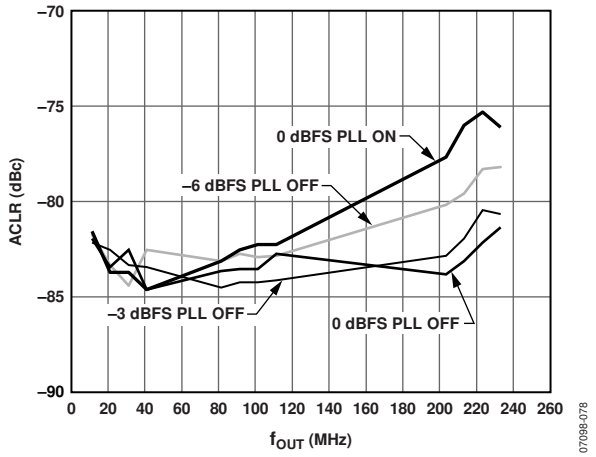

Figure 18. AD9788 ACLR for Third Adjacent Band WCDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, NCO Translates Baseband Signal to IF

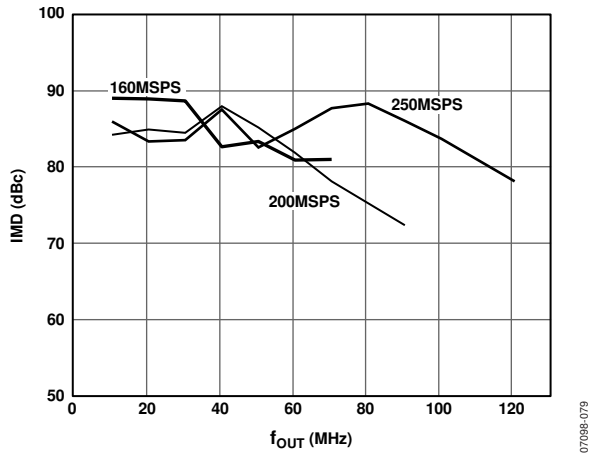

Figure 19. AD9788 IMD vs. f_{OUT}, 1× Interpolation

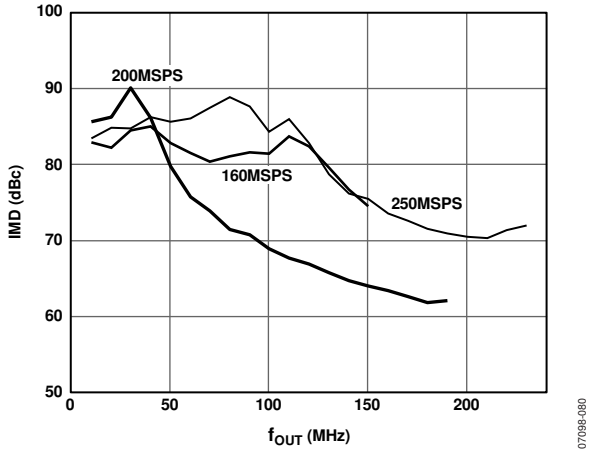

Figure 20. AD9788 IMD vs. f_{OUT}, 2× Interpolation

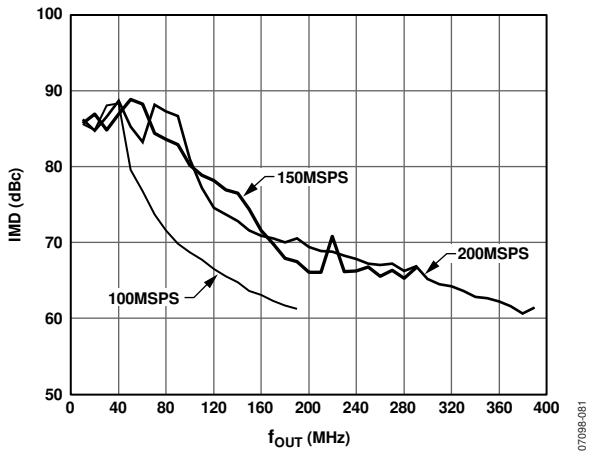

Figure 21. AD9788 IMD vs. f_{OUT}, 4× Interpolation

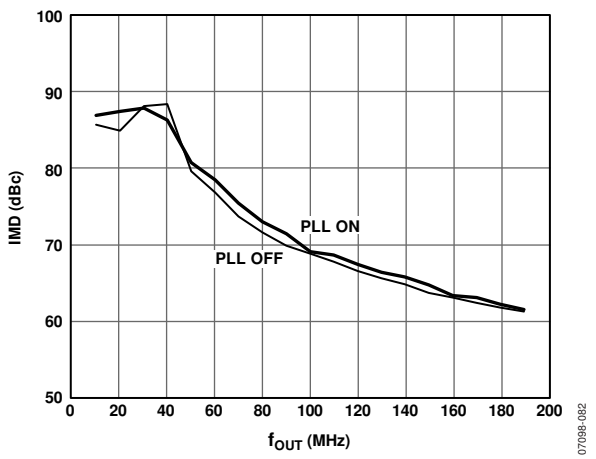

Figure 22. AD9788 IMD vs. f_{OUT}, 8× Interpolation, f_{DATA} = 100 MSPS, PLL On/PLL Off

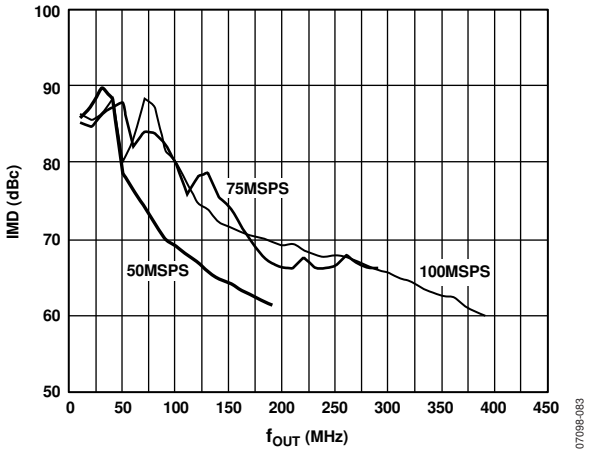

Figure 23. AD9788 IMD vs. f_{OUT}, 8× Interpolation

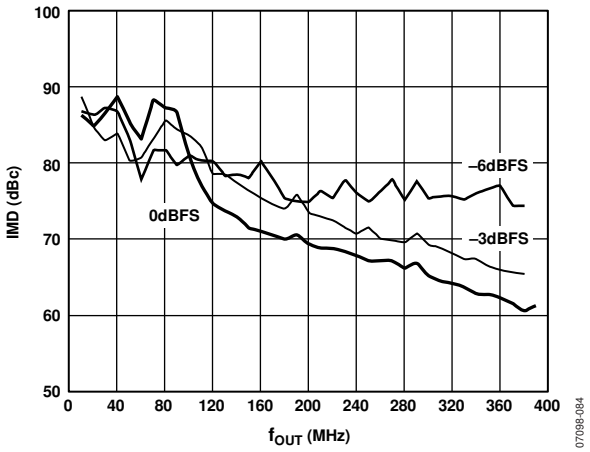

Figure 24. AD9788 IMD Performance vs. Digital Full-Scale Input, 4× Interpolation, f_{DATA} = 200 MSPS

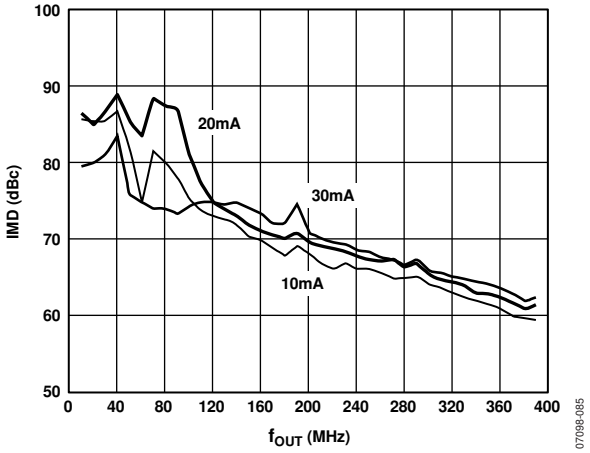

Figure 25. AD9788 IMD Performance vs. Full-Scale Output Current, 4× Interpolation, f_{DATA} = 200 MSPS

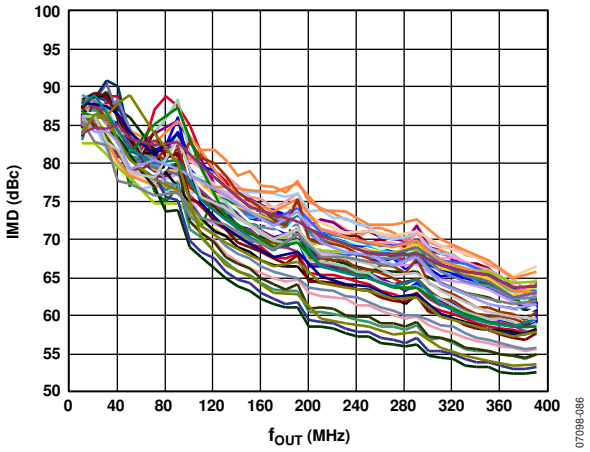

Figure 26. AD9788 IMD vs. f_{OUT}, over 50 Parts, 4× Interpolation, f_{DATA} = 200 MSPS

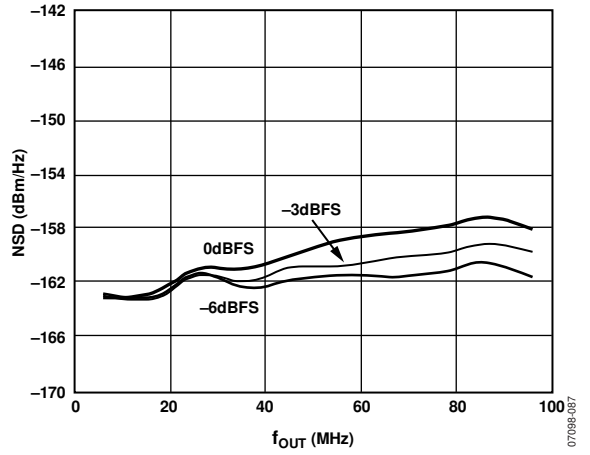

Figure 27. AD9788 Noise Spectral Density vs. Digital Full-Scale Single-Tone Input, f_{DATA} = 200 MSPS, 2× Interpolation

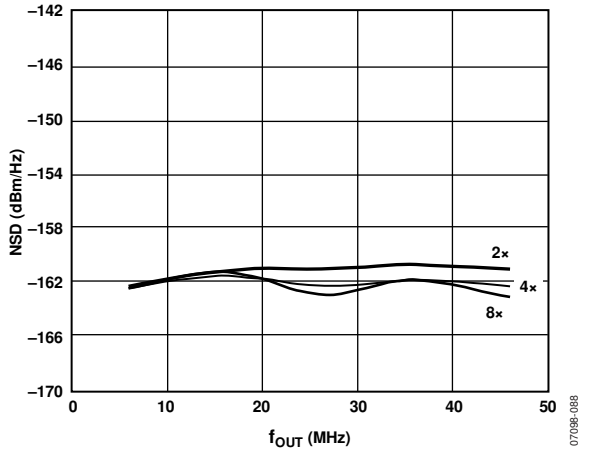

Figure 28. AD9788 Noise Spectral Density vs. f_{OUT}, Multitone Input, f_{DATA} = 100 MSPS

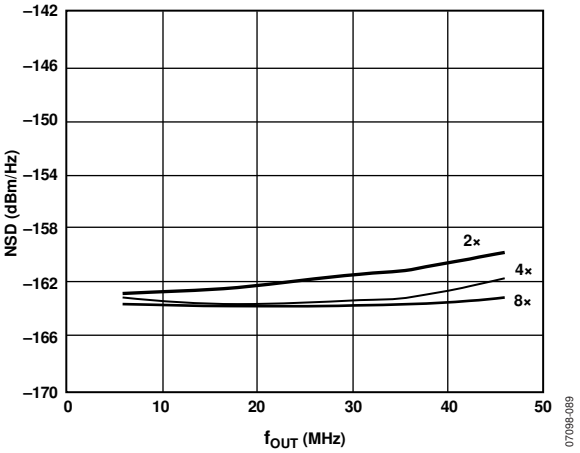

Figure 29. AD9788 Noise Spectral Density vs. f_{OUT}, Single-Tone Input, f_{DATA} = 100 MSPS

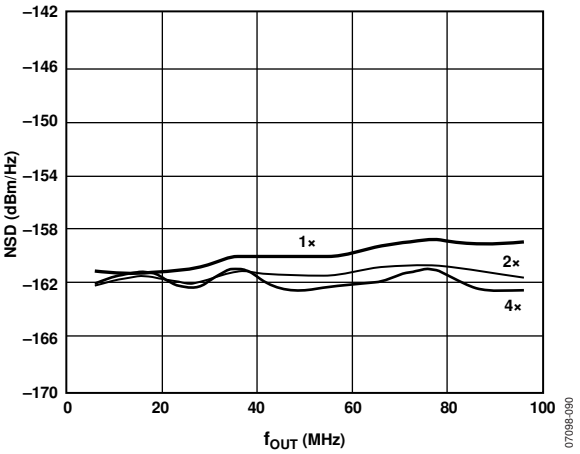

Figure 30. AD9788 Noise Spectral Density vs. f_{DAC}, Eight-Tone Input with 500 kHz Spacing, f_{DATA} = 200 MSPS

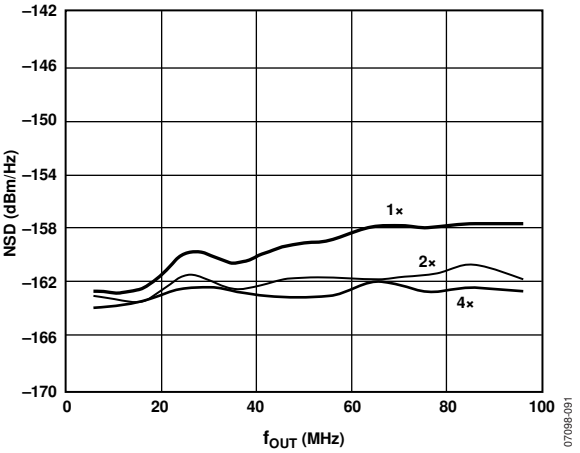

Figure 31. AD9788 Noise Spectral Density vs. f_{DAC}, Full-Scale Single-Tone Input at −6 dB, f_{DATA} = 200 MSPS

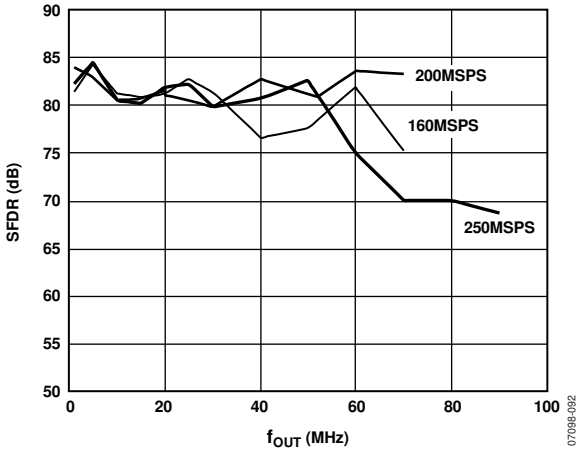

Figure 32. AD9788 In-Band SFDR vs. f_{OUT}, 1× Interpolation

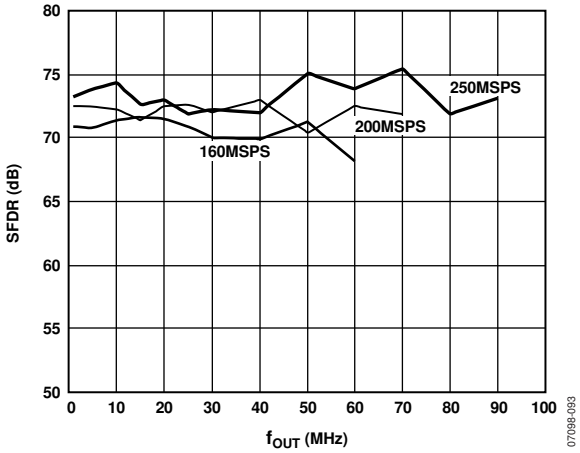

Figure 33. AD9788 Out-of-Band SFDR vs. f_{OUT}, 2× Interpolation

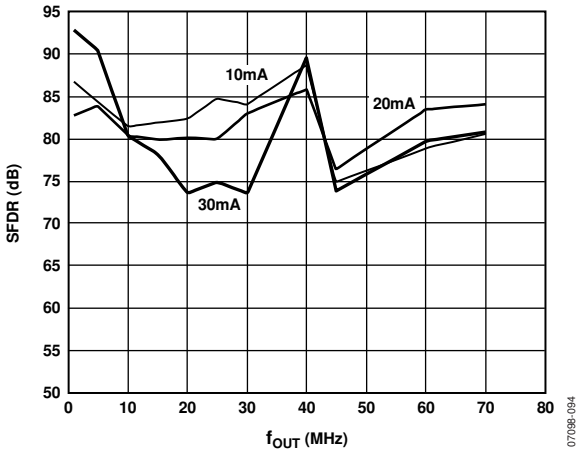

Figure 34. AD9788 In-Band SFDR vs. Full-Scale Output Current, 2× Interpolation, f_{DATA} = 200 MSPS

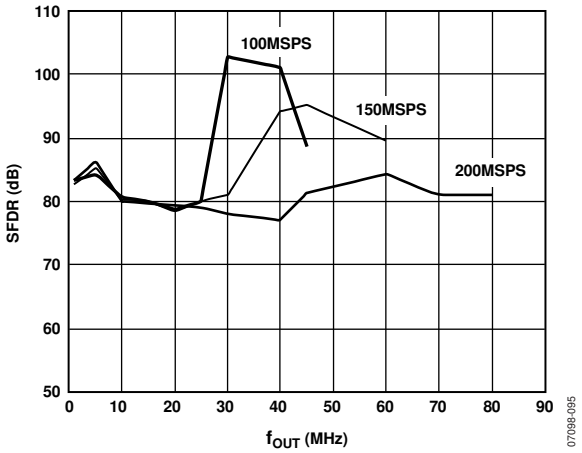

Figure 35. AD9788 In-Band SFDR vs. f_{OUT}, 4× Interpolation

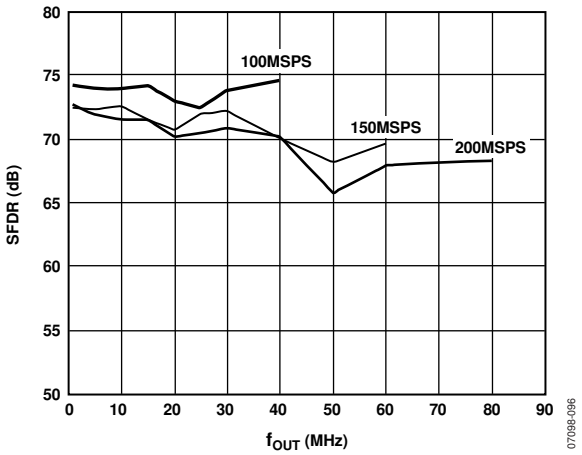

Figure 36. AD9788 Out-of-Band SFDR vs. f_{OUT}, 4× Interpolation

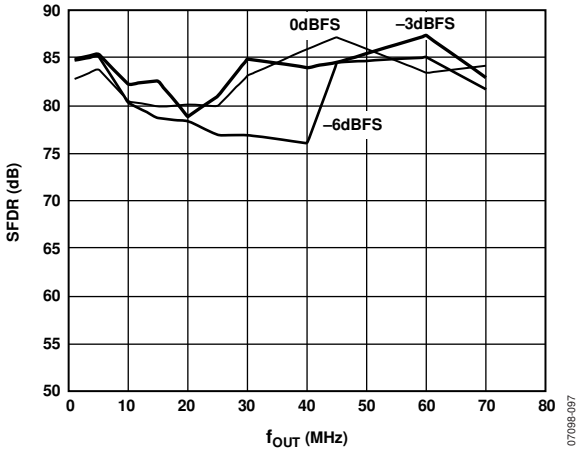

Figure 37. AD9788 In-Band SFDR vs. Digital Full-Scale Input, 2× Interpolation, f_{DATA} = 200 MSPS

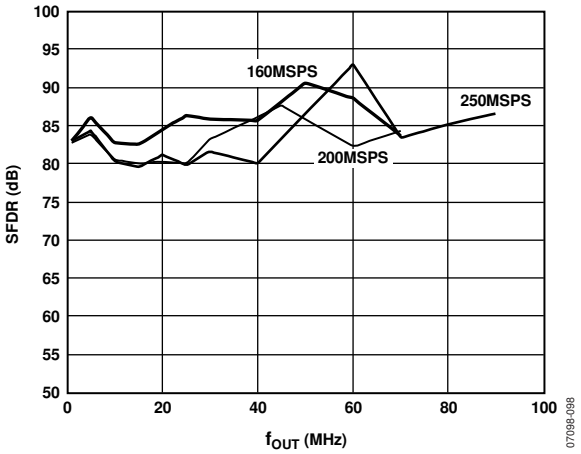

Figure 38. AD9788 In-Band SFDR vs. f_{OUT}, 2× Interpolation

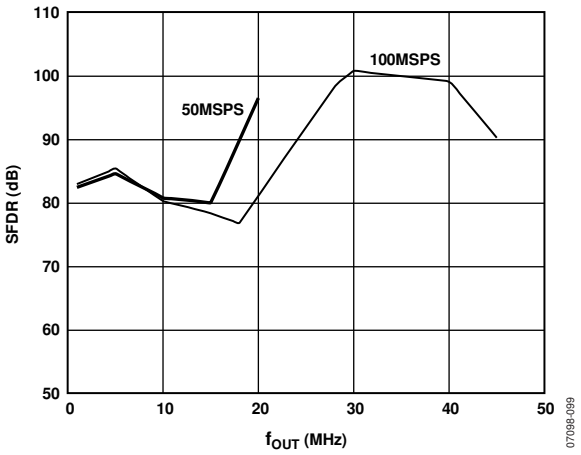

Figure 39. AD9788 In-Band SFDR vs. f_{OUT}, 8× Interpolation

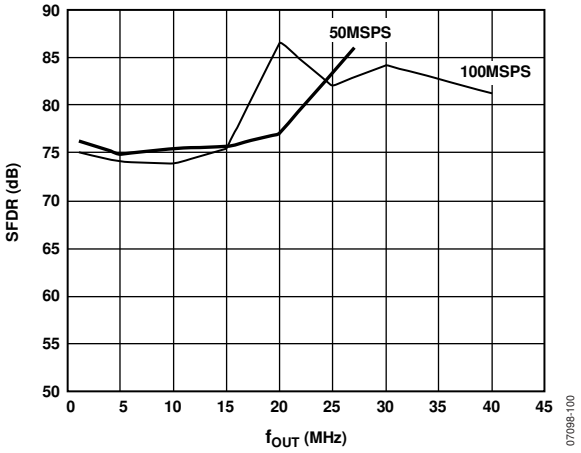

Figure 40. AD9788 Out-of-Band SFDR vs. f_{OUT}, 8× Interpolation

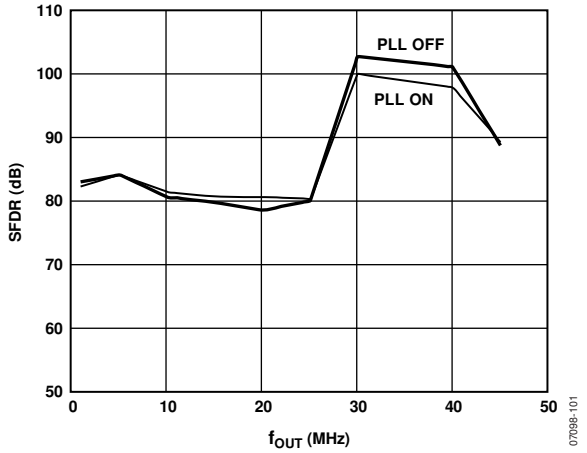

Figure 41. AD9788 In-Band SFDR vs. f_{OUT}, 4× Interpolation, f_{DATA} = 100 MSPS, PLL On/PLL Off

TERMINOLOGY

Integral Nonlinearity (INL)
INL is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called offset error. For I_{OUTA}, 0 mA output is expected when the inputs are all 0s. For I_{OUTB}, 0 mA output is expected when all inputs are set to 1.

Gain Error
The difference between the actual and ideal output span is called gain error. The actual span is determined by the difference between the output when all inputs are set to 1 and the output when all inputs are set to 0.

Output Compliance Range
The output compliance range is the range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree Celsius. For reference drift, the drift is reported in ppm per degree Celsius.

Power Supply Rejection (PSR)
PSR is the maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

Spurious-Free Dynamic Range (SFDR)
Spurious-free dynamic range is the difference, in decibels, between the peak amplitude of the output signal and the peak amplitude of the largest spurious signal in a given frequency band from the signal. For out-of-band SFDR, the frequency band is 0 to one half the DAC sample rate. For in-band SFDR, the frequency band is 0 to one half the input data rate.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured fundamental. It is expressed as a percentage or in decibels.

Noise Spectral Density (NSD)
NSD is the noise power at the analog output measured in a 1 Hz bandwidth.

Interpolation Filter
If the digital inputs to the DAC are sampled at a multiple rate of f_{DATA} (interpolation rate), a digital filter can be constructed that has a sharp transition band near $f_{DATA}/2$. Images that typically appear around f_{DAC} (output data rate) can be greatly suppressed.

Adjacent Channel Leakage Ratio (ACLR)
ACLR is the ratio in dBc between the measured power within a channel relative to its adjacent channel.

Complex Image Rejection
In a traditional two-part upconversion, two images are created around the second intermediate frequency (IF). These images have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

Sinc
Sinc is shorthand for the mathematical function

$$\text{sinc}(x) = \sin(x)/x$$

This function is a useful tool for digital signal processing. The normalized sinc function is used here and is defined as follows:

$$\text{sinc}(x) = \sin(\pi \times x)/(\pi \times x)$$

THEORY OF OPERATION

The AD9785/AD9787/AD9788 devices combine many features that make them very attractive DACs for wired and wireless communications systems. The dual digital signal path and dual DAC structure allow an easy interface to common quadrature modulators when designing single sideband transmitters. The speed and performance of the AD9785/AD9787/AD9788 allow wider bandwidths and more carriers to be synthesized than in previously available DACs. In addition, these devices include an innovative low power, 32-bit complex NCO that greatly increases the ease of frequency placement.

The AD9785/AD9787/AD9788 offer features that allow simplified synchronization with incoming data and between multiple parts, as well as the capability to phase synchronize NCOs on multiple devices. Auxiliary DACs are also provided on chip for output dc offset compensation (for LO compensation in SSB transmitters) and for gain matching (for image rejection optimization in SSB transmitters). Another innovative feature in the devices is the digitally programmable output phase compensation, which increases the amount of image cancellation capability in SSB (single sideband) transmitters.

SERIAL PORT INTERFACE

The AD9785/AD9787/AD9788 serial port is a flexible, synchronous serial communications port allowing easy interface to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola® 6905/11 SPI and the Intel® 8051 SSR protocols.

The serial interface allows read/write access to all registers that configure the AD9785/AD9787/AD9788. MSB first and LSB first transfer formats are supported. In addition, the serial interface port can be configured as a single-pin I/O (SDIO), which allows a 3-wire interface, or two unidirectional pins for input/output (SDIO/SDO), which enables a 4-wire interface. One optional pin, $\overline{\text{SPI\_CS}}$ (chip select), allows enabling of multiple devices on a single bus.

With the AD9785/AD9787/AD9788, the instruction byte specifies read/write operation and the register address. Serial operations on the AD9785/AD9787/AD9788 occur only at the register level, not at the byte level, due to the lack of byte address space in the instruction byte.

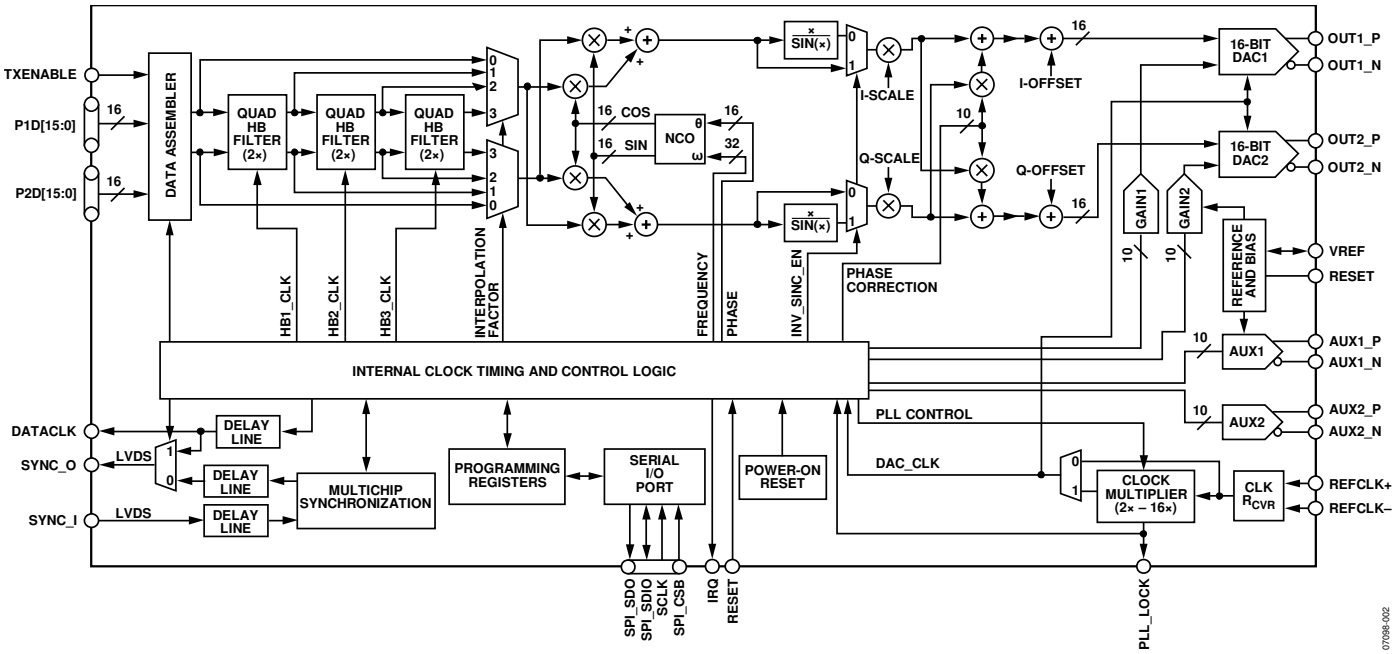

Figure 42. Functional Block Diagram

There are two phases to a communication cycle with the AD9785/AD9787/AD9788. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9785/AD9787/AD9788, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9785/AD9787/AD9788 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The instruction byte defines whether the upcoming data transfer is read or write and the serial address of the register being accessed.

The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9785/AD9787/AD9788. The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9785/AD9787/AD9788 and the system controller. The number of bytes transferred during Phase 2 of the communication cycle is a function of the register being accessed.

For example, when accessing the frequency tuning word (FTW) register, which is four bytes wide, Phase 2 requires that four bytes be transferred. If accessing the amplitude scale factor (ASF) register, which is three bytes wide, Phase 2 requires that three bytes be transferred. After transferring all data bytes per the instruction byte, the communication cycle is completed.

At the completion of any communication cycle, the AD9785/AD9787/AD9788 serial port controller expects the next eight rising SCLK edges to be the instruction byte of the next communication cycle.

All data input is registered on the rising edge of SCLK. All data is driven out of the AD9785/AD9787/AD9788 on the falling edge of SCLK.

Figure 43 through Figure 46 are useful in understanding the general operation of the AD9785/AD9787/AD9788 serial port.

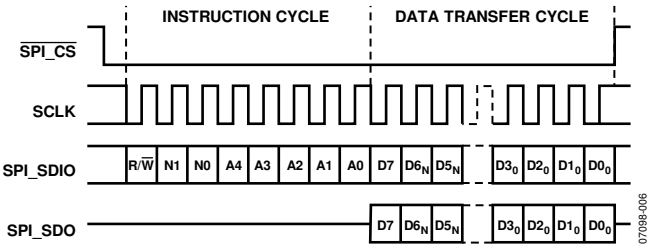

Figure 43. Serial Register Interface Timing, MSB First

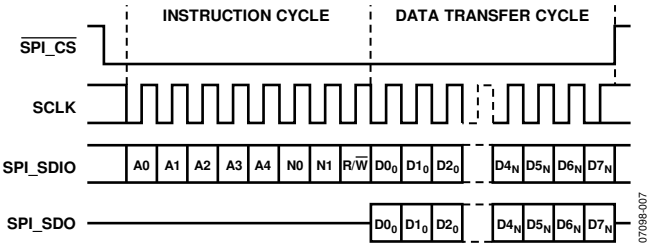

Figure 44. Serial Register Interface Timing, LSB First

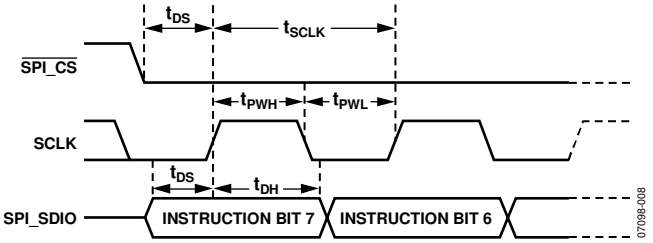

Figure 45. SPI Register Write Timing

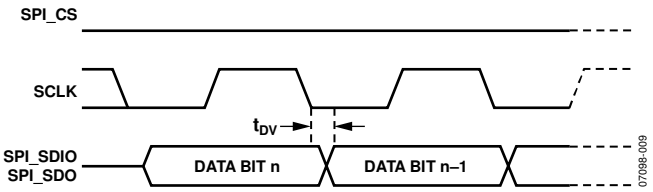

Figure 46. SPI Register Read Timing Instruction Byte

Instruction Byte

The instruction byte contains the following information as shown in the instruction byte bit map.

Instruction Byte Information Bit Map

MSB							LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/$\overline{W}$	X	X	A4	A3	A2	A1	A0

R/$\overline{W}$—Bit 7 of the instruction byte determines whether a read or write data transfer occurs after the instruction byte write. Logic 1 indicates a read operation. Logic 0 indicates a write operation.

X, X —Bit 6 and Bit 5 of the instruction byte are don't care. In previous TxDAC devices, such as the AD9779, these bits define the number of registers written to or read from in an SPI read/write operation. In the AD9785/AD9787/AD9788, the register itself now defines how many bytes are written to or read from.

A4, A3, A2, A1, A0—Bit 4, Bit 3, Bit 2, Bit 1, and Bit 0 of the instruction byte determine which register is accessed during the data transfer portion of the communication cycle.

Serial Interface Port Pin Description

SCLK—Serial Clock

The serial clock pin is used to synchronize data to and from the AD9785/AD9787/AD9788 and to run the internal state machines. SCLK maximum frequency is 40 MHz.

$\overline{SPI\_CS}$—Chip Select

Active low input that allows more than one device on the same serial communications line. The SPI_SDO and SPI_SDIO pins go to a high impedance state when this input is high. If driven high during any communication cycle, that cycle is suspended until $\overline{SPI\_CS}$ is reactivated low. Chip select can be tied low in systems that maintain control of SCLK.

SPI_SDIO—Serial Data I/O

Data is always written into the AD9785/AD9787/AD9788 on this pin. However, this pin can be used as a bidirectional data line. Bit 7 of Register 0x00 controls the configuration of this pin. The default is Logic 0, which configures the SPI_SDIO pin for input only (4-wire) operation.

SPI_SDO—Serial Data Output

Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9785/AD9787/AD9788 operate in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

MSB/LSB Transfers

The AD9785/AD9787/AD9788 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by Bit 6 of the communication (COMM) register. The default value of COMM Register Bit 6 is low (MSB first). When COMM Register Bit 6 is set high, the serial port is in LSB first format. The instruction byte must be written in the format indicated by COMM Register Bit 6. That is, if the device is in LSB first mode, the instruction byte must be written from least significant bit to most significant bit.

For MSB first operation, the serial port controller generates the most significant byte (of the specified register) address first, followed by the next lesser significant byte addresses until the I/O operation is complete. All data written to or read from the AD9785/AD9787/AD9788 must be in MSB first order.

If the LSB mode is active, the serial port controller generates the least significant byte address first, followed by the next greater significant byte addresses until the I/O operation is complete. All data written to or read from the AD9785/AD9787/AD9788 must be in LSB first order.

SPI Resynchronization Capability

If the SPI port becomes unsynchronized at any time, toggling SCLK for eight or more cycles with $\overline{SPI\_CS}$ held high resets the SPI port state machine. The device is then ready for the next register read or write access.

SPI REGISTER MAP

When reading Table 9, note that the AD9785/AD9787/AD9788 is a 32-bit part and, therefore, the 4th through the 11th columns (beginning with the MSB and ending with the LSB) represent a set of eight bits. Refer to the Bit Range column for the actual bits being described.

Table 9.

Address	Register Name	Bit Range	MSB	MSB – 1	MSB – 2	MSB – 3	MSB – 4	MSB – 5	MSB – 6	LSB	Default
0x00	Comm. (COMM) Register	[7:0]	SPI_SDIO bidirectional (active high, 3-wire)	LSB first	Software reset	Power-down mode	Auto power-down enable	I/O transfer (self-reset)	Automatic I/O transfer enable	Open	0x02
0x01	Digital Control Register	[7:0]	Interpolation Factor [1:0]		Data format	Single-port mode	Real mode	IQ select invert	Q first	Modulator gain control	0x00
		[15:8]	Reserved	Clear phase accumulator	PN code sync enable	Sync mode select	Pulse sync enable	Reserved	Inverse sinc enable	DATACLK output enable	0x31
0x02	Data Sync Control Register	[7:0]	Data Timing Margin [0]	LVDS data clock enable	DATACLK invert	DATACLK delay enable	Data timing mode	Set high	Data sync polarity	Reserved	0x00
		[15:8]	DATACLK Delay [4:0]					Data Timing Margin [3:1]			0x00
0x03	Multichip Sync Control Register	[7:0]	Clock State [3:0]				Sync Timing Margin [3:0]				0x00
		[15:8]	SYNC _O Delay [4:0]					Set high	SYNC_O polarity	Sync loopback enable	0x00
		[23:16]	SYNC_I Delay [4:0]					Sync error check mode	Set low	DATACLK input	0x00
		[31:24]	Correlate Threshold [4:0]					SYNC_I enable	SYNC _O enable	Set low	0x80
0x04	PLL Control Register	[7:0]	PLL Band Select [5:0]						PLL VCO Drive [1:0]		0xCF
		[15:8]	PLL enable	PLL VCO Divisor [1:0]		PLL Loop Divisor [1:0]		PLL Bias [2:0]			0x37
		[23:16]	VCO Control Voltage [2:0]			PLL Loop Bandwidth [4:0]					0x38
0x05	I DAC Control Register	[7:0]	I DAC Gain Adjustment [7:0]								0xF9
		[15:8]	I DAC sleep	I DAC power-down	Reserved				I DAC Gain Adjustment [9:8]		0x01
0x06	Auxiliary DAC 1 Control Register	[7:0]	Auxiliary DAC 1 Data [7:0]								0x00
		[15:8]	Auxiliary DAC 1 sign	Auxiliary DAC 1 current direction	Auxiliary DAC 1 power-down	Reserved			Auxiliary DAC 1 Data [9:8]		0x00
0x07	Q DAC Control Register	[7:0]	Q DAC Gain Adjustment [7:0]								0xF9
		[15:8]	Q DAC sleep	Q DAC power-down	Reserved				Q DAC Gain Adjustment [9:8]		0x01
0x08	Auxiliary DAC 2 Control Register	[7:0]	Auxiliary DAC 2 Data [7:0]								0x00
		[15:8]	Auxiliary DAC 2 sign	Auxiliary DAC 2 current direction	Auxiliary DAC 2 power-down	Reserved			Auxiliary DAC 2 Data [9:8]		0x00
0x09	Interrupt Control Register	[7:0]	Data timing error IRQ	Sync timing error IRQ	Data timing error type	Sync timing error type	PLL lock indicator	Reserved	Data port IRQ enable	Sync port IRQ enable	0x00
		[15:8]	Reserved			Clear lock indicator (self-reset)	Sync lock lost status	Sync lock status	Reserved		0x00
0x0A	Frequency Tuning Word Register	[31:0]	Frequency Tuning Word [31:0]								0x00

Address	Register Name	Bit Range	MSB	MSB – 1	MSB – 2	MSB – 3	MSB – 4	MSB – 5	MSB – 6	LSB	Default
0x0B	Phase Control Register	[15:0]	NCO Phase Offset Word [15:0]								0x00
		[23:16]	Phase Correction Word [7:0]								0x00
		[31:24]	Reserved						Phase Correction Word [9:8]		0x00
0x0C	Amplitude Scale Factor Register	[7:0]	I DAC Amplitude Scale Factor [7:0]								0x80
		[15:8]	Q DAC Amplitude Scale Factor [6:0]							I DAC Amplitude Scale Factor [8]	0x00
		[23:16]	Reserved						Q DAC Amplitude Scale Factor [8:7]		0x01
0x0D	Output Offset Register	[15:0]	I DAC Offset [15:0]								0x00
		[31:16]	Q DAC Offset [15:0]								0x00
0x0E[1]	Version Register	[7:0]	Version ID								
		[15:8]	Reserved								
0x1D[1]	RAM	[31:0]	RAM								
0x1E	Test Register	[23:0]	Test								

[1] Address space between Address 0x0E and Address 0x1D is intentionally left open.

SPI REGISTER DESCRIPTIONS

The communication (COMM) register comprises one byte located at Address 0x00.

Table 10. Communication (COMM) Register

Address	Bit	Name	Description
0x00	[7]	SPI_SDIO bidirectional	0: Default. Use the SPI_SDIO pin for input data only, 4-wire serial mode. 1: Use SPI_SDIO as a read/write pin, 3-wire serial mode.
	[6]	LSB first	0: Default. MSB first format is active. 1: Serial interface accepts serial data in LSB first format.
	[5]	Software reset	0: Default. Bit is in the inactive state. 1: In the AD9785/AD9787/AD9788, all programmable bits return to their power-up state except for the COMM register bits, which are unaffected by the software reset. The software reset remains in effect until this bit is set to 0 (inactive state).
	[4]	Power-down mode	0: Default. The full chip power-down is not active. 1: The AD9785/AD9787/AD9788 enter a power-down mode in which all functions are powered down. This power-down puts the part into its lowest possible power dissipation state. The part remains in this low power state until the user sets this bit to a Logic 0. The analog circuitry requires 250 ms to become operational.
	[3]	Auto power-down enable	0: Default. Inactive state, automatic power-down feature is not enabled. 1: The device automatically switches into its low power mode whenever TXENABLE is deasserted for a sufficiently long period of time.
	[2]	I/O transfer (self-reset)	0: Default. Inactive state. 1: The contents of the frequency tuning word memory buffer, phase control memory buffer, amplitude scale factor memory buffer, and the output offset memory buffer are moved to a memory location that affects operation of the device. The one-word memory buffer is employed to simultaneously update the NCO frequency, phase, amplitude, and offset control. Note that this bit automatically clears itself after the I/O transfer occurs. For this reason, unless the reference clock is stopped, it is difficult to read back a Logic 1 on this bit.
	[1]	Automatic I/O transfer enable	0: Automatic I/O transfer disabled. The I/O transfer bit (Bit 2) must be set to update the device in the event that changes have been made to Register 0x0A, Register 0x0B, Register 0x0C, or Register 0x0D. This allows the user to change important operating modes of the device all at once, rather than one at a time with individual SPI writes. 1: Default. Automatic I/O transfer enabled. The device updates its operation immediately when SPI writes are completed to Register 0x0A, Register 0x0B, Register 0x0C, or Register 0x0D.