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14-Bit, 2400 MSPS RF DAC with 4-Channel Signal Processing

AD9789

FEATURES

DOCSIS 3.0 performance: 4 QAM carriers
- **ACLR over full band (47 MHz to 1 GHz)**
  - **−75 dBc @ f_{OUT} = 200 MHz**
  - **−72 dBc @ f_{OUT} = 800 MHz (noise)**
  - **−67 dBc @ f_{OUT} = 800 MHz (harmonics)**
- **Unequalized MER = 42 dB**

On chip and bypassable
- **4 QAM encoders with SRRC filters, 16× to 512× interpolation, rate converters, and modulators**

Flexible data interface: 4, 8, 16, or 32 bits wide with parity
Power: 1.6 W (I_{FS} = 20 mA, f_{DAC} = 2.4 GHz, LVDS interface)
Direct to RF synthesis support with f_S mix mode
Built-in self-test (BIST) support
- **Input connectivity check**
- **Internal random number generator**

APPLICATIONS

Broadband communications systems
CMTS/DVB
Cellular infrastructure
Point-to-point wireless

GENERAL DESCRIPTION

The AD9789 is a flexible QAM encoder/interpolator/upconverter combined with a high performance, 2400 MSPS, 14-bit RF digital-to-analog converter (DAC). The flexible digital interface can accept up to four channels of complex data. The QAM encoder supports constellation sizes of 16, 32, 64, 128, and 256 with SRRC filter coefficients for all standards.

The on-chip rate converter supports a wide range of baud rates with a fixed DAC clock. The digital upconverter can place the channels from 0 to 0.5 × f_{DAC}. This permits four contiguous channels to be synthesized and placed anywhere from dc to $f_{DAC}/2$.

The AD9789 includes a serial peripheral interface (SPI) for device configuration and status register readback. The flexible digital interface can be configured for data bus widths of 4, 8, 16, and 32 bits. It can accept real or complex data.

The AD9789 operates from 1.5 V, 1.8 V, and 3.3 V supplies for a total power consumption of 1.6 W. It is supplied in a 164-ball chip scale package ball grid array for lower thermal impedance and reduced package parasitics. No special power sequencing is required. The clock receiver powers up muted to prevent start-up noise.

PRODUCT HIGHLIGHTS

1. Highly integrated and configurable QAM mappers, interpolators, and upconverters for direct synthesis of one to four DOCSIS- or DVB-C-compatible channels in a block.
2. Low noise and intermodulation distortion (IMD) performance enable high quality synthesis of signals up to 1 GHz.
3. Flexible data interface supports LVDS for improved SFDR or CMOS input data for less demanding applications.
4. Interface is configurable from 4-bit nibbles to 32-bit words and can run at up to 150 MHz CMOS or 150 MHz LVDS double data rate (DDR).
5. Manufactured on a CMOS process, the AD9789 uses a proprietary switching technique that enhances dynamic performance.

FUNCTIONAL BLOCK DIAGRAM

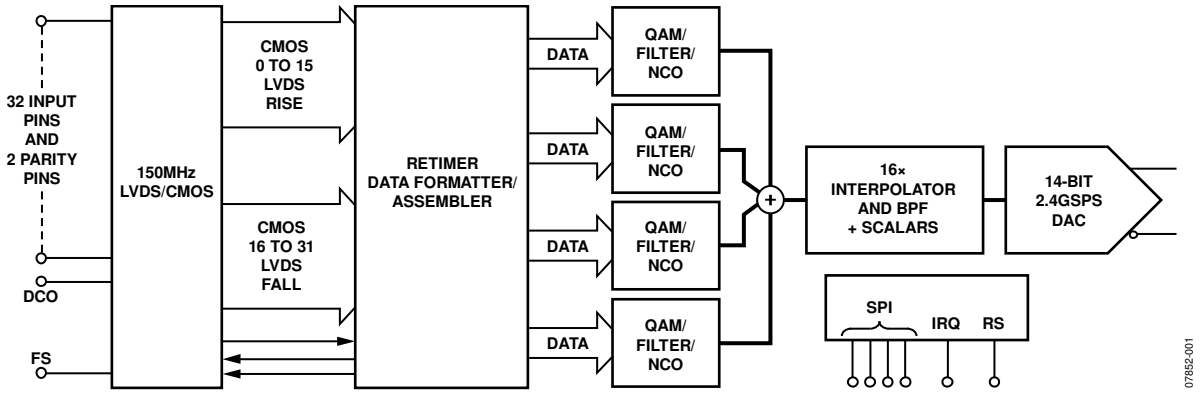

Figure 1.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

AD9789* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9789 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9789: 14-Bit, 2400 MSPS RF DAC with 4-Channel Signal Processing Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD9789 Evaluation Board, DAC-FMC Interposer & Xilinx ML605 Reference Design

TOOLS AND SIMULATIONS

- AD9789 IBIS Model

REFERENCE MATERIALS

Informational

- Advantiv™ Advanced TV Solutions

Solutions Bulletins & Brochures

- Digital to Analog Converters ICs Solutions Bulletin
- Digital-to-Analog Converter ICs Solutions Bulletin, Volume 10, Issue 1

DESIGN RESOURCES

- AD9789 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9789 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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4/09—Revision 0: Initial Version

DETAILED FUNCTIONAL BLOCK DIAGRAMS

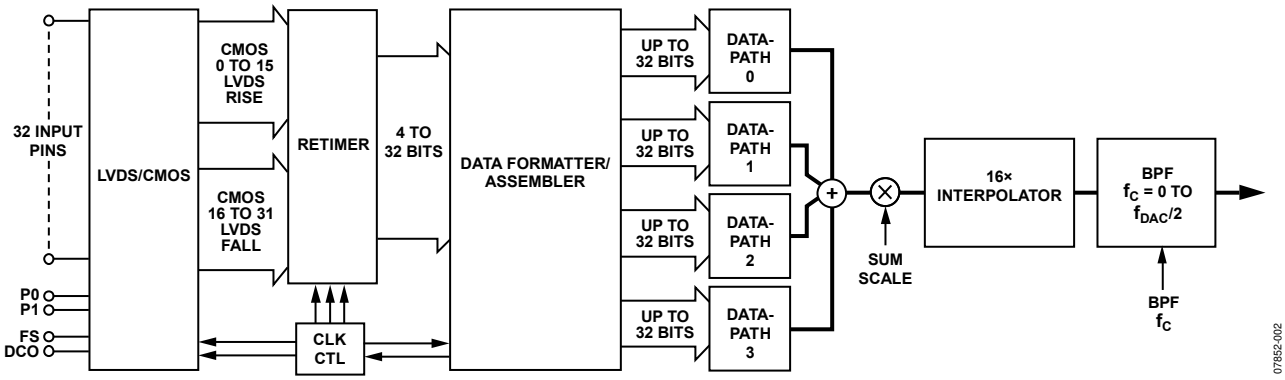


Figure 2. Digital Signal Processing Functional Block Diagram

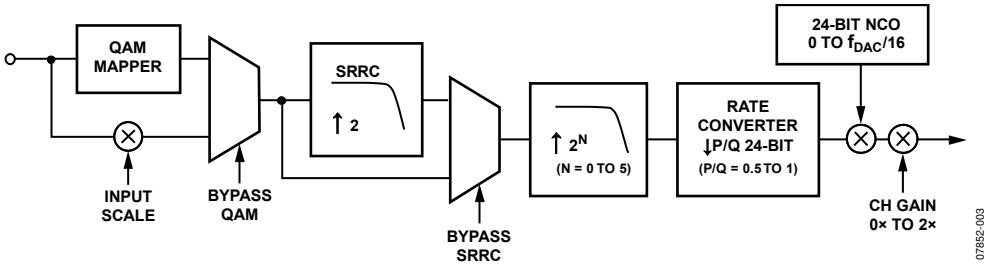


Figure 3. Channel 0 Through Channel 3 Datapath Block Detail (I and Q Paths Are Identical So Only One Is Shown)

SPECIFICATIONS

DC SPECIFICATIONS

AVDD33 = DVDD33 = 3.3 V, CVDD18 = DVDD18 = 1.8 V, DVDD15 = 1.5 V, f_{DAC} = 2.4 GHz, I_{FS} = 20 mA, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
DAC RESOLUTION		14		Bits
ANALOG OUTPUTS				
Offset Error		6.5		% FSR
Gain Error (with Internal Reference)		3.5		% FSR
Full-Scale Output Current (Monotonicity Guaranteed)	8.66	20.2	31.66	mA
Output Compliance Range	−1.0		+1.0	V
Output Resistance		70		Ω
Output Capacitance		1		pF
TEMPERATURE DRIFT				
Gain		135		ppm/°C
Reference Voltage		25		ppm/°C
REFERENCE				
Internal Reference Voltage		1.2		V
Output Resistance[1]		5		kΩ
ANALOG SUPPLY VOLTAGES				
AVDD33	3.14	3.3	3.47	V
CVDD18	1.71	1.8	1.89	V
DIGITAL SUPPLY VOLTAGES				
DVDD33	3.14	3.3	3.47	V
DVDD18	1.71	1.8	1.89	V
DVDD15	1.43	1.5	1.58	V
SUPPLY CURRENTS AND POWER DISSIPATION				
f_{DAC} = 2.4 GSPS, f_{OUT} = 930 MHz, I_{FS} = 25 mA, Four Channels Enabled				
I_{AVDD33}		45		mA
I_{DVDD18}		72		mA
I_{CVDD18}		180		mA
I_{DVDD33}				
CMOS Interface		42		mA
LVDS Interface		16		mA
I_{DVDD15}		640		mA
f_{DAC} = 2.0 GSPS, f_{OUT} = 70 MHz, I_{FS} = 20 mA, CMOS Interface				
I_{AVDD33}		37.4	38.5	mA
I_{DVDD18}		67.3	70.5	mA
I_{CVDD18}		155.4	180	mA
I_{DVDD33}		40.3	50.7	mA
I_{DVDD15} (Four Channels Enabled, All Signal Processing Enabled)		517	556	mA
I_{DVDD15} (One Channel Enabled, 16× Interpolation Only)		365	391	mA
Power Dissipation				
f_{DAC} = 2.4 GSPS, f_{OUT} = 930 MHz, I_{FS} = 25 mA, Four Channels Enabled				
CMOS Interface		1.7		W
LVDS Interface		1.63		W

[1] Use an external amplifier to drive any external load.

DIGITAL SPECIFICATIONS

AVDD33 = DVDD33 = 3.3 V, CVDD18 = DVDD18 = 1.8 V, DVDD15 = 1.5 V, f_{DAC} = 2.4 GHz, I_{FS} = 20 mA, LVDS drivers and receivers are compliant with the IEEE Std 1596.3-1996 reduced range link, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
CMOS DATA INPUTS (D[31:0], P0, P1)				
Input Voltage High, V_{IH}	2.0	3.3		V
Input Voltage Low, V_{IL}		0	0.8	V
Input Current High, I_{IH}	−10		+10	µA
Input Current Low, I_{IL}	−10		+10	µA
Input Capacitance		2		pF
Setup Time, CMOS Data Input to CMOS_DCO[1]	5.3			ns
Hold Time, CMOS Data Input to CMOS_DCO[1]	−1.4			ns
CMOS OUTPUTS (CMOS_FS, CMOS_DCO)				
Output Voltage High, V_{OH}	2.4		3.3	V
Output Voltage Low, V_{OL}	0		0.4	V
Output Current High, I_{OH}		12		mA
Output Current Low, I_{OL}		12		mA
Maximum Clock Rate (CMOS_DCO)	150			MHz
CMOS_DCO to CMOS_FS Delay	0.28		0.85	ns
LVDS DATA INPUTS (D[15:0]P, D[15:0]N, PARP, PARN)				
Input Voltage Range, V_{IA} or V_{IB}	825		1575	mV
Input Differential Threshold, V_{IDTH}	−100		+100	mV
Input Differential Hysteresis, V_{IDTHH}, V_{IDTHL}		25		mV
Input Differential Input Impedance, R_{IN}	80		120	Ω
Maximum LVDS Input Rate	150			MSPS
Setup Time, LVDS Differential Input Data to Differential DCOx[2]	1.41			ns
Hold Time, LVDS Differential Input Data to Differential DCOx[2]	0.24			ns
LVDS OUTPUTS (DCOP, DCON, FSP, FSN) DCOP, FSP = V_{OA}; DCON, FSN = V_{OB}; 100 Ω Termination				
Output Voltage High, V_{OA} or V_{OB}			1375	mV
Output Voltage Low, V_{OA} or V_{OB}	1025			mV
Output Differential Voltage, $\|V_{OD}\|$	150	200	250	mV
Output Offset Voltage, V_{OS}	1150		1250	mV
Output Impedance, Single Ended, R_O	40		140	Ω
R_O Mismatch Between A and B, ΔR_O			10	%
Change in $\|V_{OD}\|$ Between 0 and 1, $\|\Delta V_{OD}\|$			25	mV
Change in V_{OS} Between 0 and 1, ΔV_{OS}			25	mV
Output Current—Driver Shorted to Ground, I_{SA}, I_{SB}			20	mA
Output Current—Drivers Shorted Together, I_{SAB}			4	mA
Power-Off Output Leakage, $\|I_{XA}\|$, $\|I_{XB}\|$			10	mA
Maximum Clock Rate (DCOP, DCON)	150			MHz
DCOx to FSx Delay	0.12		0.37	ns
DAC CLOCK INPUT (CLKP, CLKN)[3]				
Differential Peak Voltage	1.4	1.8		V
Common-Mode Voltage		900		mV
DAC Clock Rate			2400	MHz
SERIAL PERIPHERAL INTERFACE				
Maximum Clock Rate (f_{SCLK}, $1/t_{SCLK}$)			25	MHz
Minimum Pulse Width High, t_{PWH}	20			ns
Minimum Pulse Width Low, t_{PWL}	20			ns
Minimum SDIO and $\overline{CS}$ to SCLK Setup, t_{DS}		10		ns

Parameter	Min	Typ	Max	Unit
Minimum SCLK to SDIO Hold, t_{DH}		5		ns
Maximum SCLK to Valid SDIO and SDO, t_{DV}		20		ns
Minimum SCLK to Invalid SDIO and SDO, t_{DNV}		5		ns
INPUTS (SDIO, SCLK, $\overline{CS}$)				
Input Voltage High, V_{IH}	2.0	3.3		V
Input Voltage Low, V_{IL}		0	0.8	V
Input Current High, I_{IH}	−10		+10	μA
Input Current Low, I_{IL}	−10		+10	μA
OUTPUTS (SDO, SDIO)				
Output Voltage High, V_{OH}	2.4		3.6	V
Output Voltage Low, V_{OL}	0		0.4	V
Output Current High, I_{OH}		4		mA
Output Current Low, I_{OL}		4		mA

[1] See the CMOS Interface Timing section for more information.
[2] See the LVDS Interface Timing section for more information.
[3] See the Clock Phase Noise Effects on AC Performance section for more information.

AC SPECIFICATIONS

AVDD33 = DVDD33 = 3.3 V, CVDD18 = DVDD18 = 1.8 V, DVDD15 = 1.5 V, f_{DAC} = 2.4 GHz, I_{FS} = 20 mA, digital scale = 0 dBFS, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
DAC Update Rate				2400	MSPS
Adjusted DAC Update Rate[1]				150	MSPS
Output Settling Time (t_{ST})	To 0.025%		13		ns
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{DAC} = 2000 MSPS					
f_{OUT} = 100 MHz			70		dBc
f_{OUT} = 316 MHz			63		dBc
f_{OUT} = 550 MHz			58		dBc
f_{DAC} = 2400 MSPS					
f_{OUT} = 100 MHz			70		dBc
f_{OUT} = 316 MHz			70		dBc
f_{OUT} = 550 MHz			60		dBc
f_{OUT} = 850 MHz			60		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)	$f_{OUT2} = f_{OUT1}$ + 1.25 MHz				
f_{DAC} = 2000 MSPS					
f_{OUT} = 100 MHz			86		dBc
f_{OUT} = 316 MHz			73		dBc
f_{OUT} = 550 MHz			62		dBc
f_{DAC} = 2400 MSPS					
f_{OUT} = 100 MHz			86		dBc
f_{OUT} = 316 MHz			74		dBc
f_{OUT} = 550 MHz			66		dBc
f_{OUT} = 850 MHz			66		dBc
NOISE SPECTRAL DENSITY (NSD)					
1-Channel QAM	f_{DAC} = 2400 MSPS				
f_{OUT} = 100 MHz	P_{OUT} = −14.5 dBm		−167		dBm/Hz
f_{OUT} = 316 MHz	P_{OUT} = −15.5 dBm		−166.5		dBm/Hz
f_{OUT} = 550 MHz	P_{OUT} = −18 dBm		−166.5		dBm/Hz
f_{OUT} = 850 MHz	P_{OUT} = −18.5 dBm		−166.5		dBm/Hz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADJACENT CHANNEL LEAKAGE RATIO (ACLR)	f_{DAC} = 2293.76 MSPS measured in 6 MHz channels				
1-Channel QAM					
f_{OUT} = 200 MHz (Harmonics)			−76		dBc
f_{OUT} = 200 MHz (Noise Floor)			−82		dBc
f_{OUT} = 500 MHz (Harmonics)			−74.5		dBc
f_{OUT} = 500 MHz (Noise Floor)			−78		dBc
f_{OUT} = 800 MHz (Harmonics)			−69		dBc
f_{OUT} = 800 MHz (Noise Floor)			−78		dBc
2-Channel QAM					
f_{OUT} = 200 MHz (Harmonics)			−77.5		dBc
f_{OUT} = 200 MHz (Noise Floor)			−81		dBc
f_{OUT} = 500 MHz (Harmonics)			−68		dBc
f_{OUT} = 500 MHz (Noise Floor)			−76		dBc
f_{OUT} = 800 MHz (Harmonics)			−66		dBc
f_{OUT} = 800 MHz (Noise Floor)			−76		dBc
4-Channel QAM					
f_{OUT} = 200 MHz (Harmonics)			−75		dBc
f_{OUT} = 200 MHz (Noise Floor)			−76		dBc
f_{OUT} = 500 MHz (Harmonics)			−69		dBc
f_{OUT} = 500 MHz (Noise Floor)			−72		dBc
f_{OUT} = 800 MHz (Harmonics)			−67		dBc
f_{OUT} = 800 MHz (Noise Floor)			−72		dBc
WCDMA ACLR	f_{DAC} = 2304 MSPS, mix mode second Nyquist zone				
Single Carrier	f_{OUT} = 1850 MHz				
First Adjacent Channel			−70		dBc
Second Alternate Channel			−72.5		dBc
Third Alternate Channel			−74		dBc
Single Carrier	f_{OUT} = 2100 MHz				
First Adjacent Channel			−68		dBc
Second Alternate Channel			−70.4		dBc
Third Alternate Channel			−72.7		dBc
Four Carrier	f_{OUT} = 2100 MHz				
First Adjacent Channel			−63.5		dBc
Second Alternate Channel			−65.1		dBc
Third Alternate Channel			−66.9		dBc

[1] Adjusted DAC update rate is calculated as f_{DAC} divided by the minimum required interpolation factor. For the AD9789, the minimum interpolation factor is 16. Thus, with f_{DAC} = 2400 MSPS, F_{DACadj} = 2400 MSPS/16 = 150 MSPS.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
AVDD33 to AVSS	−0.3 V to +3.6 V
DVDD18 to DVSS	−0.3 V to +1.98 V
DVDD33 to DVSS	−0.3 V to +3.6 V
DVDD15 to DVSS	−0.3 V to +1.98 V
CVDD18 to AVSS	−0.3 V to +1.98 V
AVSS to DVSS	−0.3 V to +0.3 V
CLKP, CLKN to AVSS	−0.3 V to CVDD18 + 0.3 V
FS, DCO to DVSS	−0.3 V to DVDD33 + 0.3 V
CMOS and LVDS Data Inputs to DVSS	−0.3 V to DVDD33 + 0.3 V
IOUTN, IOUTP to AVSS	−1.0 V to AVDD33 + 0.3 V
I120, VREF, IPTAT to AVSS	−0.3 V to AVDD33 + 0.3 V
IRQ, $\overline{CS}$, SCLK, SDO, SDIO, RESET to DVSS	−0.3 V to DVDD33 + 0.3 V
Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit	Notes
164-Ball CSP_BGA	25.5	14.4	6.8	°C/W	4-layer board, no vias
	24.4			°C/W	4-layer board, 4 PCB vias
	19.0			°C/W	8-layer board, 4 PCB vias
	17.2			°C/W	8-layer board, 16 PCB vias

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

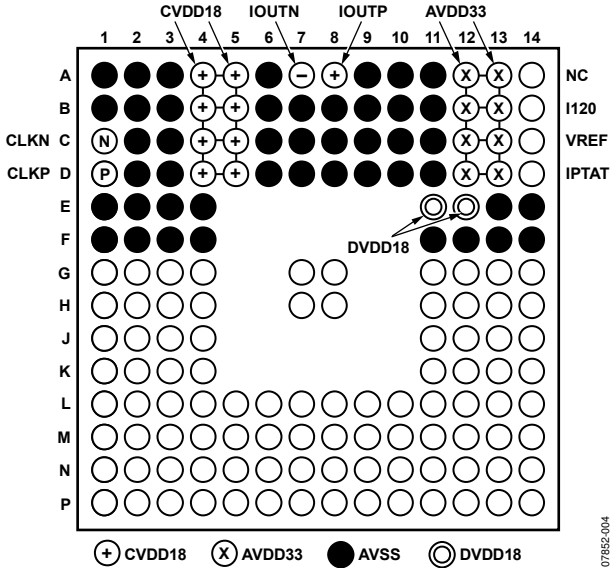


Figure 4. Clock and Analog Pins (Top View)

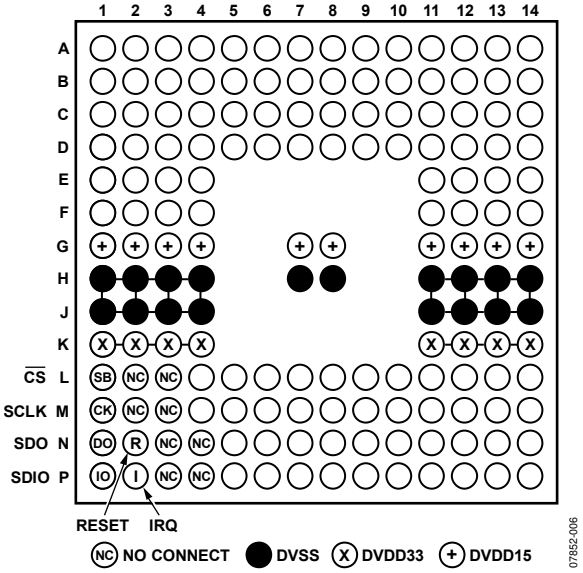


Figure 6. Digital Supply and SPI Pins (Top View)

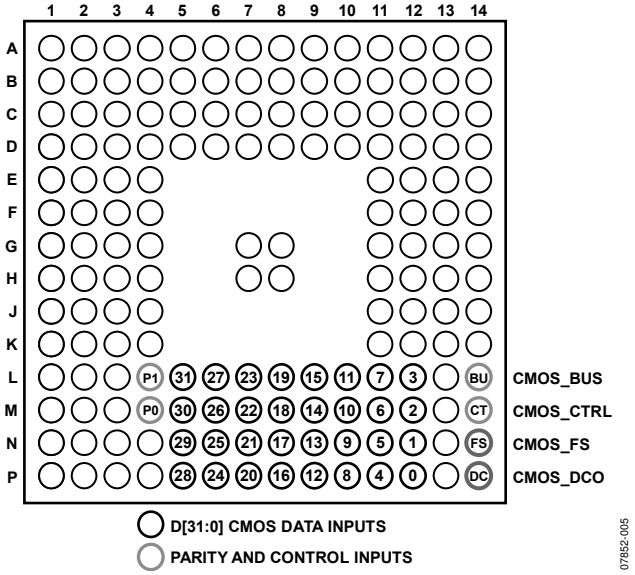


Figure 5. CMOS Mode Data Input Pins (Top View)

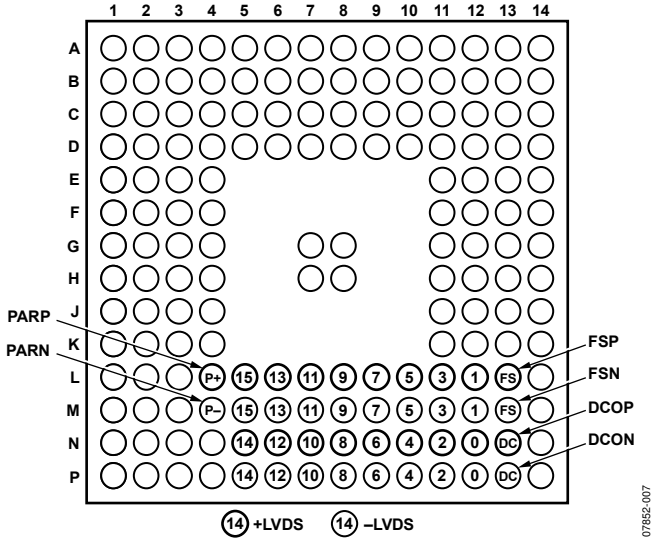


Figure 7. LVDS Mode Data Input Pins (Top View)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1, A2, A3, A6, A9, A10, A11, B1, B2, B3, B6, B7, B8, B9, B10, B11, C2, C3, C6, C7, C8, C9, C10, C11, D2, D3, D6, D7, D8, D9, D10, D11, E1, E2, E3, E4, E13, E14, F1, F2, F3, F4, F11, F12, F13, F14	AVSS	Analog Supply Ground.
A4, A5, B4, B5, C4, C5, D4, D5	CVDD18	1.8 V Clock Supply.
A7	IOUTN	DAC Negative Output Current.
A8	IOUTP	DAC Positive Output Current.
A12, A13, B12, B13, C12, C13, D12, D13	AVDD33	3.3 V Analog Supply.
A14	NC	No Connect. Leave floating.
B14	I120	Tie this pin to analog ground with a 10 kΩ resistor to generate a 120 µA reference current.
C1	CLKN	Negative DAC Clock Input (DACCLK).
C14	VREF	Band Gap Voltage Reference I/O. Decouple to analog ground with a 1 nF capacitor. Output impedance is approximately 5 kΩ.
D1	CLKP	Positive DAC Clock Input (DACCLK).
D14	IPTAT	Factory Test Pin. Output current, proportional to absolute temperature, is approximately 10 µA at 25°C with a slope of approximately 20 nA/°C.
E11, E12	DVDD18	1.8 V Digital Supply.
G1, G2, G3, G4, G7, G8, G11, G12, G13, G14	DVDD15	1.5 V Digital Supply.
H1, H2, H3, H4, H7, H8, H11, H12, H13, H14, J1, J2, J3, J4, J11, J12, J13, J14	DVSS	Digital Supply Ground.
K1, K2, K3, K4, K11, K12, K13, K14	DVDD33	3.3 V Digital Supply.
L1	$\overline{CS}$	Active Low Chip Select for SPI.
L2, L3, M2, M3, N3, N4, P3, P4	NC	Not Used. Leave unconnected.
L4	P1/PARP	CMOS/LVDS Parity Bit.
L5	D31/D15P	CMOS/LVDS Data Input.
L6	D27/D13P	CMOS/LVDS Data Input.
L7	D23/D11P	CMOS/LVDS Data Input.
L8	D19/D9P	CMOS/LVDS Data Input.
L9	D15/D7P	CMOS/LVDS Data Input.
L10	D11/D5P	CMOS/LVDS Data Input.
L11	D7/D3P	CMOS/LVDS Data Input.
L12	D3/D1P	CMOS/LVDS Data Input.
L13	FSP	Positive LVDS Frame Sync (FSP) for Data Bus.
L14	CMOS_BUS	Active High Input. Configures data bus for CMOS inputs. Low input configures data bus to accept LVDS inputs.
M1	SCLK	Qualifying Clock for SPI.
M4	P0/PARN	CMOS/LVDS Parity Bit.
M5	D30/D15N	CMOS/LVDS Data Input.
M6	D26/D13N	CMOS/LVDS Data Input.
M7	D22/D11N	CMOS/LVDS Data Input.
M8	D18/D9N	CMOS/LVDS Data Input.
M9	D14/D7N	CMOS/LVDS Data Input.
M10	D10/D5N	CMOS/LVDS Data Input.
M11	D6/D3N	CMOS/LVDS Data Input.
M12	D2/D1N	CMOS/LVDS Data Input.
M13	FSN	Negative LVDS Frame Sync (FSN) for Data Bus.

Pin No.	Mnemonic	Description
M14	CMOS_CTRL	Active High Input. Enables CMOS_DCO and CMOS_FS signals and disables DCOP/DCON and FSP/FSN signals. Low input disables CMOS_DCO and CMOS_FS signals and enables DCOP/DCON and FSP/FSN signals.
N1	SDO	Serial Data Output for SPI.
N2	RESET	Active High Input. Resets the AD9789.
N5	D29/D14P	CMOS/LVDS Data Input.
N6	D25/D12P	CMOS/LVDS Data Input.
N7	D21/D10P	CMOS/LVDS Data Input.
N8	D17/D8P	CMOS/LVDS Data Input.
N9	D13/D6P	CMOS/LVDS Data Input.
N10	D9/D4P	CMOS/LVDS Data Input.
N11	D5/D2P	CMOS/LVDS Data Input.
N12	D1/D0P	CMOS/LVDS Data Input.
N13	DCOP	Positive LVDS Data Clock Output (DCOP) for Data Bus.
N14	CMOS_FS	CMOS Frame Sync for Data Bus.
P1	SDIO	Serial Data Input/Output for SPI.
P2	IRQ	Active Low, Open-Drain Interrupt Request Output. Pull up to DVDD33 with a 10 kΩ resistor.
P5	D28/D14N	CMOS/LVDS Data Input.
P6	D24/D12N	CMOS/LVDS Data Input.
P7	D20/D10N	CMOS/LVDS Data Input.
P8	D16/D8N	CMOS/LVDS Data Input.
P9	D12/D6N	CMOS/LVDS Data Input.
P10	D8/D4N	CMOS/LVDS Data Input.
P11	D4/D2N	CMOS/LVDS Data Input.
P12	D0/D0N	CMOS/LVDS Data Input.
P13	DCON	Negative LVDS Data Clock Output (DCON) for Data Bus.
P14	CMOS_DCO	CMOS Data Clock Output for Data Bus.

TYPICAL PERFORMANCE CHARACTERISTICS

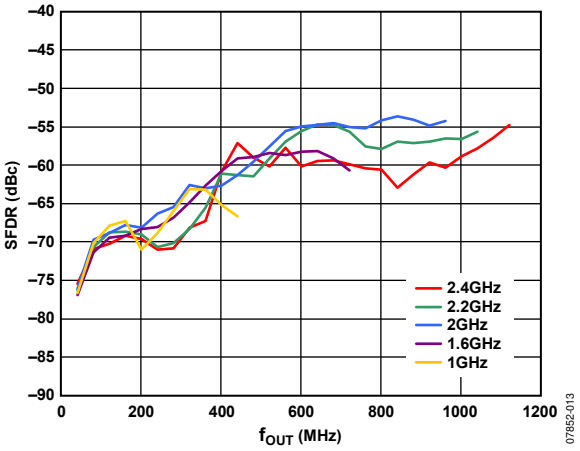


Figure 8. SFDR vs. f_{OUT} over f_{DAC}, Full-Scale Current = 20 mA, Digital Scale = 0 dBFS, Temperature = 25°C

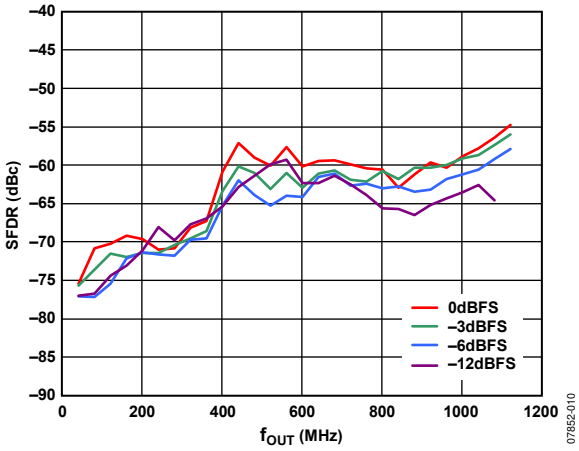


Figure 11. SFDR vs. f_{OUT} over Digital Full Scale, f_{DAC} = 2.4 GHz, Full-Scale Current = 20 mA, Temperature = 25°C

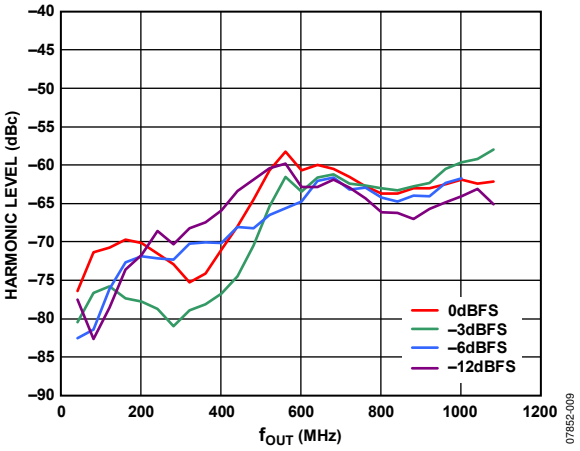


Figure 9. Second-Order Harmonic vs. f_{OUT} over Digital Full Scale, f_{DAC} = 2.4 GHz, Full-Scale Current = 20 mA, Temperature = 25°C

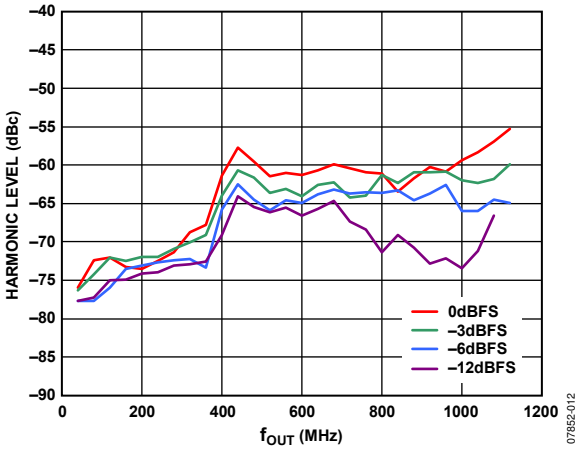


Figure 12. Third-Order Harmonic vs. f_{OUT} over Digital Full Scale, f_{DAC} = 2.4 GHz, Full-Scale Current = 20 mA, Temperature = 25°C

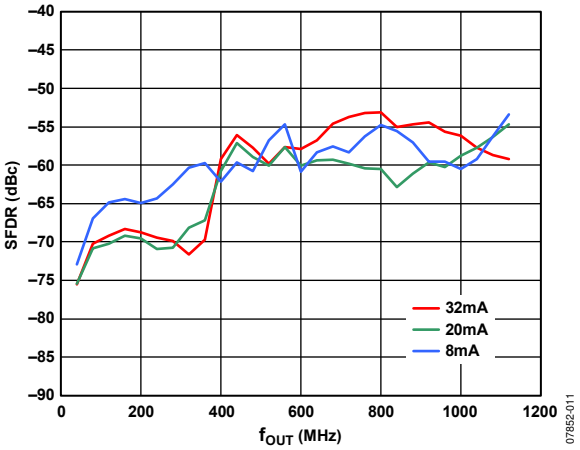


Figure 10. SFDR vs. f_{OUT} over Full-Scale Current, f_{DAC} = 2.4 GHz, Digital Scale = 0 dBFS, Temperature = 25°C

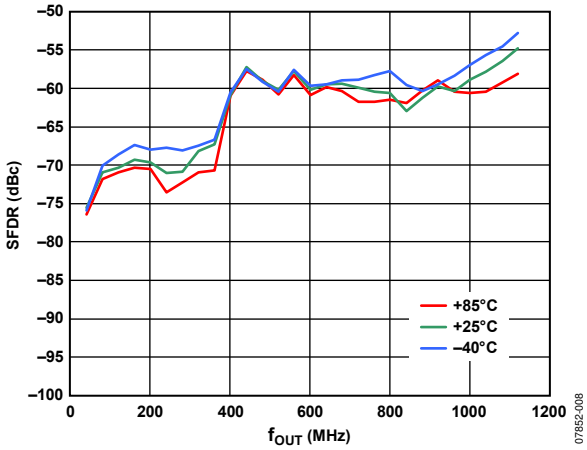


Figure 13. SFDR vs. f_{OUT} over Temperature, f_{DAC} = 2.4 GHz, Full-Scale Current = 20 mA, Digital Scale = 0 dBFS

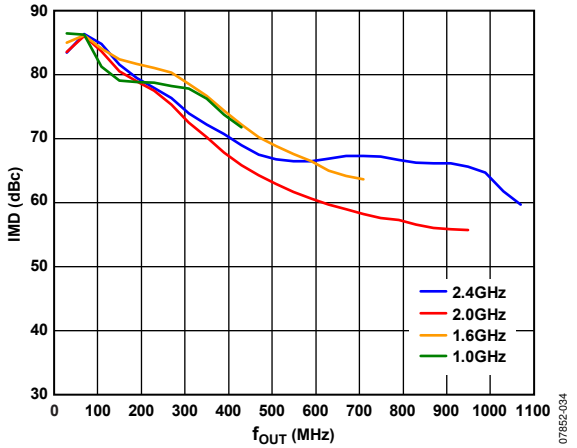


Figure 14. Third-Order IMD vs. f_{OUT} over f_{DAC}, Full-Scale Current = 20 mA, Digital Scale = 0 dBFS, Temperature = 25°C

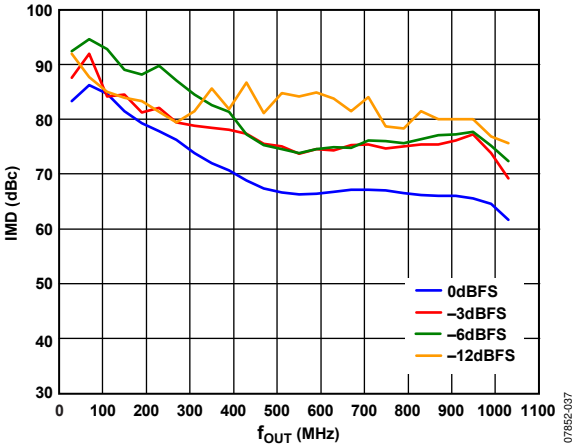


Figure 17. Third-Order IMD vs. f_{OUT} over Digital Full Scale, f_{DAC} = 2.4 GHz, Full-Scale Current = 20 mA, Temperature = 25°C

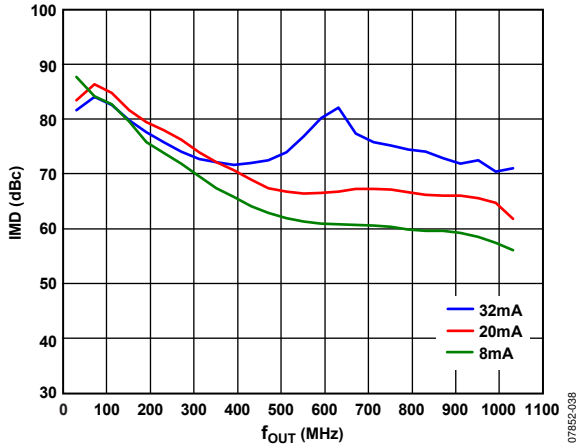


Figure 15. Third-Order IMD vs. f_{OUT} over Full-Scale Current, f_{DAC} = 2.4 GHz, Digital Scale = 0 dBFS, Temperature = 25°C

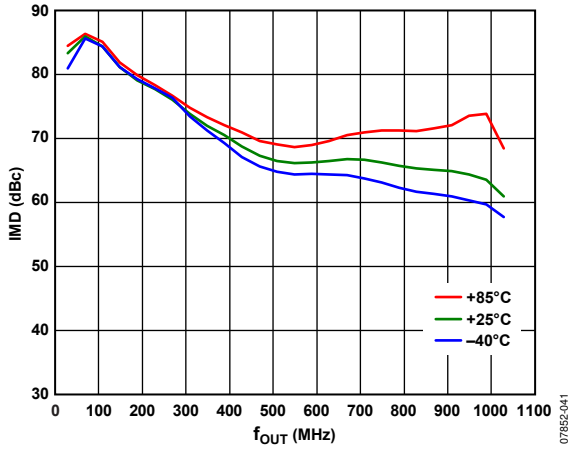


Figure 18. Third-Order IMD vs. f_{OUT} over Temperature, f_{DAC} = 2.4 GHz, Full-Scale Current = 20 mA, Digital Scale = 0 dBFS

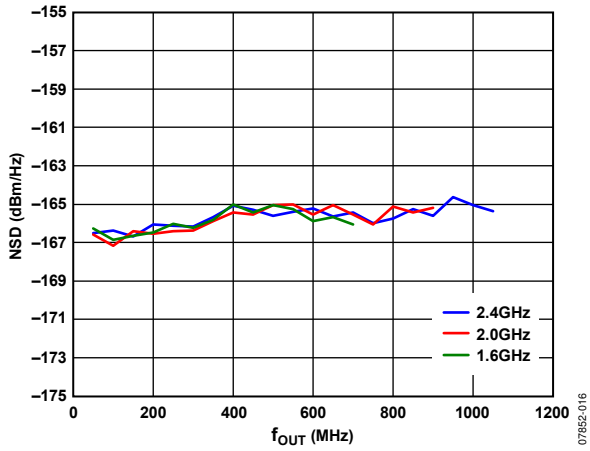


Figure 16. NSD vs. f_{OUT} over f_{DAC}, 1-Channel QAM, Full-Scale Current = 20 mA

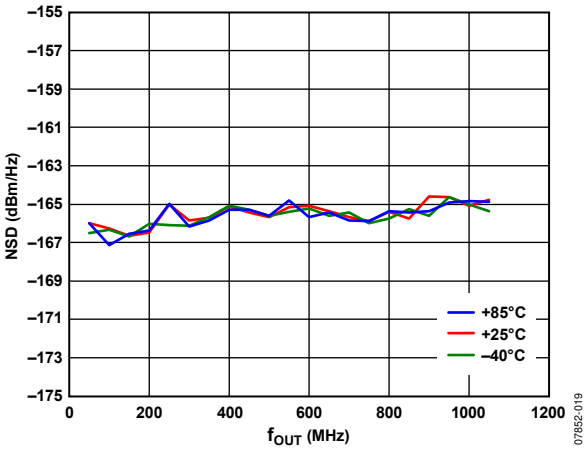


Figure 19. NSD vs. f_{OUT} over Temperature, 1-Channel QAM, f_{DAC} = 2.4 GHz, Full-Scale Current = 20 mA

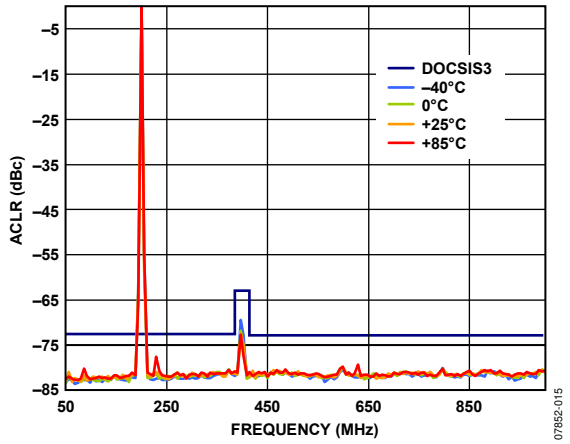


Figure 20. ACLR Performance over Temperature, 1-Channel QAM, f_{DAC} = 2.3 GHz, Full-Scale Current = 20 mA, f_{OUT} = 200 MHz, Sum Scale = 48 (DOCSIS SPEC Is −73 dBc; Harmonic Exception Is −63 dBc)

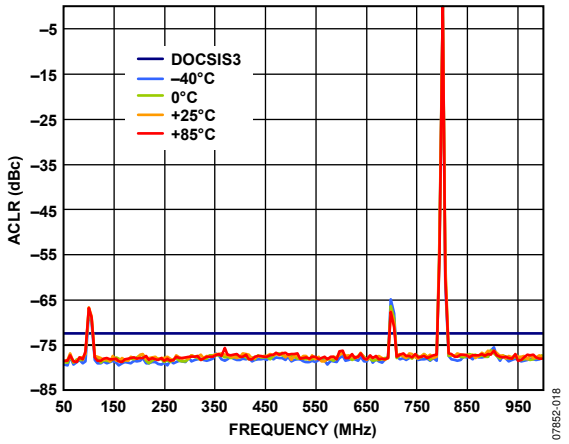


Figure 23. ACLR Performance over Temperature, 1-Channel QAM, f_{DAC} = 2.3 GHz, Full-Scale Current = 20 mA, f_{OUT} = 800 MHz, Sum Scale = 48 (DOCSIS SPEC Is −73 dBc)

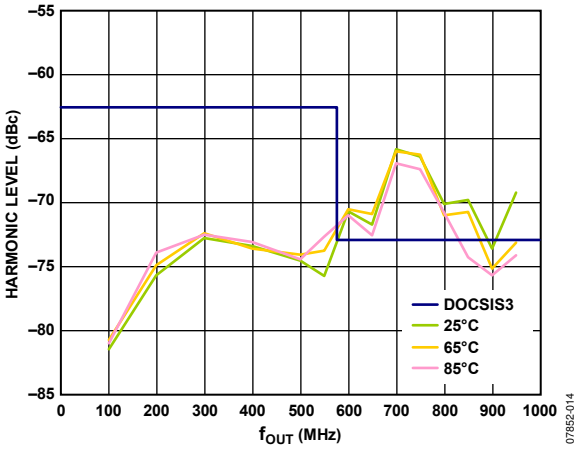


Figure 21. Second-Order Harmonic Performance vs. f_{OUT} over Temperature, 1-Channel QAM, f_{DAC} = 2.3 GHz, Full-Scale Current = 20 mA, Sum Scale = 48 (DOCSIS SPEC Is −73 dBc; Harmonic Exception Is −63 dBc)

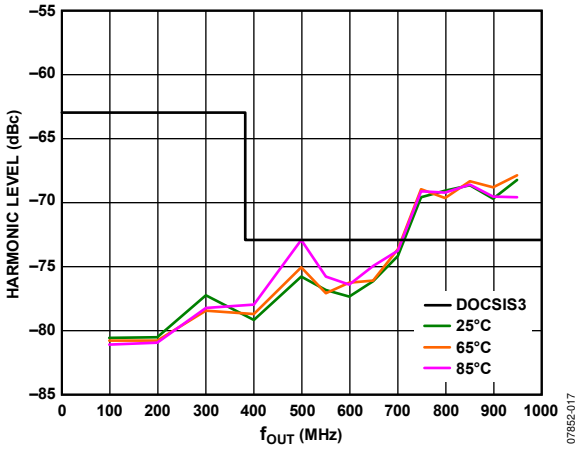


Figure 24. Third-Order Harmonic Performance vs. f_{OUT} over Temperature, 1-Channel QAM, f_{DAC} = 2.3 GHz, Full-Scale Current = 20 mA, Sum Scale = 48 (DOCSIS SPEC Is −73 dBc; Harmonic Exception Is −63 dBc)

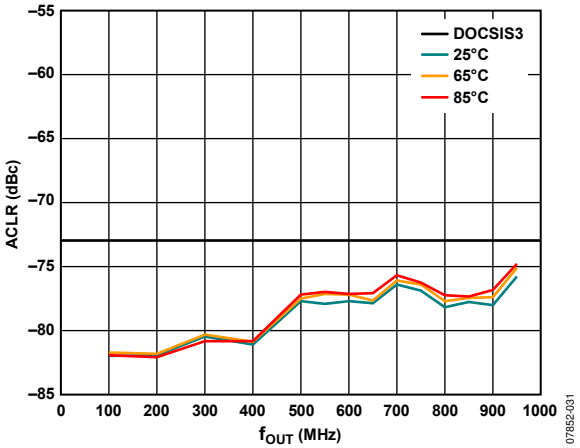


Figure 22. Noise Floor vs. f_{OUT} over Temperature (ACLR Measured Beyond 30 MHz), 1-Channel QAM, f_{DAC} = 2.3 GHz, Full-Scale Current = 20 mA, Sum Scale = 48 (DOCSIS SPEC Is −73 dBc)

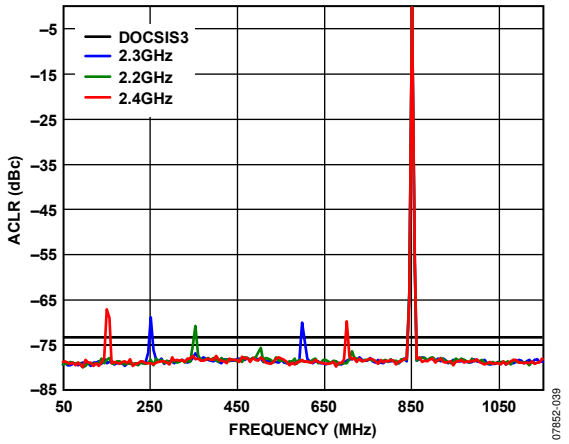


Figure 25. ACLR Performance over f_{DAC}, 1-Channel QAM, f_{OUT} = 850 MHz, Full-Scale Current = 20 mA, Temperature = 25°C, Sum Scale = 48 (DOCSIS SPEC Is −73 dBc)

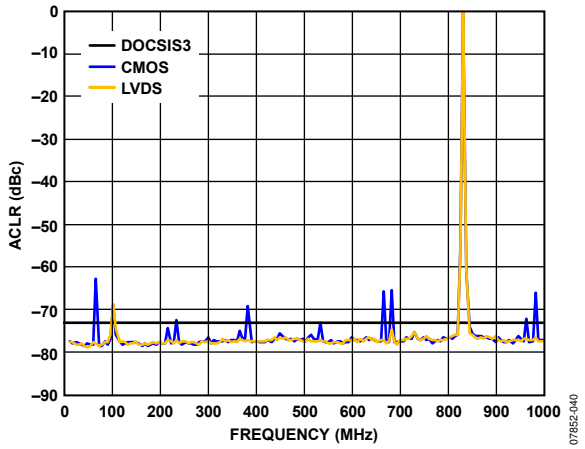


Figure 26. ACLR Performance for CMOS and LVDS Interfaces, 1-Channel QAM, f_{OUT} = 840 MHz, f_{DAC} = 2.4 GHz, Full-Scale Current = 20 mA, Sum Scale = 48 (DOCSIS SPEC Is −73 dBc)

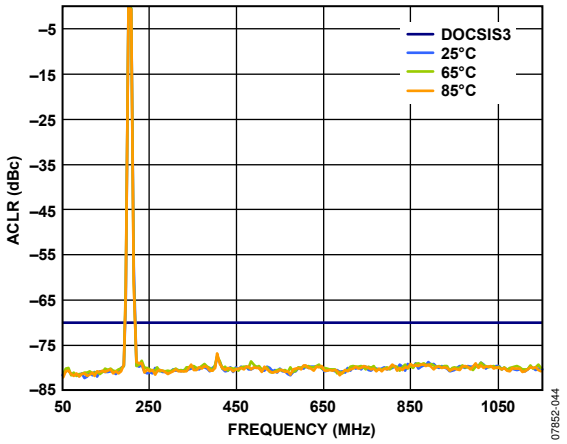


Figure 29. ACLR Performance over Temperature, 2-Channel QAM, f_{OUT} = 200 MHz, f_{DAC} = 2.3 GHz, Full-Scale Current = 25 mA, Sum Scale = 32 (DOCSIS SPEC Is −70 dBc; Harmonic Exception Is −63 dBc)

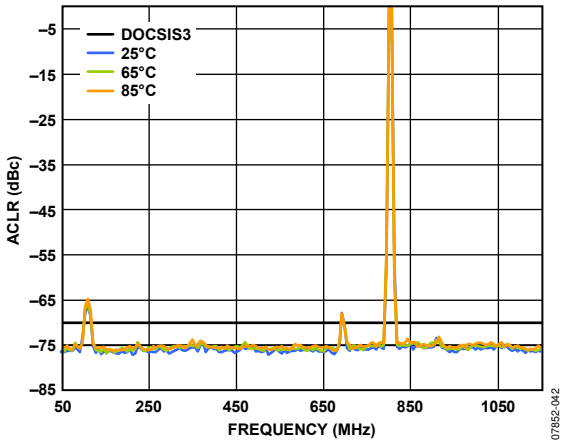


Figure 27. ACLR Performance over Temperature, 2-Channel QAM, f_{OUT} = 800 MHz, f_{DAC} = 2.3 GHz, Full-Scale Current = 25 mA, Sum Scale = 32 (DOCSIS SPEC Is −70 dBc)

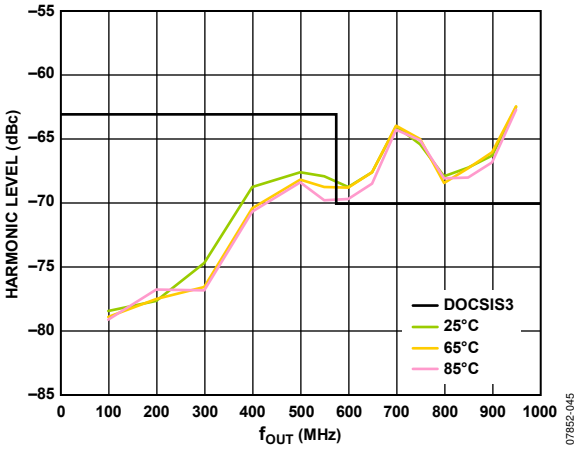


Figure 30. Second Harmonic Performance vs. f_{OUT} over Temperature, 2-Channel QAM, f_{DAC} = 2.3 GHz, Full-Scale Current = 25 mA, Sum Scale = 32 (DOCSIS SPEC Is −70 dBc; Harmonic Exception Is −63 dBc)

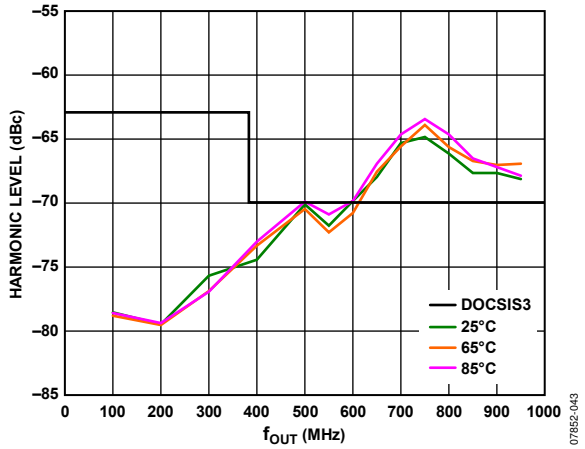


Figure 28. Third-Order Harmonic Performance vs. f_{OUT} over Temperature, 2-Channel QAM, f_{DAC} = 2.3 GHz, Full-Scale Current = 25 mA, Sum Scale = 32 (DOCSIS SPEC Is −70 dBc; Harmonic Exception Is −63 dBc)

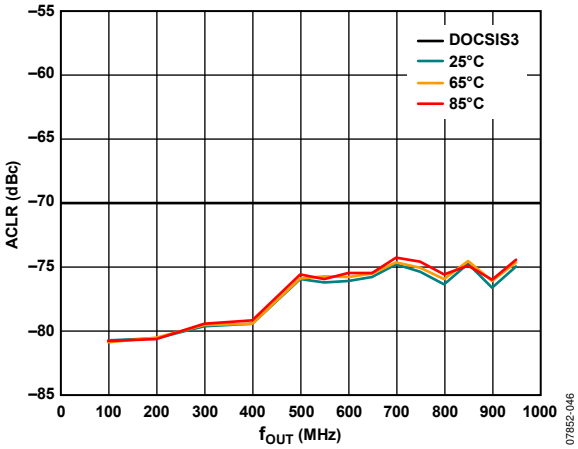


Figure 31. Noise Floor vs. f_{OUT} over Temperature (ACLR Measured Beyond 30 MHz), 2-Channel QAM, f_{DAC} = 2.3 GHz, Full-Scale Current = 25 mA, Sum Scale = 32 (DOCSIS SPEC Is −70 dBc)

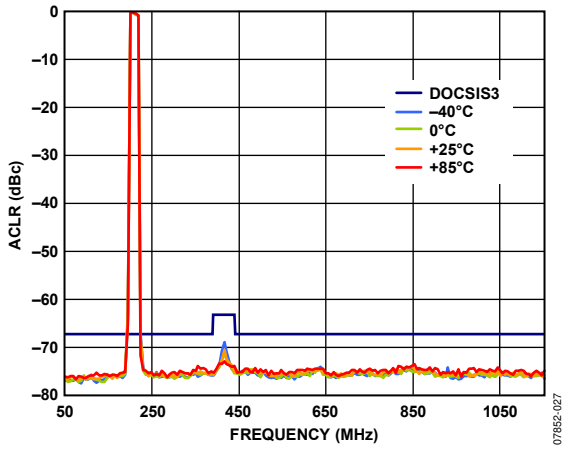


Figure 32. ACLR Performance over Temperature, 4-Channel QAM, f_{OUT} = 200 MHz, f_{DAC} = 2.3 GHz, Full-Scale Current = 25 mA, Sum Scale = 20 (DOCSIS SPEC Is −67 dBc; Harmonic Exception Is −63 dBc)

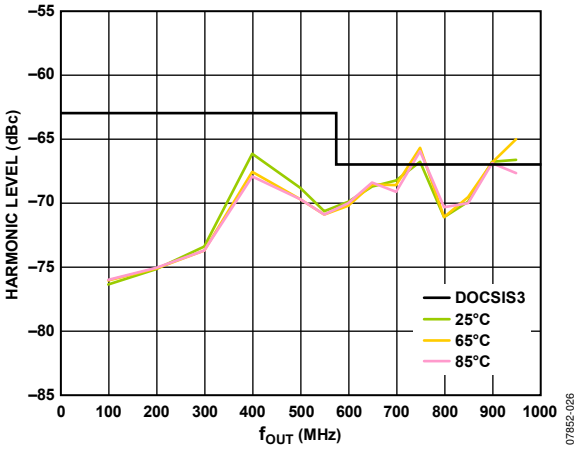


Figure 33. Second-Order Harmonic Performance vs. f_{OUT} over Temperature, 4-Channel QAM, f_{DAC} = 2.3 GHz, Full-Scale Current = 25 mA, Sum Scale = 20 (DOCSIS SPEC Is −67 dBc; Harmonic Exception Is −63 dBc)

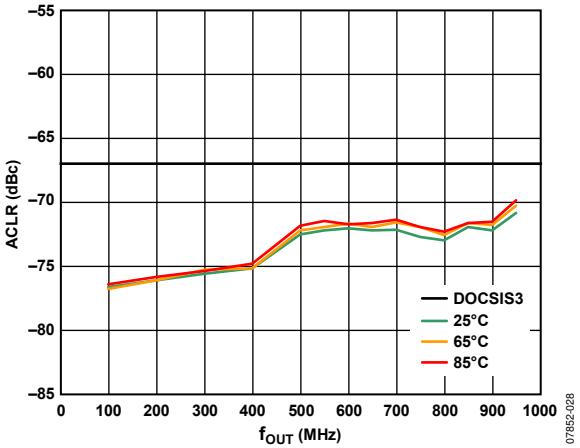


Figure 34. Noise Floor vs. f_{OUT} over Temperature (ACLR Measured Beyond 30 MHz), 4-Channel QAM, f_{DAC} = 2.3 GHz, Full-Scale Current = 25 mA, Sum Scale = 20 (DOCSIS SPEC Is −67 dBc)

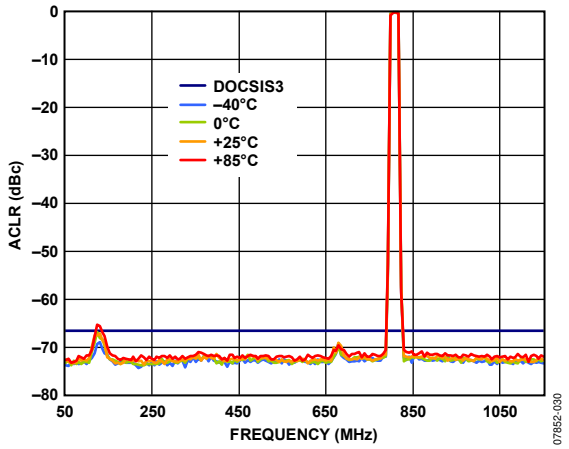


Figure 35. ACLR Performance over Temperature, 4-Channel QAM, f_{OUT} = 800 MHz, f_{DAC} = 2.3 GHz, Full-Scale Current = 25 mA, Sum Scale = 20 (DOCSIS SPEC Is −67 dBc)

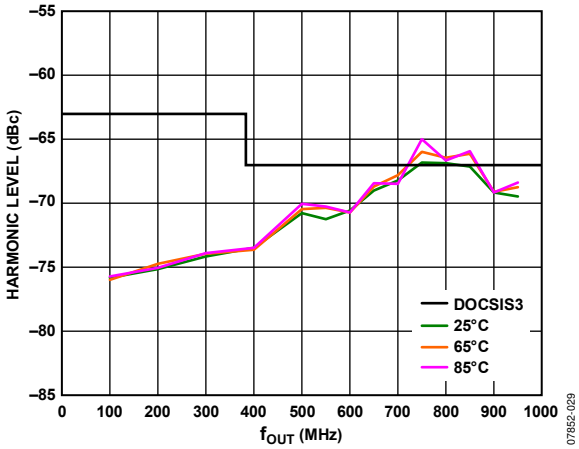


Figure 36. Third-Order Harmonic Performance vs. f_{OUT} over Temperature, 4-Channel QAM, f_{DAC} = 2.3 GHz, Full-Scale Current = 25 mA, Sum Scale = 20 (DOCSIS SPEC Is −67 dBc; Harmonic Exception Is −63 dBc)

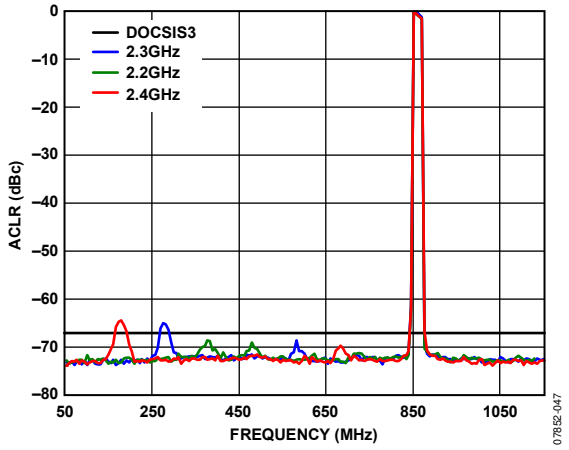
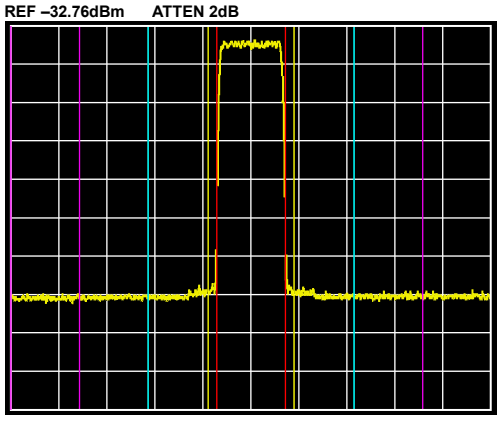


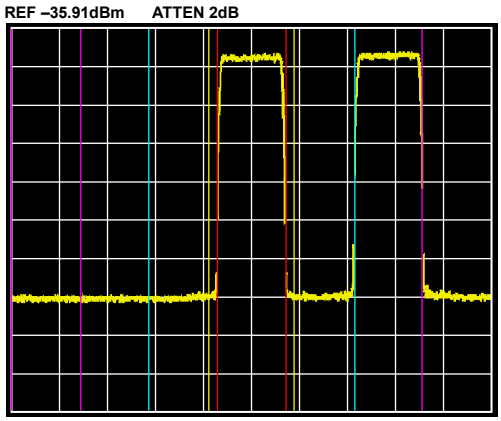
Figure 37. ACLR Performance over f_{DAC}, 4-Channel QAM, f_{OUT} = 850 MHz, Full-Scale Current = 25 mA, Temperature = 25°C, Sum Scale = 20 (DOCSIS SPEC Is −67 dBc)



RMS RESULTS	FREQ. OFFSET	REF BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm
CARRIER POWER –18.10dBm/ 6.00000MHz	3.375MHz	750.0kHz	–65.57	–83.66	–68.98	–87.07
	6.375MHz	5.250MHz	–75.01	–93.11	–74.62	–92.71
	12.00MHz	6.000MHz	–76.83	–94.92	–76.46	–94.55
	18.00MHz	6.000MHz	–77.17	–95.26	–76.56	–94.66

07852-020

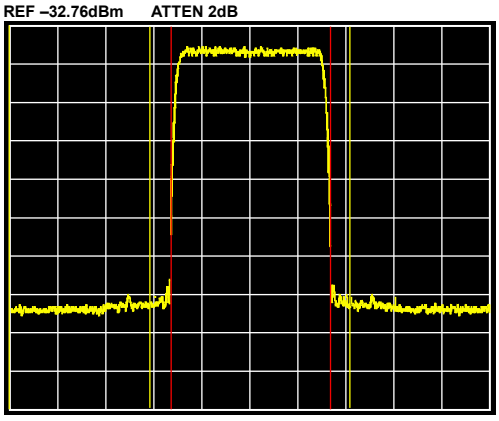
Figure 38. 1-Channel QAM ACLR, f_{OUT} = 840 MHz, Temperature = 25°C, Sum Scale = 48, Full-Scale Current = 20 mA, Span = 42 MHz



RMS RESULTS	FREQ. OFFSET	REF BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm
CARRIER POWER –21.75dBm/ 6.00000MHz	3.375MHz	750.0kHz	–71.64	–93.39	–72.50	–94.25
	6.375MHz	5.250MHz	–73.71	–95.47	–66.72	–88.47
	12.00MHz	6.000MHz	–73.58	–95.33	0.50	–21.10
	18.00MHz	6.000MHz	–73.70	–95.45	–66.72	–88.48

07852-061

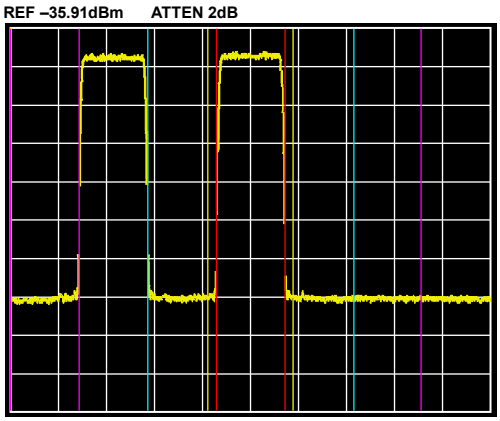
Figure 39. 2-Channel QAM ACLR, f_{OUT} = 840 MHz, Sum Scale = 32, Full-Scale Current = 25 mA, Span = 42 MHz, Channel 1



RMS RESULTS	FREQ. OFFSET	REF BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm
CARRIER POWER –17.98dBm/ 6.00000MHz	3.375MHz	750.0kHz	–73.99	–91.97	–74.93	–92.91
	6.375MHz	5.250MHz	–74.94	–92.92	–75.35	–93.33

07852-023

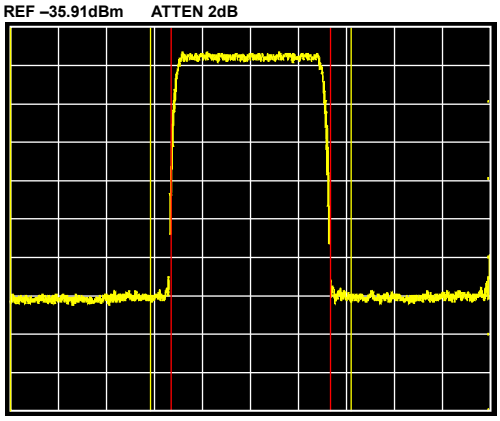
Figure 40. 1-Channel QAM ACLR, f_{OUT} = 840 MHz, Temperature = 25°C, Sum Scale = 48, Full-Scale Current = 20 mA, Span = 18 MHz



RMS RESULTS	FREQ. OFFSET	REF BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm
CARRIER POWER –21.29dBm/ 6.00000MHz	3.375MHz	750.0kHz	–70.07	–92.16	–73.20	–94.49
	6.375MHz	5.250MHz	–69.05	–90.34	–73.87	–95.16
	12.00MHz	6.000MHz	–0.49	–21.78	–73.29	–94.58
	18.00MHz	6.000MHz	–66.61	–87.90	–73.98	–95.27

07852-066

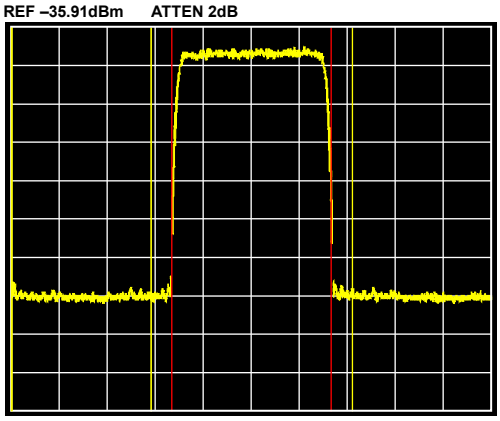
Figure 41. 2-Channel QAM ACLR, f_{OUT} = 840 MHz, Sum Scale = 32, Full-Scale Current = 25 mA, Span = 42 MHz, Channel 2



RMS RESULTS	FREQ. OFFSET	REF BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm
CARRIER POWER –21.56dBm/ 6.00000MHz	3.375MHz	750.0kHz	–75.37	–96.93	–75.56	–97.11
	6.375MHz	5.250MHz	–73.85	–95.41	–72.54	–94.10

07852-065

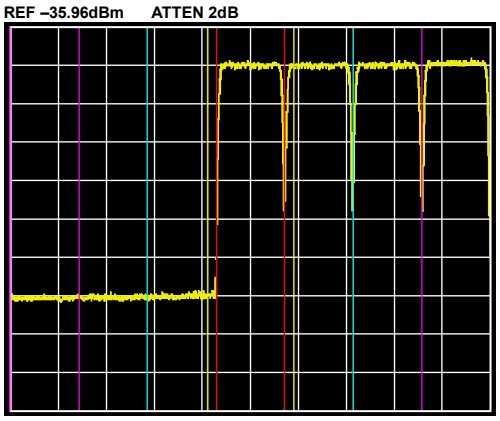
Figure 42. Zoomed 2-Channel QAM ACLR, f_{OUT} = 840 MHz, Sum Scale = 32, Full-Scale Current = 25 mA, Span = 18 MHz, Channel 1



RMS RESULTS	FREQ. OFFSET	REF BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm
CARRIER POWER –21.03dBm/ 6.00000MHz	3.375MHz	750.0kHz	–75.51	–96.54	–75.17	–96.20
	6.375MHz	5.250MHz	–72.55	–93.58	–73.90	–94.93

07852-067

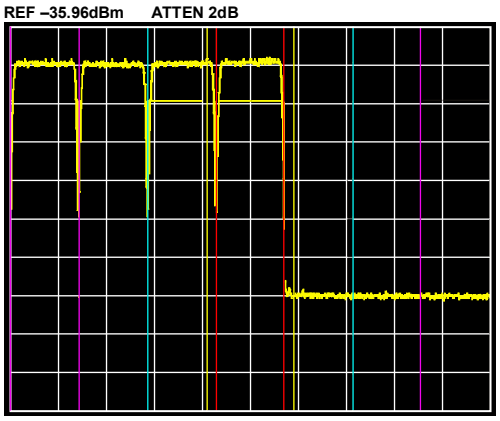
Figure 44. Zoomed 2-Channel QAM ACLR, f_{OUT} = 840 MHz, Sum Scale = 32, Full-Scale Current = 25 mA, Span = 18 MHz, Channel 2



RMS RESULTS	FREQ. OFFSET	REF BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm
CARRIER POWER –23.63dBm/ 6.00000MHz	3.375MHz	750.0kHz	–70.33	–93.96	–11.07	–34.70
	6.375MHz	5.250MHz	–69.04	–92.67	–0.49	–24.12
	12.00MHz	6.000MHz	–70.38	–94.01	0.00	–23.63
	18.00MHz	6.000MHz	–71.02	–94.65	0.43	–23.20

07852-021

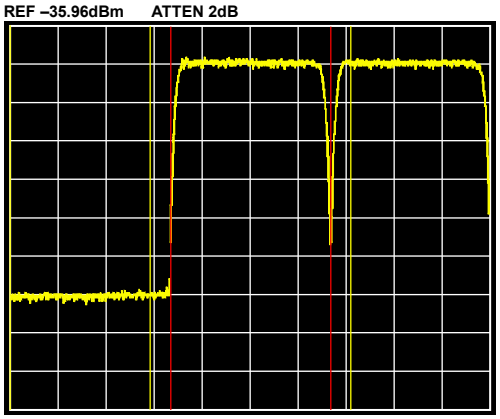
Figure 43. 4-Channel QAM ACLR, f_{OUT} = 840 MHz, Temperature = 25°C, Sum Scale = 20, Full-Scale Current = 25 mA, Span = 42 MHz, Channel 1



RMS RESULTS	FREQ. OFFSET	REF BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm
CARRIER POWER –23.23dBm/ 6.00000MHz	3.375MHz	750.0kHz	–11.10	–34.32	–72.19	–95.42
	6.375MHz	5.250MHz	–0.75	–23.98	–68.97	–92.20
	12.00MHz	6.000MHz	–0.59	–23.81	–70.32	–93.55
	18.00MHz	6.000MHz	–0.35	–23.58	–70.70	–93.93

07852-022

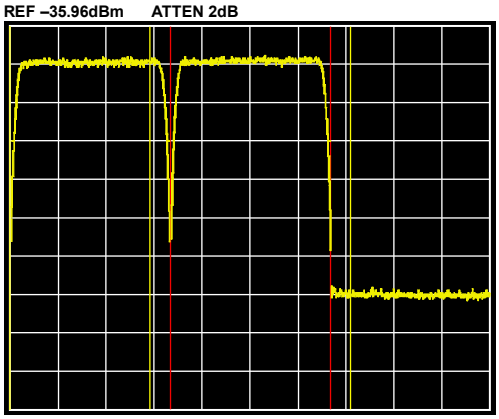
Figure 45. 4-Channel QAM ACLR, f_{OUT} = 840 MHz, Temperature = 25°C, Sum Scale = 20, Full-Scale Current = 25 mA, Span = 42 MHz, Channel 4



RMS RESULTS	FREQ. OFFSET	REF BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm
CARRIER POWER –23.62dBm/ 6.00000MHz	3.375MHz	750.0kHz	–72.95	–96.56	–10.86	–34.48
	6.375MHz	5.250MHz	–69.38	–92.99	–0.51	–24.13

07852-024

Figure 46. Zoomed 4-Channel QAM ACLR, f_{OUT} = 840 MHz, Temperature = 25°C, Sum Scale = 20, Full-Scale Current = 25 mA, Span = 18 MHz, Channel 1



RMS RESULTS	FREQ. OFFSET	REF BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm
CARRIER POWER –23.20dBm/ 6.00000MHz	3.375MHz	750.0kHz	–11.20	–34.40	–74.44	–97.64
	6.375MHz	5.250MHz	–0.77	–23.96	–69.07	–92.26

07852-025

Figure 49. Zoomed 4-Channel QAM ACLR, f_{OUT} = 840 MHz, Temperature = 25°C, Sum Scale = 20, Full-Scale Current = 25 mA, Span = 18 MHz, Channel 4

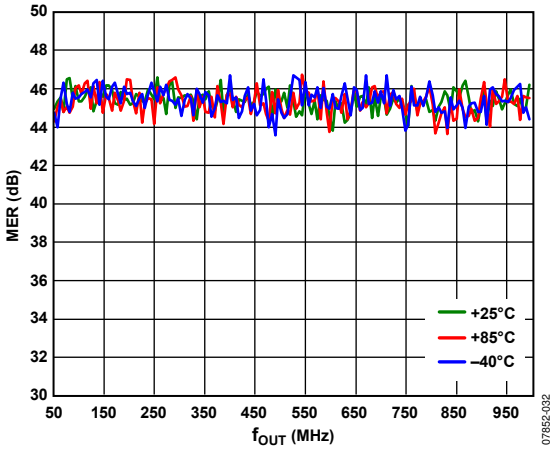


Figure 47. Modulation Error Ratio, Equalized, 1-Channel 256-QAM, f_{DAC} = 2.29376 GHz, Full-Scale Current = 20 mA, Sum Scale = 48 (Equalization Filter from Demodulation Toolbox on Spectrum Analyzer Used)

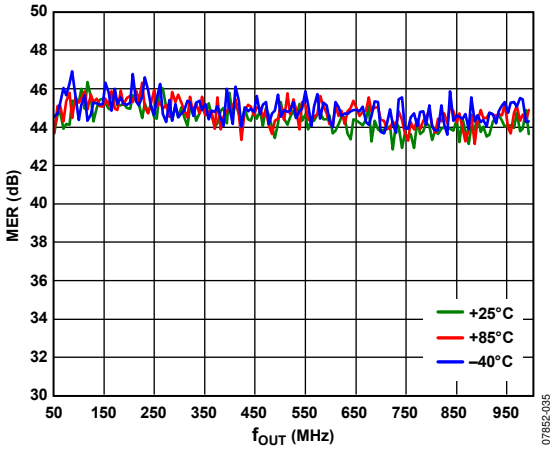


Figure 50. Modulation Error Ratio, Equalized, 4-Channel 256-QAM, f_{DAC} = 2.29376 GHz, Full-Scale Current = 25 mA, Sum Scale = 20 (Equalization Filter from Demodulation Toolbox on Spectrum Analyzer Used)

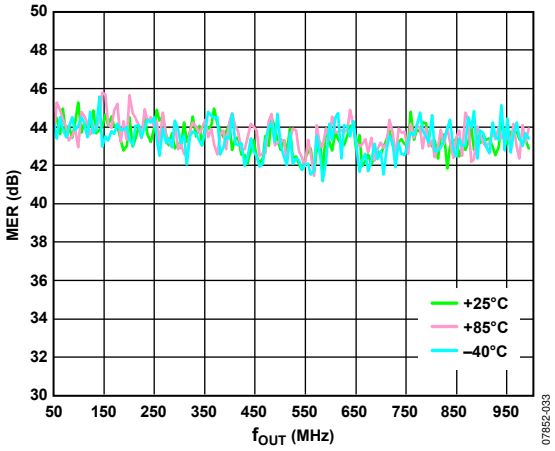


Figure 48. Modulation Error Ratio, Unequalized, 1-Channel 256-QAM, f_{DAC} = 2.29376 GHz, Full-Scale Current = 20 mA, Sum Scale = 48

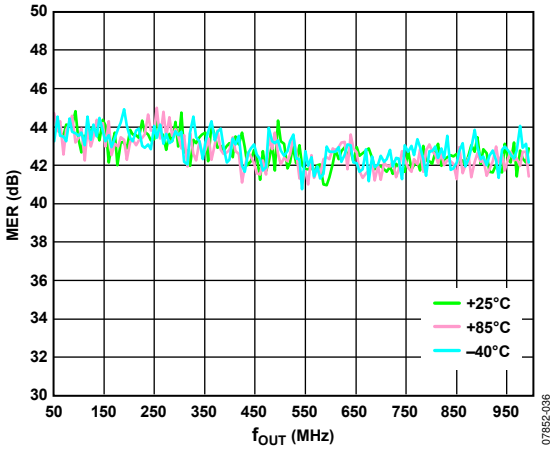


Figure 51. Modulation Error Ratio, Unequalized, 4-Channel 256-QAM, f_{DAC} = 2.29376 GHz, Full-Scale Current = 25 mA, Sum Scale = 20

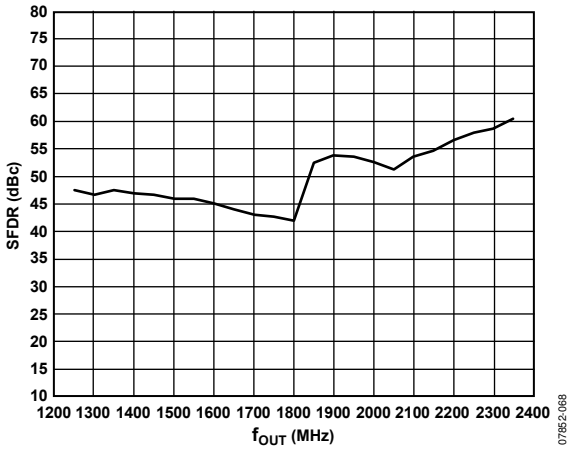


Figure 52. SFDR vs. f_{OUT} in Mix Mode, f_{DAC} = 2.4 GHz, Full-Scale Current = 20 mA (Second Nyquist Zone Performance)

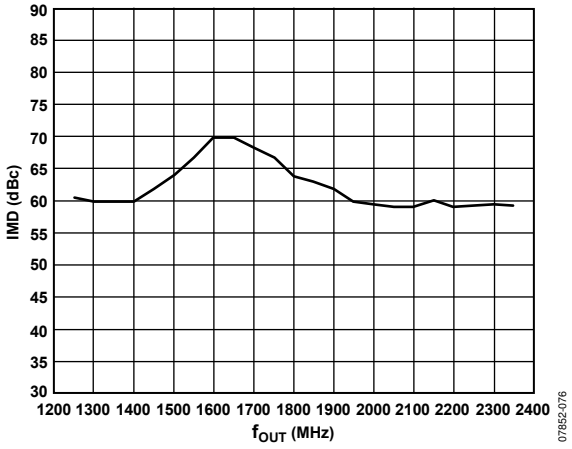


Figure 53. IMD vs. f_{OUT} in Mix Mode, f_{DAC} = 2.4 GHz, Full-Scale Current = 20 mA (Second Nyquist Zone Performance)

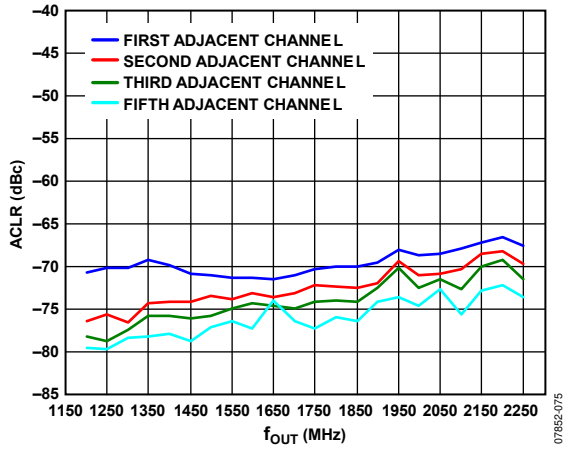
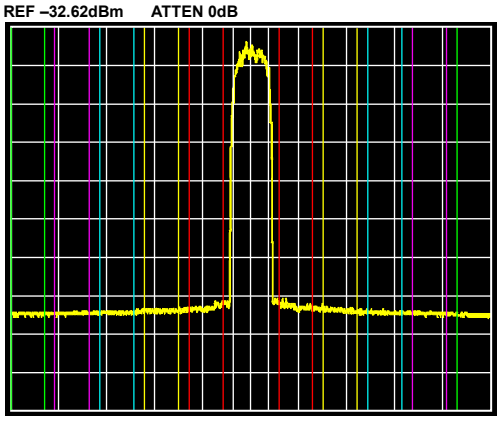


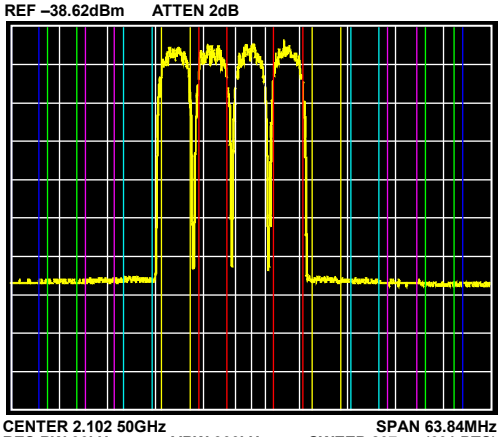
Figure 54. ACLR vs. f_{OUT} in Mix Mode with One-Carrier WCDMA, f_{DAC} = 2304 MHz, Full-Scale Current = 20 mA (Second Nyquist Zone Performance)



RMS RESULTS	FREQ. OFFSET	REF BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm
CARRIER POWER –19.95dBm/ 3.84000MHz	5.000MHz	3.840MHz	–68.93	–88.88	–67.99	–87.94
	10.00MHz	3.840MHz	–71.31	–91.26	–70.42	–90.37
	15.00MHz	3.840MHz	–73.43	–93.37	–72.68	–92.63
	20.00MHz	3.840MHz	–75.12	–95.07	–74.89	–94.84
	25.00MHz	3.840MHz	–75.60	–95.55	–76.51	–96.46

07852-092

Figure 55. One-Carrier WCDMA ACLR in Mix Mode, f_{OUT} = 2.1 GHz, f_{DAC} = 2304 MHz, Full-Scale Current = 20 mA



RMS RESULTS	FREQ. OFFSET	REF BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm
CARRIER POWER –26.06dBm/ 3.84000MHz	5.000MHz	3.840MHz	–0.25	–26.31	–0.42	–26.47
	10.00MHz	3.840MHz	–0.42	–26.48	–63.50	–89.56
	15.00MHz	3.840MHz	–64.07	–90.13	–65.13	–91.18
	20.00MHz	3.840MHz	–65.36	–91.42	–66.97	–93.03
	25.00MHz	3.840MHz	–66.86	–92.92	–68.70	–94.76
	30.00MHz	3.840MHz	–67.83	–93.89	–68.64	–94.70

07852-093

Figure 56. Four-Carrier WCDMA ACLR in Mix Mode, f_{OUT} = 2.1 GHz, f_{DAC} = 2304 MHz, Full-Scale Current = 20 mA

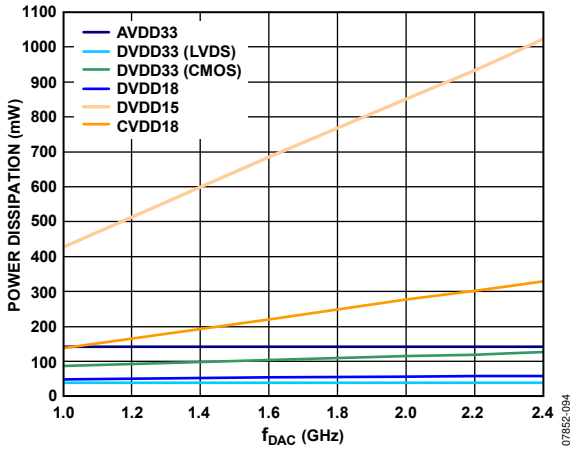


Figure 57. Power Dissipation by Supply vs. f_{DAC}, 4-Channel DOCSIS, f_{OUT} = 915 MHz, Full-Scale Current = 25 mA (Datapath Configuration: QAM Encoder On, SRRC Filter On, Four 2× Interpolation Filters On)

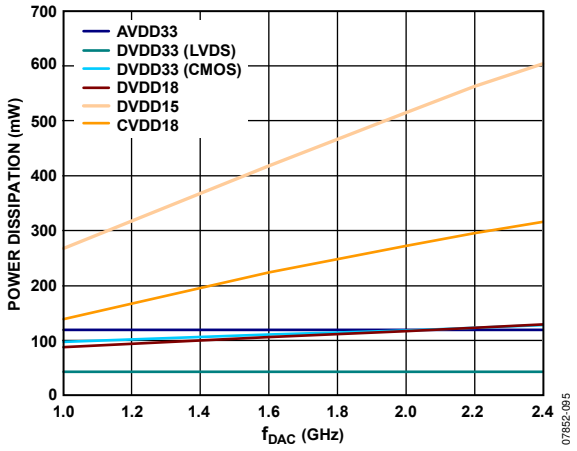


Figure 58. Power Dissipation by Supply vs. f_{DAC}, 16× Interpolation, One Channel Enabled, f_{OUT} = 70 MHz, Full-Scale Current = 20 mA

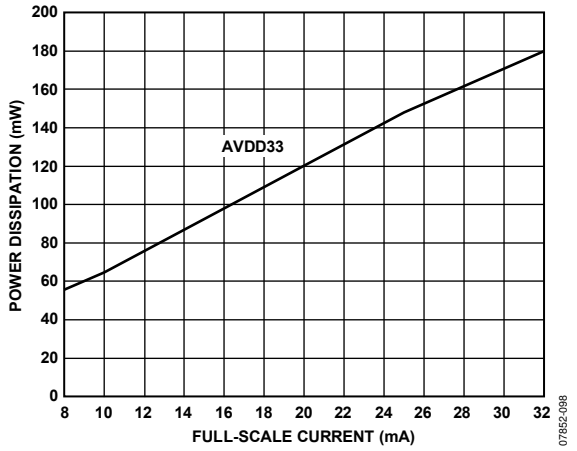


Figure 59. AVDD33 Power Dissipation vs. Full-Scale Current

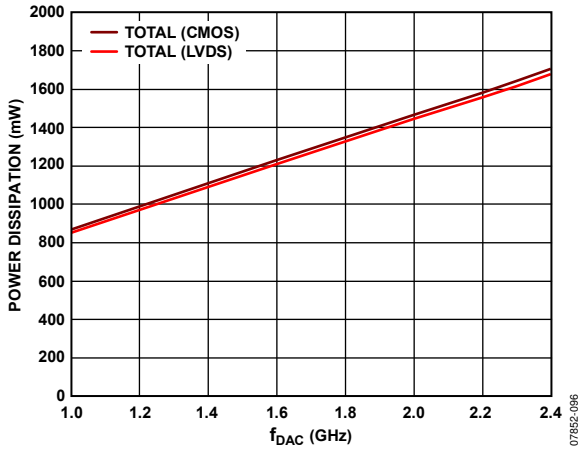


Figure 60. Total Power Dissipation vs. f_{DAC}, 4-Channel DOCSIS, f_{OUT} = 915 MHz, Full-Scale Current = 25 mA (Datapath Configuration: QAM Encoder On, SRRC Filter On, Four 2× Interpolation Filters On)

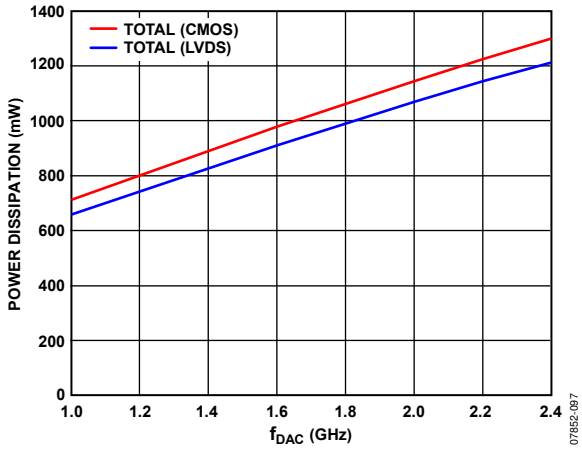


Figure 61. Total Power Dissipation vs. f_{DAC}, 16× Interpolation, One Channel Enabled, f_{OUT} = 70 MHz, Full-Scale Current = 20 mA

TERMINOLOGY

Monotonicity
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
Offset error is the deviation of the output current from the ideal of 0. For IOUTP, 0 mA output is expected when all inputs are set to 0. For IOUTN, 0 mA output is expected when all inputs are set to 1.

Gain Error
Gain error is the difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Temperature Drift

Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset, gain, and reference drift, the drift is reported in ppm per °C.

Power Supply Rejection (PSR)
PSR is the maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Output Compliance Range
The output compliance range is the range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in dB, between the peak amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Noise Spectral Density (NSD)
NSD is the converter noise power per unit of bandwidth. NSD is usually specified in dBm/Hz in the presence of a 0 dBm full-scale signal.

Adjacent Channel Leakage Ratio (ACLR)
The adjacent channel leakage (power) ratio is the ratio, in dBc, between the measured power within a channel relative to its adjacent channels.

Modulation Error Ratio (MER)
Modulated signals create a discrete set of output values referred to as a constellation. Each symbol creates an output signal corresponding to one point on the constellation. MER is a measure of the discrepancy between the average output symbol magnitude and the rms error magnitude of the individual symbol.

Intermodulation Distortion (IMD)
IMD is the result of two or more signals at different frequencies mixing together. Many products are created according to the formula $af_1 \pm bf_2$, where a and b are integer values.

SERIAL CONTROL PORT

The AD9789 serial control port is a flexible, synchronous serial communications port that allows an easy interface to many industry-standard microcontrollers and microprocessors. The AD9789 serial control port is compatible with most synchronous transfer formats, including both the Motorola SPI® and Intel® SSR protocols. The serial control port allows read/write access to all registers that configure the AD9789. Single- or multiple-byte transfers are supported, as well as MSB first or LSB first transfer formats. The AD9789 serial control port can be configured for a single bidirectional I/O pin (SDIO only) or for two unidirectional I/O pins (SDIO/SDO). By default, the AD9789 is in unidirectional long instruction mode (long instruction mode is the only instruction mode supported).

SERIAL CONTROL PORT PIN DESCRIPTIONS

The SCLK (serial clock) pin is the serial shift clock. This pin is an input. SCLK is used to synchronize serial control port reads and writes. Write data bits are registered on the rising edge of this clock, and read data bits are registered on the falling edge. This pin is internally pulled down by a 30 kΩ resistor to ground.

SDIO (serial data input/output) is a dual-purpose pin that acts as an input only (unidirectional mode) or as both an input and an output (bidirectional mode). The AD9789 defaults to the unidirectional I/O mode (Register 0x00[7] = 0).

The SDO (serial data output) pin is used only in the unidirectional I/O mode as a separate output pin for reading back data.

$\overline{CS}$ (chip select bar) is an active low control that gates the read and write cycles. When $\overline{CS}$ is high, SDO and SDIO are in a high impedance state. This pin is internally pulled up by a 30 kΩ resistor to DVDD33.

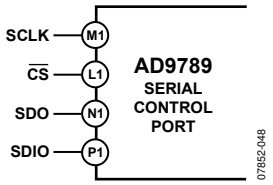


Figure 62. Serial Control Port

GENERAL OPERATION OF SERIAL CONTROL PORT

A write or read operation to the AD9789 is initiated by pulling $\overline{CS}$ low. $\overline{CS}$ stall high is supported in modes where three or fewer bytes of data (plus the instruction data) are transferred (see Table 7). In these modes, $\overline{CS}$ can temporarily return high on any byte boundary, allowing time for the system controller to process the next byte. $\overline{CS}$ can go high on byte boundaries only and can go high during either part (instruction or data) of the transfer.

During $\overline{CS}$ stall high mode, the serial control port state machine enters a wait state until all data is sent. If the system controller decides to abort the transfer before all of the data is sent, the state machine must be reset by either completing the remaining transfers or by returning $\overline{CS}$ low for at least one complete SCLK cycle (but less than eight SCLK cycles). Raising $\overline{CS}$ on a nonbyte boundary terminates the serial transfer and flushes the buffer.

In streaming mode (see Table 7), any number of data bytes can be transferred in a continuous stream. The register address is automatically incremented or decremented (see the MSB/LSB First Transfers section). $\overline{CS}$ must be raised at the end of the last byte to be transferred, thereby ending streaming mode.

Communication Cycle—Instruction Plus Data

There are two parts to a communication cycle with the AD9789. In the first part, a 16-bit instruction word is written to the AD9789, coincident with the first 16 SCLK rising edges. The instruction word provides the AD9789 serial control port with information regarding the data transfer, which is the second part of the communication cycle. The instruction word defines whether the upcoming data transfer is a read or a write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer.

Write

If the instruction word is for a write operation, the second part of the communication cycle is the transfer of data into the serial control port buffer of the AD9789. Data bits are registered on the rising edge of SCLK.

The length of the transfer (one, two, or three bytes or streaming mode) is indicated by two bits (N1 and N0) in the instruction byte. When the transfer is one, two, or three bytes (but not streaming mode), $\overline{CS}$ can be raised after each sequence of eight bits to stall the bus, except after the last byte, where it ends the cycle. When the bus is stalled, the serial transfer resumes when $\overline{CS}$ is lowered. Raising $\overline{CS}$ on a nonbyte boundary resets the serial control port. During a write, streaming mode does not skip reserved or blank registers; therefore, the user must know what bit pattern to write to the reserved registers to preserve proper operation of the part. It does not matter what data is written to blank registers.

Most writes to the control registers immediately reconfigure the device. However, Register 0x16 through Register 0x1D do not directly control device operation. They provide data to internal logic that must perform additional operations on the data before it is downloaded and the device configuration is changed. For any updates to Register 0x16 through Register 0x1D to take effect, the FREQNEW bit (Register 0x1E[7]) must be set to 1 (this bit is self-clearing). Any number of bytes of data can be changed before updating registers. Setting the FREQNEW bit simultaneously updates Register 0x16 through Register 0x1D.

In a similar fashion, any changes to Register 0x22 and Register 0x23 require PARMNEW (Register 0x24[7]) to be toggled from a low state to a high state before the new values take effect. Unlike the FREQNEW bit, PARMNEW is not self-clearing.

Read

If the instruction word is for a read operation, the next N × 8 SCLK cycles clock out the data from the address specified in the instruction word, where N is 1 to 3 as determined by Bits[N1:N0]. If N = 4, the read operation is in streaming mode, continuing until $\overline{CS}$ is raised. Streaming mode does not skip over reserved or blank registers. The readback data is valid on the falling edge of SCLK.

The default mode of the AD9789 serial control port is the unidirectional mode. In unidirectional mode, the readback data appears on the SDO pin. It is also possible to set the AD9789 to bidirectional mode using the SDIO_DIR bit (Register 0x00[7]). In bidirectional mode, both the sent data and the readback data appear on the SDIO pin.

A readback request reads the data that is in the serial control port buffer area or the data in the active registers (see Figure 63).

The AD9789 supports only the long instruction mode; therefore, Register 0x00[4:3] reads 11 (this register uses mirrored bits). Long instruction mode is the default at power-up or reset, and writing to these bits has no effect.

The AD9789 uses Register Address 0x00 to Register Address 0x55.

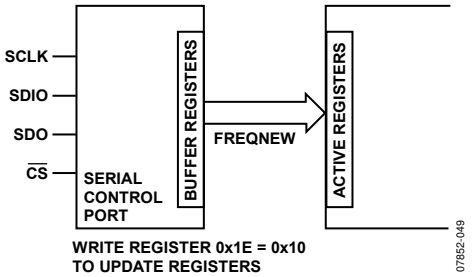


Figure 63. Relationship Between Serial Control Port Buffer Registers and Active Registers of the AD9789

INSTRUCTION WORD (16 BITS)

The MSB of the instruction word is R/$\overline{W}$, which indicates whether the instruction is a read or a write. The next two bits, N1 and N0, indicate the length of the transfer in bytes. The final 13 bits (Bits[A12:A0]) are the address at which to begin the read or write operation.

For a write, the instruction word is followed by the number of bytes of data indicated by Bits[N1:N0] (see Table 7).

Table 7. Byte Transfer Count

N1	N0	Bytes to Transfer
0	0	1
0	1	2
1	0	3
1	1	Streaming mode

Bits[A12:A0] select the address within the register map that is written to or read from during the data transfer portion of the communication cycle. Only Bits[A6:A0] are needed to cover the range of the 0x55 registers used by the AD9789. Bits[A12:A7] must always be 0. For multibyte transfers, this address is the starting byte address. In MSB first mode, subsequent bytes increment the address.

MSB/LSB FIRST TRANSFERS

The AD9789 instruction word and byte data can be MSB first or LSB first. Any data written to Register 0x00 must be mirrored, the upper four bits (Bits[7:4]) with the lower four bits (Bits [3:0]). This makes it irrelevant whether LSB first or MSB first is in effect. As an example of this mirroring, the default setting for Register 0x00[7:0] is 0x18, which mirrors Bit 4 and Bit 3. These bits set the long instruction mode (the default and the only mode supported). The default for the AD9789 is MSB first.

When LSB first is set by Register 0x00[1] and Register 0x00[6], it takes effect immediately. In multibyte transfers, subsequent bytes reflect any changes in the serial port configuration.

When MSB first mode is active, the instruction and data bytes must be written from MSB to LSB. Multibyte data transfers in MSB first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes must follow in order from the high address to the low address. In MSB first mode, the serial control port internal address generator decrements for each data byte of the multibyte transfer cycle.

When LSB first mode is active, the instruction and data bytes must be written from LSB to MSB. Multibyte data transfers in LSB first format start with an instruction byte that includes the register address of the least significant data byte followed by multiple data bytes. The internal byte address generator of the serial control port increments for each byte of the multibyte transfer cycle.

The AD9789 serial control port register address decrements from the register address just written toward 0x00 for multibyte I/O operations if the MSB first mode is active (default). If the LSB first mode is active, the register address of the serial control port increments from the address just written toward 0x55 for multibyte I/O operations.

Streaming mode always terminates when it reaches Address 0x2F. Note that unused addresses are not skipped during multibyte I/O operations.

Table 8. Streaming Mode (No Addresses Are Skipped)

Write Mode	Address Direction	Stop Sequence
LSB First	Increment	0x02D, 0x02E, 0x02F, stop
MSB First	Decrement	0x001, 0x000, 0x02F, stop