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CMOS 300 MSPS Quadrature Complete DDS

AD9854

FEATURES

- 300 MHz internal clock rate
- FSK, BPSK, PSK, chirp, AM operation
- Dual integrated 12-bit digital-to-analog converters (DACs)
- Ultrahigh speed comparator, 3 ps rms jitter
- Excellent dynamic performance
  - 80 dB SFDR at 100 MHz (±1 MHz) A_{OUT}
- 4× to 20× programmable reference clock multiplier
- Dual 48-bit programmable frequency registers
- Dual 14-bit programmable phase offset registers
- 12-bit programmable amplitude modulation and on/off output shaped keying function
- Single-pin FSK and BPSK data interfaces
- PSK capability via input/output interface
- Linear or nonlinear FM chirp functions with single-pin frequency hold function
- Frequency-ramped FSK
- <25 ps rms total jitter in clock generator mode
- Automatic bidirectional frequency sweeping
- Sin(x)/x correction
- Simplified control interfaces
  - 10 MHz serial 2- or 3-wire SPI compatible
  - 100 MHz parallel 8-bit programming
- 3.3 V single supply
- Multiple power-down functions
- Single-ended or differential input reference clock
- Small, 80-lead LQFP or TQFP with exposed pad

APPLICATIONS

- Agile, quadrature LO frequency synthesis
- Programmable clock generators
- FM chirp source for radar and scanning systems
- Test and measurement equipment
- Commercial and amateur RF exciters

FUNCTIONAL BLOCK DIAGRAM

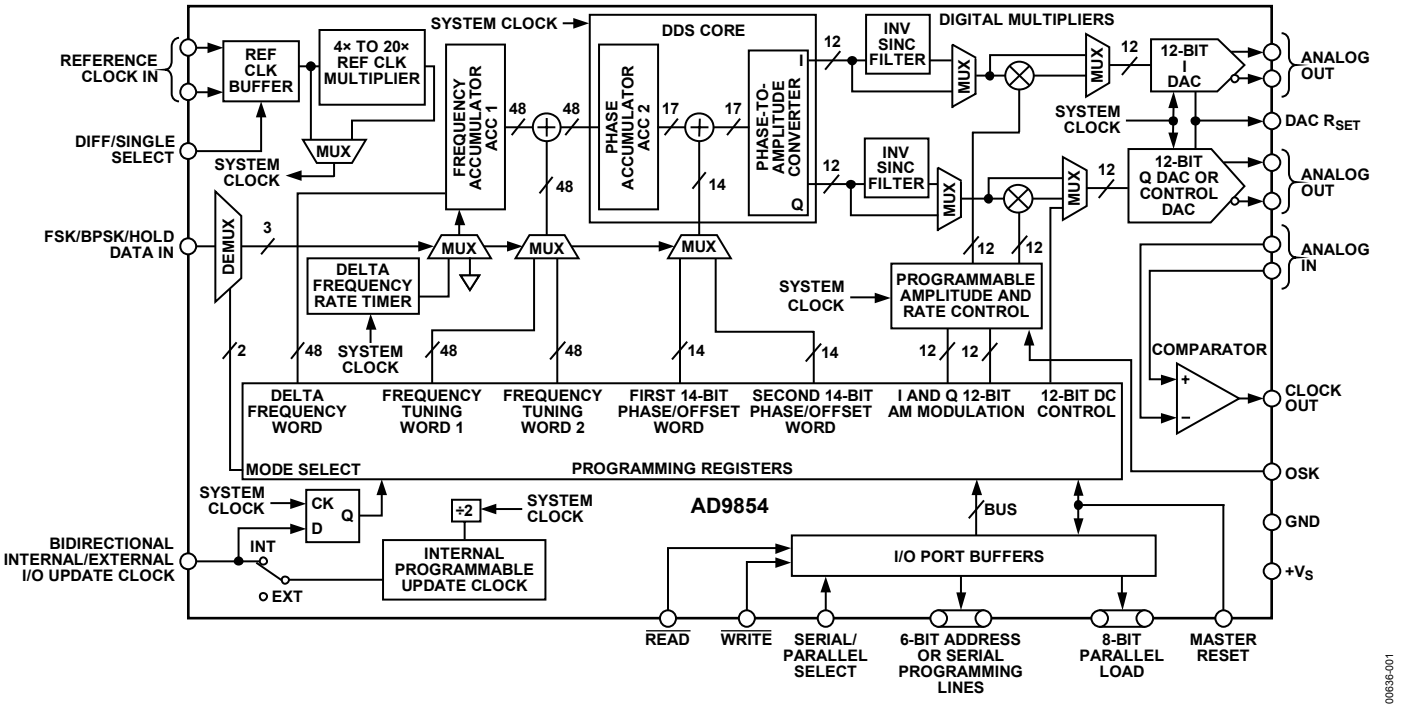

Figure 1.

Rev. E

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
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COMPARABLE PARTS

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EVALUATION KITS

- AD9854 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1389: Recommended Rework Procedure for the Lead Frame Chip Scale Package (LFCSP)
- AN-237: Choosing DACs for Direct Digital Synthesis
- AN-280: Mixed Signal Circuit Technologies
- AN-342: Analog Signal-Handling for High Speed and Accuracy
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-419: A Discrete, Low Phase Noise, 125 MHz Crystal Oscillator for the AD9850
- AN-423: Amplitude Modulation of the AD9850 Direct Digital Synthesizer
- AN-543: High Quality, All-Digital RF Frequency Modulation Generation with the ADSP-2181 and the AD9850 DDS
- AN-557: An Experimenter's Project:
- AN-587: Synchronizing Multiple AD9850/AD9851 DDS-Based Synthesizers
- AN-605: Synchronizing Multiple AD9852 DDS-Based Synthesizers
- AN-621: Programming the AD9832/AD9835
- AN-632: Provisionary Data Rates Using the AD9951 DDS as an Agile Reference Clock for the ADN2812 Continuous-Rate CDR
- AN-769: Generating Multiple Clock Outputs from the AD9540
- AN-772: A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)
- AN-823: Direct Digital Synthesizers in Clocking Applications Time
- AN-837: DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance
- AN-843: Measuring a Loudspeaker Impedance Profile Using the AD5933
- AN-847: Measuring a Grounded Impedance Profile Using the AD5933
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design
- AN-927: Determining if a Spur is Related to the DDS/DAC or to Some Other Source (For Example, Switching Supplies)

- AN-939: Super-Nyquist Operation of the AD9912 Yields a High RF Output Signal
- AN-953: Direct Digital Synthesis (DDS) with a Programmable Modulus

Data Sheet

- AD9854: CMOS 300 MSPS Quadrature Complete DDS Data Sheet

Product Highlight

- Introducing Digital Up/Down Converters: VersaCOMM™ Reconfigurable Digital Converters

Technical Books

- A Technical Tutorial on Digital Signal Synthesis, 1999

TOOLS AND SIMULATIONS

- ADIsimDDS (Direct Digital Synthesis)

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

Technical Articles

- 400-MSample DDSs Run On Only +1.8 VDC
- ADI Buys Korean Mobile TV Chip Maker
- Basics of Designing a Digital Radio Receiver (Radio 101)
- DDS Applications
- DDS Circuit Generates Precise PWM Waveforms
- DDS Design
- DDS Device Produces Sawtooth Waveform
- DDS Device Provides Amplitude Modulation
- DDS IC Initiates Synchronized Signals
- DDS IC Plus Frequency-To-Voltage Converter Make Low-Cost DAC
- DDS Simplifies Polar Modulation
- Digital Potentiometers Vary Amplitude In DDS Devices
- Digital Up/Down Converters: VersaCOMM™ White Paper
- Digital Waveform Generator Provides Flexible Frequency Tuning for Sensor Measurement
- Improved DDS Devices Enable Advanced Comm Systems
- Integrated DDS Chip Takes Steps To 2.7 GHz
- Simple Circuit Controls Stepper Motors
- Speedy A/Ds Demand Stable Clocks
- Synchronized Synthesizers Aid Multichannel Systems
- The Year of the Waveform Generator
- Two DDS ICs Implement Amplitude-shift Keying
- Video Portables and Cameras Get HDMI Outputs

DESIGN RESOURCES

- AD9854 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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GENERAL DESCRIPTION

The AD9854 digital synthesizer is a highly integrated device that uses advanced DDS technology, coupled with two internal high speed, high performance quadrature DACs to form a digitally programmable I and Q synthesizer function. When referenced to an accurate clock source, the AD9854 generates highly stable, frequency-phase, amplitude-programmable sine and cosine outputs that can be used as an agile LO in communications, radar, and many other applications. The innovative high speed DDS core of the AD9854 provides 48-bit frequency resolution (1 μHz tuning resolution with 300 MHz SYSCLK). Maintaining 17 bits ensures excellent SFDR.

The circuit architecture of the AD9854 allows the generation of simultaneous quadrature output signals at frequencies up to 150 MHz, which can be digitally tuned at a rate of up to 100 million new frequencies per second. The sine wave output (externally filtered) can be converted to a square wave by the internal comparator for agile clock generator applications. The device provides two 14-bit phase registers and a single pin for BPSK operation.

For higher-order PSK operation, the I/O interface can be used for phase changes. The 12-bit I and Q DACs, coupled with the innovative DDS architecture, provide excellent wideband and narrow-band output SFDR. The Q DAC can also be configured as a user-programmable control DAC if the quadrature function is not desired. When configured with the comparator, the 12-bit control DAC facilitates static duty cycle control in high speed clock generator applications.

Two 12-bit digital multipliers permit programmable amplitude modulation, on/off output shaped keying, and precise amplitude control of the quadrature output. Chirp functionality is also included to facilitate wide bandwidth frequency sweeping applications. The programmable 4× to 20× REFCLK multiplier circuit of the AD9854 internally generates the 300 MHz system clock from an external lower frequency reference clock. This saves the user the expense and difficulty of implementing a 300 MHz system clock source.

Direct 300 MHz clocking is also accommodated with either single-ended or differential inputs. Single-pin conventional FSK and the enhanced spectral qualities of ramped FSK are supported. The AD9854 uses advanced 0.35 μm CMOS technology to provide a high level of functionality on a single 3.3 V supply.

The AD9854 is pin-for-pin compatible with the AD9852 single-tone synthesizer. It is specified to operate over the extended industrial temperature range of −40°C to +85°C.

SPECIFICATIONS

V_S = 3.3 V ± 5%, R_{SET} = 3.9 kΩ, external reference clock frequency = 30 MHz with REFCLK multiplier enabled at 10× for AD9854ASVZ, external reference clock frequency = 20 MHz with REFCLK multiplier enabled at 10× for AD9854ASTZ, unless otherwise noted.

Table 1.

		Test	AD9854ASVZ			AD9854ASTZ			
Parameter	**Temp**	**Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
REFERENCE CLOCK INPUT CHARACTERISTICS[1]									
Internal System Clock Frequency Range									
REFCLK Multiplier Enabled	Full	VI	20		300	20		200	MHz
REFCLK Multiplier Disabled	Full	VI	DC		300	DC		200	MHz
External Reference Clock Frequency Range									
REFCLK Multiplier Enabled	Full	VI	5		75	5		50	MHz
REFCLK Multiplier Disabled	Full	VI	DC		300	DC		200	MHz
Duty Cycle	25°C	IV	45	50	55	45	50	55	%
Input Capacitance	25°C	IV		3			3		pF
Input Impedance	25°C	IV		100			100		kΩ
Differential Mode Common-Mode Voltage Range									
Minimum Signal Amplitude[2]	25°C	IV	400			400			mV p-p
Common-Mode Range	25°C	IV	1.6	1.75	1.9	1.6	1.75	1.9	V
V_{IH} (Single-Ended Mode)	25°C	IV	2.3			2.3			V
V_{IL} (Single-Ended Mode)	25°C	IV			1			1	V
DAC STATIC OUTPUT CHARACTERISTICS									
Output Update Speed	Full	I			300			200	MSPS
Resolution	25°C	IV		12			12		Bits
I and Q Full-Scale Output Current	25°C	IV	5	10	20	5	10	20	mA
I and Q DAC DC Gain Imbalance[3]	25°C	I	−0.5	+0.15	+0.5	−0.5	+0.15	+0.5	dB
Gain Error	25°C	I	−6		+2.25	−6		+2.25	% FS
Output Offset	25°C	I			2			2	µA
Differential Nonlinearity	25°C	I		0.3	1.25		0.3	1.25	LSB
Integral Nonlinearity	25°C	I		0.6	1.66		0.6	1.66	LSB
Output Impedance	25°C	IV		100			100		kΩ
Voltage Compliance Range	25°C	I	−0.5		+1.0	−0.5		+1.0	V
DAC DYNAMIC OUTPUT CHARACTERISTICS									
I and Q DAC Quadrature Phase Error	25°C	IV		0.2	1		0.2	1	Degrees
DAC Wideband SFDR									
1 MHz to 20 MHz A_{OUT}	25°C	V		58			58		dBc
20 MHz to 40 MHz A_{OUT}	25°C	V		56			56		dBc
40 MHz to 60 MHz A_{OUT}	25°C	V		52			52		dBc
60 MHz to 80 MHz A_{OUT}	25°C	V		48			48		dBc
80 MHz to 100 MHz A_{OUT}	25°C	V		48			48		dBc
100 MHz to 120 MHz A_{OUT}	25°C	V		48			48		dBc
DAC Narrow-Band SFDR									
10 MHz A_{OUT} (±1 MHz)	25°C	V		83			83		dBc
10 MHz A_{OUT} (±250 kHz)	25°C	V		83			83		dBc
10 MHz A_{OUT} (±50 kHz)	25°C	V		91			91		dBc
41 MHz A_{OUT} (±1 MHz)	25°C	V		82			82		dBc
41 MHz A_{OUT} (±250 kHz)	25°C	V		84			84		dBc
41 MHz A_{OUT} (±50 kHz)	25°C	V		89			89		dBc
119 MHz A_{OUT} (±1 MHz)	25°C	V		71			71		dBc
119 MHz A_{OUT} (±250 kHz)	25°C	V		77			77		dBc
119 MHz A_{OUT} (±50 kHz)	25°C	V		83			83		dBc

Parameter	Temp	Test Level	AD9854ASVZ Min	AD9854ASVZ Typ	AD9854ASVZ Max	AD9854ASTZ Min	AD9854ASTZ Typ	AD9854ASTZ Max	Unit
Residual Phase Noise									
(A_{OUT} = 5 MHz, External Clock = 30 MHz									
REFCLK Multiplier Engaged at 10×)									
1 kHz Offset	25°C	V		140			140		dBc/Hz
10 kHz Offset	25°C	V		138			138		dBc/Hz
100 kHz Offset	25°C	V		142			142		dBc/Hz
(A_{OUT} = 5 MHz, External Clock = 300 MHz,									
REFCLK Multiplier Bypassed)									
1 kHz Offset	25°C	V		142			142		dBc/Hz
10 kHz Offset	25°C	V		148			148		dBc/Hz
100 kHz Offset	25°C	V		152			152		dBc/Hz
PIPELINE DELAYS[4, 5, 6]									
DDS Core (Phase Accumulator and Phase-to-Amp Converter)	25°C	IV		33			33		SYSCLK cycles
Frequency Accumulator	25°C	IV		26			26		SYSCLK cycles
Inverse Sinc Filter	25°C	IV		16			16		SYSCLK cycles
Digital Multiplier	25°C	IV		9			9		SYSCLK cycles
DAC	25°C	IV		1			1		SYSCLK cycles
I/O Update Clock (Internal Mode)	25°C	IV		2			2		SYSCLK cycles
I/O Update Clock (External Mode)	25°C	IV		3			3		SYSCLK cycles
MASTER RESET DURATION	25°C	IV	10			10			SYSCLK cycles
COMPARATOR INPUT CHARACTERISTICS									
Input Capacitance	25°C	V		3			3		pF
Input Resistance	25°C	IV		500			500		kΩ
Input Current	25°C	I		±1	±5		±1	±5	µA
Hysteresis	25°C	IV		10	20		10	20	mV p-p
COMPARATOR OUTPUT CHARACTERISTICS									
Logic 1 Voltage, High-Z Load	Full	VI	3.1			3.1			V
Logic 0 Voltage, High-Z Load	Full	VI			0.16			0.16	V
Output Power, 50 Ω Load, 120 MHz Toggle Rate	25°C	I	9	11		9	11		dBm
Propagation Delay	25°C	IV		3			3		ns
Output Duty Cycle Error[7]	25°C	I	−10	±1	+10	−10	±1	+10	%
Rise/Fall Times, 5 pF Load	25°C	V		2			2		ns
Toggle Rate, High-Z Load	25°C	IV	300	350		300	350		MHz
Toggle Rate, 50 Ω Load	25°C	IV	375	400		375	400		MHz
Output Cycle-to-Cycle Jitter[8]		IV			4.0			4.0	ps rms
COMPARATOR NARROW-BAND SFDR[9]									
10 MHz (±1 MHz)	25°C	V		84			84		dBc
10 MHz (±250 MHz)	25°C	V		84			84		dBc
10 MHz (±50 MHz)	25°C	V		92			92		dBc
41 MHz (±1 MHz)	25°C	V		76			76		dBc
41 MHz (±250 MHz)	25°C	V		82			82		dBc
41 MHz (±50 MHz)	25°C	V		89			89		dBc
119 MHz (±1 MHz)	25°C	V		73					dBc
119 MHz (±250 MHz)	25°C	V		73					dBc
119 MHz (±50 MHz)	25°C	V		83					dBc
CLOCK GENERATOR OUTPUT JITTER[9]									
5 MHz A_{OUT}	25°C	V		23			23		ps rms
40 MHz A_{OUT}	25°C	V		12			12		ps rms
100 MHz A_{OUT}	25°C	V		7			7		ps rms

Parameter	Temp	Test Level	AD9854ASVZ Min	AD9854ASVZ Typ	AD9854ASVZ Max	AD9854ASTZ Min	AD9854ASTZ Typ	AD9854ASTZ Max	Unit
PARALLEL I/O TIMING CHARACTERISTICS									
t_{ASU} (Address Setup Time to $\overline{WR}$ Signal Active)	Full	IV	8.0	7.5		8.0	7.5		ns
t_{ADHW} (Address Hold Time to $\overline{WR}$ Signal Inactive)	Full	IV	0			0			ns
t_{DSU} (Data Setup Time to $\overline{WR}$ Signal Inactive)	Full	IV	3.0	1.6		3.0	1.6		ns
t_{DHD} (Data Hold Time to $\overline{WR}$ Signal Inactive)	Full	IV		0		0			ns
t_{WRLOW} ($\overline{WR}$ Signal Minimum Low Time)	Full	IV	2.5	1.8		2.5	1.8		ns
t_{WRHIGH} ($\overline{WR}$ Signal Minimum High Time)	Full	IV	7			7			ns
t_{WR} (Minimum $\overline{WR}$ Time)	Full	IV	10.5			10.5			ns
t_{ADV} (Address to Data Valid Time)	Full	V	15		15	15		15	ns
t_{ADHR} (Address Hold Time to $\overline{RD}$ Signal Inactive)	Full	IV	5			5			ns
t_{RDLOV} ($\overline{RD}$ Low to Output Valid)	Full	IV			15			15	ns
t_{RDHOZ} ($\overline{RD}$ High to Data Three-State)	Full	IV			10			10	ns
SERIAL I/O TIMING CHARACTERISTICS									
t_{PRE} ($\overline{CS}$ Setup Time)	Full	IV	30			30			ns
t_{SCLK} (Period of Serial Data Clock)	Full	IV	100			100			ns
t_{DSU} (Serial Data Setup Time)	Full	IV	30			30			ns
$t_{SCLKPWH}$ (Serial Data Clock Pulse Width High)	Full	IV	40			40			ns
$t_{SCLKPWL}$ (Serial Data Clock Pulse Width Low)	Full	IV	40			40			ns
t_{DHLD} (Serial Data Hold Time)	Full	IV	0			0			ns
t_{DV} (Data Valid Time)	Full	V		30			30		ns
CMOS LOGIC INPUTS[10]									
Logic 1 Voltage	25°C	I	2.2			2.2			V
Logic 0 Voltage	25°C	I			0.8			0.8	V
Logic 1 Current	25°C	IV			±5			±12	µA
Logic 0 Current	25°C	IV			±5			±12	µA
Input Capacitance	25°C	V		3			3		pF
POWER SUPPLY[11, 15]									
V_S Current[11, 12, 15]	25°C	I		1050	1210		755	865	mA
V_S Current[11, 13, 15]	25°C	I		710	816		515	585	mA
V_S Current[14]	25°C	I		600	685		435	495	mA
P_{DISS}[11, 12, 15]	25°C	I		3.475	4.190		2.490	3.000	W
P_{DISS}[11, 13, 15]	25°C	I		2.345	2.825		1.700	2.025	W
P_{DISS}[14]	25°C	I		1.975	2.375		1.435	1.715	W
P_{DISS} Power-Down Mode	25°C	I		1	50		1	50	mW

[1] The reference clock inputs are configured to accept a 1 V p-p (typical) dc offset square or sine wave centered at one-half the applied V_{DD} or a 3 V TTL-level pulse input.
[2] An internal 400 mV p-p differential voltage swing equates to 200 mV p-p applied to both REFCLK input pins.
[3] The I and Q gain imbalance is digitally adjustable to less than 0.01 dB.
[4] Pipeline delays of each individual block are fixed; however, if the first eight MSBs of a tuning word are 0s, the delay appears longer. This is due to insufficient phase accumulation per system clock period to produce enough LSB amplitude to the DAC.
[5] If a feature such as the inverse sinc, which has 16 pipeline delays, can be bypassed, the total delay is reduced by that amount.
[6] The I/O UD CLK transfers data from the I/O port buffers to the programming registers. This transfer is measured in system clocks.
[7] Change in duty cycle from 1 MHz to 100 MHz with 1 V p-p sine wave input and 0.5 V threshold.
[8] Represents the comparator's inherent cycle-to-cycle jitter contribution. The input signal is a 1 V, 40 MHz square wave, and the measurement device is a Wavecrest DTS-2075.
[9] Comparator input originates from the analog output section via the external 7-pole elliptic low-pass filter. Single-ended input, 0.5 V p-p. Comparator output terminated in 50 Ω.
[10] Avoid overdriving digital inputs. (Refer to the equivalent circuits in Figure 3.)
[11] If all device functions are enabled, it is not recommended to simultaneously operate the device at the maximum ambient temperature of 85°C and at the maximum internal clock frequency. This configuration may result in violating the maximum die junction temperature of 150°C. Refer to the Power Dissipation and Thermal Considerations section for derating and thermal management information.
[12] All functions engaged.
[13] All functions except inverse sinc engaged.
[14] All functions except inverse sinc and digital multipliers engaged.
[15] In most cases, disabling the inverse sinc filter reduces power consumption by approximately 30%.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Maximum Junction Temperature	150°C
V_S	4 V
Digital Inputs	−0.7 V to +V_S
Digital Output Current	5 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Maximum Clock Frequency (ASVZ)	300 MHz
Maximum Clock Frequency (ASTZ)	200 MHz

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

The heat sink of the AD9854ASVZ 80-lead TQFP package must be soldered to the PCB.

Table 3.

Thermal Characteristic	TQFP	LQFP
θ_{JA} (0 m/sec airflow)[1, 2, 3]	16.2°C/W	38°C/W
θ_{JMA} (1.0 m/sec airflow)[2, 3, 4, 5]	13.7°C/W	
θ_{JMA} (2.5 m/sec airflow)[2, 3, 4, 5]	12.8°C/W	
Ψ_{JT}[1, 2]	0.3°C/W	
θ_{JC}[6, 7]	2.0°C/W	

[1] Per JEDEC JESD51-2 (heat sink soldered to PCB).
[2] 2S2P JEDEC test board.
[3] Values of θ_{JA} are provided for package comparison and PCB design considerations.
[4] Per JEDEC JESD51-6 (heat sink soldered to PCB).
[5] Airflow increases heat dissipation, effectively reducing θ_{JA}. Furthermore, the more metal that is directly in contact with the package leads from metal traces through holes, ground, and power planes, the more θ_{JA} is reduced.
[6] Per MIL-Std 883, Method 1012.1.
[7] Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

To determine the junction temperature on the application PCB use the following equation:

$$T_J = T_{case} + (\Psi_{JT} \times PD)$$

where:
T_J is the junction temperature expressed in degrees Celsius.
T_{case} is the case temperature expressed in degrees Celsius, as measured by the user at the top center of the package.
Ψ_{JT} = 0.3°C/W.
PD is the power dissipation (PD); see the Power Dissipation and Thermal Considerations section for the method to calculate PD.

EXPLANATION OF TEST LEVELS

Table 3.

Test Level	Description
I	100% production tested.
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
VI	Devices are 100% production tested at 25°C and guaranteed by design and characterization testing for industrial operating temperature range.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

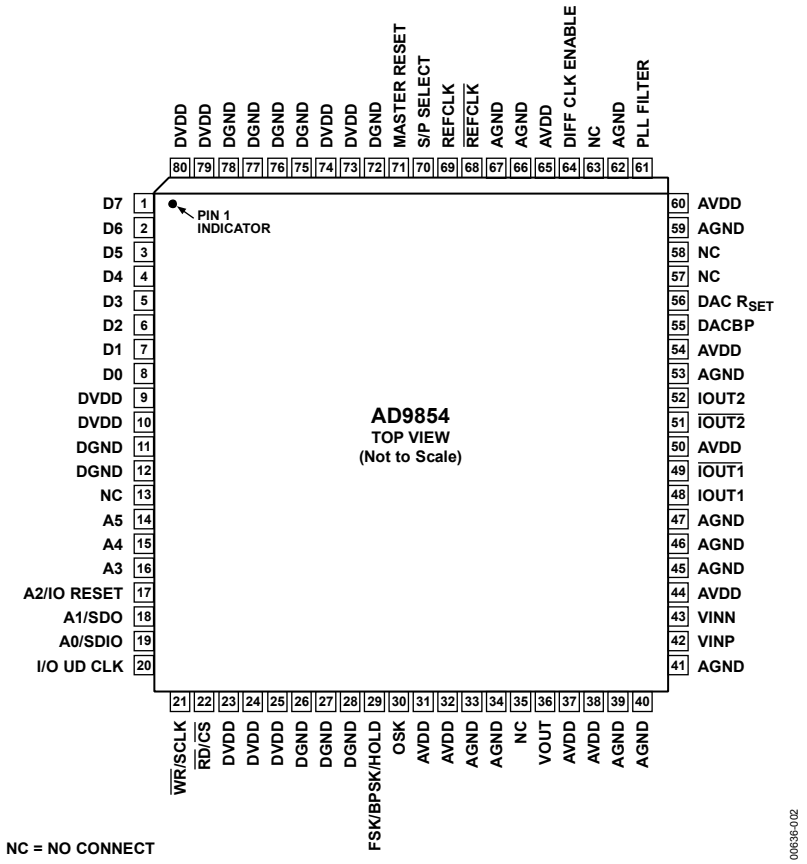

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 8	D7 to D0	8-Bit Bidirectional Parallel Programming Data Inputs. Used only in parallel programming mode.
9, 10, 23, 24, 25, 73, 74, 79, 80	DVDD	Connections for the Digital Circuitry Supply Voltage. Nominally 3.3 V more positive than AGND and DGND.
11, 12, 26, 27, 28, 72, 75 to 78	DGND	Connections for the Digital Circuitry Ground Return. Same potential as AGND.
13, 35, 57, 58, 63	NC	No Internal Connection.
14 to 16	A5 to A3	Parallel Address Inputs for Program Registers (Part of 6-Bit Parallel Address Inputs for Program Register, A5:A0). Used only in parallel programming mode.
17	A2/IO RESET	Parallel Address Input for Program Registers (Part of 6-Bit Parallel Address Inputs for Program Register, A5:A0)/IO Reset. A2 is used only in parallel programming mode. IO RESET is used when the serial programming mode is selected, allowing an IO RESET of the serial communication bus that is unresponsive due to improper programming protocol. Resetting the serial bus in this manner does not affect previous programming, nor does it invoke the default programming values listed in Table 8. Active high.
18	A1/SDO	Parallel Address Input for Program Registers (Part of 6-Bit Parallel Address Inputs for Program Register, A5:A0)/Unidirectional Serial Data Output. A1 is used only in parallel programming mode. SDO is used in 3-wire serial communication mode when the serial programming mode is selected.
19	A0/SDIO	Parallel Address Input for Program Registers (Part of 6-Bit Parallel Address Inputs for Program Register, A5:A0)/Bidirectional Serial Data I/O. A0 is used only in parallel programming mode. SDIO is used in 2-wire serial communication mode.

Pin No.	Mnemonic	Description
20	I/O UD CLK	Bidirectional I/O Update Clock. Direction is selected in control register. If this pin is selected as an input, a rising edge transfers the contents of the I/O port buffers to the programming registers. If I/O UD CLK is selected as an output (default), an output pulse (low to high) with a duration of eight system clock cycles indicates that an internal frequency update has occurred.
21	$\overline{WR}$/SCLK	Write Parallel Data to I/O Port Buffers. Shared function with SCLK. Serial clock signal associated with the serial programming bus. Data is registered on the rising edge. This pin is shared with $\overline{WR}$ when the parallel mode is selected. The mode is dependent on Pin 70 (S/P SELECT).
22	$\overline{RD}$/$\overline{CS}$	Read Parallel Data from Programming Registers. Shared function with $\overline{CS}$. Chip-select signal associated with the serial programming bus. Active low. This pin is shared with $\overline{RD}$ when the parallel mode is selected.
29	FSK/BPSK/HOLD	Multifunction pin according to the mode of operation selected in the programming control register. In FSK mode, logic low selects F1 and logic high selects F2. In BPSK mode, logic low selects Phase 1 and logic high selects Phase 2. In chirp mode, logic high engages the hold function, causing the frequency accumulator to halt at its current location. To resume or commence chirp mode, logic low is asserted.
30	OSK	Output Shaped Keying. Must first be selected in the programming control register to function. A logic high causes the I and Q DAC outputs to ramp up from zero-scale to full-scale amplitude at a preprogrammed rate. Logic low causes the full-scale output to ramp down to zero scale at the preprogrammed rate.
31, 32, 37, 38, 44, 50, 54, 60, 65	AVDD	Connections for the Analog Circuitry Supply Voltage. Nominally 3.3 V more positive than AGND and DGND.
33, 34, 39, 40, 41, 45, 46, 47, 53, 59, 62, 66, 67	AGND	Connections for Analog Circuitry Ground Return. Same potential as DGND.
36	VOUT	Noninverted Output of the Internal High Speed Comparator. Designed to drive 10 dBm to 50 Ω load as well as standard CMOS logic levels.
42	VINP	Voltage Input Positive. The noninverting input of the internal high speed comparator.
43	VINN	Voltage Input Negative. The inverting input of the internal high speed comparator.
48	IOUT1	Unipolar Current Output of I, or the Cosine DAC. (Refer to Figure 3.)
49	$\overline{IOUT1}$	Complementary Unipolar Current Output of I, or the Cosine DAC.
51	$\overline{IOUT2}$	Complementary Unipolar Current Output of Q, or the Sine DAC.
52	IOUT2	Unipolar Current Output of Q, or the Sine DAC. This DAC can be programmed to accept external 12-bit data in lieu of internal sine data, allowing the AD9854 to emulate the AD9852 control DAC function.
55	DACBP	Common Bypass Capacitor Connection for Both I and Q DACs. A 0.01 µF chip capacitor from this pin to AVDD improves harmonic distortion and SFDR slightly. No connect is permissible, but results in a slight degradation in SFDR.
56	DAC R_{SET}	Common Connection for Both I and Q DACs. Used to set the full-scale output current. $R_{SET} = 39.9/I_{OUT}$. Normal R_{SET} range is from 8 kΩ (5 mA) to 2 kΩ (20 mA).
61	PLL FILTER	Connection for the External Zero-Compensation Network of the REFCLK Multiplier's PLL Loop Filter. The zero-compensation network consists of a 1.3 kΩ resistor in series with a 0.01 µF capacitor. The other side of the network should be connected to AVDD as close as possible to Pin 60. For optimum phase noise performance, the REFCLK multiplier can be bypassed by setting the bypass PLL bit in Control Register 1E hex.
64	DIFF CLK ENABLE	Differential REFCLK Enable. A high level of this pin enables the differential clock inputs, REFCLK and $\overline{REFCLK}$ (Pin 69 and Pin 68, respectively).
68	$\overline{REFCLK}$	Complementary (180° Out of Phase) Differential Clock Signal. User should tie this pin high or low when single-ended clock mode is selected. Same signal levels as REFCLK.
69	REFCLK	Single-Ended Reference Clock Input (CMOS Logic Levels Required) or One of Two Differential Clock Signals. In differential reference clock mode, both inputs can be CMOS logic levels or have greater than 400 mV p-p square or sine waves centered about 1.6 V dc.
70	S/P SELECT	Selects serial programming mode (logic low) or parallel programming mode (logic high).
71	MASTER RESET	Initializes the serial/parallel programming bus to prepare for user programming; sets programming registers to a do-nothing state defined by the default values listed in Table 8. Active on logic high. Asserting this pin is essential for proper operation upon power-up.

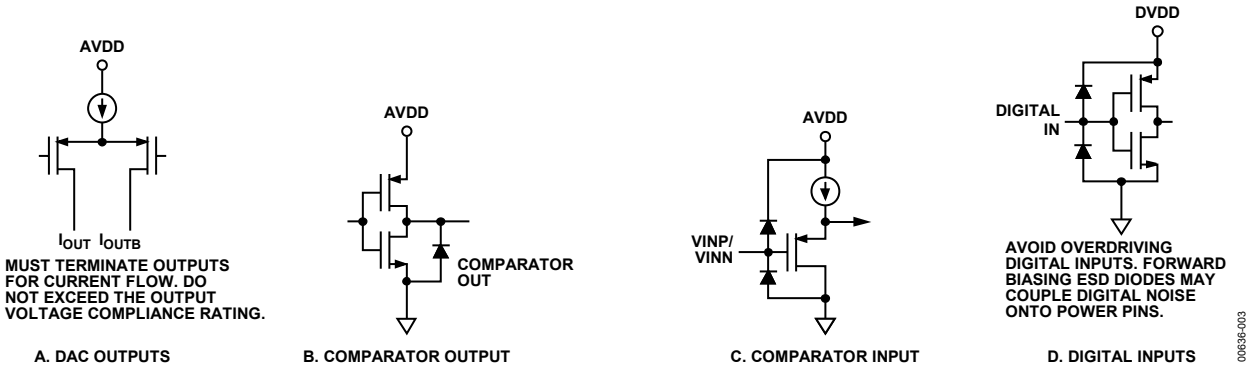

Figure 3. Equivalent Input and Output Circuits

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 4 to Figure 9 indicate the wideband harmonic distortion performance of the AD9854 from 19.1 MHz to 119.1 MHz fundamental output, reference clock = 30 MHz, REFCLK multiplier = 10×. Each graph is plotted from 0 MHz to 150 MHz (Nyquist).

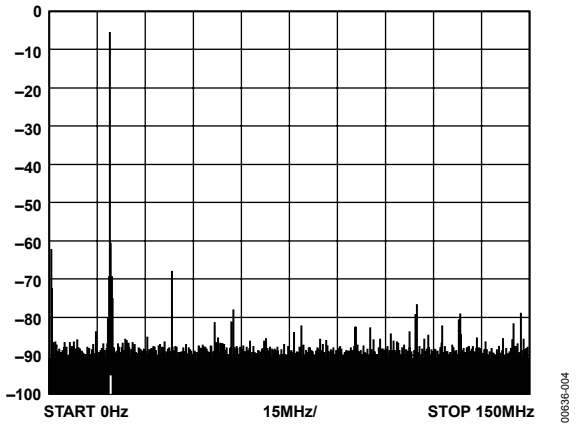

Figure 4. Wideband SFDR, 19.1 MHz

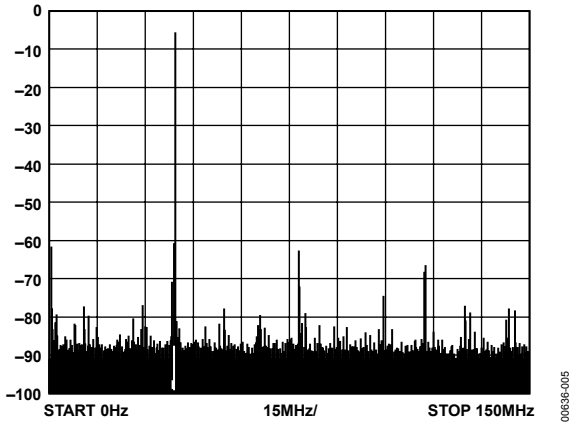

Figure 5. Wideband SFDR, 39.1 MHz

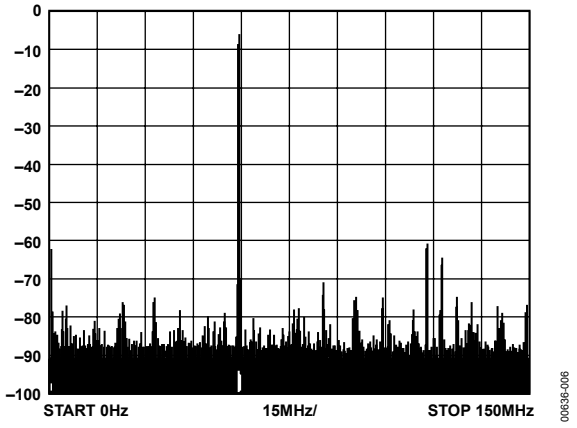

Figure 6. Wideband SFDR, 59.1 MHz

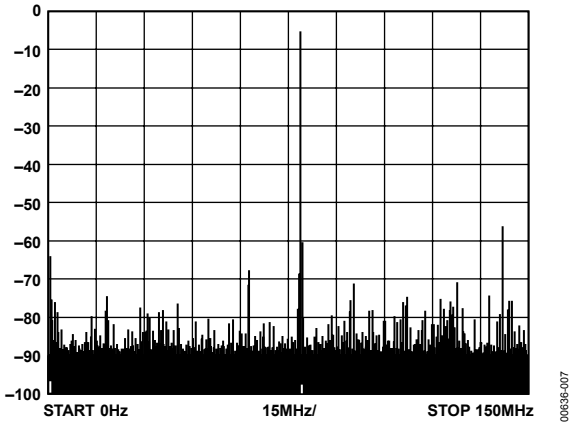

Figure 7. Wideband SFDR, 79.1 MHz

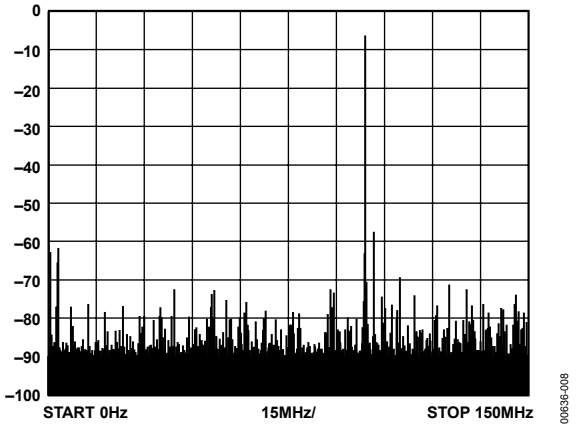

Figure 8. Wideband SFDR, 99.1 MHz

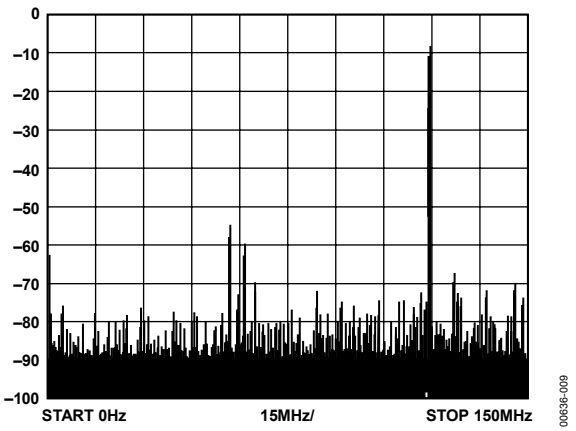

Figure 9. Wideband SFDR, 119.1 MHz

Figure 10 to Figure 15 show the trade-off in elevated noise floor, increased phase noise (PN), and discrete spurious energy when the internal REFCLK multiplier circuit is engaged. Plots with wide (1 MHz) and narrow (50 kHz) spans are shown. Compare the noise floor of Figure 11 and Figure 12 with that of Figure 14 and Figure 15. The improvement seen in Figure 11 and Figure 12 is a direct result of sampling the fundamental at a higher rate. Sampling at a higher rate spreads the quantization noise of the DAC over a wider bandwidth, which effectively lowers the noise floor.

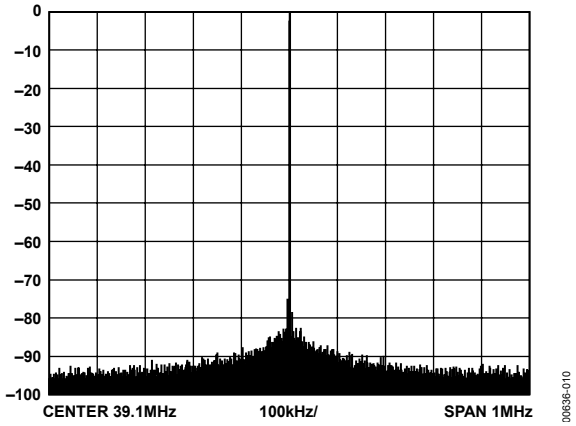

Figure 10. Narrow-Band SFDR, 39.1 MHz, 1 MHz BW, 300 MHz REFCLK with REFCLK Multiplier Bypassed

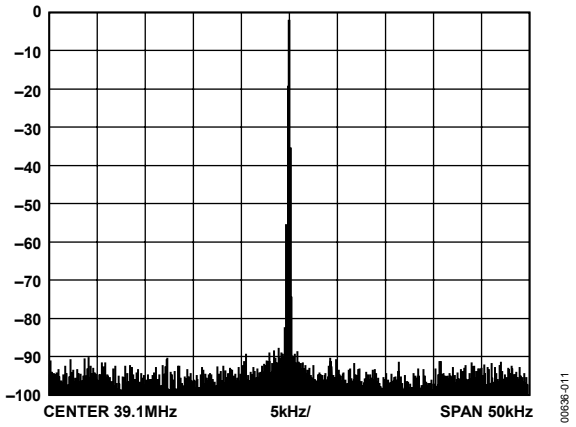

Figure 11. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 300 MHz REFCLK with REFCLK Multiplier Bypassed

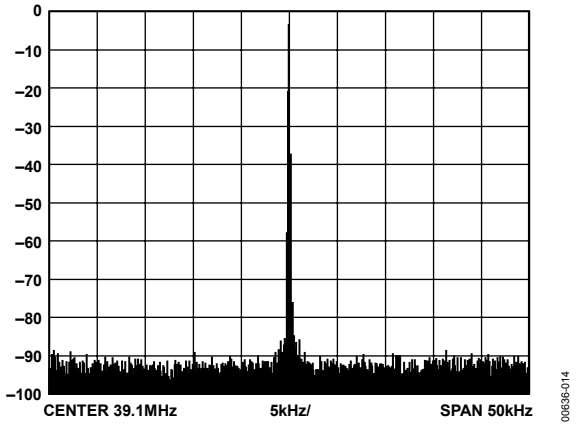

Figure 12. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 100 MHz REFCLK with REFCLK Multiplier Bypassed

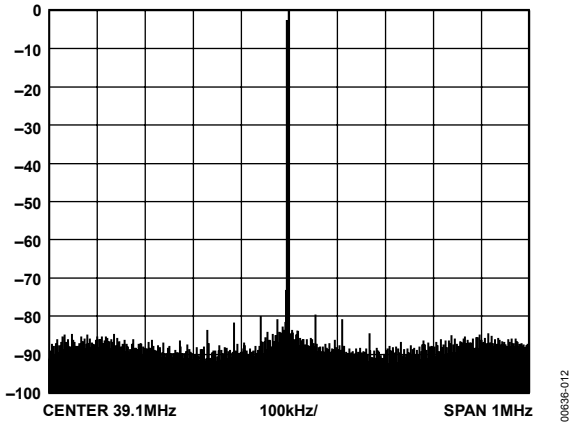

Figure 13. Narrow-Band SFDR, 39.1 MHz, 1 MHz BW, 30 MHz REFCLK with REFCLK Multiplier = 10×

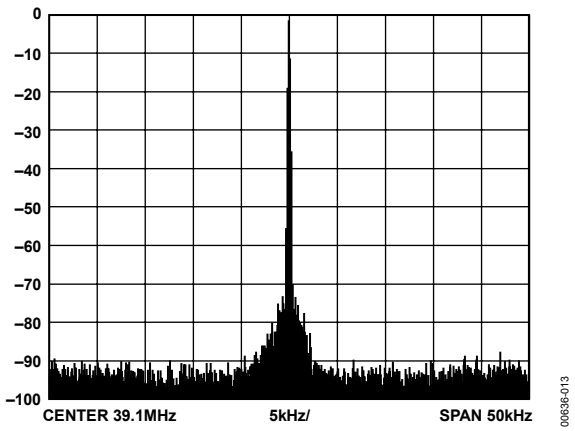

Figure 14. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 30 MHz REFCLK with REFCLK Multiplier = 10×

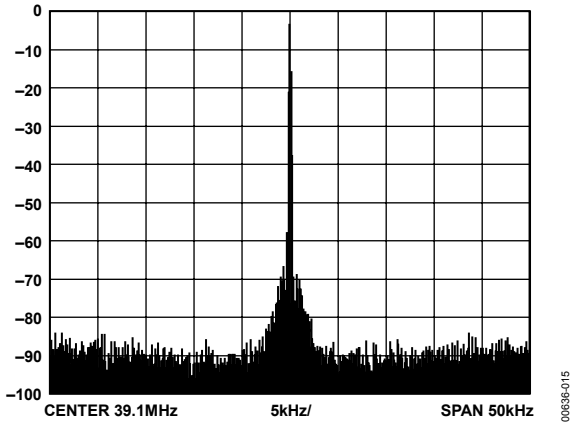

Figure 15. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 10 MHz REFCLK with REFCLK Multiplier = 10×

Figure 16 and Figure 17 show the narrow-band performance of the AD9854 when operating with a 200 MHz reference clock with the REFCLK multiplier bypassed vs. a 20 MHz reference clock and the REFCLK multiplier enabled at 10×.

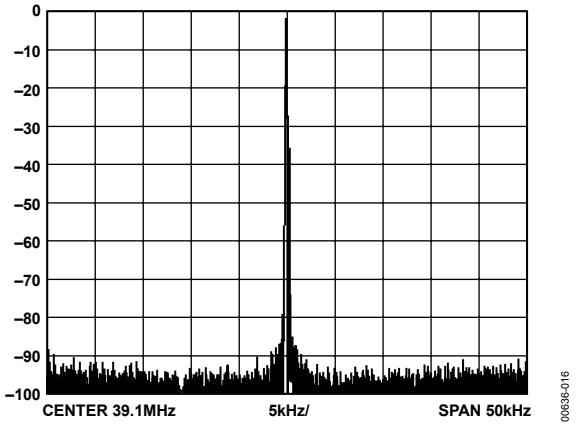

Figure 16. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 200 MHz REFCLK with REFCLK Multiplier Bypassed

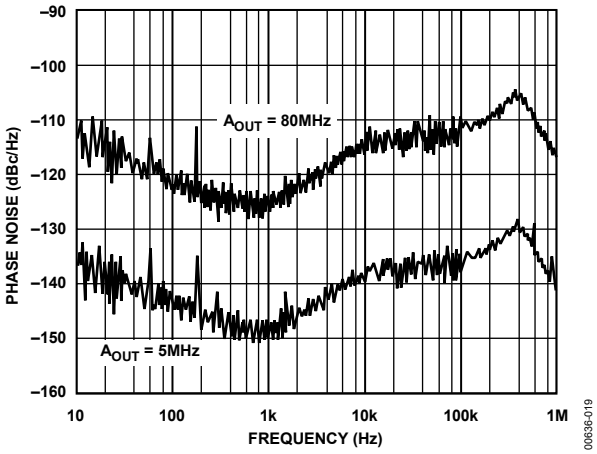

Figure 19. Residual Phase Noise, 30 MHz REFCLK with REFCLK Multiplier = 10×

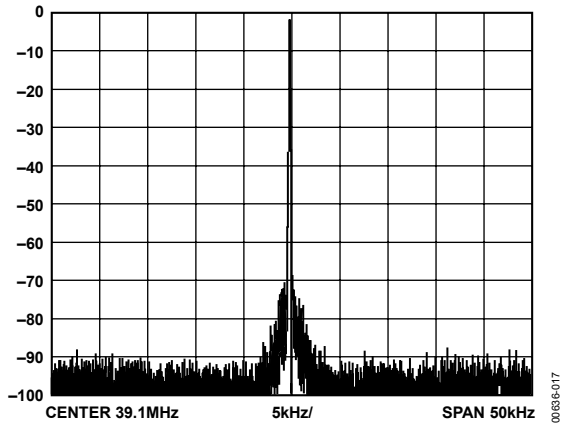

Figure 17. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 20 MHz REFCLK with REFCLK Multiplier = 10×

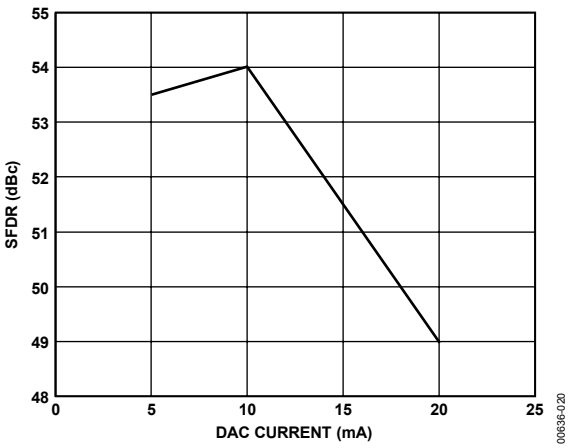

Figure 20. SFDR vs. DAC Current, 59.1 A_{OUT}, 300 MHz REFCLK with REFCLK Multiplier Bypassed

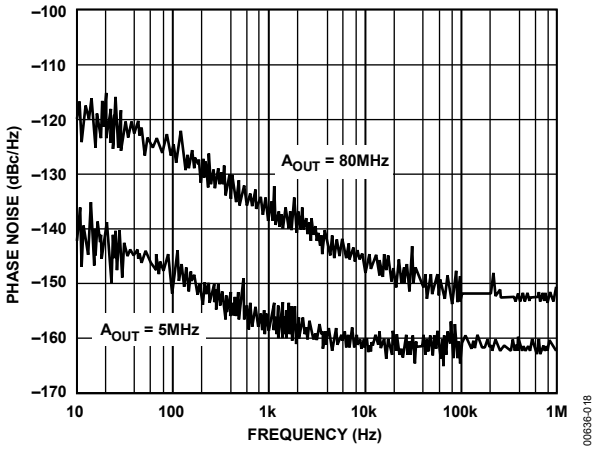

Figure 18. Residual Phase Noise, 300 MHz REFCLK with REFCLK Multiplier Bypassed

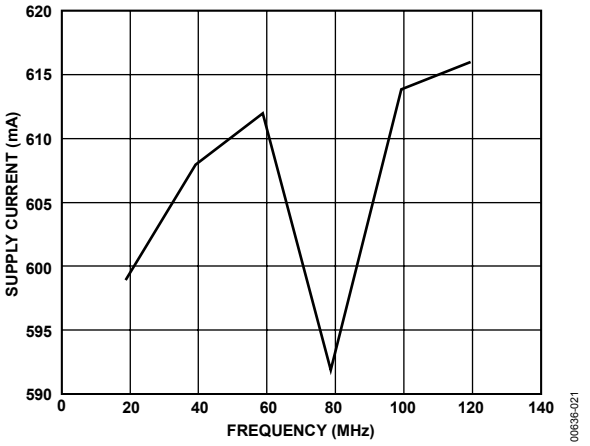

Figure 21. Supply Current vs. Output Frequency (Variation Is Minimal, Expressed as a Percentage, and Heavily Dependent on Tuning Word)

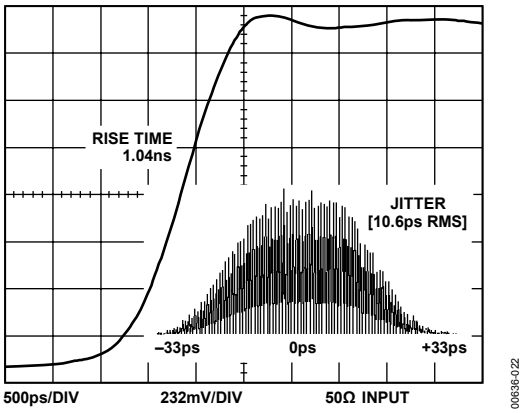

Figure 22. Typical Comparator Output Jitter, 40 MHz A_{OUT}, 300 MHz RFCLK with REFCLK Multiplier Bypassed

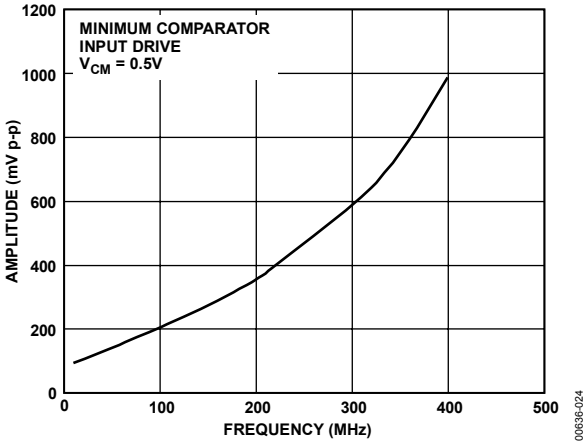

Figure 24. Comparator Toggle Voltage Requirement

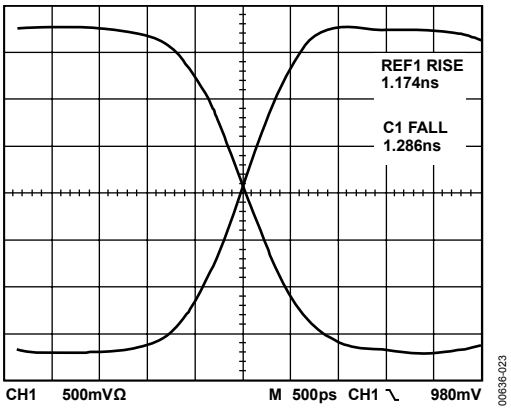

Figure 23. Comparator Rise/Fall Times

TYPICAL APPLICATIONS

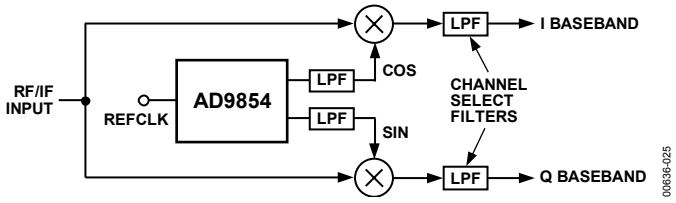

Figure 25. Quadrature Downconversion

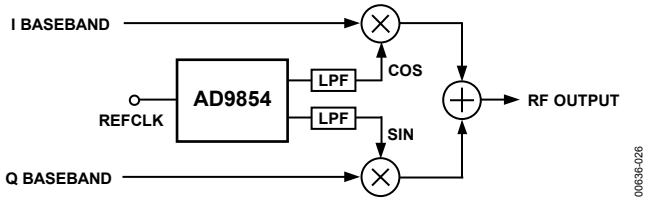

Figure 26. Direct Conversion Quadrature Upconverter

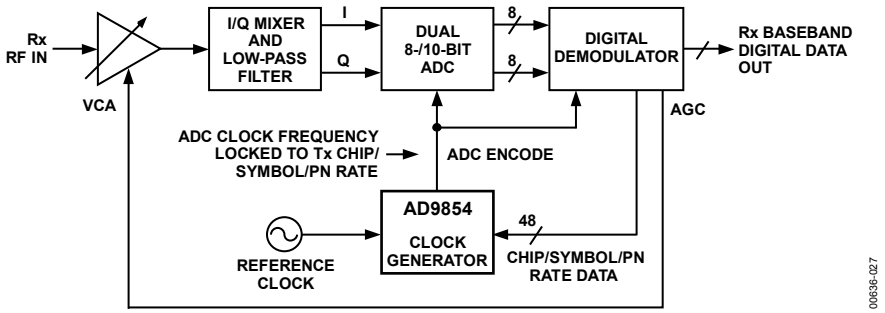

Figure 27. Chip Rate Generator in Spread Spectrum Application

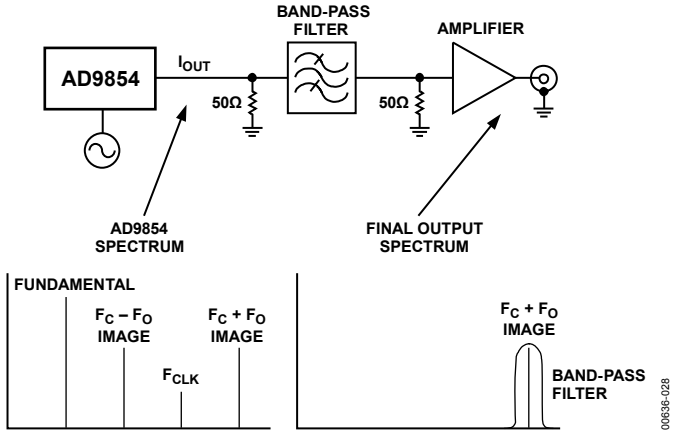

Figure 28. Using an Aliased Image to Generate a High Frequency

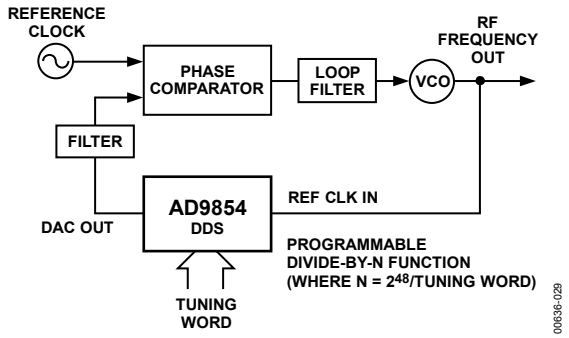

Figure 29. Programmable Fractional Divide-by-N Synthesizer

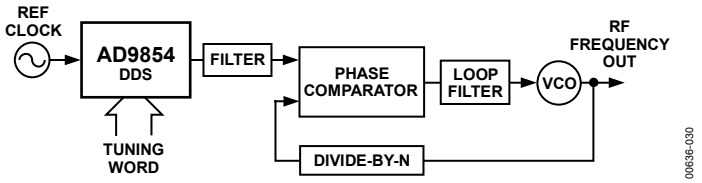

Figure 30. Agile High Frequency Synthesizer

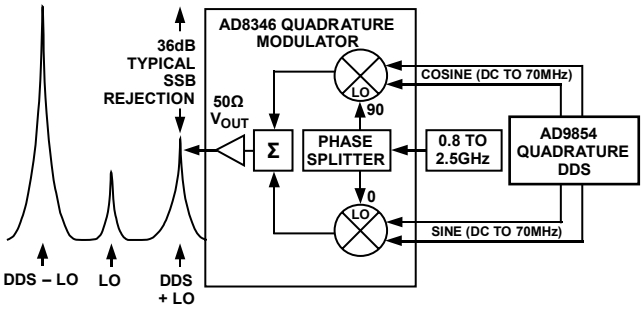

Figure 31. Single Sideband Upconversion

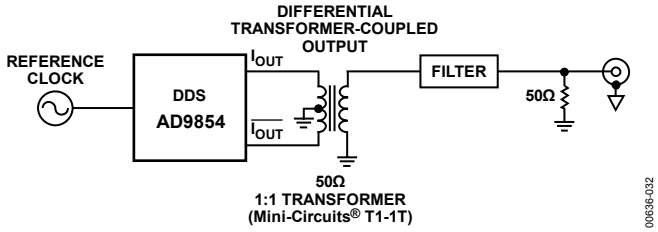

Figure 32. Differential Output Connection for Reduction of Common-Mode Signals

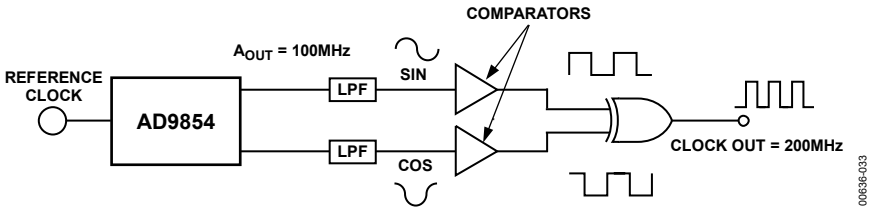

Figure 33. Clock Frequency Doubler

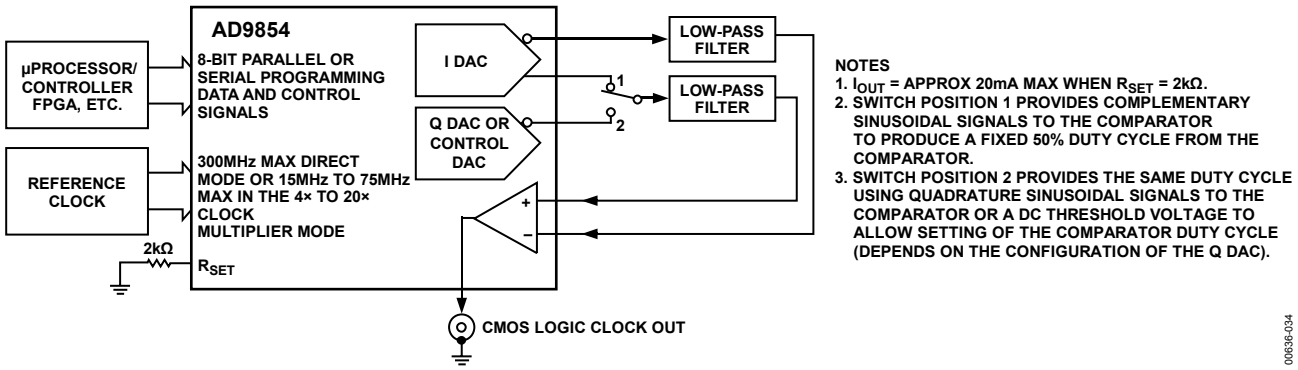

Figure 34. Frequency Agile Clock Generator Applications for the AD9854

THEORY OF OPERATION

The AD9854 quadrature output digital synthesizer is a highly flexible device that addresses a wide range of applications. The device consists of an NCO with a 48-bit phase accumulator, a programmable reference clock multiplier, inverse sinc filters, digital multipliers, two 12-bit/300 MHz DACs, a high speed analog comparator, and interface logic. This highly integrated device can be configured to serve as a synthesized LO, an agile clock generator, or an FSK/BPSK modulator.

Analog Devices, Inc., provides a technical tutorial about the operational theory of the functional blocks of the device. The tutorial includes a technical description of the signal flow through a DDS device and provides basic applications information for a variety of digital synthesis implementations. The document, *A Technical Tutorial on Digital Signal Synthesis,* is available from the DDS Technical Library, on the Analog Devices DDS website at www.analog.com/dds.

MODES OF OPERATION

The AD9854 has five programmable operational modes. To select a mode, three bits in the control register (parallel Address 1F hex) must be programmed, as described in Table 5.

Table 5. Mode Selection Table

Mode 2	Mode 1	Mode 0	Result
0	0	0	Single tone
0	0	1	FSK
0	1	0	Ramped FSK
0	1	1	Chirp
1	0	0	BPSK

In each mode, some functions may be prohibited. Table 6 lists the functions and their availability for each mode.

Single Tone (Mode 000)

This is the default mode when the MASTER RESET pin is asserted. It can also be accessed if the user programs this mode into the control register. The phase accumulator, responsible for generating an output frequency, is presented with a 48-bit value from the Frequency Tuning Word 1 registers that have default values of 0. Default values from the remaining applicable registers further define the single-tone output signal qualities.

The default values after a master reset configure the device with an output signal of 0 Hz and zero phase. At power-up and reset, the output from the I and Q DACs is a dc value equal to the midscale output current. This is the default mode amplitude setting of 0. See the On/Off Output Shaped Keying (OSK) section for more details about the output amplitude control. All or some of the 28 program registers must be programmed to produce a user-defined output signal.

Figure 35 shows the transition from the default condition (0 Hz) to a user-defined output frequency (F1).

Table 6. Functions Available for Modes

	Mode				
Function	**Single Tone**	**FSK**	**Ramped FSK**	**Chirp**	**BPSK**
Phase Adjust 1	●	●	●	●	●
Phase Adjust 2					●
Single-Pin FSK/BPSK or HOLD		●	●	●	●
Single-Pin Shaped Keying	●	●	●	●	●
Phase Offset or Modulation	●	●	●	●	
Amplitude Control or Modulation	●	●	●	●	●
Inverse Sinc Filter	●	●	●	●	●
Frequency Tuning Word 1	●	●	●	●	●
Frequency Tuning Word 2		●	●		
Automatic Frequency Sweep			●	●	

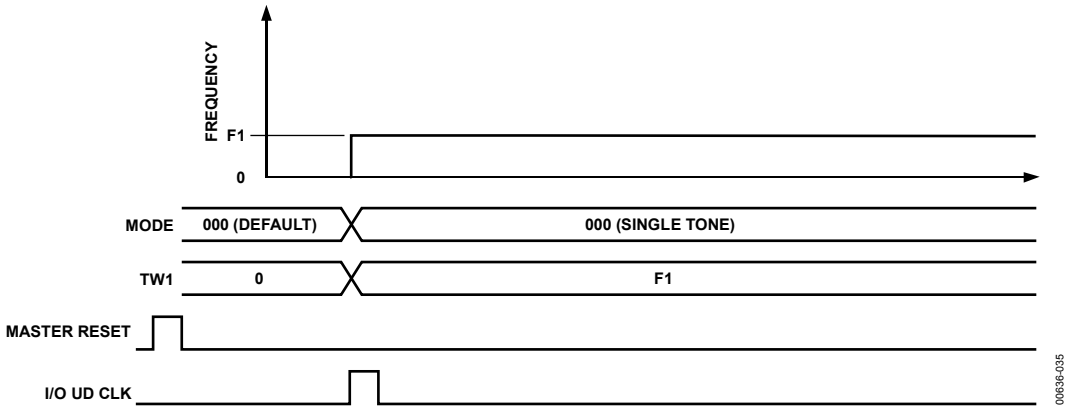

Figure 35. Default State to User-Defined Output Transition

As with all Analog Devices DDS devices, the value of the frequency tuning word is determined by

$$FTW = (Desired\ Output\ Frequency \times 2^N)/SYSCLK$$

where:
N is the phase accumulator resolution (48 bits in this instance).
Desired Output Frequency is expressed in hertz.
FTW (frequency tuning word) is a decimal number.

After a decimal number has been calculated, it must be rounded to an integer and then converted to binary format, that is, a series of 48 binary-weighted 1s and 0s. The fundamental sine wave DAC output frequency range is from dc to one-half SYSCLK.

Changes in frequency are phase continuous, meaning that the first sampled phase value of the new frequency is referenced from the time of the last sampled phase value of the previous frequency.

The I and Q DACs of the AD9854 are always 90° out of phase. The 14-bit phase registers do not independently adjust the phase of each DAC output. Instead, both DACs are affected equally by a change in phase offset.

The single-tone mode allows the user to control the following signal qualities:

- Output frequency to 48-bit accuracy
- Output amplitude to 12-bit accuracy
  - Fixed, user-defined amplitude control
  - Variable, programmable amplitude control
  - Automatic, programmable, single-pin-controlled on/off output shaped keying
- Output phase to 14-bit accuracy

These qualities can be changed or modulated via the 8-bit parallel programming port at a 100 MHz parallel byte rate or at a 10 MHz serial rate. Incorporating this attribute permits FM, AM, PM, FSK, PSK, and ASK operation in single-tone mode.

Unramped FSK (Mode 001)

When the unramped FSK mode is selected, the output frequency of the DDS is a function of the values loaded into Frequency Tuning Word Register 1 and Frequency Tuning Word Register 2 and the logic level of Pin 29 (FSK/BPSK/HOLD). A logic low on Pin 29 chooses F1 (Frequency Tuning Word 1, Parallel Address 4 hex to Parallel Address 9 hex), and a logic high chooses F2 (Frequency Tuning Word 2, Parallel Register Address A hex to Parallel Register Address F hex). Changes in frequency are phase continuous and are internally coincident with the FSK data pin (Pin 29); however, there is deterministic pipeline delay between the FSK data signal and the DAC output. (Refer to the pipeline delays in Table 1.)

The unramped FSK mode, shown in Figure 36, represents traditional FSK, radio teletype (RTTY), or teletype (TTY) transmission of digital data. FSK is a very reliable means of digital communication; however, it makes inefficient use of the bandwidth in the RF spectrum. Ramped FSK, shown in Figure 37, is a method of conserving bandwidth.

Ramped FSK (Mode 010)

This mode is a method of FSK whereby changes from F1 to F2 are not instantaneous, but are accomplished in a frequency sweep or ramped fashion (the ramped notation implies that the sweep is linear). Although linear sweeping, or frequency ramping, is easily and automatically accomplished, it is only one of many schemes. Other frequency transition schemes can be implemented by changing the ramp rate and ramp step size on the fly in a piecewise fashion.

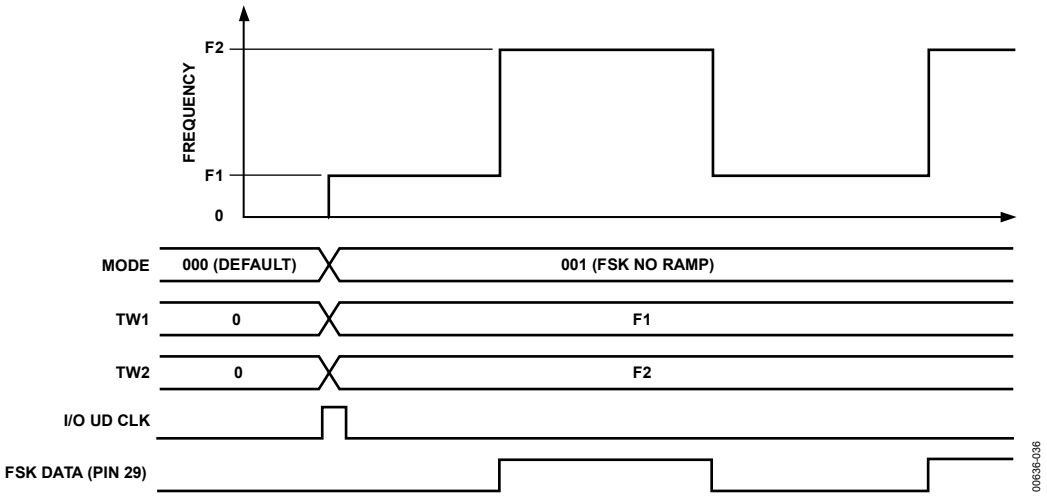

Figure 36. Unramped (Traditional) FSK Mode

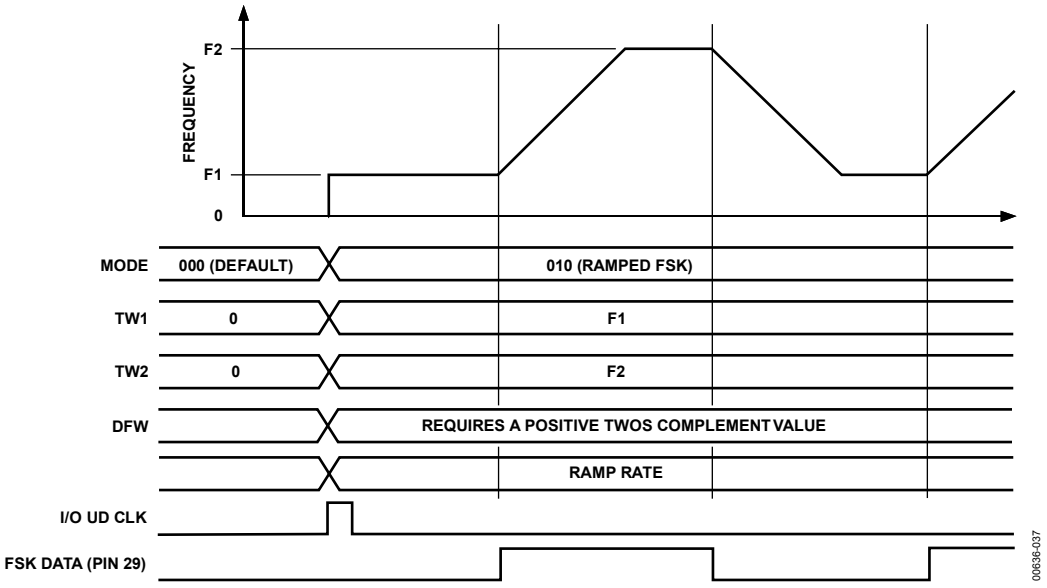

Figure 37. Ramped FSK Mode (Start at F1)

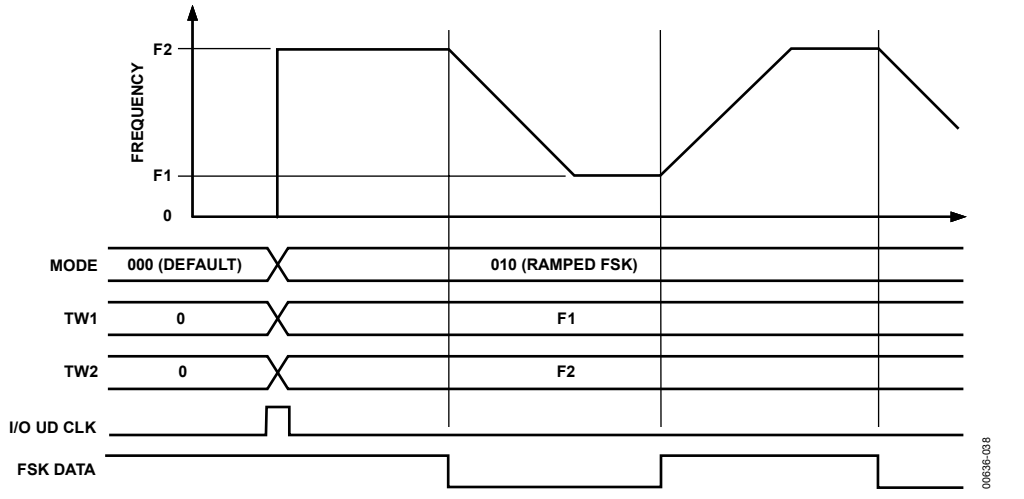

Figure 38. Ramped FSK Mode (Start at F2)

Frequency ramping, whether linear or nonlinear, necessitates that many intermediate frequencies between F1 and F2 are output in addition to the primary F1 and F2 frequencies. Figure 37 and Figure 38 depict the frequency vs. time characteristics of a linear ramped FSK signal.

Note that in ramped FSK mode, the delta frequency word (DFW) is required to be programmed as a positive twos complement value. Another requirement is that the lowest frequency (F1) be programmed in the Frequency Tuning Word 1 register.

The purpose of ramped FSK is to provide better bandwidth containment than traditional FSK by replacing the instantaneous frequency changes with more gradual, user-defined frequency changes. The dwell time at F1 and F2 can be equal to or much greater than the time spent at each intermediate frequency. The user controls the dwell time at F1 and F2, the number of intermediate frequencies, and the time spent at each frequency. Unlike unramped FSK, ramped FSK requires the lowest frequency to be loaded into F1 registers and the highest frequency to be loaded into F2 registers.

Several registers must be programmed to instruct the DDS on the resolution of intermediate frequency steps (48 bits) and the time spent at each step (20 bits). Furthermore, the CLR ACC1 bit in the control register should be toggled (low-high-low) prior to operation to ensure that the frequency accumulator is starting from an all 0s output condition. For piecewise, nonlinear frequency transitions, it is necessary to reprogram the registers while the frequency transition is in progress to affect the desired response.

Parallel Register Address 1A hex to Parallel Register Address 1C hex comprise the 20-bit ramp rate clock registers. This is a countdown counter that outputs a single pulse whenever the count reaches 0. The counter is activated when a logic level change occurs on the FSK input, Pin 29. This counter is run at the system clock rate, 300 MHz maximum. The time period between each output pulse is given as

$$(N + 1) \times \textit{System Clock Period}$$

where N is the 20-bit ramp rate clock value programmed by the user.

The allowable range of N is from 1 to $(2^{20} - 1)$. The output of this counter clocks the 48-bit frequency accumulator shown in Figure 39. The ramp rate clock determines the amount of time spent at each intermediate frequency between F1 and F2. The counter stops automatically when the destination frequency is achieved. The dwell time spent at F1 and F2 is determined by the duration that the FSK input, Pin 29, is held high or low after the destination frequency has been reached.

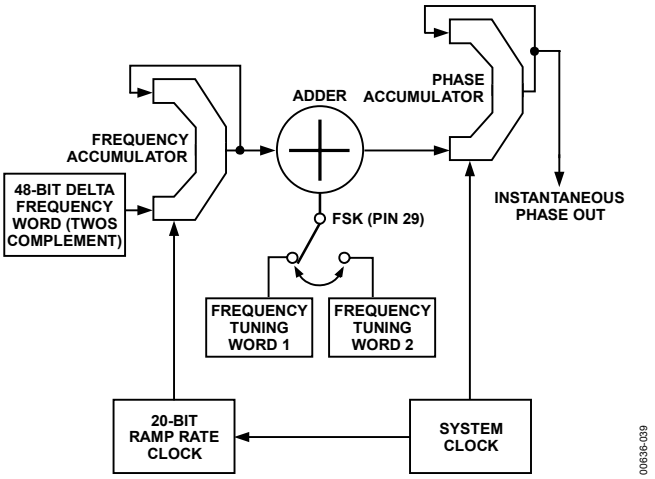

Figure 39. Block Diagram of Ramped FSK Function

Parallel Register Address 10 hex to Parallel Register Address 15 hex comprise the 48-bit, twos complement, delta frequency word registers. This 48-bit word is accumulated (added to the accumulator's output) every time it receives a clock pulse from the ramp rate counter. The output of this accumulator is added to or subtracted from the F1 or F2 frequency word, which is then fed into the input of the 48-bit phase accumulator that forms the numerical phase steps for the sine and cosine wave outputs. In this fashion, the output frequency is ramped up and down in frequency according to the logic state of Pin 29. This ramping rate is a function of the 20-bit ramp rate clock. When the destination frequency is achieved, the ramp rate clock is stopped, halting the frequency accumulation process.

Generally speaking, the delta frequency word is a much smaller value compared with the value of the F1 or F2 tuning word. For example, if F1 and F2 are 1 kHz apart at 13 MHz, the delta frequency word might be only 25 Hz.

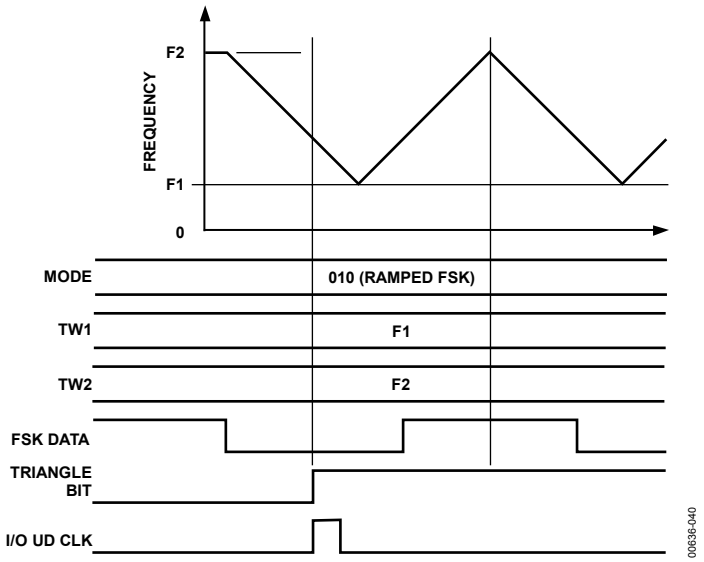

Figure 40. Effect of Triangle Bit in Ramped FSK Mode

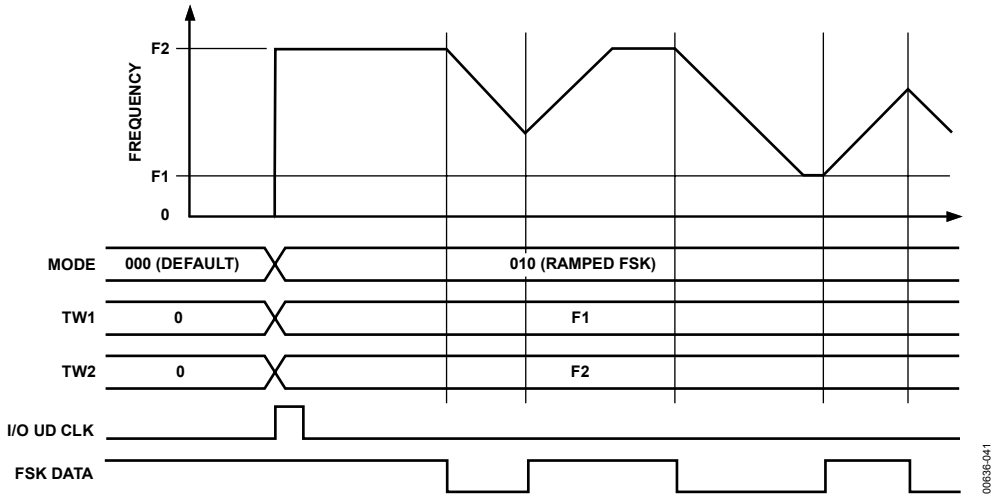

Figure 41. Effect of Premature Ramped FSK Data

Figure 41 shows that premature toggling causes the ramp to immediately reverse itself and proceed at the same rate and resolution until the original frequency is reached.

The control register contains a triangle bit at Parallel Register Address 1F hex. Setting this bit high in Mode 010 causes an automatic ramp-up and ramp-down between F1 and F2 to occur without toggling Pin 29, as shown in Figure 40. The logic state of Pin 29 has no effect once the triangle bit is set high. This function uses the ramp rate clock time period and the step size of the delta frequency word to form a continuously sweeping linear ramp from F1 to F2 and back to F1 with equal dwell times at every frequency. Use this function to automatically sweep between any two frequencies from dc to Nyquist.

In the ramped FSK mode with the triangle bit set high, an automatic frequency sweep begins at either F1 or F2, according to the logic level on Pin 29 (FSK input pin) when the triangle bit's rising edge occurs (Figure 42). If the FSK data bit is high instead of low, F2, rather than F1, is chosen as the start frequency.

Additional flexibility in the ramped FSK mode is provided by the AD9854's ability to respond to changes in the 48-bit delta frequency word and/or the 20-bit ramp rate counter at any time during the ramping from F1 to F2 or vice versa. To create these nonlinear frequency changes, it is necessary to combine several linear ramps with different slopes in a piecewise fashion. This is done by programming and executing a linear ramp at a rate or slope and then altering the slope (by changing the ramp rate clock or delta frequency word, or both). Changes in slope can be made as often as needed before the destination frequency has been reached to form the desired nonlinear frequency sweep response. These piecewise changes can be precisely timed using