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CMOS 200 MHz Quadrature Digital Upconverter

AD9856

FEATURES

- Universal low cost modulator solution for communications applications
- DC to 80 MHz output bandwidth
- Integrated 12-bit D/A converter
- Programmable sample rate interpolation filter
- Programmable reference clock multiplier
- Internal SIN(x)/x compensation filter
- >52 dB SFDR @ 40 MHz A_{OUT}
- >48 dB SFDR @ 70 MHz A_{OUT}
- >80 dB narrow-band SFDR @ 70 MHz A_{OUT}
- +3 V single-supply operation
- Space-saving surface-mount packaging
- Bidirectional control bus interface
- Supports burst and continuous Tx modes
- Single-tone mode for frequency synthesis applications
- Four programmable, pin-selectable, modulator profiles
- Direct interface to AD8320/AD8321 PGA cable driver

APPLICATIONS

- HFC data, telephony, and video modems
- Wireless and satellite communications
- Cellular base stations

GENERAL DESCRIPTION

The AD9856 integrates a high speed, direct digital synthesizer (DDS), a high performance, high speed, 12-bit digital-to-analog converter (DAC), clock multiplier circuitry, digital filters, and other DSP functions on a single chip to form a complete quadrature digital upconverter device. The AD9856 is intended to function as a universal I/Q modulator and agile upconverter for communications applications where cost, size, power dissipation, and dynamic performance are critical attributes.

The AD9856 is available in a space-saving surface-mount package, and is specified to operate over the extended industrial temperature range of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

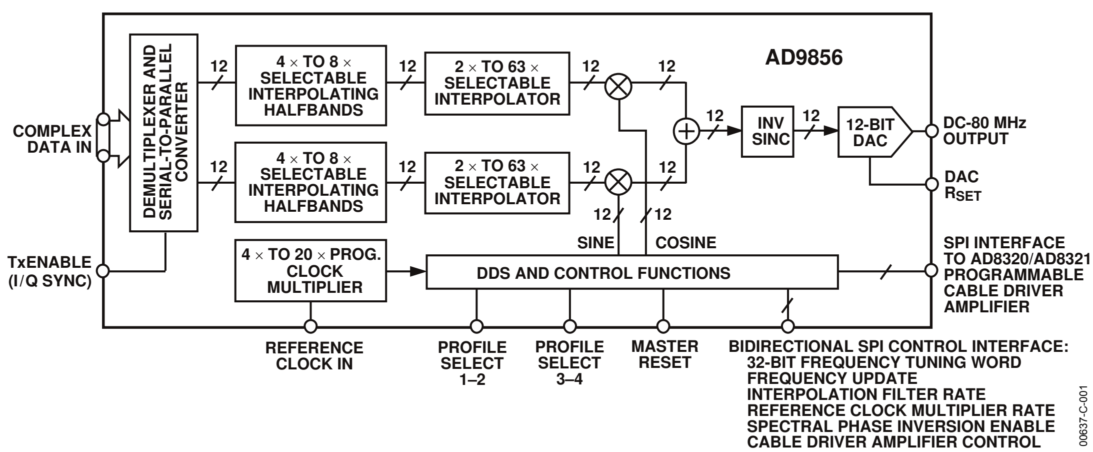

Figure 1.

Rev. C

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Fax: 781.326.8703

AD9856* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-1389: Recommended Rework Procedure for the Lead Frame Chip Scale Package (LFCSP)
- AN-237: Choosing DACs for Direct Digital Synthesis
- AN-772: A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)
- AN-823: Direct Digital Synthesizers in Clocking Applications Time
- AN-837: DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance
- AN-847: Measuring a Grounded Impedance Profile Using the AD5933
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design
- AN-922: Digital Pulse-Shaping Filter Basics
- AN-924: Digital Quadrature Modulator Gain

Data Sheet

- AD9856: CMOS 200 MHz Quadrature Digital Upconverter Data Sheet

Product Highlight

- Introducing Digital Up/Down Converters: VersaCOMM™ Reconfigurable Digital Converters

Technical Books

- A Technical Tutorial on Digital Signal Synthesis, 1999

REFERENCE MATERIALS

Technical Articles

- Basics of Designing a Digital Radio Receiver (Radio 101)
- DDS Simplifies Polar Modulation
- Digital Up/Down Converters: VersaCOMM™ White Paper
- Improved DDS Devices Enable Advanced Comm Systems
- Speedy A/Ds Demand Stable Clocks
- The Year of the Waveform Generator

DESIGN RESOURCES

- AD9856 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9856 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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Updates to Direct Digital Synthesizer Function Section 25
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Updated Outline Dimensions 35
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9/99—Rev. A to Rev. B

SPECIFICATIONS

V_S = +3 V ± 5%, R_{SET} = 3.9 kΩ, external reference clock frequency = 10 MHz with REFCLK multiplier enabled at 20×.

Table 1.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
REF CLOCK INPUT CHARACTERISTICS						
Frequency Range						
REFCLK Multiplier Disabled	Full	VI	5		200[1]	MHz
REFCLK Multiplier Enabled at 4 ×	Full	VI	5		50	MHz
REFCLK Multiplier Enabled at 20 ×	Full	VI	5		10	MHz
Duty Cycle	25°C	V		50		%
Input Capacitance	25°C	V		3		pF
Input Impedance	25°C	V		100		MΩ
DAC OUTPUT CHARACTERISTICS						
Resolution				12		Bits
Full-Scale Output Current			5	10	20	mA
Gain Error	25°C	I	−10		+10	%FS
Output Offset	25°C	I			10	μ A
Differential Nonlinearity	25°C	V		0.5		LSB
Integral Nonlinearity	25°C	V		1		LSB
Output Capacitance	25°C	V		5		pF
Phase Noise @ 1 kHz Offset, 40 MHz A_{OUT}						
REFCLK Multiplier Enabled at 20×	25°C	V		−85		dBc/Hz
REFCLK Multiplier at 4×	25°C	V		−100		dBc/Hz
REFCLK Multiplier Disabled	25°C	V		−110		dBc/Hz
Voltage Compliance Range	25°C	I	−0.5		1.5	V
Wideband SFDR:						
1 MHz Analog Out	25°C	IV		70		dBc
20 MHz Analog Out	25°C	IV		65		dBc
42 MHz Analog Out	25°C	IV		60		dBc
65 MHz Analog Out	25°C	IV		55		dBc
80 MHz Analog Out	25°C	IV		50		dBc
Narrow-Band SFDR: (± 100 kHz Window)						
70 MHz Analog Out	25°C	IV		80		dBc
MODULATOR CHARACTERISTICS						
Adjacent Channel Power (CH Power = −6.98 dBm)	25°C	IV	50			dBm
Error Vector Magnitude	25°C	IV		1	2	%
I/Q Offset	25°C	IV	50	55		dB
Inband Spurious Emissions	25°C	IV	45	50		dBc
Pass-Band Amplitude Ripple (DC to 80 MHz)	25°C	V		±0.3		dB

[1] For 200 MHz operation in modulation mode at 85°C operating temperature, V_S must be 3 V minimum.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
TIMING CHARACTERISTICS						
Serial Control Bus						
Maximum Frequency	Full	IV			10	MHz
Minimum Clock Pulse Width High (t_{PWH})	Full	IV	30			ns
Minimum Clock Pulse Width Low (t_{PWL})	Full	IV	30			ns
Maximum Clock Rise/Fall Time	Full	IV			1	ms
Minimum Data Setup Time (t_{DS})	Full	IV	25			ns
Minimum Data Hold Time (t_{DH})	Full	IV	0			ns
Maximum Data Valid Time (t_{DV})	Full	IV	30			ns
Wake-Up Time[2]	Full	IV			1	ms
Minimum RESET Pulse Width High (t_{RH})	Full	IV	5			REFCLK cycles
CMOS LOGIC INPUTS						
Logic 1 Voltage	25°C	I	2.6			V
Logic 0 Voltage	25°C	I			0.4	V
Logic 1 Current	25°C	I			12	μA
Logic 0 Current	25°C	I			12	μA
Input Capacitance	25°C	V		3		pF
CMOS LOGIC OUTPUTS (1 mA LOAD)						
Logic 1 Voltage	25°C	I	2.7			mA
Logic 0 Voltage	25°C	I			0.4	mA
POWER SUPPLY						
$+V_S$ Current						
Full Operating Conditions[3]	25°C	I			530	mA
Burst Operation (25%)	25°C	I			450	mA
Single-Tone Mode	25°C	I			495	mA
160 MHz Clock	25°C	I			445	mA
120 MHz Clock	25°C	I			345	mA
Power-Down Mode	25°C	I			2	mA

[2] Assuming 1.3 kΩ and 0.01 μF loop filter components.
[3] Assuming 1.3 kW and 0.01 mF loop filter components.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

Table 2.

Parameter	Rating
Maximum Junction Temperature	150°C
Storage Temperature	−65°C to +150°C
V_S	4 V
Operating Temperature	−40°C to +85°C
Digital Inputs	−0.7 V to $+V_S$
Lead Temperature (Soldering 10 sec)	300°C
Digital Output Current	5 mA
θ_{JA} Thermal Impedance	38°C/W

EXPLANATION OF TEST LEVELS

I. 100% production tested.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. Devices are 100% production tested at 25°C and guaranteed by design and characterization testing for industrial operating temperature range.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

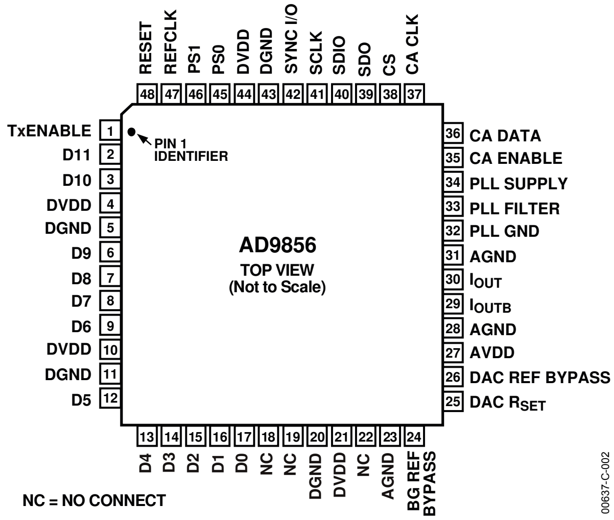

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Pin Function	Pin No.	Mnemonic	Pin Function
1	TxENABLE	Input Pulse that Synchronizes the Data Stream	32	PLL GND	PLL Ground
2	D11	Input Data (Most Significant Bit)	33	PLL FILTER	PLL Loop Filter Connection
3	D10	Input Data	34	PLL SUPPLY	PLL Voltage Supply
4, 10, 21, 44	DVDD	Digital Supply Voltage	35	CA ENABLE	Cable Driver Amp Enable
5, 11, 20, 43	DGND	Digital Ground	36	CA DATA	Cable Driver Amp Data
6 to 9	D9 to D6	Input Data	37	CA CLK	Cable Driver Amp Clock
12 to 16	D5 to D1	Input Data	38	$\overline{CS}$	Chip Select
17	D0	Input Data (Least Significant Bit)	39	SDO	Serial Data Output
18, 19, 22	NC	No Internal Connection	40	SDIO	Serial Port I/O
23, 28, 31	AGND	Analog Ground	41	SCLK	Serial Port Clock
24	BG REF BYPASS	No External Connection[1]	42	SYNC I/O	Performs I/O Synchronization
25	DAC R_{SET}	R_{SET} Resistor Connection	45	PS0	Profile Select 0
26	DAC REF BYPASS	No External Connection	46	PS1	Profile Select 1
27	AVDD	Analog Supply Voltage	47	REFCLK	Reference Clock Input
29	I_{OUTB}	Complementary Analog Current Output of the DAC	48	RESET	Master Reset
30	I_{OUT}	True Analog Current Output of DAC			

[1] In most cases, optimal performance is achieved with no external connection. For extremely noisy environments, BG REF BYPASS can be bypassed with up to a 0.1 μF capacitor to AGND (Pin 23). DAC REF BYPASS can be bypassed with up to a 0.1 μF capacitor to AVDD (Pin 27).

Table 4. Functional Block Mode Descriptions

Functional Block	Mode Description
Operating Modes	1. Complex quadrature modulator mode.
	2. Single-tone output mode.
Input Data Format	Programmable: 12-bit, 6-bit, or 3-bit input formats. Data input to the AD9856 is 12-bit, twos complement. Complex I/Q symbol component data is required to be at least 2× oversampled, depending upon configuration.
Input Sample Rate	Up to 50 Msamples/sec @ 200 MHz SYSCLK rate.
Input Reference Clock Frequency	For DC to 80 MHz A_{OUT} operation (200 MHz SYSCLK rate) with REFCLK multiplier enabled: 10 MHz to50 MHz, programmable via control bus; with REFCLK multiplier disabled: 200 MHz.
	Note: For optimum data synchronization, the AD9856 reference clock and the input data clock should be derived from the same clock source.
Internal Reference Clock Multiplier	Programmable in integer steps over the range of 4× to 20×. Can be disabled (effective REFCLK multiplier = 1) via control bus. Output of REFCLK multiplier = SYSCLK rate, which is the internal clock rate applied to the DDS and DAC function.
Profile Select	Four pin-selectable, preprogrammed formats. Available for modulation and single-tone operating modes.
Interpolating Range	Fixed 4×, selectable 2×, and selectable 2× to 63× range.
Half-Band Filters	Interpolating filters that provide upsampling and reduce the effects of the CIC passband roll-off characteristics.
TxENABLE Function–Burst Mode	When burst mode is enabled via the control bus, the rising edge of the applied TxENABLE pulse should be coincident with, and frame, the input data packet. This establishes data sampling synchronization.
TxENABLE Function–Continuous Mode	When continuous mode is enabled via the control bus, the TxENABLE pin becomes an I/Q control line. A Logic 1 on TxENABLE indicates I data is being presented to the AD9856. A Logic 0 on TxENABLE indicates Q data is being presented to the AD9856. Each rising edge of TxENABLE resynchronizes the AD9856 input sampling capability.
Inverse SINC Filter	Precompensates for SIN(x)/x roll-off of DAC; user bypassable.
I/Q Channel Invert	$[I \times Cos(\omega t) + Q \times Sin(\omega t)]$ or $[I \times Cos(\omega t) - Q \times Sin(\omega t)]$ (default), configurable via control bus, per profile.
Full Sleep Mode	Power dissipation reduced to less than 6 mW when full sleep mode is active; programmable via the control bus.

TYPICAL PERFORMANCE CHARACTERISTICS

TYPICAL MODULATED OUTPUT SPECTRAL PLOTS

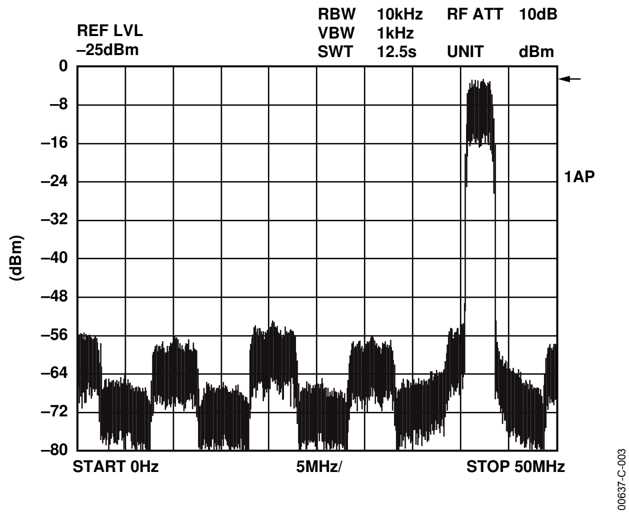

Figure 3. QPSK at 42 MHz and 2.56 MS/sec; 10.24 MHz External Clock with REFCLK Multiplier = 12, CIC = 3, HB3 On, 2× Data

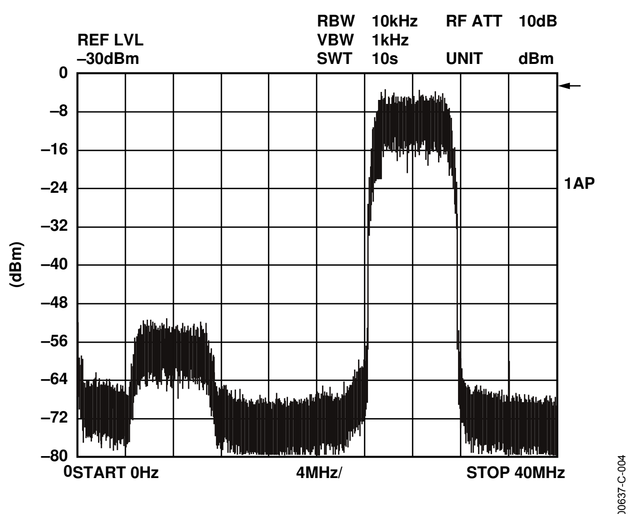

Figure 4. 64-QAM at 28 MHz and 6 MS/sec; 36 MHz External Clock with REFCLK Multiplier = 4, CIC = 2, HB3 Off, 3× Data

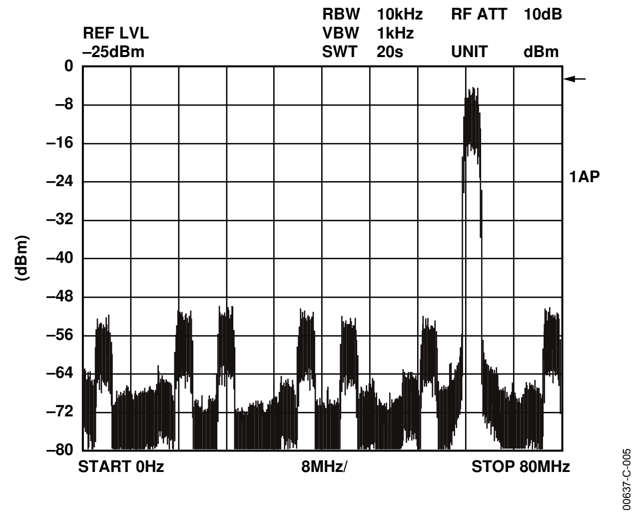

Figure 5. 16-QAM at 65 MHz and 2.56 MS/sec; 10.24 MHz External Clock with REFCLK Multiplier = 18, CIC = 9, HB3 Off, 2× Data

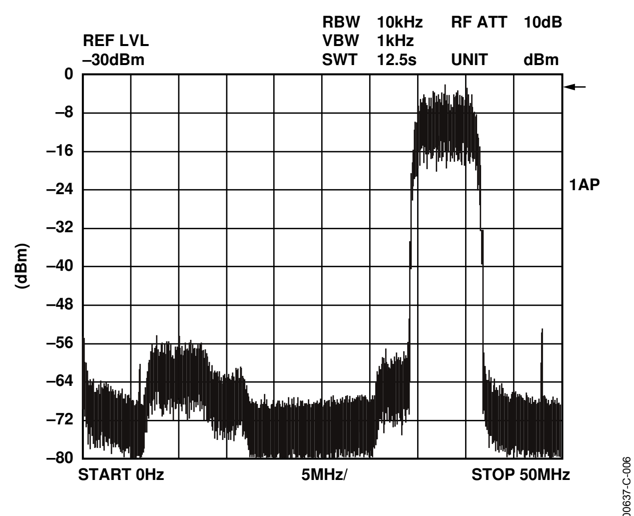

Figure 6. 256-QAM at 38 MHz and 6 MS/sec; 48 MHz External Clock with REFCLK Multiplier = 4, CIC = 2, HB3 Off, 4× Data

TYPICAL SINGLE-TONE OUTPUT SPECTRAL PLOTS

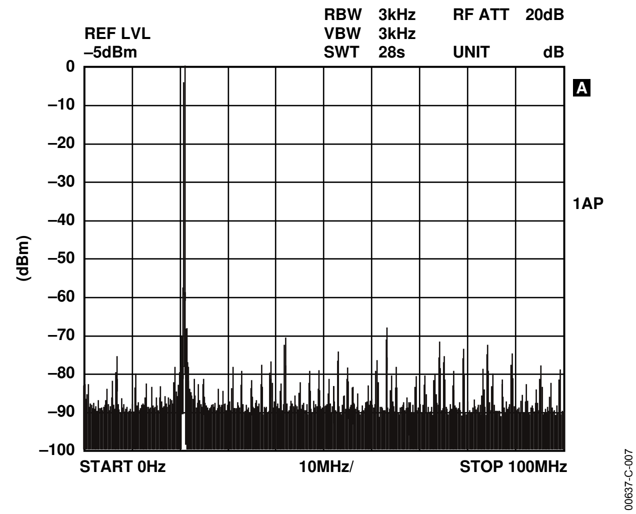

Figure 7. 21 MHz CW Output

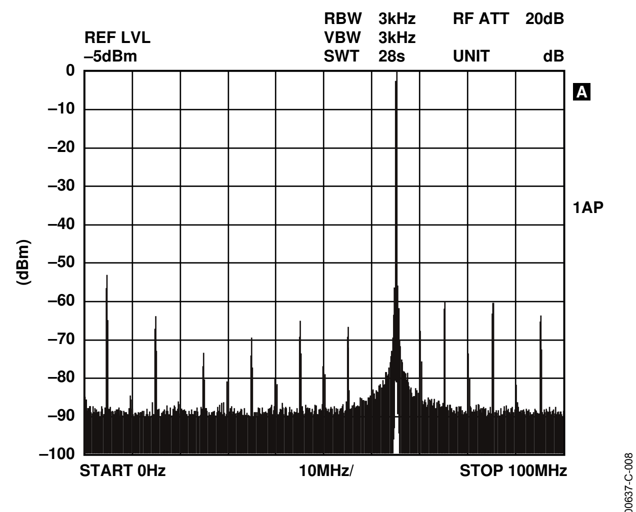

Figure 8. 65 MHz CW Output

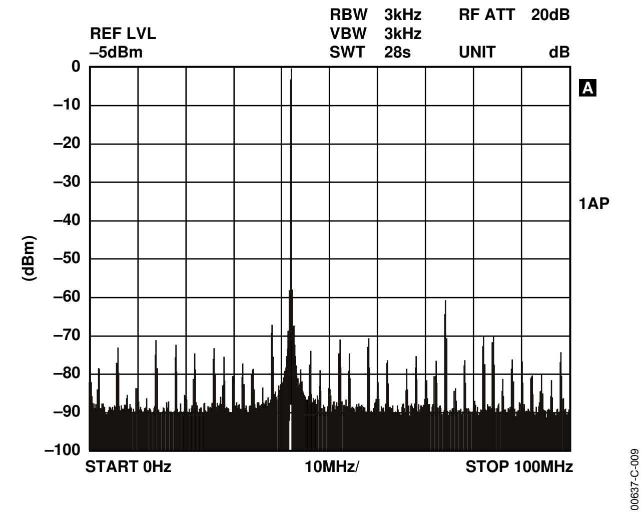

Figure 9. 42 MHz CW Output

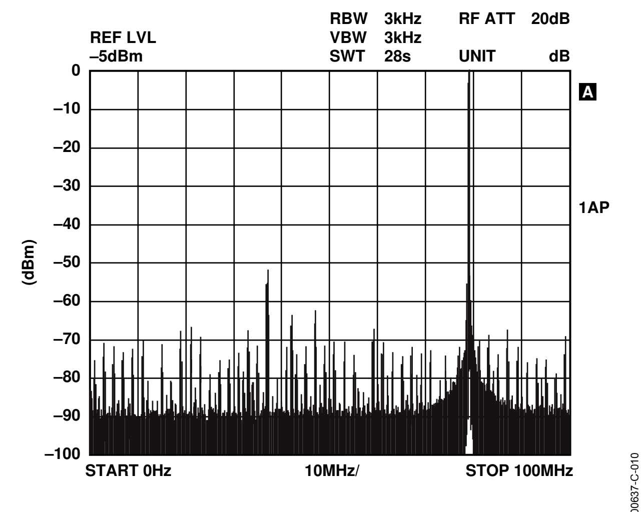

Figure 10. 79 MHz CW Output

TYPICAL NARROW-BAND SFDR SPECTRAL PLOTS

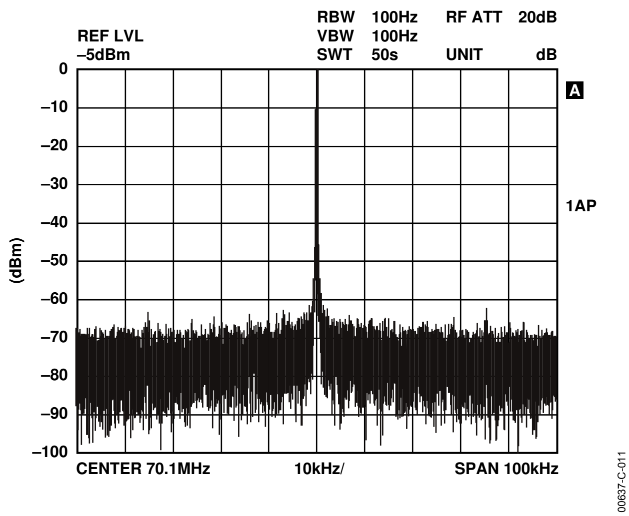

Figure 11. 70.1 MHz Narrow-Band SFDR, 10 MHz External Clock with REFCLK Multiplier = 20×

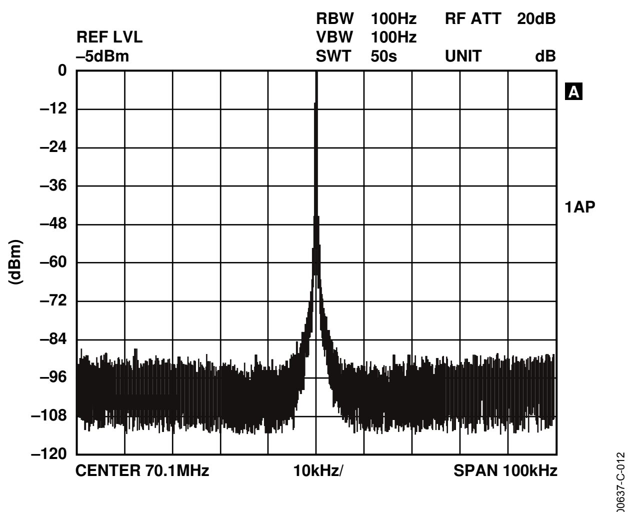

Figure 12. 70.1 MHz Narrow-Band SFDR, 200 MHz External Clock with REFCLK Multiplier Disabled

TYPICAL PHASE NOISE SPECTRAL PLOTS

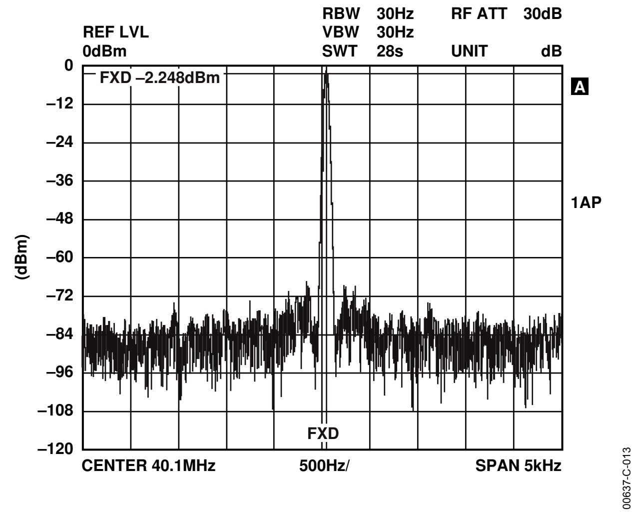

Figure 13. 40.1 MHz Output, 10 MHz External Clock with REFCLK Multiplier = 20×

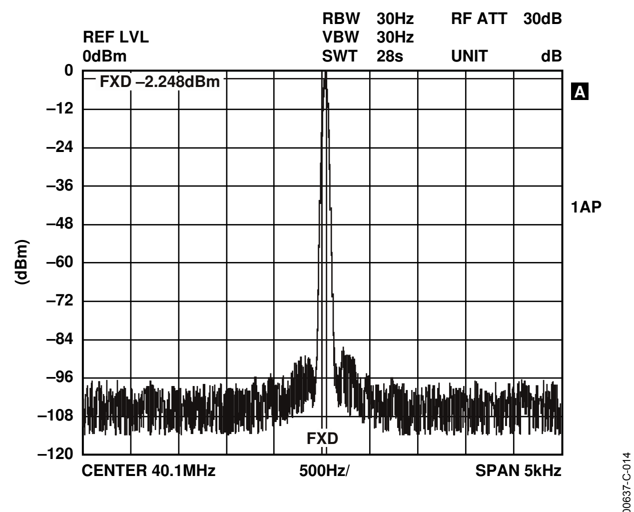

Figure 14. 40.1 MHz Output, 200 MHz External Clock with REFCLK Multiplier Disabled

TYPICAL PLOTS OF OUTPUT CONSTELLATIONS

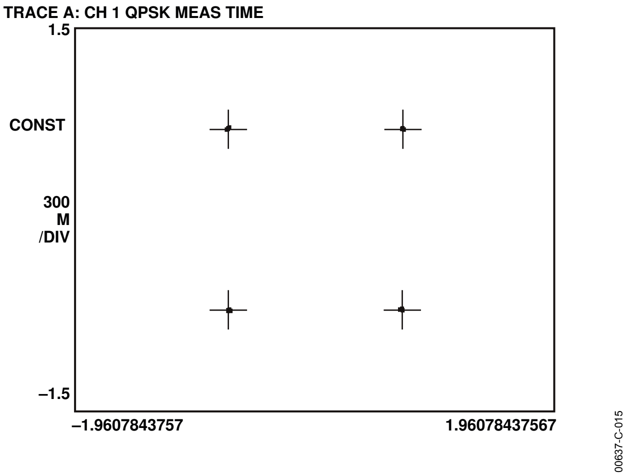

Figure 15. QPSK, 65 MHz, 2.56 MS/sec

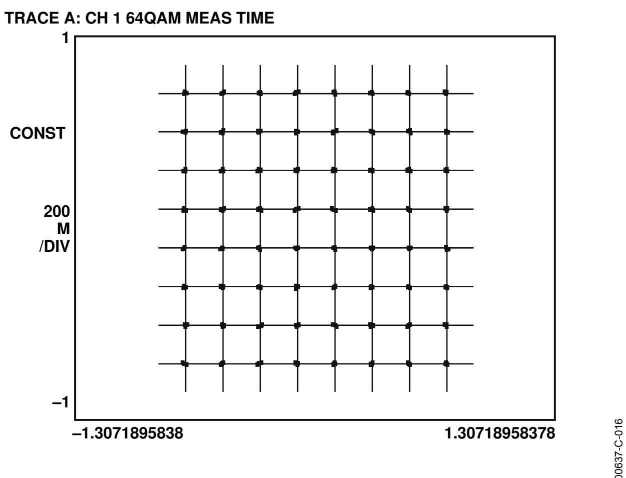

Figure 16. 64-QAM, 42 MHz, 6 MS/sec

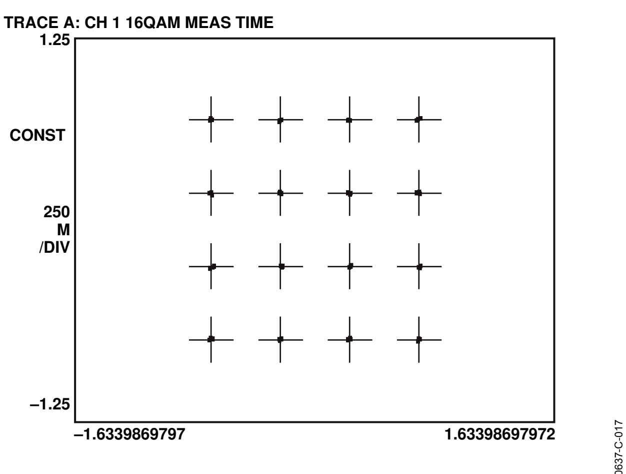

Figure 17. 16-QAM, 65 MHz, 2.56 MS/sec

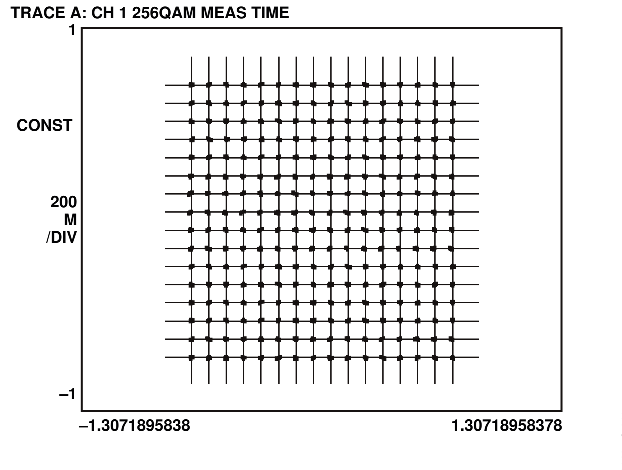

Figure 18. 256-QAM, 42 MHz, 6 MS/sec

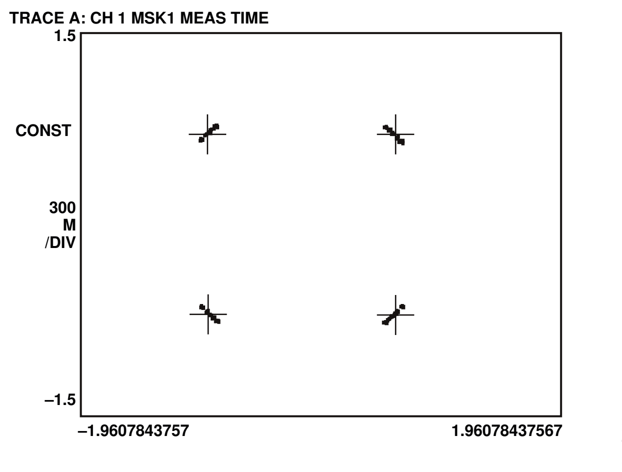

Figure 19. GMSK Modulation, 13 MS/sec

POWER CONSUMPTION

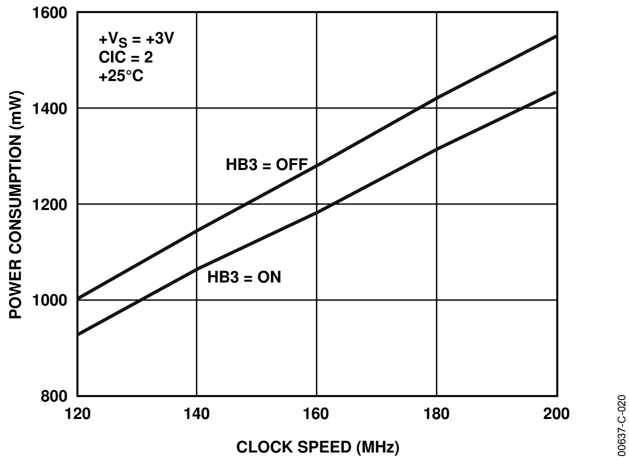

Figure 20. Power Consumption vs. Clock Speed; V_S = 3 V, CIC = 2, 25°C

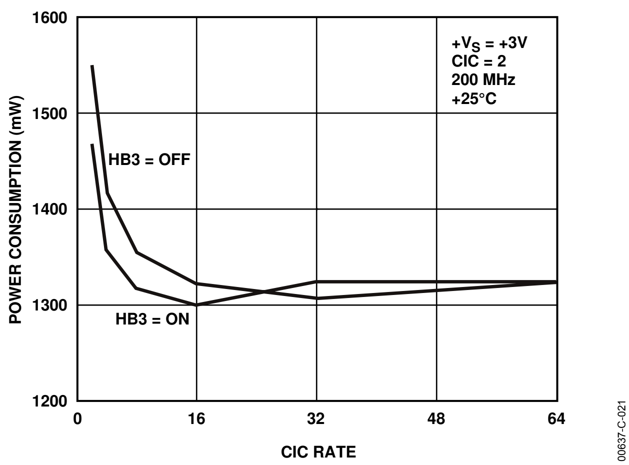

Figure 21. Power Consumption vs. CIC Rate; V_S = 3 V, 200 MHz, 2°C

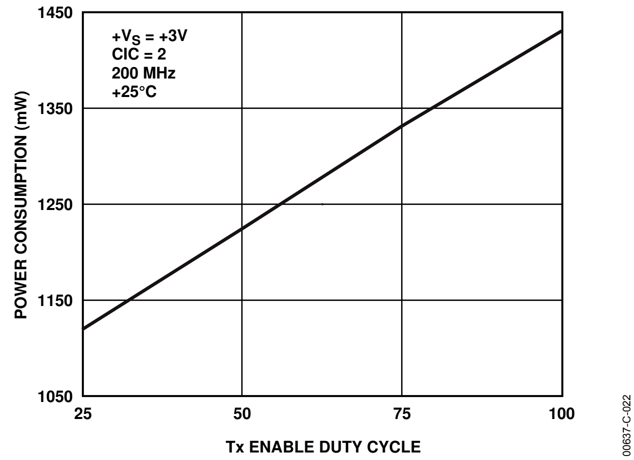

Figure 22. Power Consumption vs. Burst Duty Cycle; V_S = 3 V, CIC = 2, 200 MHz, 25°C

SERIAL CONTROL BUS REGISTER

Table 5. Serial Control Bus Register Layout

Register	AD9856 Register Layout									
Address (hex)	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Default (hex)**	**Profile**
00	SDO Active	LSB First	REFCLK Mult.<4>	REFCLK Mult.<3>	REFCLK Mult.<2>	REFCLK Mult.<1>	REFCLK Mult.<0>	Reserved	15	N/A
01	CIC Gain	Continuous Mode	Full Sleep Mode	Single-tone Mode	Bypass Inverse Sinc Filter	Bypass REFCLK Mult.	Input Format Select <1>	Input Format Select <0>	06	N/A
02	Frequency Tuning Word <7:0>								04	1
03	Frequency Tuning Word <15:8>								00	1
04	Frequency Tuning Word <23:16>								00	1
05	Frequency Tuning Word <31:24>								00	1
06	Interpolator Rate <5>	Interpolator Rate <4>	Interpolator Rate <3>	Interpolator Rate <2>	Interpolator Rate <1>	Interpolator Rate <0>	Spectral Inversion	Bypass the Third Half-Band Filter	FC	1
07	AD8320/AD8321 Gain Control Bits <7:0>								00	1
08	Frequency Tuning Word <7:0>								00	2
09	Frequency Tuning Word <15:8>								00	2
0A	Frequency Tuning Word <23:16>								00	2
0B	Frequency Tuning Word <31:24>								80	2
0C	Interpolator Rate <5>	Interpolator Rate <4>	Interpolator Rate <3>	Interpolator Rate <2>	Interpolator Rate <1>	Interpolator Rate <0>	Spectral Inversion	Bypass the Third Half-Band Filter	1E	2
0D	AD8320/AD8321 Gain Control Bits <7:0>								00	2
0E	Frequency Tuning Word <7:0>								Unset	3
0F	Frequency Tuning Word <15:8>								Unset	3
10	Frequency Tuning Word <23:16>								Unset	3
11	Frequency Tuning Word <31:24>								Unset	3
12	Interpolator Rate <5>	Interpolator Rate <4>	Interpolator Rate <3>	Interpolator Rate <2>	Interpolator Rate <1>	Interpolator Rate <0>	Spectral Inversion	Bypass the Third Half-Band Filter	Unset	3
13	AD8320/AD8321 Gain Control Bits <7:0>								00	3
14	Frequency Tuning Word <7:0>								Unset	4
15	Frequency Tuning Word <15:8>								Unset	4
16	Frequency Tuning Word <23:16>								Unset	4
17	Frequency Tuning Word <31:24>								Unset	4
18	Interpolator Rate <5>	Interpolator Rate <4>	Interpolator Rate <3>	Interpolator Rate <2>	Interpolator Rate <1>	Interpolator Rate <0>	Spectral Inversion	Bypass the Third Half-Band Filter	Unset	4
19	AD8320/AD8321 Gain Control Bits <7:0>								00	4

REGISTER BIT DEFINITIONS

Control Bits—Register Address 00h and 01h

SDO Active—Register Address 00h, Bit 7. Active high indicates serial port uses dedicated in/out lines. Default low configures serial port as single-line I/O.

LSB First—Register Address 00h, Bit 6. Active high indicates serial port access is LSB-to-MSB format. Default low indicates MSB-to-LSB format.

REFCLK Multiplier—Register Address 00h, Bits 5, 4, 3, 2, 1 form the reference clock multiplier. Valid entries range from 4–20 (decimal). Straight binary to decimal conversion is implemented. For example, to multiply the reference clock by 19 decimal, Program Register Address 00h, Bits 5–1, as 13h. Default value is 0A (hex).

Reserved Bit—Register Address 00h, Bit 0. This bit is reserved. Always set this bit to Logic 1 when writing to this register.

CIC Gain—Register Address 01h, Bit 7. The CIC GAIN bit multiplies the CIC filter output by 2. See the Cascaded Integrator Comb (CIC) Filter section for more details. Default value is 0 (inactive).

Continuous Mode—Register Address 01h, Bit 6 is the continuous mode configuration bit. Active high configures the AD9856 to accept continuous-mode timing on the TxENABLE input. A low configures the device for burst-mode timing. Default value is 0 (burst mode).

Full Sleep Mode—Register Address 01h, Bit 5. Active high full sleep mode bit. When activated, the AD9856 enters a full shutdown mode, consuming less than 2 mA after completing a shutdown sequence. Default value is 0 (awake).

Single-Tone Mode—Register Address 01h, Bit 4. Active high configures the AD9856 for single-tone applications. The AD9856 supplies a single-frequency output as determined by the frequency tuning word (FTW) selected by the active profile. In this mode, the 12 input data pins are ignored but should be tied high or low. Default value is 0 (inactive).

Bypass Inverse Sinc Filter—Register Address 01h, Bit 3. Active high configures the AD9856 to bypass the SIN(x)/x compensation filter. Default value is 0 (inverse SINC filter enabled).

Bypass REFCLK Multiplier—Register Address 01h, Bit 2. Active high configures the AD9856 to bypass the REFCLK multiplier function. When active, effectively causes the REFCLK multiplier factor to be 1. Default value is 1 (REFCLK multiplier bypassed).

Input Format Select—Register Address 01h, Bits 1 and 0, form the input format mode bits.

10b = 12-bit mode
01b = 6-bit mode
00b = 3-bit mode

Default value is 10b (12-bit mode).

Profile 1 Registers—Active when PROFILE Inputs are 00b

Frequency Tuning Word (FTW)—The frequency tuning word for Profile 1 is formed via a concatenation of register addresses 05h, 04h, 03h, and 02h. Bit 7 of Register Address 05h is the most significant bit of the Profile 1 frequency tuning word. Bit 0 of Register Address 02h is the least significant bit of the Profile 1 frequency tuning word. The output frequency equation is given as: f_{OUT} = (FTW SYSCLK)/2^{32}.

Interpolation Rate—Register Address 06h, Bit 7 through Bit 2 form the Profile 1 CIC filter interpolation rate value. Allowed values range from 2 to 63 (decimal).

Spectral Inversion—Register Address 06h, Bit 1. Active high, Profile 1 spectral inversion bit. When active, inverted modulation is performed [I Cos(ωt) + Q × Sin(t)]. The Default is inactive, Logic 0, noninverted modulation [I × Cos(ωt) − Q × Sin(ωt)].

Bypass Half-Band Filter 3—Register Address 06h, Bit 0. Active high, causes the AD9856 to bypass the third half-band filter stage that precedes the CIC interpolation filter. Bypassing the third half-band filter negates the 2× upsample inherent with this filter and reduces the overall interpolation rate of the half-band filter chain from 8× to 4×. Default value is 0 (Half-Band 3 enabled).

AD8320/AD8321 Gain Control—Register Address 07h, Bit 7 through Bit 0 form the Profile 1 AD8320/AD8321 gain bits. The AD9856 dedicates three output pins, which directly interface to the AD8320/AD8321 cable driver amp. This allows direct control of the cable driver via the AD9856. See the **Error! Reference source not found.** section for more details. Bit 7 is the MSB, Bit 0 is the LSB. Default value is 00h.

Profile 2 Registers—Active when PROFILE Inputs are 01b

Profile 2 register functionality is identical to Profile 1, with the exception of the register addresses.

Profile 3 Registers—Active when PROFILE Inputs are 10b

Profile 3 register functionality is identical to Profile 1, with the exception of the register addresses.

Profile 4 Registers—Active when PROFILE Inputs are 11b

Profile 4 register functionality is identical to Profile 1, with the exception of the register addresses.

THEORY OF OPERATION

To gain a general understanding of the functionality of the AD9856, it is helpful to refer to Figure 23, a block diagram of the device architecture. The following is a general description of the device functionality. Later sections detail each of the data path building blocks.

MODULATION MODE OPERATION

The AD9856 accepts 12-bit data-words, which are strobed into the data assembler via an internal clock. The input, TxENABLE, serves as the valve that allows data to be accepted or ignored by the data assembler. The user has the option to feed the 12-bit data-words to the AD9856 as single 12-bit words, dual 6-bit words, or quad 3-bit words. This provides the user with the flexibility to use fewer interface pins, if desired. Furthermore, the incoming data is assumed to be complex in that alternating 12-bit words are regarded as the inphase (I) and quadrature (Q) components of a symbol.

The rate at which the 12-bit words are presented to the AD9856 is referred to as the input sample rate (f_{IN}). Note that f_{IN} is not the same as the baseband data rate provided by the user. Rather, the user's baseband data is required to be upsampled by at least a factor of two (2) before being applied to the AD9856 in order to minimize the frequency-dependent attenuation associated with the CIC filter stage (see the Cascaded Integrator Comb (CIC) Filter section).

The data assembler splits the incoming data-word pairs into separate I/Q data streams. The rate at which the I/Q data-word pairs appear at the output of the data assembler is referred to as the I/Q sample rate (f_{IQ}). Because two 12-bit input data-words are used to construct the individual I and Q data paths, the input sample rate is twice the I/Q sample rate (i.e., $f_{IN} = 2 \times f_{IQ}$).

Once through the data assembler, the I/Q data streams are fed through two half-band filters (Half-Band Filters 1 and 2). The combination of these two filters results in a factor of four (4) increase of the sample rate. Thus, at the output of Half-Band Filter 2, the sample rate is $4 \times f_{IQ}$. In addition to the sample rate increase, the half-band filters provide the low-pass filtering characteristic necessary to suppress the spectral images produced by the upsampling process. Further upsampling is available via an optional third half-band filter (Half-Band Filter 3). When selected, this provides an overall upsampling factor of eight (8). Thus, if Half-Band Filter 3 is selected, the sample rate at its output is $8 \times f_{IQ}$.

After passing through the half-band filter stages, the I/Q data streams are fed to a cascaded integrator comb (CIC) filter. This filter is configured as an interpolating filter, which allows further upsampling rates of any integer value between 2 and 63, inclusive. The CIC filter, like the half-bands, has a built-in low-pass characteristic. Again, this provides for suppression of the spectral images produced by the upsampling process.

The digital quadrature modulator stage following the CIC filters is used to frequency shift the baseband spectrum of the incoming data stream up to the desired carrier frequency (a process known as upconversion). The carrier frequency is controlled numerically by a direct digital synthesizer (DDS). The DDS uses its internal reference clock (SYSCLK) to generate the desired carrier frequency with a high degree of precision. The carrier is applied to the I and Q multipliers in quadrature fashion (90° phase offset) and summed to yield a data stream that is the modulated carrier. Note that the incoming data has been converted from an input sample rate of f_{IN} to an output sample rate of SYSCLK (see Figure 23).

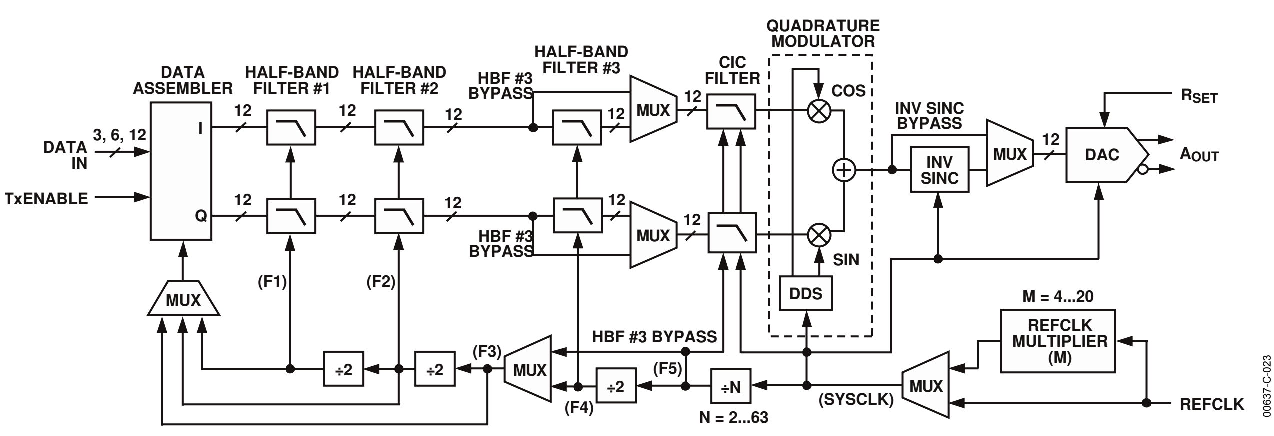

Figure 23. AD9856 Block Diagram

The sampled carrier is ultimately destined to serve as the input data to the digital-to-analog converter (DAC) integrated on the AD9856. The DAC output spectrum is distorted due to the intrinsic zero-order hold effect associated with DAC-generated signals. This distortion is deterministic, however, and follows the familiar SIN(x)/x (or SINC) envelope. Because the SINC distortion is predictable, it is also correctable—therefore, the presence of the optional inverse SINC filter preceding the DAC. This is a FIR filter, which has a transfer function conforming to the inverse of the SINC response. Thus, when selected, it modifies the incoming data stream so that the SINC distortion, which would otherwise appear in the DAC output spectrum, is virtually eliminated.

As mentioned earlier, the output data is sampled at the rate of SYSCLK. Because the AD9856 is designed to operate at SYSCLK frequencies up to 200 MHz, there is the potential difficulty of trying to provide a stable input clock (REFCLK). Although stable, commercial high frequency oscillators tend to be cost prohibitive. To alleviate this problem, the AD9856 has a built-in programmable clock multiplier circuit. This allows the user to use a relatively low frequency (thus, less expensive) oscillator to generate the REFCLK signal. The low frequency REFCLK signal can then be multiplied in frequency by an integer factor between 4 and 20, inclusive, to become the SYSCLK signal.

Single-Tone Output Operation

The AD9856 can be configured for frequency synthesis applications by writing the single-tone bit true. In single-tone mode, the AD9856 disengages the modulator and preceding data path logic to output a spectrally pure, single-frequency sine wave. The AD9856 provides for a 32-bit frequency tuning word, which results in a tuning resolution of 0.046 Hz at a SYSCLK rate of 200 MHz.

When using the AD9856 as a frequency synthesizer, a general rule is to limit the fundamental output frequency to 40% of SYSCLK. This avoids generating aliases too close to the desired fundamental output frequency, thus minimizing the cost of filtering the aliases.

All applicable programming features of the AD9856 apply when configured in single-tone mode. These features include:

- Frequency hopping via the profile inputs and associated tuning word, which allows frequency shift keying (FSK) modulation.
- Ability to bypass the REFCLK multiplier, which results in lower phase noise and reduced output jitter.
- Ability to bypass the SIN(x)/x compensation filter.
- Full power-down mode.

INPUT WORD RATE (F_W) vs. REFCLK RELATIONSHIP

There is a fundamental relationship between the input word rate (f_W) and the frequency of the clock that serves as the timing source for the AD9856 (REFCLK). The f_W is defined as the rate at which K-bit data-words (K = 3, 6, or 12) are presented to the AD9856. However, the following factors affect this relationship:

- The interpolation rate of the CIC filter stage.
- Whether or not Half-Band Filter 3 is bypassed.
- The value of the REFCLK multiplier (if selected).
- Input word length.

This relationship can be summed as

$$REFCLK = (2\ HNf_W)/MI$$

where *H, N, I*, and *M* are integers determined as follows:

H	=	1: Half-Band Filter 3 bypassed
		2: Half-Band Filter 3 enabled
M	=	1: REFCLK multiplier bypassed
		$4 \le M \le 20$: REFCLK multiplier enabled
I	=	1: Full-word input format
		2: Half-word input format
		4: Quarter-Word input format
N	=	CIC interpolation rate ($2 \le N \le 63$)

These conditions show that REFCLK and f_W have an integer ratio relationship. It is very important that users choose a value of REFCLK to ensure that this integer ratio relationship is maintained.

I/Q DATA SYNCHRONIZATION

As mentioned previously, the AD9856 accepts I/Q data pairs and a twos complement numbering system in three different word length modes. The full-word mode accepts 12-bit parallel I and Q data. The half-word mode accepts dual 6-bit I and Q data inputs to form a 12-bit word. The quarter-word mode accepts multiple 3-bit I and Q data inputs to form a 12-bit word. For all word length modes, the AD9856 assembles the data for signal processing into time-aligned, parallel, 12-bit I/Q pairs. In addition to the word length flexibility, the AD9856 has two input timing modes, burst or continuous, that are programmable via the serial port.

For burst-mode input timing, no external data clock needs to be provided, because the data is oversampled at the D<11:0> pins using the system clock (SYSCLK). The TxENABLE pin is required to frame the data burst, because the rising edge of TxENABLE is used to synchronize the AD9856 to the input data rate. The AD9856 registers the input data at the approximate center of the data valid time. Thus, for larger CIC interpolation rates, more SYSCLK cycles are available to oversample the input data, maximizing clock jitter tolerances.

For continuous-mode input timing, the TxENABLE pin can be thought of as a data input clock running at half the input sample rate ($f_W/2$). In addition to synchronization, for continuous mode timing, the TxENABLE input indicates whether an I or Q input is being presented to the D<11:0> pins. It is intended that data is presented in alternating fashion such that I data is followed by Q data. Stated another way, the TxENABLE pin should maintain approximately a 50/50 duty cycle. As in burst mode, the rising edge of TxENABLE synchronizes the AD9856 to the input data rate and the data is registered at the approximate center of the data-valid time. The continuous operating mode can only be used in conjunction with the full-word input format.

Burst Mode Input Timing

Figure 24 through Figure 28 show the input timing relationship between TxENABLE and the 12-bit input data-word for all three input format modes when the AD9856 is configured for burst input timing. Also shown in these diagrams is the time-aligned, 12-bit parallel I/Q data as assembled by the AD9856.

Figure 24 shows the classic burst-mode timing, for full-word input mode, in which TxENABLE frames the input data stream. Note that sequential input of alternating I/Q data, starting with I data, is required.

The input sample rate for full-word mode, when the third half-band filter is engaged, is given by

$$f_{IN} = SYSCLK/4N$$

where N is the CIC interpolation rate.

The input sample rate for full-word mode, when the third half-band filter is not engaged is given by:

$$f_{IN} = SYSCLK/2N$$

where N is the CIC interpolation rate

Figure 25 shows an alternate timing method for TxENABLE when the AD9856 is configured in full-word, burst-mode operation. The benefit of this timing is that the AD9856 resynchronizes the input sampling logic when the rising edge of TxENABLE is detected. The low time on TxENABLE is limited to one input sample period and must be low during the Q data period. The maximum high time on TxENABLE is unlimited. Thus, unlimited high time on TxENABLE results in the timing diagram of Figure 24. See Figure 28 for the ramifications of violating the TxENABLE low time constraint when operating in burst mode.

Figure 26 shows the input timing for half-word mode, burst input timing operation.

In half-word mode, data is input on the D<11:6> inputs. The D<5:0> inputs are unused in this mode and should be tied to DGND or DVDD. The AD9856 expects the data to be input in the following manner: I<11:6>, I<5:0>, Q<11:6>, Q<5:0>. Data is twos complement; the sign bit is D<11> in the notation I<11:0>, Q<11:0>.

The input sample rate for half-word mode, when the third half-band filter is engaged, is given by

$$f_{IN} = SYSCLK/4N$$

where N is the CIC interpolation rate.

The input sample rate for half-word mode, when the third half-band filter is not engaged is given by:

$$f_{IN} = SYSCLK/2N$$

where N is the CIC interpolation rate.

Figure 27 shows the input timing for quarter-word, burst input timing operation.

In quarter-word mode, data is input on the D<11:9> inputs. The D<8:0> inputs are unused in this mode and should be tied to DGND or DVDD. The AD9856 expects the data to be input in the following manner: I<11:9>, I<8:6>, I<5:3>, I<2:0>, Q<11:9>, Q<8:6>, Q<5:3>, Q<2:0>. Data is twos complement; the sign bit is D<11> in the notation I<11:0>, Q<11:0>.

The input sample rate for quarter-word mode, when the third half-band filter is engaged, is given by:

$$f_{IN} = SYSCLK/N$$

where N is the CIC interpolation rate.

Note that Half-Band Filter 3 must be engaged when operating in quarter-word mode.

Figure 28 describes the end of burst timing and internal data assembly. Note that in burst-mode operation, if the TxENABLE input is low for more than one input sample period, numerical zeros are internally generated and passed to the data path logic for signal processing. This is not valid for continuous-mode operation, as is discussed later.

To ensure proper operation, the minimum time between falling and rising edges of TxENABLE is one input sample period.

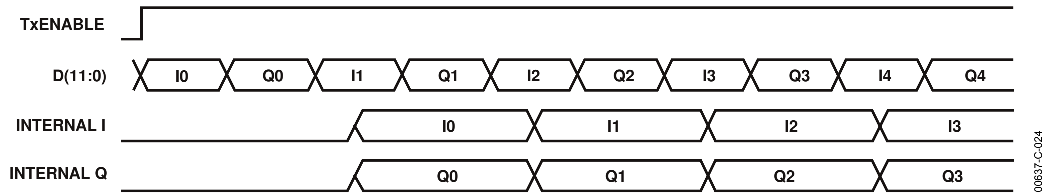

Figure 24. 12-Bit Input Mode, Classic Burst Timing

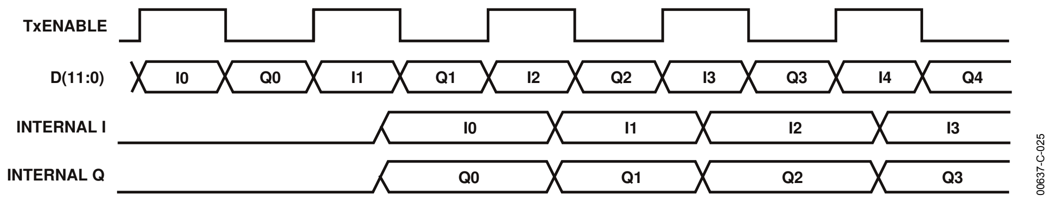

Figure 25. 12-Bit Input Mode, Alternate TxENABLE Timing

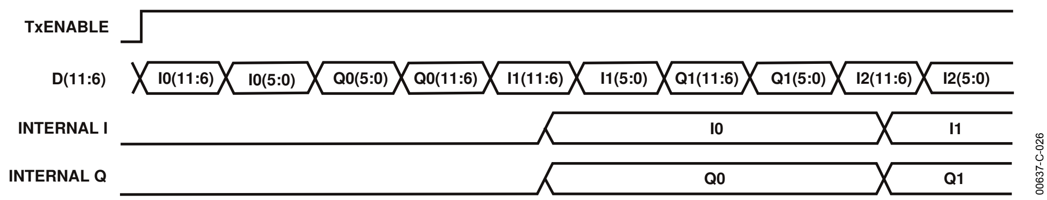

Figure 26. 6-Bit Input Mode, Burst Mode Timing

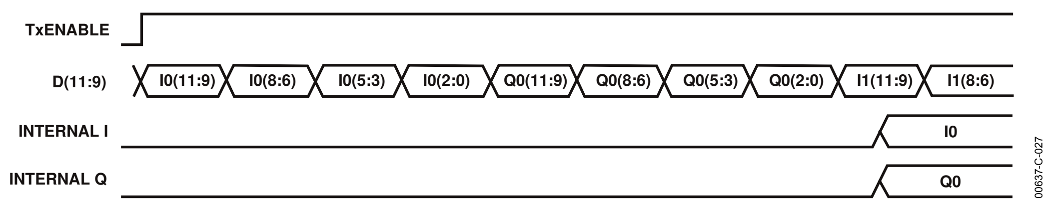

Figure 27. 3-Bit Input Mode, Burst Mode Timing

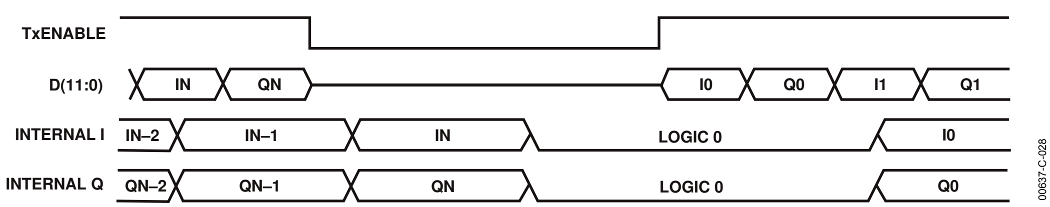

Figure 28. End of Burst Mode Input Timing

Continuous Mode Input Timing

The AD9856 is configured for continuous mode input timing by writing the continuous mode bit true (Logic 1). The continuous mode bit is in register address 01h, Bit 6. The AD9856 must be configured for full-word input format when operating in continuous mode input timing. The input data rate equations described previously for full-word mode apply for continuous mode. Figure 25, which is the alternate burst mode timing diagram, is also the continuous mode input timing. Figure 29 and Figure 30 show what the internal data assembler presents to the signal processing logic when the TxENABLE input is held static for greater than one input sample period. Please note that the timing diagram shown in Figure 29 and Figure 30 detail INCORRECT timing relationships between TxENABLE and data. They are only presented to indicate that the AD9856 resynchronizes properly after detecting a rising edge of TxENABLE. Also note that the significant difference between burst and continuous mode operation is that in addition to synchronizing the data, TxENABLE is used to indicate whether an I or Q input is being sampled.

Do not engage continuous mode simultaneously with the REFCLK multiplier function. This corrupts the CIC interpolating filter, forcing unrecoverable mathematical overflow that can only be resolved by issuing a RESET command. The problem is due to the PLL failing to be locked to the reference clock while nonzero data is being clocked into the interpolation stages from the data inputs. The recommended sequence is to first engage the REFCLK multiplier function (allowing at least 1 ms for loop stabilization) and then engage continuous mode via software.

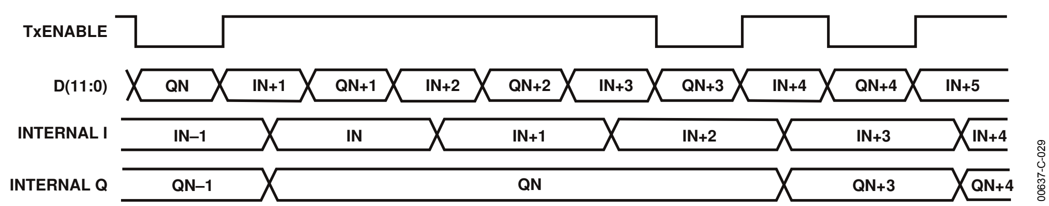

Figure 29. Continuous Mode Input Timing—TxENABLE Static High (for illustrative purposes only)

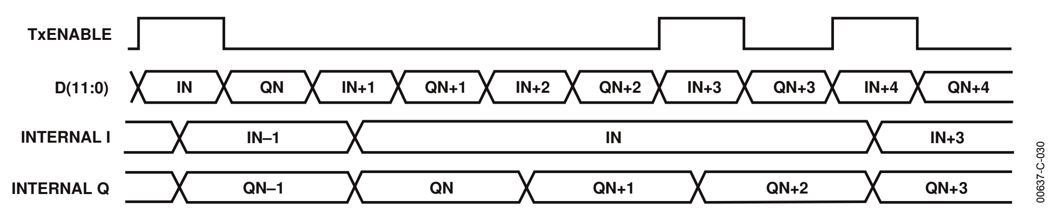

Figure 30. Continuous Mode Input Timing—TxENABLE Static Low (for illustrative purposes only)

HALF-BAND FILTERS (HBFS)

Before presenting a detailed description of the HBFs, recall that the input data stream is representative of complex data; i.e., two input samples are required to produce one I/Q data pair. The I/Q sample rate is one-half the input data rate. The I/Q sample rate (the rate at which I or Q samples are presented to the input of the first half-band filter) is referred to as f_{IQ}. Because the AD9856 is a quadrature modulator, f_{IQ} represents the baseband of the internal I/Q sample pairs. It should be emphasized here that f_{IQ} is not the same as the baseband of the user's symbol rate data, which must be upsampled before presentation to the AD9856 (as is explained later). The I/Q sample rate (f_{IQ}) puts a limit on the minimum bandwidth necessary to transmit the f_{IQ} spectrum. This is the familiar Nyquist limit and is equal to one half f_{IQ}, which is referred to as f_{NYQ}.

HBF 1 is a 47-tap filter that provides a factor-of-two increase in the sampling rate. HBF 2 is a 15-tap filter offering an additional factor-of-two increase in the sampling rate. Together, HBF 1 and HBF 2 provide a factor-of-four increase in the sampling rate ($4 \times f_{IQ}$ or $8 \times f_{NYQ}$). Their combined insertion loss is a mere 0.01 dB, so virtually no loss of signal level occurs through the first two HBFs. HBF 3 is an 11-tap filter and, if selected, increases the sampling rate by an additional factor of two. Thus, the output sample rate of HBF 3 is $8 \times f_{IQ}$ or $16 \times f_{NYQ}$. HBF 3 exhibits 0.03 dB of signal-level loss. As such, the loss in signal level through all three HBFs is only 0.04 dB and may be ignored for all practical purposes.

In relation to phase response, all three HBFs are linear phase filters. As such, virtually no phase distortion is introduced within the pass band of the filters. This is an important feature as phase distortion is generally intolerable in a data transmission system.

In addition to knowledge of the insertion loss and phase response of the HBFs, some knowledge of the frequency response of the HBFs is useful as well. The combined frequency response of HBF 1 and 2 is shown in Figure 31 and Figure 32.

The usable bandwidth of the filter chain puts a limit on the maximum data rate that can be propagated through the device. A look at the pass-band detail of the HBF 1 and HFB 2 response indicates that to maintain an amplitude error of no more than 1 dB, users are restricted to signals having a bandwidth of no more than about 90% of f_{NYQ}. To keep the bandwidth of the data in the flat portion of the filter pass band, users must oversample the baseband data by at least a factor of two prior to presenting it to the AD9856. Without over-sampling, the Nyquist bandwidth of the baseband data corresponds to the f_{NYQ}. As such, the upper end of the data bandwidth suffers 6 dB or more of attenuation due to the frequency response of HBF 1 and HBF 2. Furthermore, if the baseband data applied to the AD9856 has been pulse shaped, there is an additional concern. Typically, pulse shaping is applied to the baseband data via a filter having a raised cosine response. In such cases, an α value is used to modify the bandwidth of the data where the value of α is such that $0 \le \alpha \le 1$. A value of 0 causes the data bandwidth to correspond to the Nyquist bandwidth. A value of 1 causes the data bandwidth to be extended to twice the Nyquist bandwidth. Thus, with 2× oversampling of the baseband data and $\alpha = 1$, the Nyquist bandwidth of the data corresponds with the I/Q Nyquist bandwidth. As stated earlier, this results in problems near the upper edge of the data bandwidth due to the frequency response of HBF 1 and 2.

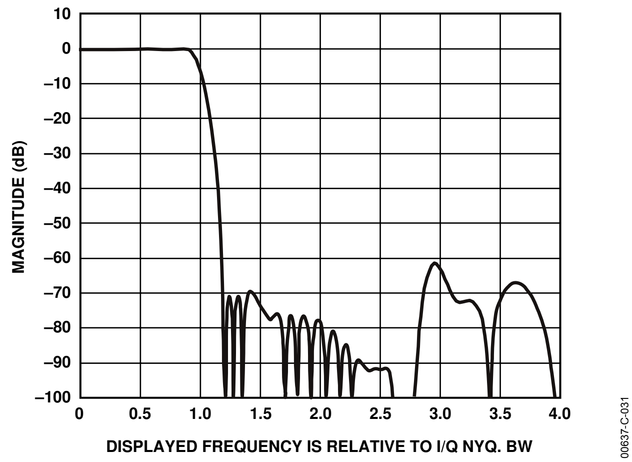

Figure 31. Half-Band 1 and 2 Frequency Response

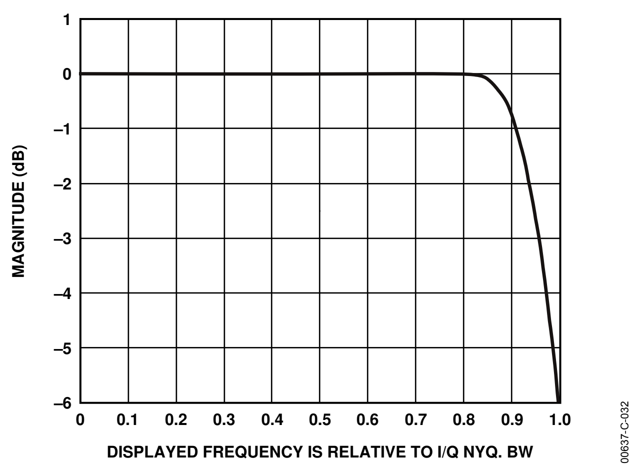

Figure 32. Pass-Band Detail: Combined Frequency Response of HBF 1 and 2

To reiterate, the user must *oversample* the baseband data by at least a *factor of two* (2). In addition, there is a further restriction on pulse shaping—the maximum value of α that can be implemented is 0.8. This is because the data bandwidth becomes $1/2(1 + \alpha)\ f_{NYQ} = 0.9\ f_{NYQ}$, which puts the data bandwidth at the extreme edge of the flat portion of the filter response. If a particular application requires an α value between 0.8 and 1, then the user must *oversample* the baseband data by at least a *factor of four* (4).

In applications requiring both a low data rate and a high output sample rate, a third HBF is available (HBF 3). Selecting HBF 3 offers an upsampling ratio of eight (8) instead of four (4). The combined frequency response of HBF 1, 2, and 3 is shown in Figure 33 and Figure 34. Comparing the pass-band detail of HBF 1 and 2 with the pass-band detail of HBF 1, 2, and 3, HBF 3 has virtually no impact on frequency response from 0 to 1 (where 1 corresponds to f_{NYQ}).

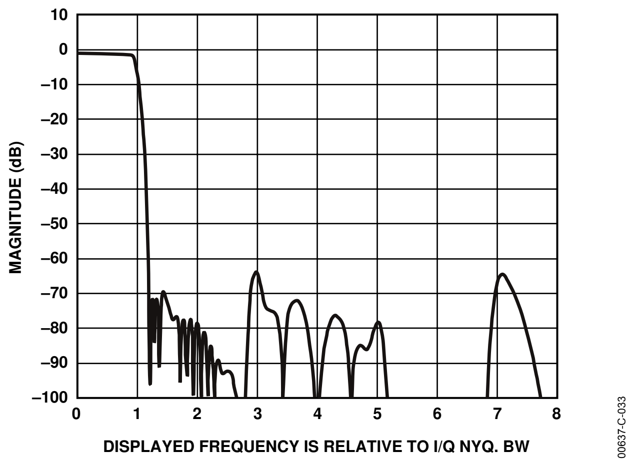

Figure 33. Half-Band 1, 2, and 3 Frequency Response

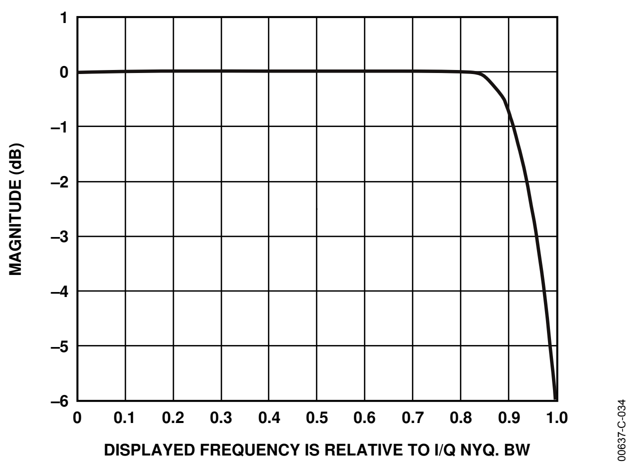

Figure 34. Pass-Band Detail: Combined Frequency Response of HBF 1 to 3

CASCADED INTEGRATOR COMB (CIC) FILTER

A CIC filter is unlike a typical FIR filter in that it offers the flexibility to handle differing input and output sample rates (only in integer ratios, however). In the purest sense, a CIC filter can provide either an increase or a decrease in the sample rate at the output relative to the input, depending on the architecture. If the integration stage precedes the comb stage, the CIC filter provides sample rate reduction (decimation). When the comb stage precedes the integrator stage the CIC filter provides an increase in sample rate (interpolation). In the AD9856, the CIC filter is configured as an interpolator—a programmable interpolator—and provides a sample rate increase, R, such that $2 \le R \le 63$.

In addition to the ability to provide a change in sample rate between input and output, a CIC filter also has an intrinsic low-pass frequency response characteristic. The frequency response of a CIC filter depends on:

- The rate change ratio, *R*.
- The order of the filter, *N*.
- The number of unit delays per stage, *M*.

The system function, H(z), of a CIC filter is given by:

$$H(z) = \left(\frac{1 - z^{-RM}}{1 - z^{-1}} \right)^N = \left(\sum_{\kappa=0}^{RM-1} z^{-\kappa} \right)^N$$

The form on the far right has the advantage of providing a result for z = 1 (corresponding to zero frequency or dc). The alternate form yields an indeterminate form (0/0) for z = 1, but is otherwise identical. The only variable parameter for the AD9856 CIC filter is R. M and N are fixed at 1 and 4, respectively. Thus, the CIC system function for the AD9856 simplifies to:

$$H(z) = \left(\frac{1 - z^{-R}}{1 - z^{-1}} \right)^4 = \left(\sum_{\kappa=0}^{R-1} z^{-\kappa} \right)^4$$

The transfer function is given by:

$$H(f) = \left(\frac{1 - e^{-j(2\pi fR)}}{1 - e^{-j(2\pi f)}} \right)^4 = \left(\sum_{\kappa=0}^{R-1} e^{-j(2\pi f\kappa)} \right)^4$$

The frequency response in this form is such that f is scaled to the output sample rate of the CIC filter. That is, f = 1 corresponds to the frequency of the output sample rate of the CIC filter. H(f/R) yields the frequency response with respect to the input sample of the CIC filter. Figure 35 to Figure 44 show the CIC frequency response and pass-band detail for R = 2 and R = 63, with HBF 3 bypassed. Figure 45 to Figure 50 are similar, but HBF 3 is selected. Note the flatter pass-band response when HBF 3 is employed.

As with HBFs, consideration must be given to the frequency-dependent attenuation that the CIC filter introduces over the frequency range of the data to be transmitted. Note that the CIC frequency response figures have f_{NYQ} as their reference frequency; i.e., unity (1) on the frequency scale corresponds to f_{NYQ}. If the incoming data that is applied to the AD9856 is oversampled by a factor of 2 (as required), then the Nyquist bandwidth of the applied data is one-half f_{NYQ} on the CIC frequency response figures. A look at the 0.5 point on the pass-band detail figures reveals a worst-case attenuation of about 0.25 dB (HBF 3 bypassed, R = 63). This, of course, assumes pulse-shaped data with α = 0 (minimum bandwidth scenario). When a value of α = 1 is used, the bandwidth of the data corresponds to f_{NYQ} (the point1.0 on the CIC frequency scale). Thus, the worst-case attenuation for α = 1 is about 0.9 dB.

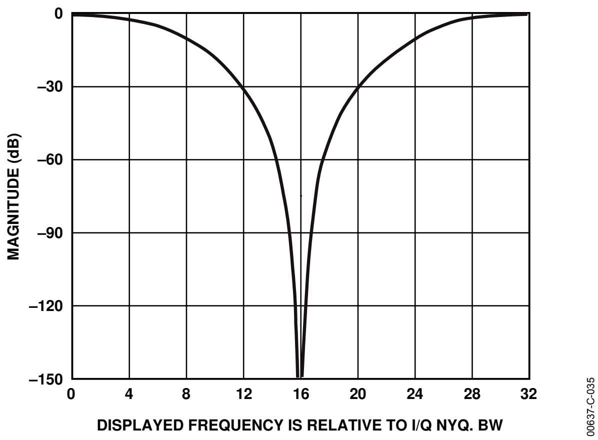

Figure 35. CIC Filter Frequency Response (R = 2, HFB 3 Bypassed)

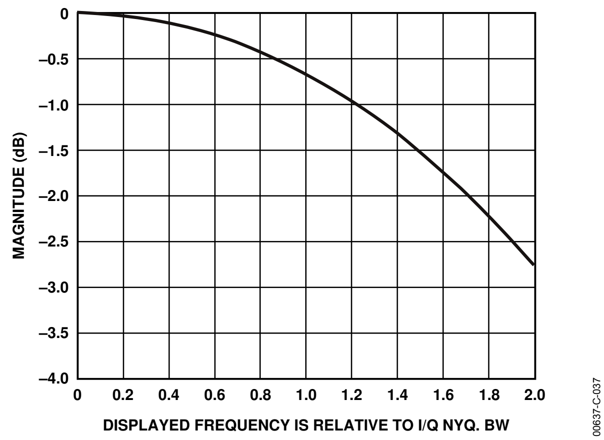

Figure 36. Pass-Band Detail (R = 2, HFB 3 Bypassed)

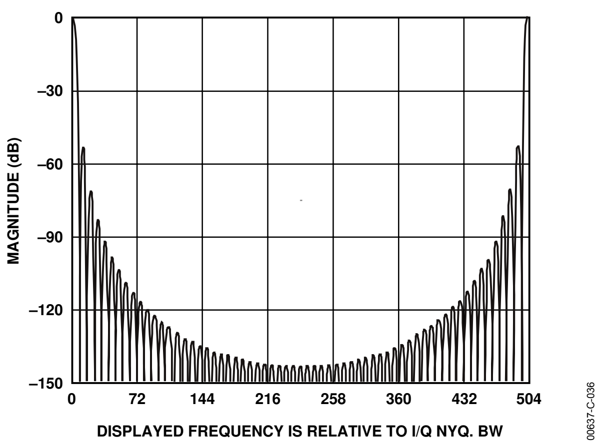

Figure 37. CIC Filter Frequency Response (R = 63, HFB 3 Bypassed)

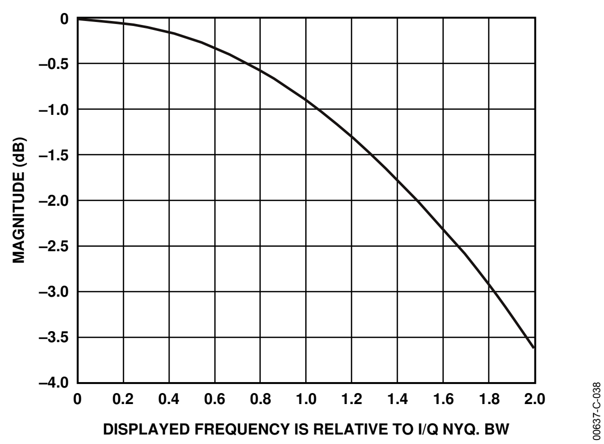

Figure 38. Pass-Band Detail (R = 63, HFB 3 Bypassed)

The degree of the impact of the attenuation introduced by the CIC filter over the Nyquist bandwidth of the data is application specific. The user must decide how much attenuation is acceptable. If less attenuation is desired, then additional oversampling of the baseband data must be employed. Alternatively, the user can precompensate the baseband data before presenting it to the AD9856. That is, if the data is precompensated through a filter that has a frequency response characteristic, which is the inverse of the CIC filter response, then the overall system response can be nearly perfectly flattened over the bandwidth of the data.

Another issue to consider with the CIC filters is insertion loss. Unfortunately, CIC insertion loss is not fixed, but is a function of R, M, and N. Because M, and N are fixed for the AD9856, the CIC insertion loss is a function of R only.

Interpolation rates that are an integer power-of-2 result in no insertion loss. However, all noninteger power-of-2 interpolation rates result in a specific amount of insertion loss.

To help overcome the insertion loss problem, the AD9856 provides the user a means to boost the gain through the CIC stage by a factor of 2 (via the CIC Gain bit—see the Serial Control Bus Register section). The reason for this feature is to allow the user to take advantage of the full dynamic range of the DAC, thus maximizing the signal-to-noise ratio (SNR) at the output of the DAC stage. It is best to operate the DAC over its full-scale range in order to minimize the inherent quantization effects associated with a DAC. Any significant loss through the CIC stage is reflected at the DAC output as a reduction in SNR. The degradation in SNR can be overcome by boosting the CIC output level. Table 6 tabulates insertion loss as a function of R. The values are provided in linear and decibel form, both with and without the factor-of-2 gain employed.

A word of caution: When the CIC Gain bit is active, ensure that the data supplied to the AD9856 is scaled down to yield an overall gain of unity (1) through the CIC filter stage. Gains in excess of unity are likely to cause overflow errors in the data path, compromising the validity of the analog output signal.

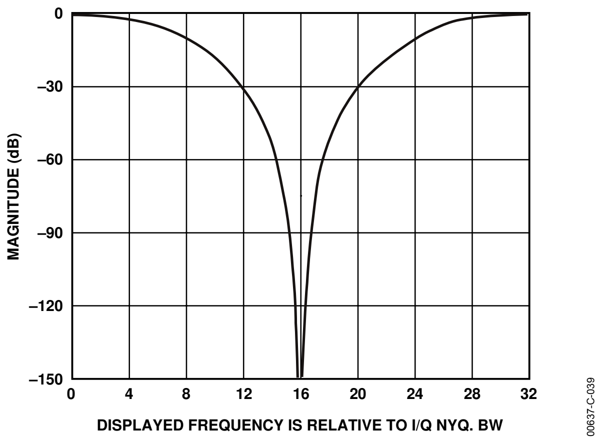

Figure 39. CIC Filter Frequency Response (R = 2, HBF 3 Selected)

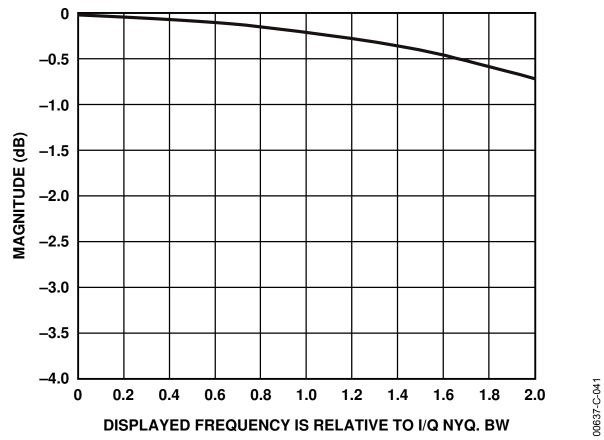

Figure 40. Pass-Band Detail (R = 2, HBF 3 Selected)

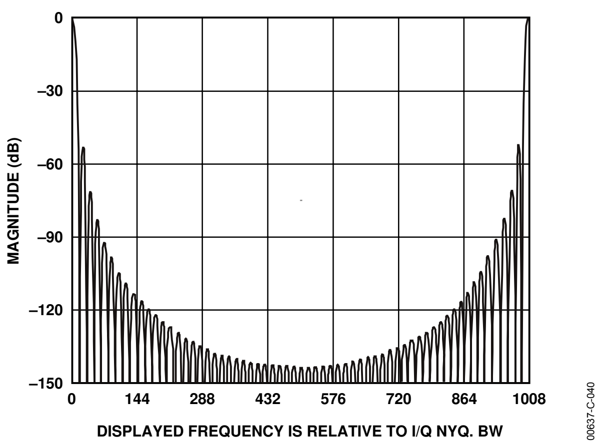

Figure 41. CIC Filter Frequency Response (R = 63, HBF 3 Active)

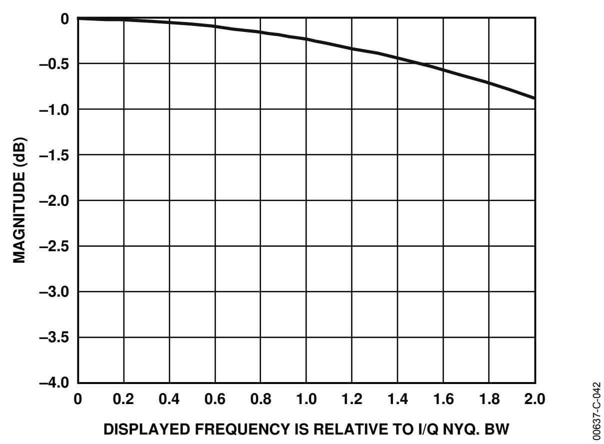

Figure 42. Pass-Band Detail (R = 63, HBF 3 Active)

DIGITAL QUADRATURE MODULATOR

Following the CIC filter stage the I and Q data (which have been processed independently up to this point) are mixed in the modulator stage to produce a digital modulated carrier. The carrier frequency is selected by programming the direct digital synthesizer (see the Direct Digital Synthesizer Function section) with the appropriate 32-bit tuning word via the AD9856 control registers. The DDS simultaneously generates a digital (sampled) sine and cosine wave at the programmed carrier frequency. The digital sine and cosine data is multiplied by the Q and I data, respectively, to create the quadrature components of the original data upconverted to the carrier frequency. The quadrature components are digitally summed and passed on to the subsequent stages.

The key point is that the modulation is done digitally, which eliminates the phase and gain imbalance and crosstalk issues typically associated with analog modulators. Note that the modulated signal is actually a number stream sampled at the rate of SYSCLK, which is the same rate at which the DAC is clocked (see Figure 23).

Note that the architecture of the quadrature modulator results in a 3 dB loss of signal level. To visualize this, assume that both the I data and Q data are fixed at the maximum possible digital value, x. Then the output of the modulator, y, is:

$$y = x \times \cos(\omega) + x \times \sin(\omega) = x \times [\cos(\omega) + \sin(\omega)]$$

From this equation, y assumes a maximum value of $x\sqrt{2}$ (a gain of 3 dB). However, if the same number of bits were used to represent the y values, as is used to represent the x values, an overflow would occur. To prevent this, an effective divide-by-two is implemented on the y values, which reduces the maximum value of y by a factor of two. Because division by two results in a 6 dB loss, the modulator yields an overall loss of 3 dB (3 dB – 6 dB = –3 dB, or 3 dB of loss).

Table 6. CIC Interpolation Filter Insertion Loss Table

Interpolation Rate	Default Gain		2 × Gain	
	(Linear)	(dB)	(Linear)	(dB)
2	1.0000	0.000	2.0000	6.021
3	0.8438	−1.476	1.6875	4.545
4	1.0000	0.000	2.0000	6.021
5	0.9766	−0.206	1.9531	5.815
6	0.8438	−1.476	1.6875	4.545
7	0.6699	−3.480	1.3398	2.541
8	1.0000	0.000	2.0000	6.021
9	0.7119	−2.951	1.4238	3.069
10	0.9766	−0.206	1.9531	5.815
11	0.6499	−3.743	1.2998	2.278
12	0.8438	−1.476	1.6875	4.545
13	0.5364	−5.411	1.0728	0.610
14	0.6699	−3.480	1.3398	2.541
15	0.8240	−1.682	1.6479	4.339
16	1.0000	0.000	2.0000	6.021
17	0.5997	−4.441	1.1995	1.580
18	0.7119	−2.951	1.4238	3.069
19	0.8373	−1.543	1.6746	4.478
20	0.9766	−0.206	1.9531	5.815
21	0.5652	−4.955	1.1305	1.065
22	0.6499	−3.743	1.2998	2.278
23	0.7426	−2.585	1.4852	3.436
24	0.8438	−1.476	1.6875	4.545
25	0.9537	−0.412	1.9073	5.609
26	0.5364	−5.411	1.0728	0.610
27	0.6007	−4.427	1.2014	1.593
28	0.6699	−3.480	1.3398	2.541
29	0.7443	−2.565	1.4886	3.455
30	0.8240	−1.682	1.6479	4.339
31	0.9091	−0.827	1.8183	5.193
32	1.0000	0.000	2.0000	6.021
33	0.5484	−5.219	1.0967	0.802
34	0.5997	−4.441	1.1995	1.580
35	0.6542	−3.686	1.3084	2.335
36	0.7119	−2.951	1.4238	3.069
37	0.7729	−2.237	1.5458	3.783
38	0.8373	−1.543	1.6746	4.478
39	0.9051	−0.866	1.8103	5.155
40	0.9766	−0.206	1.9531	5.815
41	0.5258	−5.583	1.0517	0.437
42	0.5652	−4.955	1.1305	1.065
43	0.6066	−4.342	1.2132	1.679
44	0.6499	−3.743	1.2998	2.278
45	0.6952	−3.157	1.3905	2.863
46	0.7426	−2.585	1.4852	3.436
47	0.7921	−2.024	1.5842	3.996
48	0.8438	−1.476	1.6875	4.545
49	0.8976	−0.938	1.7952	5.082
50	0.9537	−0.412	1.9073	5.609
51	0.5060	−5.917	1.0120	0.104
52	0.5364	−5.411	1.0728	0.610
53	0.5679	−4.914	1.1358	1.106
54	0.6007	−4.427	1.2014	1.593
55	0.6347	−3.949	1.2693	2.072
56	0.6699	−3.480	1.3398	2.541
57	0.7065	−3.018	1.4129	3.002
58	0.7443	−2.565	1.4886	3.455
59	0.7835	−2.120	1.5669	3.901
60	0.8240	−1.682	1.6479	4.339
61	0.8659	−1.251	1.7317	4.770
62	0.9091	−0.827	1.8183	5.193
63	0.9539	−0.410	1.9077	5.610

INVERSE SINC FILTER (ISF)

The AD9856 is almost entirely a digital device. The input signal is made up of a time series of digital data-words. These data-words propagate through the device as numbers. Ultimately, this number stream must be converted to an analog signal. To this end, the AD9856 incorporates an integrated DAC. The output waveform of the DAC is the familiar staircase pattern typical of a signal that is sampled and quantized. The staircase pattern is a result of the finite time that the DAC holds a quantized level until the next sampling instant. This is known as a zero-order hold function. The spectrum of the zero-order hold function is the SIN(x)/x, or SINC, envelope.

The series of digital data-words presented at the input of the DAC represent an impulse stream. It is the spectrum of this impulse stream, which is the desired output signal. Due to the zero-order hold effect of the DAC, however, the output spectrum is the product of the zero-order hold spectrum (the SINC envelope) and the Fourier transform of the impulse stream. Thus, there is an intrinsic distortion in the output spectrum, which follows the SINC response.

The SINC response is deterministic and totally predictable. Thus, it is possible to predistort the input data stream in a manner that compensates for the SINC envelope distortion. This can be accomplished by means of an ISF. The ISF incorporated on the AD9856 is a 17-tap, linear phase FIR filter. Its frequency response characteristic is the inverse of the SINC envelope. Data sent through the ISF is altered to correct for the SINC envelope distortion.

Note, however, that the ISF is sampled at the same rate as the DAC. Thus, the effective range of the SINC envelope compensation only extends to the Nyquist frequency (1/2 of the DAC sample rate).