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# CMOS 200 MSPS 14-Bit Quadrature Digital Upconverter

# AD9857

## FEATURES

- 200 MHz internal clock rate
- 14-bit data path
- Excellent dynamic performance:
  - 80 dB SFDR @ 65 MHz (±100 kHz) $A_{OUT}$
- 4× to 20× programmable reference clock multiplier
- Reference clock multiplier PLL lock detect indicator
- Internal 32-bit quadrature DDS
- FSK capability
- 8-bit output amplitude control
- Single-pin power-down function
- Four programmable, pin-selectable signal profiles
- SIN(x)/x correction (inverse SINC function)
- Simplified control interface
  - 10 MHz serial, 2-wire or 3-wire SPI®-compatible
- 3.3 V single supply
- Single-ended or differential input reference clock
- 80-lead LQFP surface-mount packaging
- Three modes of operation:
  - Quadrature modulator mode
  - Single-tone mode
  - Interpolating DAC mode

## APPLICATIONS

- HFC data, telephony, and video modems
- Wireless base station
- Agile, LO frequency synthesis
- Broadband communications

## FUNCTIONAL BLOCK DIAGRAM

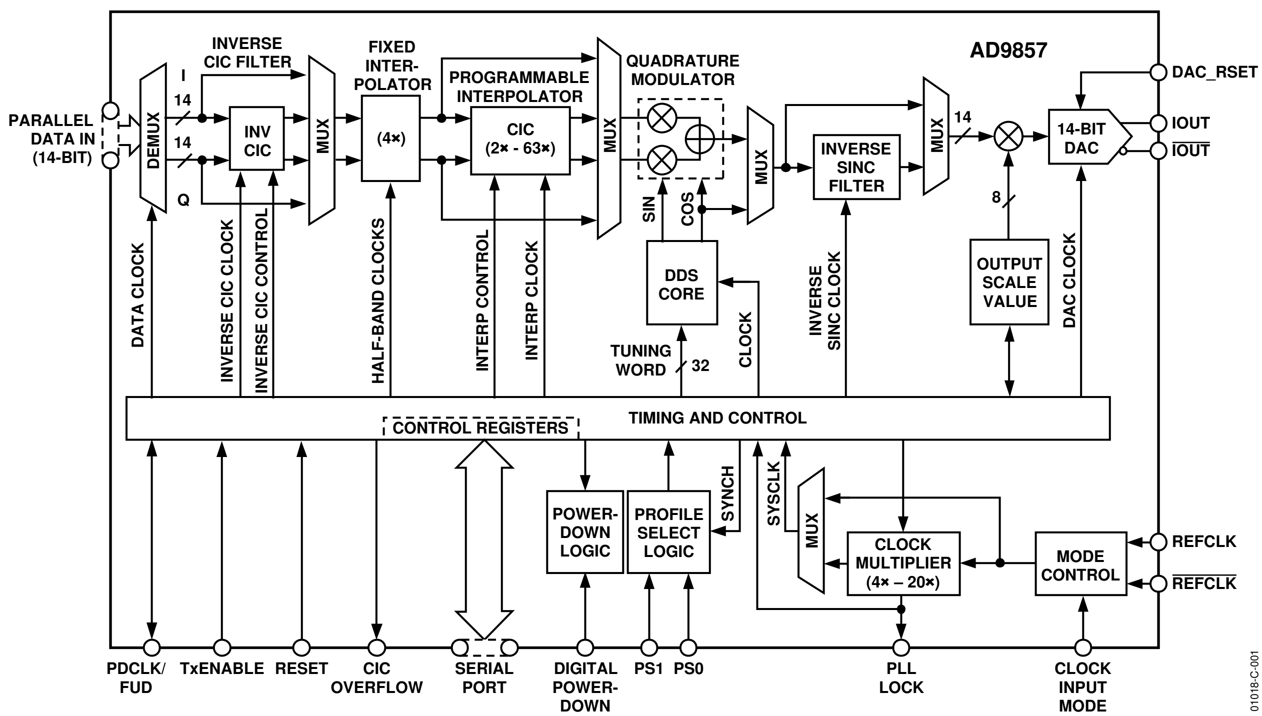


*Figure 1.*

**Rev. C**



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# AD9857* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- AD9857 Evaluation Board

## DOCUMENTATION

**Application Notes**

- AN-0996: The Advantages of Using a Quadrature Digital Upconverter (QDUC) in Point-to-Point Microwave Transmit Systems
- AN-237: Choosing DACs for Direct Digital Synthesis
- AN-823: Direct Digital Synthesizers in Clocking Applications Time
- AN-837: DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design
- AN-922: Digital Pulse-Shaping Filter Basics
- AN-924: Digital Quadrature Modulator Gain

**Data Sheet**

- AD9857: CMOS 200 MSPS 14-Bit Quadrature Digital Upconverter Data Sheet

**Product Highlight**

- Introducing Digital Up/Down Converters: VersaCOMM™ Reconfigurable Digital Converters

**Technical Books**

- A Technical Tutorial on Digital Signal Synthesis, 1999

## TOOLS AND SIMULATIONS

- AD9857 IBIS Models

## REFERENCE MATERIALS

**Technical Articles**

- Basics of Designing a Digital Radio Receiver (Radio 101)
- DDS Simplifies Polar Modulation
- Digital Up/Down Converters: VersaCOMM™ White Paper
- Digital Upconverter IC Tames Complex Modulation
- Improved DDS Devices Enable Advanced Comm Systems
- Speedy A/Ds Demand Stable Clocks
- The Year of the Waveform Generator

## DESIGN RESOURCES

- AD9857 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all AD9857 EngineerZone Discussions.

## SAMPLE AND BUY

Visit the product page to see pricing options.

## TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

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## REVISION HISTORY

**5/04—Data Sheet Changed from Rev. B to Rev. C**



**4/02—Changed from Rev. A to Rev. B**

# GENERAL DESCRIPTION

The AD9857 integrates a high speed direct digital synthesizer (DDS), a high performance, high speed, 14-bit digital-to-analog converter (DAC), clock multiplier circuitry, digital filters, and other DSP functions onto a single chip, to form a complete quadrature digital upconverter device. The AD9857 is intended to function as a universal I/Q modulator and agile upconverter, single-tone DDS, or interpolating DAC for communications applications, where cost, size, power dissipation, and dynamic performance are critical attributes.

The AD9857 offers enhanced performance over the industry-standard AD9856, as well as providing additional features.

The AD9857 is available in a space-saving, surface-mount package and is specified to operate over the extended industrial temperature range of −40°C to +85°C.

# SPECIFICATIONS

$V_S$ = 3.3 V ± 5%, $R_{SET}$ = 1.96 kΩ, external reference clock frequency = 10 MHz with REFCLK multiplier enabled at 20×.

**Table 1.**

| Parameter | Temp | Test Level | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| REF CLOCK INPUT CHARACTERISTICS | | | | | | |
| Frequency Range | | | | | | |
| REFCLK Multiplier Disabled | Full | VI | 1 | | 200 | MHz |
| REFCLK Multiplier Enabled at 4× | Full | VI | 1 | | 50 | MHz |
| REFCLK Multiplier Enabled at 20× | Full | VI | 1 | | 10 | MHz |
| Input Capacitance | 25°C | V | | 3 | | pF |
| Input Impedance | 25°C | V | | 100 | | MΩ |
| Duty Cycle | 25°C | V | | 50 | | % |
| Duty Cycle with REFCLK Multiplier Enabled | 25°C | V | 35 | | 65 | % |
| Differential Input (VDD/2) ±200 mV | 25°C | V | 1.45 | | 1.85 | V |
| DAC OUTPUT CHARACTERISTICS | | | | | | |
| Resolution | | | | 14 | | Bits |
| Full-Scale Output Current | | | 5 | 10 | 20 | mA |
| Gain Error | 25°C | I | 8.5 | | 0 | % FS |
| Output Offset | 25°C | I | | | 2 | μA |
| Differential Nonlinearity | 25°C | V | | 1.6 | | LSB |
| Integral Nonlinearity | 25°C | V | | 2 | | LSB |
| Output Capacitance | 25°C | V | | 5 | | pF |
| Residual Phase Noise @ 1 kHz Offset, 40 MHz $A_{OUT}$ | | | | | | |
| REFCLK Multiplier Enabled at 20× | 25°C | V | | −107 | | dBc/Hz |
| REFCLK Multiplier at 4× | 25°C | V | | −123 | | dBc/Hz |
| REFCLK Multiplier Disabled | 25°C | V | | −145 | | dBc/Hz |
| Voltage Compliance Range | 25°C | I | −0.5 | | +1.0 | V |
| Wideband SFDR | | | | | | |
| 1 MHz to 20 MHz Analog Out | 25°C | V | | −75 | | dBc |
| 20 MHz to 40 MHz Analog Out | 25°C | V | | −65 | | dBc |
| 40 MHz to 60 MHz Analog Out | 25°C | V | | −62 | | dBc |
| 60 MHz to 80 MHz Analog Out | 25°C | V | | −60 | | dBc |
| Narrowband SFDR | | | | | | |
| 10 MHz Analog Out (±1 MHz) | 25°C | V | | −87 | | dBc |
| 10 MHz Analog Out (±250 kHz) | 25°C | V | | −88 | | dBc |
| 10 MHz Analog Out (±50 kHz) | 25°C | V | | −92 | | dBc |
| 10 MHz Analog Out (±10 kHz) | 25°C | V | | −94 | | dBc |
| 65 MHz Analog Out (±1 MHz) | 25°C | V | | −86 | | dBc |
| 65 MHz Analog Out (±250 kHz) | 25°C | V | | −86 | | dBc |
| 65 MHz Analog Out (±50 kHz) | 25°C | V | | −86 | | dBc |
| 65 MHz Analog Out (±10 kHz) | 25°C | V | | −88 | | dBc |
| 80 MHz Analog Out (±1 MHz) | 25°C | V | | −85 | | dBc |
| 80 MHz Analog Out (±250 kHz) | 25°C | V | | −85 | | dBc |
| 80 MHz Analog Out (±50 kHz) | 25°C | V | | −85 | | dBc |
| 80 MHz Analog Out (±0 kHz) | 25°C | V | | −86 | | dBc |

| Parameter | Temp | Test Level | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| MODULATOR CHARACTERISTICS (65 MHz $A_{OUT}$) | | | | | | |
| (Input data: 2.5 MS/s, QPSK, 4× oversampled, inverse SINC filter ON, inverse CIC ON) | | | | | | |
| I/Q Offset | 25°C | IV | 55 | 65 | | dB |
| Error Vector Magnitude | 25°C | IV | | 0.4 | 1 | % |
| INVERSE SINC FILTER (variation in gain from DC to 80 MHz, inverse SINC filter ON) | 25°C | V | | ±0.1 | | dB |
| SPURIOUS POWER (off channel, measured in equivalent bandwidth), Full-Scale Output | | | | | | |
| 6.4 MHz Bandwidth | 25°C | IV | | −65 | | dBc |
| 3.2 MHz Bandwidth | 25°C | IV | | −67 | | dBc |
| 1.6 MHz Bandwidth | 25°C | IV | | −69 | | dBc |
| 0.8 MHz Bandwidth | 25°C | IV | | −69 | | dBc |
| 0.4 MHz Bandwidth | 25°C | IV | | −70 | | dBc |
| 0.2 MHz Bandwidth | 25°C | IV | | −72 | | dBc |
| SPURIOUS POWER (Off channel, measured in equivalent bandwidth), Output Attenuated 18 dB | | | | | | |
| Relative to Full Scale | | | | | | |
| 6.4 MHz Bandwidth | 25°C | IV | | −51 | | dBc |
| 3.2 MHz Bandwidth | 25°C | IV | | −54 | | dBc |
| 1.6 MHz Bandwidth | 25°C | IV | | −56 | | dBc |
| 0.8 MHz Bandwidth | 25°C | IV | | −59 | | dBc |
| 0.4 MHz Bandwidth | 25°C | IV | | −62 | | dBc |
| 0.2 MHz Bandwidth | 25°C | IV | | −63 | | dBc |
| TIMING CHARACTERISTICS | | | | | | |
| Serial Control Bus | | | | | | |
| Maximum Frequency | 25°C | I | | | 10 | MHz |
| Minimum Clock Pulse Width Low ($t_{PWL}$) | 25°C | I | 30 | | | ns |
| Minimum Clock Pulse Width High ($t_{PWH}$) | 25°C | I | 30 | | | ns |
| Maximum Clock Rise/Fall Time | 25°C | I | | | 1 | ms |
| Minimum Data Setup Time ($t_{DS}$) | 25°C | I | 30 | | | ns |
| Minimum Data Hold Time ($t_{DH}$) | 25°C | I | 0 | | | ns |
| Maximum Data Valid Time ($t_{DV}$) | 25°C | I | 35 | | | ns |
| Wake-Up Time[1] | 25°C | I | | 1 | | ms |
| Minimum RESET Pulse Width High ($t_{RH}$) | 25°C | I | 5 | | | SYSCLK[2]2Cycles |
| Minimum $\overline{CS}$ Setup Time | 25°C | I | 40 | | | ns |
| CMOS LOGIC INPUTS | | | | | | |
| Logic 1 Voltage | 25°C | IV | 2.0 | | | V |
| Logic 0 Voltage | 25°C | IV | | | 0.8 | V |
| Logic 1 Current | 25°C | I | | | 5 | μA |
| Logic 0 Current | 25°C | I | | | 5 | μA |
| Input Capacitance | 25°C | V | | 3 | | pF |
| CMOS LOGIC OUTPUTS (1 mA LOAD) | | | | | | |
| Logic 1 Voltage | 25°C | I | 2.7 | | | V |
| Logic 0 Voltage | 25°C | I | | | 0.4 | V |

| Parameter | Temp | Test Level | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| POWER SUPPLY $V_S$ CURRENT[3] (all power specifications at $V_{DD}$ = 3.3 V, 25°C, REFCLK = 200 MHz) | | | | | | |
| Full Operating Conditions | 25°C | I | | 540 | 615 | mA |
| 160 MHz Clock (×16) | 25°C | I | | 445 | 515 | mA |
| 120 MHz Clock (×12) | 25°C | I | | 345 | 400 | mA |
| Burst Operation (25%) | 25°C | I | | 395 | 450 | mA |
| Single-Tone Mode | 25°C | I | | 265 | 310 | mA |
| Power-Down Mode | 25°C | I | | 71 | 80 | mA |
| Full-Sleep Mode | 25°C | I | | 8 | 13.5 | mA |

[1] Wake-up time refers to recovery from full-sleep mode. The longest time required is for the reference clock multiplier PLL to lock up (if it is being used). The wake-up time assumes that there is no capacitor on DAC_BP, and that the recommended PLL loop filter values are used. The state of the reference clock multiplier lock can be determined by observing the signal on the PLL_LOCK pin.

[2] SYSCLK refers to the actual clock frequency used on-chip by the AD9857. If the reference clock multiplier is used to multiply the external reference frequency, the SYSCLK frequency is the external frequency multiplied by the reference clock multiplier multiplication factor. If the reference clock multiplier is not used, the SYSCLK frequency is the same as the external REFCLK frequency.

[3] CIC = 2, INV SINC ON, FTW = 40%, PLL OFF, auto power-down between burst On, TxENABLE duty cycle = 25%.

# ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 2.**

| Parameter | Rating |
|---|---|
| Maximum Junction Temperature | 150°C |
| $V_S$ | 4 V |
| Digital Input Voltage | −0.7 V to $+V_S$ |
| Digital Output Current | 5 mA |
| Storage Temperature | −65°C to +150°C |
| Operating Temperature | −40°C to +85°C |
| Lead Temperature (Soldering 10 s) | 300°C |
| $\theta_{JA}$ | 35°C/W |
| $\theta_{JC}$ | 16°C/W |

## EXPLANATION OF TEST LEVELS

**Table 3.**

| Test | Level |
|---|---|
| 1 | 100% production tested. |
| 2 | 100% production tested at 25°C and sample tested at specific temperatures. |
| 3 | Sample tested only. |
| 4 | Parameter is guaranteed by design and characterization testing. |
| 5 | Parameter is a typical value only. |
| 6 | Devices are 100% production tested at 25°C and guaranteed by design and characterization testing for industrial operating temperature range. |

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

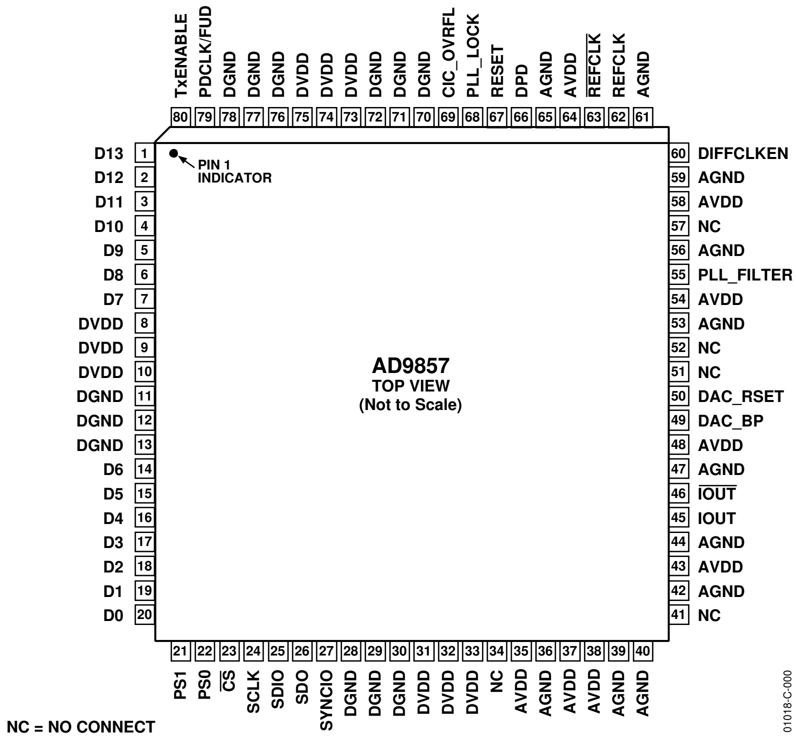



*Figure 2. Pin Configuration*

**Table 4. Pin Function Descriptions**

| Pin Number | Mnemonic | I/O | Function |
|---|---|---|---|
| 20–14, 7–1 | D0–D6, D7–D13 | I | 14-Bit Parallel Data Bus for I and Q Data. The required numeric format is twos complement with D13 as the sign bit and D12–D0 as the magnitude bits. Alternating 14-bit words are demultiplexed onto the I and Q data pathways (except when operating in the interpolating DAC mode, in which case every word is routed onto the I data path). When the TxENABLE pin is asserted high, the next accepted word is presumed to be I data, the next Q data, and so forth. |
| 8–10, 31–33, 73–75 | DVDD | | 3.3 V Digital Power pin(s). |
| 11–13, 28–30, 70–72, 76–78 | DGND | | Digital Ground pin(s). |
| 21 | PS1 | I | Profile Select Pin 1. The LSB of the two profile select pins. In conjunction with PS0, selects one of four profile configurations. |
| 22 | PS0 | I | Profile Select Pin 0. The MSB of the two profile select pins. In conjunction with P1, selects one of four profile configurations. |
| 23 | $\overline{\text{CS}}$ | I | Serial Port Chip Select pin. An active low signal that allows multiple devices to operate on a single serial bus. |
| 24 | SCLK | I | Serial Port Data Clock pin. The serial data CLOCK for the serial port. |
| 25 | SDIO | I/O | Serial Port Input/Output Data pin. Bidirectional serial DATA pin for the serial port. This pin can be programmed to operate as a serial *input only* pin, via the control register bit 00h<7>. The default state is bidirectional. |
| 26 | SDO | O | Serial Port Output Data pin. This pin serves as the serial data output pin when the SDIO pin is configured for serial input only mode. The default state is three-state. |
| 27 | SYNCIO | I | Serial Port Synchronization pin. Synchronizes the serial port without affecting the programmable register contents. This is an active high input that aborts the current serial communication cycle. |
| 34, 41, 51, 52, 57 | NC | | No connect. |

| Pin Number | Mnemonic | I/O | Function |
|---|---|---|---|
| 35, 37, 38, 43, 48, 54, 58, 64 | AVDD | | 3.3 V Analog Power pin(s). |
| 36, 39, 40, 42, 44, 47, 53, 56, 59, 61, 65 | AGND | | Analog Ground pin(s). |
| 45 | IOUT | O | DAC Output pin. Normal DAC output current (analog). |
| 46 | $\overline{\text{IOUT}}$ | O | DAC Complementary Output pin. Complementary DAC output current (analog). |
| 49 | DAC_BP | | DAC Reference Bypass. Typically not used. |
| 50 | DAC_RSET | I | DAC Current Set pin. Sets DAC reference current. |
| 55 | PLL_FILTER | O | PLL Filter. R-C network for PLL filter. |
| 60 | DIFFCLKEN | I | Clock Mode Select pin. A logic high on this pin selects DIFFERENTIAL REFCLK input mode. A logic low selects the SINGLE-ENDED REFCLK input mode. |
| 62 | REFCLK | I | Reference Clock pin. In single-ended clock mode, this pin is the Reference Clock input. In differential clock mode, this pin is the positive clock input. |
| 63 | $\overline{\text{REFCLK}}$ | I | Inverted Reference Clock pin. In differential clock mode, this pin is the negative clock input. |
| 66 | DPD | I | Digital Power-Down pin. Assertion of this pin shuts down the digital sections of the device to conserve power. However, if selected, the PLL remains operational. |
| 67 | RESET | I | Hardware RESET pin. An active high input that forces the device into a predefined state. |
| 68 | PLL_LOCK | O | PLL Lock pin. Active high output signifying, in real time, when PLL is in lock state. |
| 69 | CIC_OVRFL | O | CIC Overflow pin. Activity on this pin indicates that the CIC Filters are in “overflow” state. This pin is typically low unless a CIC overflow occurs. |
| 79 | PDCLK/FUD | I/O | Parallel Data Clock/Frequency Update pin. When not in single-tone mode, this pin is an output signal that should be used as a clock to synchronize the acceptance of the 14-bit parallel data-words on Pins D13–D0. In single-tone mode, this pin is an input signal that synchronizes the transfer of a changed frequency tuning word (FTW) in the active profile (PSx) to the accumulator (FUD = frequency update signal). When profiles are changed by means of the PS–PS1 pins, the FUD does not have to be asserted to make the FTW active. |
| 80 | TxENABLE | I | When TxENABLE is asserted, the device processes the data through the I and Q data pathways; otherwise 0s are internally substituted for the I and Q data entering the signal path. The first data word accepted when the TxENABLE is asserted high is treated as I data, the next data word is Q data, and so forth. |

# TYPICAL PERFORMANCE CHARACTERISTICS

## MODULATED OUTPUT SPECTRAL PLOTS

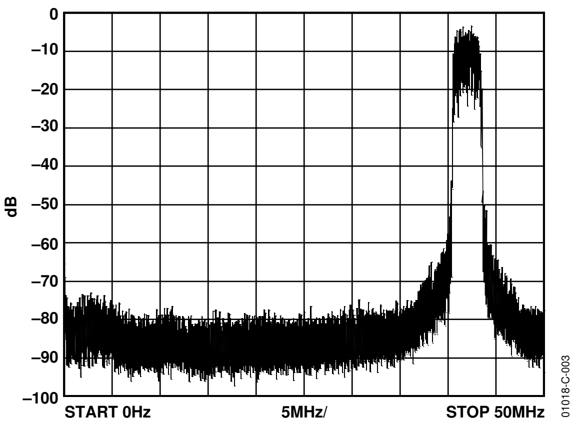



*Figure 3. QPSK at 42 MHz and 2.56 MS/s; 10.24 MHz External Clock with REFCLK Multiplier = 12, CIC Interpolation Rate = 3, 4× Oversampled Data*

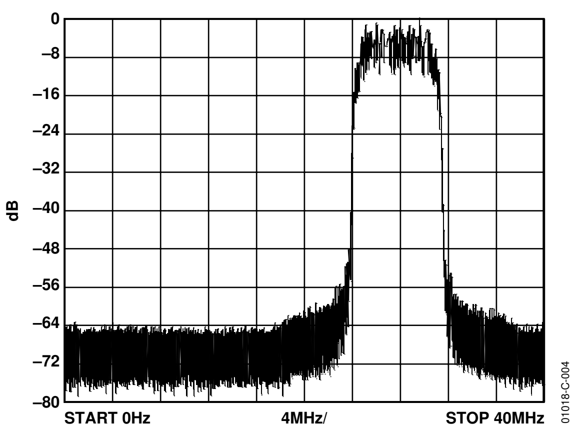



*Figure 4. 64-QAM at 28 MHz and 6 MS/s; 36 MHz External Clock with REFCLK Multiplier = 4, CIC Interpolation Rate = 2, 3× Oversampled Data*

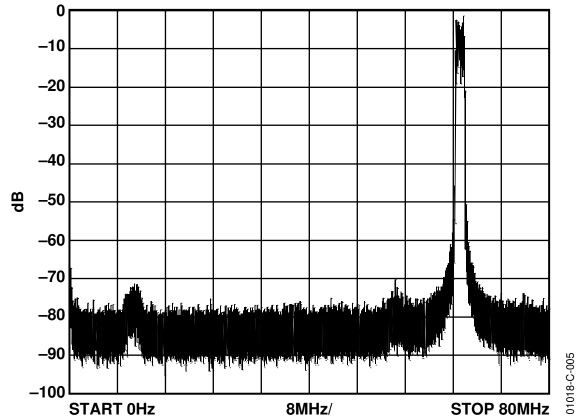



*Figure 5. 16-QAM at 65 MHz and 1.28 MS/s; 10.24 MHz External Clock with REFCLK Multiplier = 18, CIC Interpolation Rate = 9, 4× Oversampled Data*

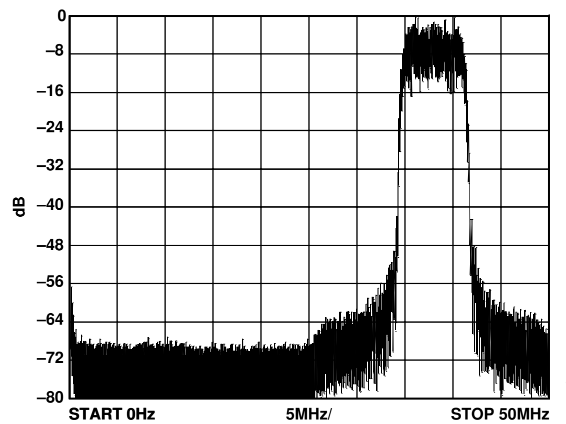



*Figure 6. 256-QAM at 38 MHz and 6 MS/s; 48 MHz External Clock with REFCLK Multiplier = 4, CIC Interpolation Rate = 2, 4× Oversampled Data*

## SINGLE-TONE OUTPUT SPECTRAL PLOTS

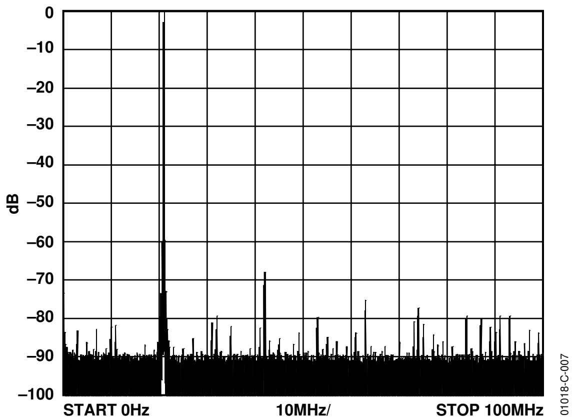



*Figure 7. 21 MHz Single-Tone Output*

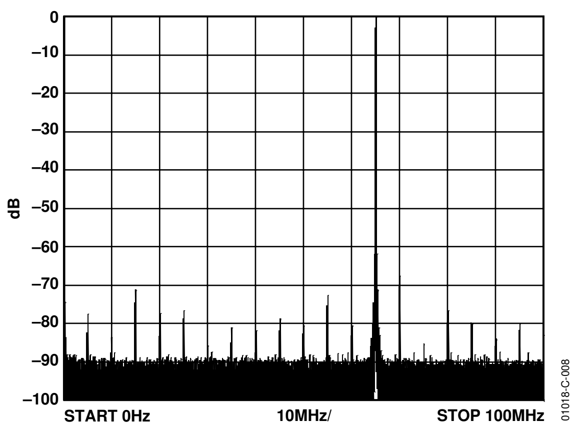



*Figure 8. 65 MHz Single-Tone Output*

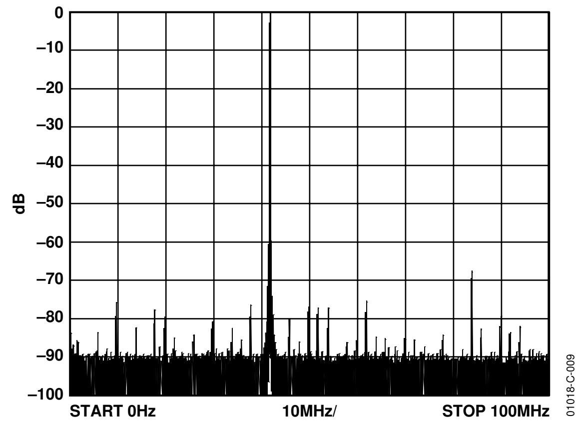



*Figure 9. 42 MHz Single-Tone Output*

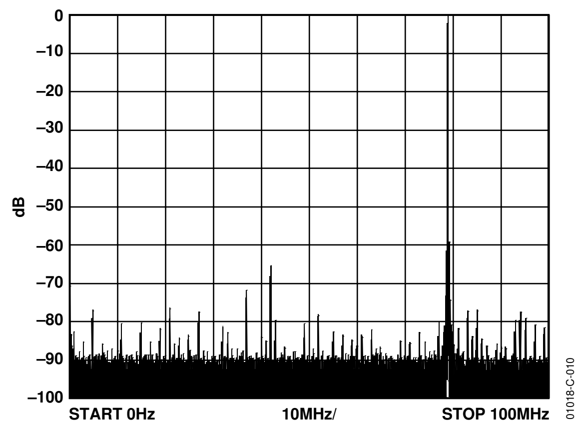



*Figure 10. 79 MHz Single-Tone Output*

## NARROW-BAND SFDR SPECTRAL PLOTS

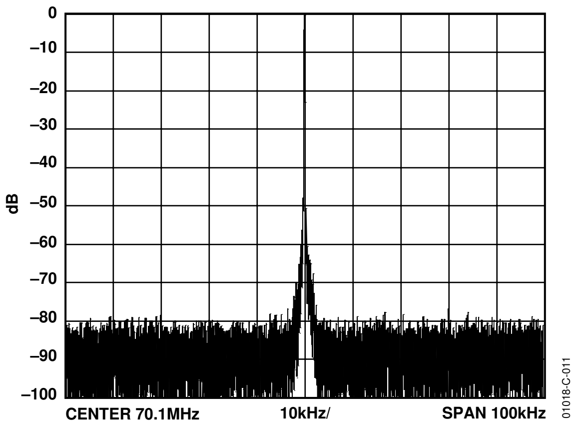



*Figure 11. 70.1 MHz Narrow-Band SFDR, 10 MHz External Clock with REFCLK Multiplier = 20*

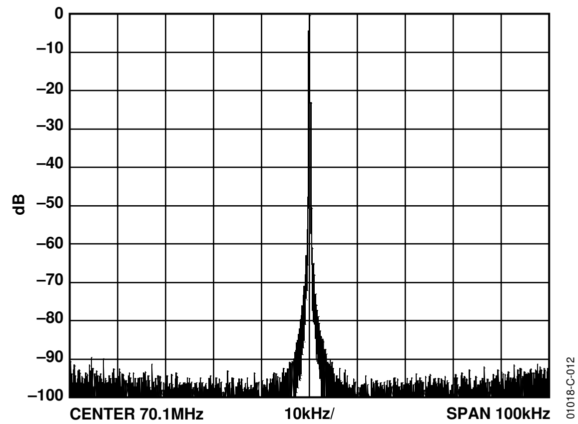



*Figure 12. 70.1 MHz Narrow-Band SFDR, 200 MHz External Clock with REFCLK Multiplier Disabled*

## OUTPUT CONSTELLATIONS

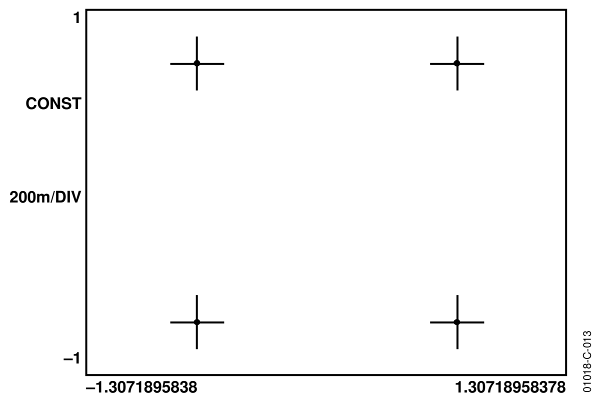



Figure 13. QPSK, 65 MHz, 2.56 MS/s

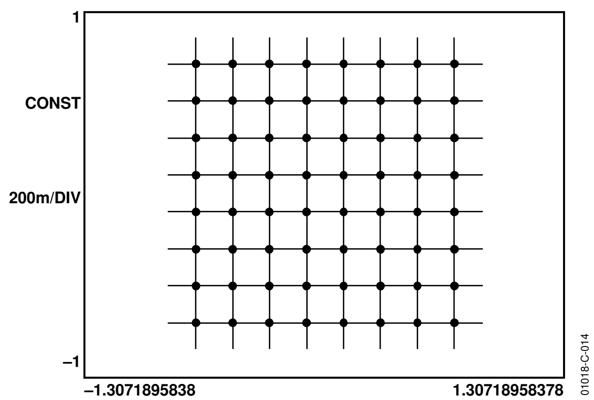



Figure 14. 64-QAM, 42 MHz, 6 MS/s

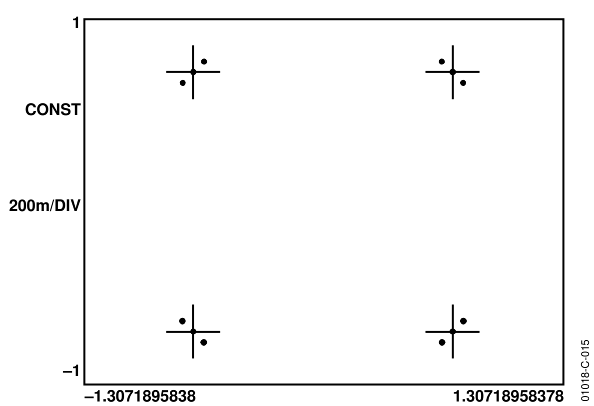



Figure 15. GMSK Modulation, 13 MS/s

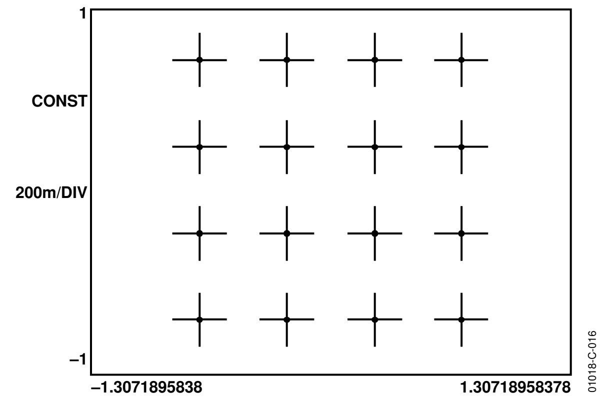



Figure 16. 16-QAM, 65 MHz, 2.56 MS/s

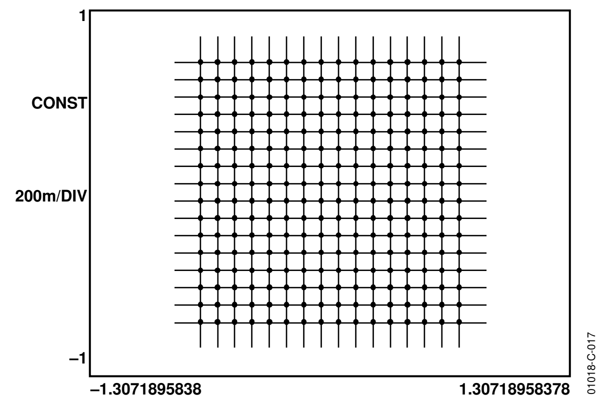



Figure 17. 256-QAM, 42 MHz, 6 MS/s

# MODES OF OPERATION

The AD9857 has three operating modes:

- Quadrature modulation mode (default)
- Single-tone mode
- Interpolating DAC mode

Mode selection is accomplished by programming a control register via the serial port. The inverse SINC filter and output scale multiplier are available in all three modes.

## QUADRATURE MODULATION MODE

In quadrature modulation mode, both the I and Q data paths are active. A block diagram of the AD9857 operating in the quadrature modulation mode is shown in Figure 18.

In quadrature modulation mode, the PDCLK/FUD pin is an output and functions as the parallel data clock (PDCLK), which serves to synchronize the input of data to the AD9857. In this mode, the input data must be synchronized with the rising edge of PDCLK. The PDCLK operates at *twice* the rate of either the I or Q data path. This is due to the fact that the I and Q data must be presented to the parallel port as two 14-bit words multiplexed in time. One I word and one Q word together comprise one internal *sample*. Each sample is propagated along the internal data pathway in parallel fashion.

The DDS core provides a quadrature (sin and cos) local oscillator signal to the quadrature modulator, where the I and Q data are multiplied by the respective phase of the carrier and summed together, to produce a quadrature-modulated data stream.

All of this occurs in the digital domain, and only then is the digital data stream applied to the 14-bit DAC to become the quadrature-modulated analog output signal.

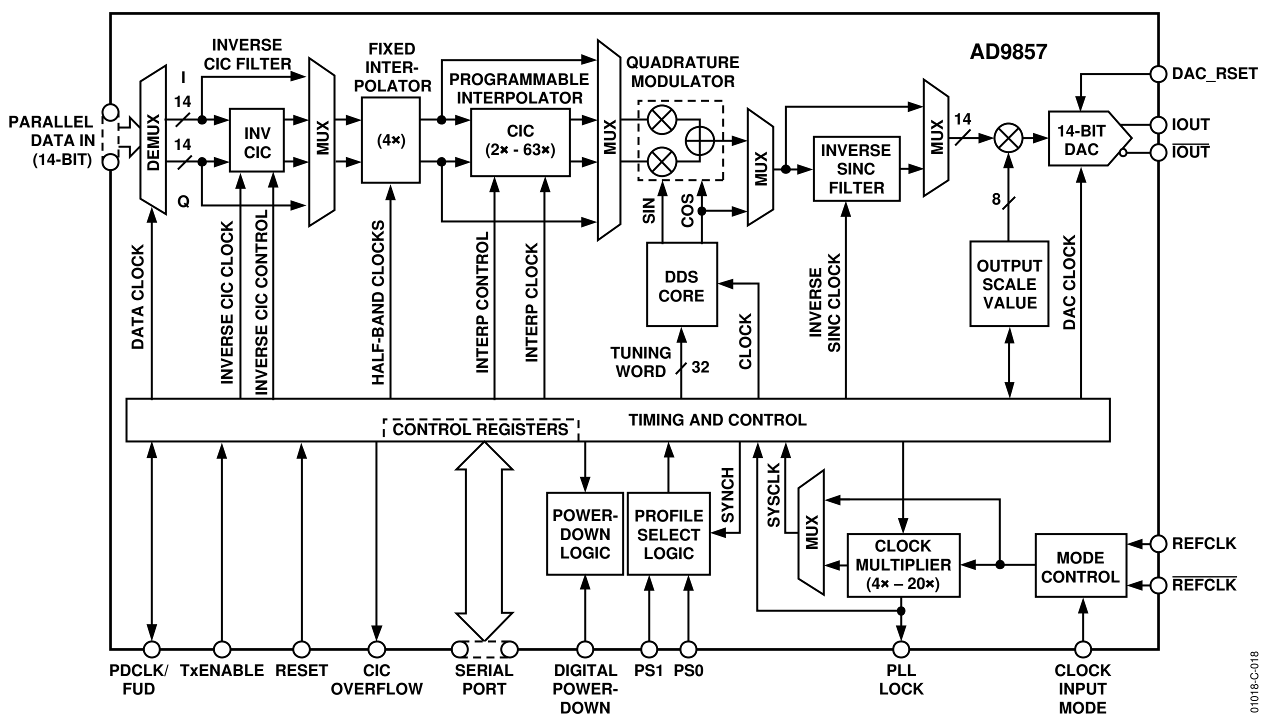



*Figure 18. Quadrature Modulation Mode*

## SINGLE-TONE MODE

A block diagram of the AD9857 operating in the single-tone mode is shown in Figure 19. In the single-tone mode, both the I and Q data paths are disabled from the 14-bit parallel data port up to and including the modulator. The PDCLK/ FUD pin is an input and functions as a frequency update (FUD) control signal. This is necessary because the frequency tuning word is programmed via the asynchronous serial port. The FUD signal causes the new frequency tuning word to become active.

In single-tone mode, the cosine portion of the DDS serves as the signal source. The output signal consists of a single frequency as determined by the tuning word stored in the appropriate control register, per each profile.

In the single-tone mode, no 14-bit parallel data is applied to the AD9857. The internal DDS core is used to produce a single frequency signal according to the tuning word. The single-tone signal then moves toward the output, where the inverse SINC filter and the output scaling can be applied. Finally, the digital single-tone signal is converted to the analog domain by the 14-bit DAC.

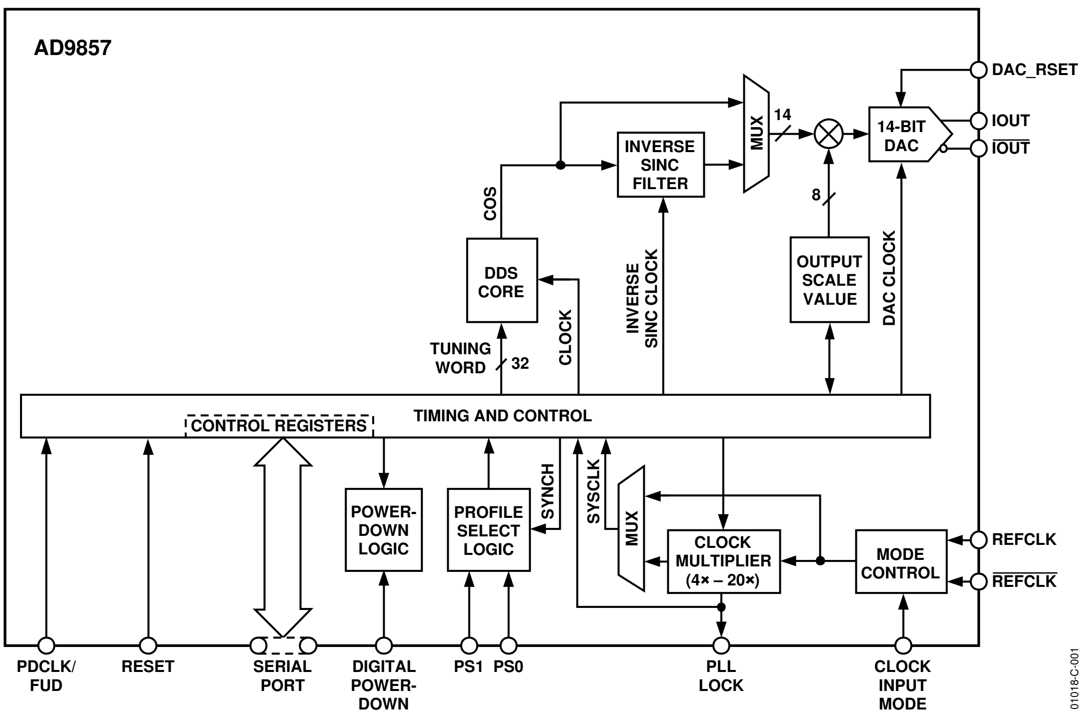



*Figure 19. Single-Tone Mode*

## INTERPOLATING DAC MODE

A block diagram of the AD9857 operating in the interpolating DAC mode is shown in Figure 20. In this mode, the DDS and modulator are both disabled and only the I data path is active. The Q data path is disabled from the 14-bit parallel data port up to and including the modulator.

As in the quadrature modulation mode, the PDCLK pin is an output and functions as a clock which serves to synchronize the input of data to the AD9857. Unlike the quadrature modulation mode, however, the PDCLK operates at the rate of the I data path. This is because only I data is being presented to the parallel port as opposed to the interleaved I/Q format of the quadrature modulation mode.

In the Interpolating DAC mode, the baseband data supplied at the parallel port remains at baseband at the output; that is, no modulation takes place. However, a sample rate conversion takes place based on the programmed interpolation rate. The interpolation hardware performs the necessary signal processing required to eliminate the aliased images at baseband that would otherwise result from a sample rate conversion. The interpolating DAC function is effectively an oversampling operation with the original input spectrum intact but sampled at a higher rate.

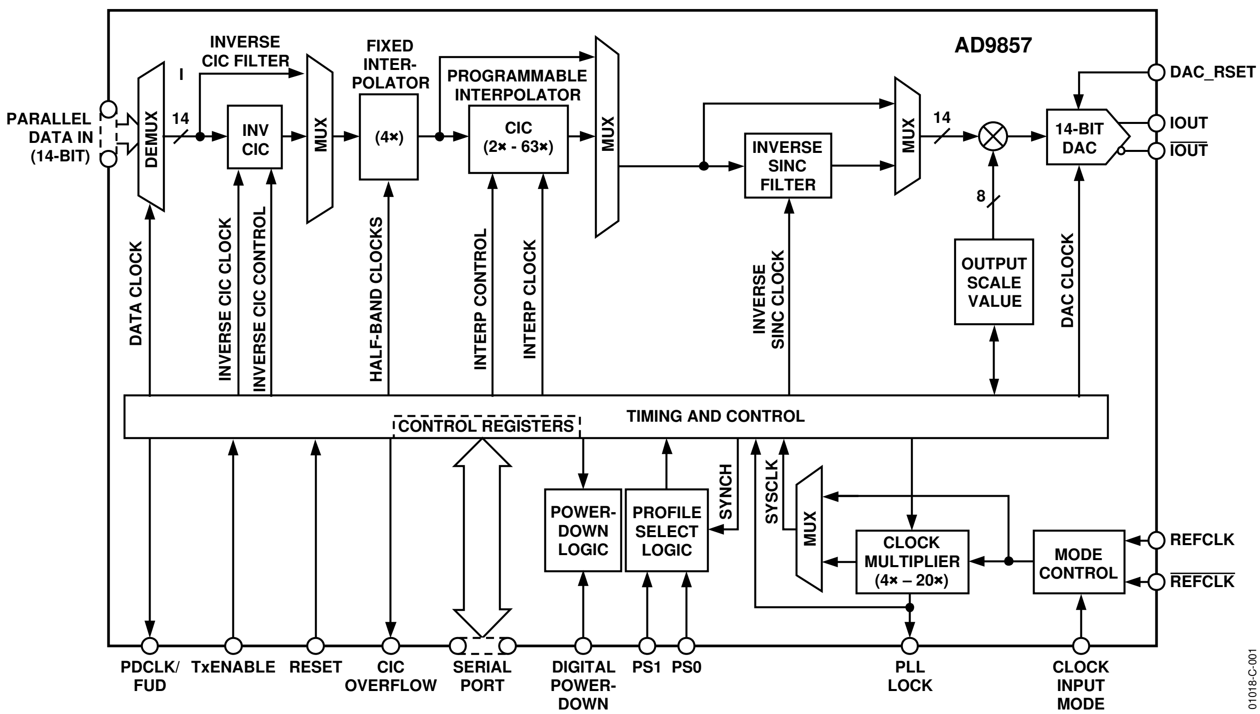



*Figure 20. Interpolating DAC Mode*

# SIGNAL PROCESSING PATH

To better understand the operation of the AD9857 it is helpful to follow the signal path from input, through the device, to the output, examining the function of each block (refer to Figure 1). The input to the AD9857 is a 14-bit parallel data path. This assumes that the user is supplying the data as interleaved I and Q values. Any encoding, interpolation, and pulse shaping of the data stream should occur *before* the data is presented to the AD9857 for upsampling.

The AD9857 demultiplexes the interleaved I and Q data into two separate data paths inside the part. This means that the input sample rate ($f_{DATA}$), the rate at which 14-bit words are presented to the AD9857, must be 2× the internal I/Q Sample Rate ($f_{IQ}$), the rate at which the I/Q pairs are processed. In other words, $f_{DATA} = 2 \times f_{IQ}$.

From the input demultiplexer to the quadrature modulator, the data path of the AD9857 is a dual I/Q path.

All timing within the AD9857 is provided by the internal system clock (SYSCLK) signal. The externally provided reference clock signal may be used as is (1×), or multiplied by the internal clock multiplier (4×–20×) to generate the SYSCLK. All other internal clocks and timing are derived from the SYSCLK.

## INPUT DATA ASSEMBLER

In the quadrature modulation or interpolating DAC modes, the device accepts 14-bit, twos complement data at its parallel data port. The timing of the data supplied to the parallel port may be easily facilitated with the PDCLK/FUD pin of the AD9857, which is an output in the quadrature modulation mode and the interpolating DAC mode. In the single-tone mode, the same pin becomes an input to the device and serves as a frequency update (FUD) strobe.

Frequency control words are programmed into the AD9857 via the serial port (see the Control Register description). Because the serial port is an asynchronous interface, when programming new frequency tuning words into the on-chip profile registers, the AD9857's internal frequency synthesizer must be synchronized with external events. The purpose of the FUD input pin is to synchronize the start of the frequency synthesizer to the external timing requirements of the user. The rising edge of the FUD signal causes the frequency tuning word of the selected profile (see the Profile section) to be transferred to the accumulator of the DDS, thus starting the frequency synthesis process.

After loading the frequency tuning word to a profile, a FUD signal is not needed when switching between profiles using the two profile select pins (PS0, PS1). When switching between profiles, the frequency tuning word in the profile register becomes effective.

In the quadrature modulation mode, the PDCLK rate is *twice* the rate of the I (or Q) data rate. The AD9857 expects interleaved I and Q data words at the parallel port with one word per PDCLK rising edge. One I word and one Q word together comprise one internal *sample*. Each sample is propagated along the internal data pathway in parallel.

In the interpolating DAC mode, however, the PDCLK rate is the same as the I data rate because the Q data path is inactive. In this mode, each PDCLK rising edge latches a data word into the I data path.

The PDCLK is provided as a continuous clock (i.e., always active). However, the assertion of PDCLK may be optionally qualified internally by the PLL lock indicator if the user elects to set the PLL lock control bit in the appropriate control register. Data supplied by the user to the 14-bit parallel port is latched into the device coincident with the rising edge of the PDCLK.

In the quadrature modulation mode, the rising edge of the TxENABLE signal is used to synchronize the device. While TxENABLE is in the Logic 0 state, the device ignores the 14-bit data applied to the parallel port and allows the internal data path to be flushed by forcing 0s down the I and Q data pathway. On the rising edge of TxENABLE, the device is ready for the first I word. The first I word is latched into the device coincident with the rising edge of PDCLK. The next rising edge of PDCLK latches in a Q word, etc., until TxENABLE is set to a Logic 0 state by the user.

When in the quadrature modulation mode, it is important that the user ensure that an even number of PDCLK intervals are observed during any given TxENABLE period. This is because the device must capture *both* an I and a Q value before the data can be processed along the internal data pathway.

The timing relationship between TxENABLE, PDCLK, and DATA is shown in Figure 21 and Figure 22.

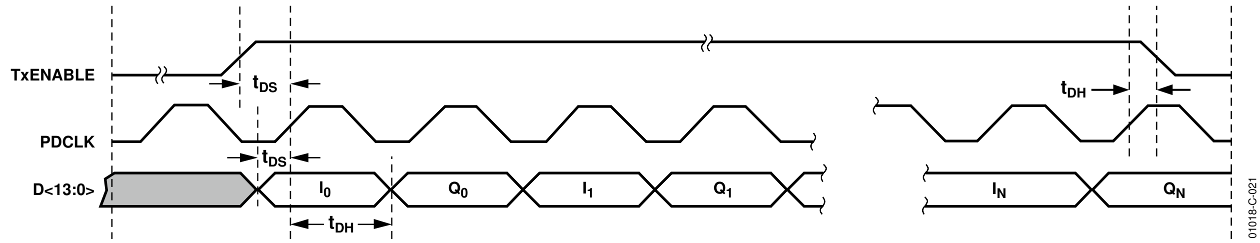



*Figure 21. 14-Bit Parallel Port Timing Diagram—Quadrature Modulation Mode*

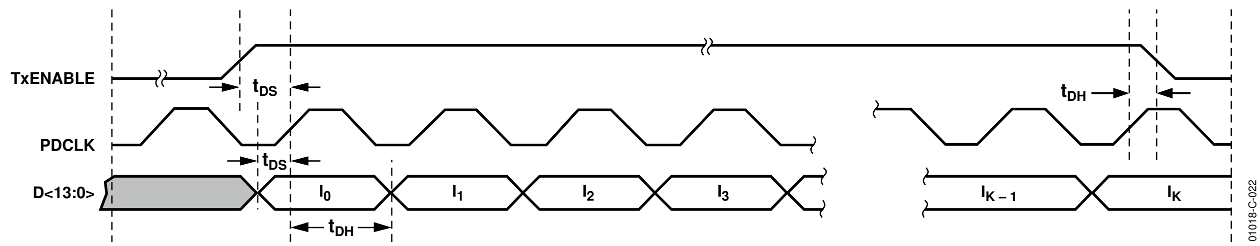



*Figure 22. 14-Bit Parallel Port Timing Diagram—Interpolating DAC Mode*

**Table 5. Parallel Data Bus Timing**

| Symbol | Definition | Minimum |
|---|---|---|
| $t_{DS}$ | Data Setup Time | 4 ns |
| $t_{DH}$ | Data Hold Time | 0 ns |

## INVERSE CIC FILTER

The inverse cascaded integrator comb (CIC) filter precompensates the data to offset the slight attenuation gradient imposed by the CIC filter. See the Programmable (2× to 63×) CIC Interpolating Filter section. The I (or Q) data entering the first half-band filter occupies a maximum bandwidth of one-half $f_{DATA}$ as defined by Nyquist (where $f_{DATA}$ is the sample rate at the input of the first half-band filter). This is shown graphically in Figure 23.

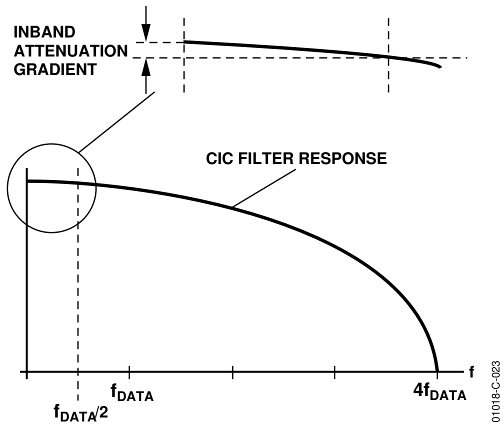



*Figure 23. CIC Filter Response*

If the CIC filter is employed, the inband attenuation gradient could pose a problem for those applications requiring an extremely flat pass band. For example, if the spectrum of the data as supplied to the AD9857 I or Q path occupies a significant portion of the one-half $f_{DATA}$ region, the higher frequencies of the data spectrum receives slightly more attenuation than the lower frequencies (the worst-case overall droop from f = 0 to one-half $f_{DATA}$ is < 0.8 dB). This may not be acceptable in certain applications. The inverse CIC filter has a response characteristic that is the inverse of the CIC filter response over the one-half $f_{DATA}$ region.

The net result is that the product of the two responses yields in an extremely flat pass band, thereby eliminating the inband attenuation gradient introduced by the CIC filter. The price to be paid is a slight attenuation of the input signal of approximately 0.5 dB for a CIC interpolation rate of 2 and 0.8 dB for interpolation rates of 3 to 63.

The inverse CIC filter is implemented as a digital FIR filter with a response characteristic that is the inverse of the programmable CIC interpolator. The product of the two responses yields a nearly flat response over the baseband Nyquist bandwidth. The inverse CIC filter provides frequency compensation that yields a response flatness of ±0.05 dB over the baseband Nyquist bandwidth, allowing the AD9857 to provide excellent SNR over its performance range.

The inverse CIC filter can be bypassed by setting Control Register 06h<0>. It is automatically bypassed if the CIC interpolation rate is 1×. Whenever this stage is bypassed, power to the stage is shutoff, thereby reducing power dissipation.

### *Fixed Interpolator (4×)*

This block is a fixed 4× interpolator. It is implemented as two half-band filters. The output of this stage is the original data upsampled by 4×.

Before presenting a detailed description of the half-band filters, recall that in the case of the quadrature modulation mode the input data stream is representative of complex data; i.e., two input samples are required to produce one I/Q data pair. The I/Q sample rate is one-half the input data rate. The I/Q sample rate (the rate at which I or Q samples are presented to the input of the first half-band filter) is referred to as $f_{IQ}$. Because the AD9857 is a quadrature modulator, $f_{IQ}$ represents the baseband of the internal I/Q sample pairs. It should be emphasized here that $f_{IQ}$ is not the same as the baseband of the user's symbol rate data, which must be upsampled before presentation to the AD9857 (as explained later). The I/Q sample rate ($f_{IQ}$) puts a limit on the minimum bandwidth necessary to transmit the $f_{IQ}$ spectrum. This is the familiar Nyquist limit and is equal to one-half $f_{IQ}$, hereafter referred to as $f_{NYQ}$.

Together, the two half-band filters provide a factor-of-four increase in the sampling rate ($4 \times f_{IQ}$ or $8 \times f_{NYQ}$). Their combined insertion loss is 0.01 dB, so virtually no loss of signal level occurs through the two half-band filters. Both half-band filters are linear phase filters, so that virtually no phase distortion is introduced within the pass band of the filters. This is an important feature as phase distortion is generally intolerable in a data transmission system.

The half-band filters are designed so that their composite performance yields a usable pass band of 80% of the baseband Nyquist frequency (0.2 on the frequency scale below). Within that pass band, the ripple does not exceed 0.002 dB. The stop band extends from 120% to 400% of the baseband Nyquist frequency (0.3 to 1.0 on the frequency scale) and offers a minimum of 85 dB attenuation. Figure 24 and Figure 25 show the composite response of the two half-band filters together.

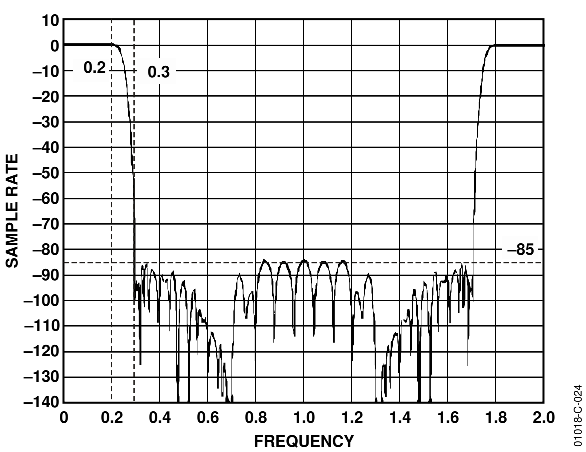



*Figure 24. Half-Band 1 and 2 Frequency Response; Frequency Relative to HB1 Output Sample Rate*

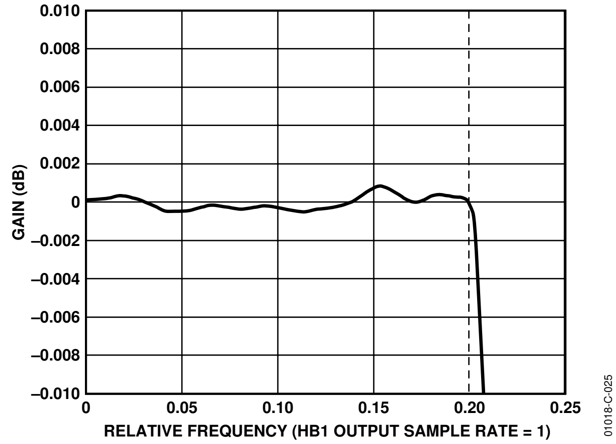



*Figure 25. Combined Half-Band 1 and 2 Pass Band Detail; Frequency Relative to HB1 Output Sample Rate*

The usable bandwidth of the filter chain puts a limit on the maximum data rate that can be propagated through the AD9857. A look at the pass band detail of the half-band filter response (Figure 25) indicates that in order to maintain an amplitude error of no more than 1 dB, signals are restricted to having a bandwidth of no more than about 90% of $f_{NYQ}$. Thus, to keep the bandwidth of the data in the flat portion of the filter pass band, the user must oversample the baseband data by at least a factor of two prior to presenting it to the AD9857. Note that without oversampling, the Nyquist bandwidth of the baseband data corresponds to the $f_{NYQ}$. Because of this, the upper end of the data bandwidth suffers 6 dB or more of attenuation due to the frequency response of the half-band filters. Furthermore, if the baseband data applied to the AD9857 has been pulse shaped, there is an additional concern.

Typically, pulse shaping is applied to the baseband data via a filter having a raised cosine response. In such cases, an α value is used to modify the bandwidth of the data where the value of α is such that ≤ α ≤ 1. A value of 0 causes the data bandwidth to correspond to the Nyquist bandwidth. A value of 1 causes the data bandwidth to be extended to twice the Nyquist bandwidth. Thus, with 2× oversampling of the baseband data and α = 1, the Nyquist bandwidth of the data corresponds with the I/Q Nyquist bandwidth. As stated earlier, this results in problems near the upper edge of the data bandwidth due to the roll-off attenuation of the half-band filters. Figure 26 illustrates the relationship between α and the bandwidth of raised cosine shaped pulses. The problem area is indicated by the shading in the tail of the pulse with α = 1 which extends into the roll-off region of the half-band filter.

The effect of raised cosine filtering on baseband pulse bandwidth, and the relationship to the half-band filter response are shown in Figure 26.

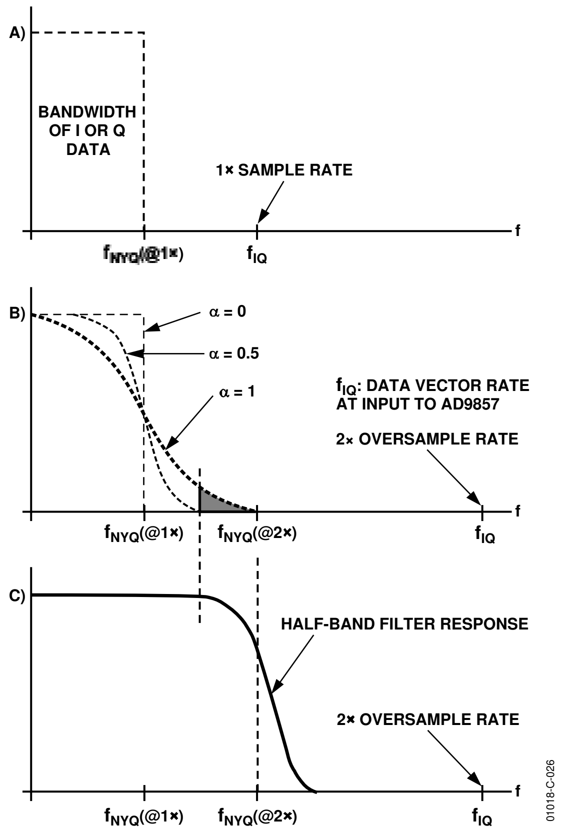



*Figure 26. Effect of Alpha*

## PROGRAMMABLE (2× TO 63×) CIC INTERPOLATING FILTER

The programmable interpolator is implemented as a CIC filter. It is programmable by a 6-bit control word, giving a range of 2× to 63× interpolation. This interpolator has a low-pass frequency characteristic that is compensated by the inverse CIC filter.

The programmable interpolator can be bypassed to yield a 1× (no interpolation) configuration by setting the bit in the appropriate control register, per each profile. Whenever the programmable interpolator is bypassed (1× CIC rate), power to the stage is removed. If the programmable interpolator is bypassed, the inverse CIC filter (see above) is automatically bypassed, because its compensation is not needed in this case.

The output of the programmable interpolator is the data from the 4× interpolator upsampled by an additional 2× to 63×, according to the rate chosen by the user. This results in the input data being upsampled by a factor of 8× to 252×.

The transfer function of the CIC interpolating filter is

$$H(f) = \left( \sum_{k=0}^{R-1} e^{-j(2\pi fk)} \right)^5 \quad (1)$$

where $R$ is the interpolation rate, and $f$ is the frequency relative to SYSCLK.

## QUADRATURE MODULATOR

The digital quadrature modulator stage is used to frequency shift the *baseband* spectrum of the incoming data stream up to the desired carrier frequency (this process is known as *upconversion*).

At this point the incoming data has been converted from an incoming sampling rate of $f_{IN}$ to an I/Q sampling rate equal to SYSCLK. The purpose of the upsampling process is to make the data sampling rate equal to the sampling rate of the carrier signal.

The carrier frequency is controlled numerically by a Direct Digital Synthesizer (DDS). The DDS uses the internal reference clock (SYSCLK) to generate the desired carrier frequency with a high degree of precision. The carrier is applied to the I and Q multipliers in quadrature fashion (90° phase offset) and summed to yield a data stream that represents the *quadrature modulated carrier*.

The modulation is done digitally which eliminates the phase and gain imbalance and crosstalk issues typically associated with analog modulators. Note that the modulated "signal" is actually a number stream sampled at the rate of SYSCLK, the same rate at which the output D/A converter is clocked.

The quadrature modulator operation is also controlled by spectral invert bits in each of the four profiles. The quadrature modulation takes the form:

$$I \times \cos(\omega) + Q \times \sin(\omega)$$

when the spectral invert bit is set to a Logic 1.

$$I \times \cos(\omega) - Q \times \sin(\omega)$$

when the spectral invert bit is set to a Logic 0.

## DDS CORE

The direct digital synthesizer (DDS) block generates the sin/cos carrier reference signals that digitally modulate the I/Q data paths. The DDS frequency is tuned via the serial control port with a 32-bit tuning word (per profile). This allows the AD9857's output carrier frequency to be very precisely tuned while still providing output frequency agility.

The equation relating output frequency ($f_{OUT}$) of the AD9857 digital modulator to the frequency tuning word (FTWORD) and the system clock (SYSCLK) is

$$f_{OUT} = (FTWORD \times SYSCLK)/2^{32} \quad (2)$$

where $f_{OUT}$ and *SYSCLK* frequencies are in Hz and *FTWORD* is a decimal number from 0 to 2,147,483,647 ($2^{31}-1$).

For example, find the FTWORD for $f_{OUT}$ = 41 MHz and SYSCLK = 122.88 MHz

If $f_{OUT}$ = 41 MHz and SYSCLK = 122.88 MHz, then

$$FTWORD = 556AAAAB \quad hex \quad (3)$$

Loading 556AAAABh into Control Bus Registers 08h–0Bh (for Profile 1) programs the AD9857 for $f_{OUT}$ = 41 MHz, given a SYSCLK frequency of 122.88 MHz.

## INVERSE SINC FILTER

The sampled carrier data stream is the input to the digital-to-analog converter (DAC) integrated onto the AD9857. The DAC output spectrum is shaped by the characteristic sin(x)/x (or SINC) envelope, due to the intrinsic zero-order hold effect associated with DAC-generated signals. Because the shape of the SINC envelope is well known, it can be compensated for. This envelope restoration function is provided by the optional inverse SINC filter preceding the DAC. This function is implemented as an FIR filter, which has a transfer function that is the exact inverse of the SINC response. When the inverse SINC filter is selected, it modifies the incoming data stream so that the desired carrier envelope, which would otherwise be shaped by the SINC envelope, is restored. However, this correction is only complete for carrier frequencies up to approximately 45% of SYSCLK.

Note also that the inverse SINC filter introduces about a 3.5 dB loss at low frequencies as compared to the gain with the inverse SINC filter turned off. This is done to flatten the overall gain from dc to 45% of SYSCLK.

The inverse SINC filter can be bypassed if it is not needed. If the inverse SINC filter is bypassed, its clock is stopped, thus reducing the power dissipation of the part.

## OUTPUT SCALE MULTIPLIER

An 8-bit multiplier (output scale value in the block diagram) preceding the DAC provides the user with a means of adjusting the final output level. The multiplier value is programmed via the appropriate control registers, per each profile. The LSB weight is $2^{-7}$, which yields a multiplier range of 0 to 1.9921875, or nearly 2×. Because the quadrature modulator has an intrinsic loss of 3 dB ($1/\sqrt{2}$), programming the multiplier for a value of $\sqrt{2}$) restores the data to the full-scale range of the DAC when the device is operating in the quadrature modulation mode.

Because the AD9857 defaults to the Modulation mode, the default value for the multiplier is B5h (which corresponds to $\sqrt{2}$).

Programming the output scale multiplier to unity gain (80h) bypasses the stage, reducing power dissipation.

## 14-BIT D/A CONVERTER

A 14-bit digital-to-analog converter (DAC) is used to convert the digitally processed waveform into an analog signal. The worst-case spurious signals due to the DAC are the harmonics of the fundamental signal and their aliases (please see the Analog Devices *DDS Technical Tutorial*, accessible from the DDS Technical Library at www.analog.com/dds for a detailed explanation of aliases). The wideband 14-bit DAC in the AD9857 maintains spurious-free dynamic range (SFDR) performance of −60 dBc up to $A_{OUT}$ = 42 MHz and −55 dBc up to $A_{OUT}$ = 65 MHz.

The conversion process produces aliased components of the fundamental signal at n × SYSCLK ± FCARRIER (n = 1, 2, 3). These are typically filtered with an external RLC filter at the DAC output. It is important for this analog filter to have a sufficiently flat gain and linear phase response across the bandwidth of interest to avoid modulation impairments.

The AD9857 provides true and complemented current outputs on $A_{OUT}$ and $\overline{A_{OUT}}$, respectively. The full-scale output current is set by the RSET resistor at DAC_RSET. The value of RSET for a particular IOUT is determined using the following equation:

$$RSET = 39.93/IOUT \quad (4)$$

For example, if a full-scale output current of 20 mA is desired, then *RSET* = (39.93/0.02), or approximately 2 kΩ. Every doubling of the RSET value halves the output current.

The full-scale output current range of the AD9857 is 5 mA–20 mA. Full-scale output currents outside of this range degrade SFDR performance. SFDR is also slightly affected by output matching; the two outputs should be terminated equally for best SFDR performance.

The output load should be located as close as possible to the AD9857 package to minimize stray capacitance and inductance. The load may be a simple resistor to ground, an op amp current-to- voltage converter, or a transformer-coupled circuit.

Driving an LC filter without a transformer requires that the filter be doubly terminated for best performance. Therefore, the filter input and output should both be resistively terminated with the appropriate values. The parallel combination of the two terminations determines the load that the AD9857 sees for signals within the filter pass band. For example, a 50 Ω terminated input/ output low-pass filter looks like a 25 Ω load to the AD9857.

The output compliance voltage of the AD9857 is −0.5 V to +1.0 V. Any signal developed at the DAC output should not exceed 1.0 V, otherwise, signal distortion results. Furthermore, the signal may extend below ground as much as 0.5 V without damage or signal distortion. The use of a transformer with a grounded center tap for common-mode rejection results in signals at the AD9857 DAC output pins that are symmetrical about ground.

As previously mentioned, by differentially combining the two signals, the user can provide some degree of common-mode signal rejection. A differential combiner might consist of a transformer or an op amp. The object is to combine or amplify only the difference between two signals and to reject any common, usually undesirable, characteristic, such as 60 Hz hum or clock feed-through that is equally present on both input signals. The AD9857 true and complement outputs can be differentially combined using a broadband 1:1 transformer with a grounded, center-tapped primary to perform differential combining of the two DAC outputs.

## REFERENCE CLOCK MULTIPLIER

It is often difficult to provide a high quality oscillator with an output in the frequency range of 100 MHz – 200 MHz. The AD9857 allows the use of a lower-frequency oscillator that can be multiplied to a higher frequency by the on-board reference clock multiplier, implemented with a phase locked loop architecture. See the Ease of Use Features section for a more thorough discussion of the reference clock multiplier feature.

# INPUT DATA PROGRAMMING

## CONTROL INTERFACE—SERIAL I/O

The AD9857 serial port is a flexible, synchronous, serial communications port allowing easy interface to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola 6905/11 SPI and Intel 8051 SSR protocols.

The interface allows read/write access to all registers that configure the AD9857. Single or multiple byte transfers are supported as well as MSB first or LSB first transfer formats. The AD9857's serial interface port can be configured as a single pin I/O (SDIO) or two unidirectional pins for in/out (SDIO/SDO).

## GENERAL OPERATION OF THE SERIAL INTERFACE

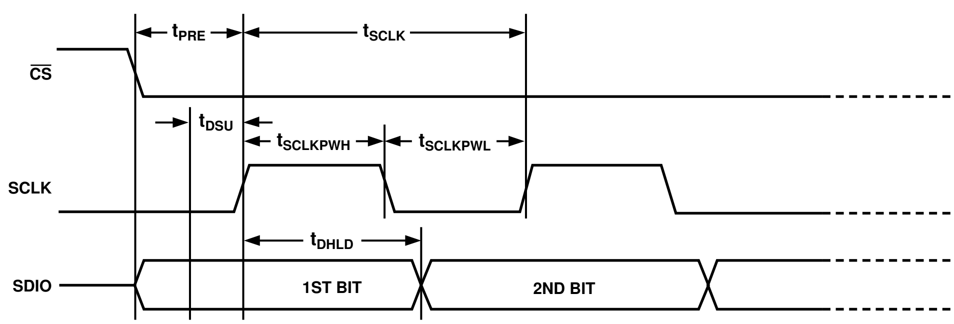
There are two phases to a communication cycle with the AD9857. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9857, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9857 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write, the number of bytes in the data transfer (1-4), and the starting register address for the first byte of the data transfer.

The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9857. The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9857 and the system controller. Phase 2 of the communication cycle is a transfer of 1, 2, 3, or 4 data bytes as determined by the instruction byte. Typically, using one communication cycle in a multibyte transfer is the preferred method. However, single-byte communication cycles are useful to reduce CPU overhead when register access requires one byte only. An example of this may be to write the AD9857 SLEEP bit.

At the completion of any communication cycle, the AD9857 serial port controller expects the next eight rising SCLK edges to be the instruction byte of the next communication cycle.

All data input to the AD9857 is registered on the rising edge of SCLK. All data is driven out of the AD9857 on the falling edge of SCLK.

Figure 27 and Figure 28 illustrate the data write and data read operations on the AD9857 serial port. Figure 29 through Figure 32 show the general operation of the AD9857 serial port.




| SYMBOL | DEFINITION | MIN |
|---|---|---|
| $t_{PRE}$ | $\overline{CS}$ SETUP TIME | 40ns |
| $t_{SCLK}$ | PERIOD OF SERIAL DATA CLOCK | 100ns |
| $t_{DSU}$ | SERIAL DATA SETUP TIME | 30ns |
| $t_{SCLKPWH}$ | SERIAL DATA CLOCK PULSE WIDTH HIGH | 40ns |
| $t_{SCLKPWL}$ | SERIAL DATA CLOCK PULSE WIDTH LOW | 40ns |
| $t_{DHLD}$ | SERIAL DATA HOLD TIME | 0ns |

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*Figure 27. Timing Diagram for Data Write to AD9857*